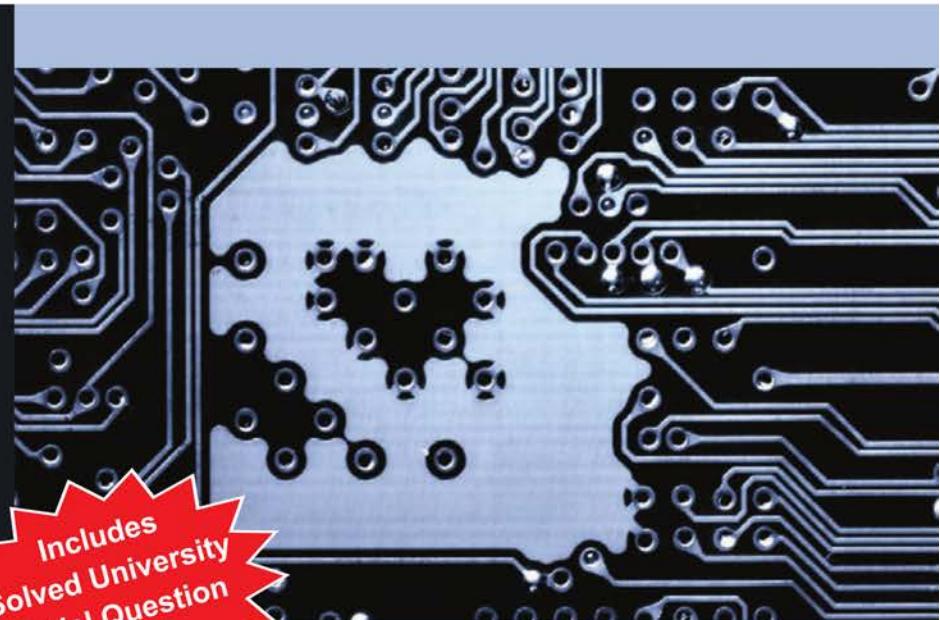


Pulse and Digital Circuits

JNTU



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Solved University
Model Question
papers

Venkata Rao K.
Rama Sudha K.
Manmadha Rao G.

Pulse
and
Digital Circuits

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Pulse and Digital Circuits

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Dedicated to my brother; Sri K. V. N. Sarma

—Venkata Rao

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Preface

Writing a textbook on a topic that has matured over the years is, for obvious reasons, truly daunting. First, a subject that continues to be important enough to be taught in classrooms even after eight decades demands that those studying it for the first time not only understand the critical concepts, but also learn to appreciate the finer nuances so that the subject and the practitioners continue to grow together. Second, almost every such mature area has some established books that have stood the test of time and continue to hold sway over a large majority of the readers. To match up to the standards set by such books is far from easy.

At the same time, we maintain that there is a need for books that meet the requirements of present-day undergraduate students of electronics and electrical engineering. Sometimes, books are written on the premise that not every minute detail needs to be presented to the student, but some things should be left to their imagination to encourage repeated reading and to stimulate their analytical ability. However, we have observed that not all students benefit from such a textbook. Neither do we believe that re-reading to reinterpret the written word improves the analytical ability of all students. A student who has tried and failed at this loses the motivation to pursue the subject further. Dealing with such a student is not easy either.

Through this book, we attempt to address these problems. This textbook, written to cater to the needs of undergraduate students of electronics and electrical engineering in various Indian universities, uses numerous simplified circuits and illustrations to explain concepts and facilitate a clear understanding of the subject matter in students, motivating them to read further. Drawing upon our experience in the classroom, we have attempted to provide lucid answers and explanations to common queries and problematic concepts for students, making this book a great resource for self-study. We have made a concerted effort to make the presentation and illustrations more student-friendly. Many examples and solved problems have been included.

The Organization of the Book

The book is organized into fifteen chapters.

Chapter 1, “An Introduction to Pulse Waveforms”, introduces pulse waveforms, touching upon the prerequisites for the study of pulse and digital circuits and recapitulating the method of analysis of various amplifier configurations and their relevance. The chapter briefly describes the relevant network theorems and their applications in pulse and digital circuits.

Chapter 2, “Linear Waveshaping: High-pass Circuits”, analyses the response of linear high-pass RC and RL circuits to various types of input signals. Except for the sinusoidal signal, all other signals undergo distortion in amplitude when passed through a high-pass circuit, the amount of distortion being dependent on the time constant employed in the circuit. The presentation is so arranged that the student is able to arrive at the response from their earlier knowledge of mathematics by writing and solving the necessary differential equations using Laplace transforms. The specific application of a high-pass circuit as a differentiator is also discussed.

Chapter 3, “Linear Waves Shaping: Low-pass Circuits, Attenuators and *RLC* Circuits”, examines the response of linear low-pass *RC* and *RL* circuits to various types of input signals. Specific applications of low-pass *RC* circuits as integrators and compensated attenuators are discussed. Finally, the response of the *RLC* circuit to step input and the under-damped *RLC* circuit as a ringing circuit are presented.

Chapter 4, “Non-linear Waves Shaping: Clipping Circuits and Comparators”, describes the use of non-linear circuit elements such as diodes and transistors in waves shaping applications such as clippers. The chapter concludes with a discussion of the application of a diode clipper as an amplitude comparator.

Chapter 5, “Non-Linear Waves Shaping: Clamping Circuits”, talks about non-linear waves shaping in applications such as clamping in which either the positive or the negative peak of the input is clamped to either a zero level or to an arbitrarily chosen dc reference level. This, in turn, means that the clamping circuit introduces a dc level that is lost while transmitting a signal through a capacitor-coupled network.

Chapter 6, “Switching Characteristics of Devices”, considers the switching characteristics of devices such as diodes and transistors in view of the influence of inter-electrode capacitances on the switching speeds of these devices. The dependence of the parameters of a transistor on temperature is also presented.

Chapter 7, “Astable Multivibrators”, examines regenerative circuits that use transistors. These circuits, essentially used to generate a square-wave output (clock pulses), can also be used to trigger some other circuits. The applications of an astable multivibrator as a voltage-to-frequency converter and as a frequency modulator are also considered.

Chapter 8, “Monostable Multivibrators”, discusses monostable multivibrators, which generate a gating signal or a pulse. Two possible circuit configurations—collector-coupled and emitter-coupled monostable multivibrators—are presented. The application of a monostable multivibrator as a voltage-to-time converter is also described.

Chapter 9, “Bistable Multivibrators”, focuses on bistable multivibrators, which are used as 1-bit memory elements in digital circuits. Two circuit variations—fixed-bias and self-bias arrangements—are presented. Both symmetric and unsymmetric methods of triggering bistable multivibrators are presented. The chapter concludes with a detailed discussion on emitter-coupled bistable multivibrators called Schmitt triggers used in waves shaping applications.

Chapter 10, “Logic Gates”, presents logic gates belonging to various families such as RTL, DTL, TTL and CMOS, while discussing the relative merits and demerits of each. The interfacing of TTL and CMOS logic gates is also described.

Chapter 11, “Sampling Gates”, analyses sampling gates that transmit the input signal to the output terminals only during the time interval decided by the control signal. Unidirectional and bidirectional sampling gates that transmit signals of either or both polarities are considered along with the methods to eliminate pedestal in the output.

Chapter 12, “Voltage Sweep Generators”, introduces voltage sweep generators that find application in CROs to move the electron beam linearly along the time axis so as to be able to display a time-varying signal applied to vertical deflecting plates. Miller and bootstrap sweep generators, which linearize an exponential sweep, are also discussed.

Chapter 13, “Current Sweep Generators”, considers current sweep generators that are used to produce large deflections of electron beams for specific applications such as in television and radar receivers. A method to improve the linearity of the current sweep by adjusting the driving waveform is also included.

Chapter 14, “Blocking Oscillators”, considers single-transistor regenerative circuits, called blocking oscillators, which use a pulse transformer to derive positive feedback by a proper choice of the winding polarities. Variations of astable and monostable blocking oscillators are also covered.

Chapter 15, “Synchronization and Frequency Division”, talks about the synchronization of the output of various waveform generators. Synchronization of the output of relaxation circuits like sweep generators and multivibrators with pulses and symmetric signals is discussed.

Features

The book uses a number of simplified, equivalent circuits to explain the operation of circuits. For instance, in Chapter 7, “Astable Multivibrator”, we use three simplified equivalent circuit diagrams in addition to the basic circuit to explain the working of a collector-coupled astable multivibrator. Further, we have incorporated several pedagogical features designed to facilitate learning and encourage analysis and problem solving.

Learning Objectives: Each chapter includes well-defined learning objectives that clearly identify what the student will learn in the chapter.

Summary: Each chapter ends with a detailed summary that captures the key points from the chapter. The students can use this to review the entire chapter.

End-of-chapter Questions: Each chapter includes both short answer and long answer questions. A mix of conceptual and analytical questions, these enable students to review concepts and apply them to solve conceptual problems.

Problems: The book includes numerous unsolved problems that will be extremely beneficial to the students. Detailed solutions to these problems are available on the companion Web site of the book.

The Teaching and Learning Package

The companion Web site, www.pearsoned.co.in/venkatara, contains resources for both instructors and students.

For Students

Important Equations: This is a compilation of the important equations from the book. This can be used to recapitulate the key equations from each chapter.

Solutions Manual: The solutions manual is a comprehensive document comprising detailed solutions to all the unsolved problems included in the book. The answers to the objective-type questions at the end of each chapter are also included in this.

Question Bank: The question bank, comprising approximately 400 multiple choice questions is an invaluable resource for students. It includes both concept-check questions and problems. The inclusion of questions from various university examinations makes it a valuable resource for self-study by students.

For Instructors

PowerPoint Presentations: PowerPoint lecture slides, designed to provide an overview of key concepts, diagrams and equations, are available for each chapter. These can be used by instructors to deliver classroom lectures in an engaging manner.

Acknowledgements

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Rama Sudha K.
Manmadha Rao G.

CHAPTER 1

An Introduction to Pulse Waveforms

LEARNING OBJECTIVES

After reading this chapter, you will be able to:

- State and use network theorems
 - Understand the relevance of the performance quantities of an amplifier
 - Understand the need and application of the three configurations of amplifiers
 - Appreciate the need for cascading amplifiers; and understand the concept of feedback in amplifiers, power amplifiers and oscillators
 - Understand the principle of operation of operational amplifiers
 - Describe the characteristics of pulse waveforms
-

1.1 INTRODUCTION

When devices such as diodes, bipolar junction transistors (BJTs) and field-effect transistors (FETs) are used in amplifiers, oscillators, rectifiers and other such applications, these devices are used either as linear or non-linear circuit elements, for which they have to be used in a limited range of the transfer characteristic (defines the relation between the input and the output). If the operation goes beyond the linear region of the transfer characteristic, unwanted frequencies called harmonics—integer multiples of the fundamental frequency—appear in the output of the circuit. However, when the signal swing is large, as in power amplifiers, the output is invariably distorted. This distortion can be minimized using a push–pull configuration as this arrangement eliminates even harmonics. To analyse a given circuit comprising such devices, it is possible to replace the device by its equivalent circuit. To simplify the analysis, it is necessary, at times, to piece-wise linearize the transfer characteristic so that the behaviour of the device can be predicted in that limited region of operation.

These devices—diodes, transistors, FETs and so on—can also be used as switches in switching applications by driving the device into the OFF state in one case and by driving the device into the ON state in the other case. However, the inter-electrode capacitances limit the switching speed. Operational amplifiers and negative resistance devices also find applications in pulse and switching circuits. This chapter presents a brief overview of the fundamentals to facilitate comprehension of the principles of pulse and switching circuits.

1.2 CURRENT AND VOLTAGE SOURCES

Normally either ac or dc sources are used as current and voltage sources. A source can be either a voltage source (Thévenin source) or a current source (Norton source). An ideal voltage source should have zero internal resistance so that when current is drawn from the source, there is no voltage drop across the internal resistance of the source and the entire source voltage is available at its output terminals. Similarly, in a current source, no appreciable amount of current should flow through the internal resistance of the generator and the entire source current should flow through the load. For this, the internal resistance of the current source should ideally be infinity.

Figure 1.1(a) shows a practical voltage or Thévenin source and Fig. 1.1(b) a current or Norton source. It is possible to convert a Thévenin source into a Norton source and vice versa. To convert the Thévenin source

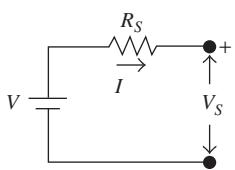


FIGURE 1.1(a) Thévenin or voltage source

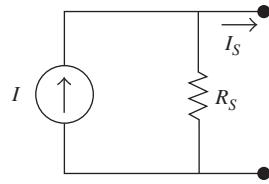


FIGURE 1.1(b) Norton or current source

[represented in Fig. 1.1(a)] into a Norton source [see Fig. 1.1(b)], we calculate the current (I) in the circuit using the relation $I = V/R_S$, where R_S is the internal resistance in shunt with the current source I . Similarly, to convert the Norton source into a Thévenin source as shown in Fig. 1.1(a), we calculate the voltage (V) across R_S as $V = IR_S$, where R_S is its internal resistance in series with the source V . Consider the single-loop network using a voltage source, as shown in Fig. 1.2. From Fig. 1.2:

$$I = \frac{V}{R_1 + R_2}$$

and

$$V_{R2} = IR_2 = \frac{VR_2}{R_1 + R_2} \quad (1.1)$$

The single-loop network shown in Fig. 1.2 is analysed using Ohm's law. In this circuit, R_1 and R_2 comprise a potential divider. So, Eq. (1.1) is used to calculate V_{R2} directly instead of first calculating the current and then the voltage.

However, to analyse a network that has more than one loop, i.e., calculate the current in a given loop or voltage across the given branch, two basic network theorems—Kirchoff's voltage law and Kirchoff's current law—are used.

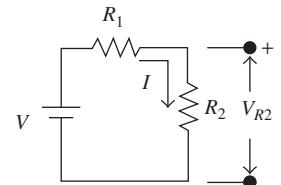


FIGURE 1.2 A single-loop network

1.3 NETWORK LAWS

Network laws or theorems help to analyse circuits in a much simpler way. In this section, we discuss some frequently used network laws and theorems, namely, Kirchoff's laws, superposition theorem, and Thévenin and Norton theorems.

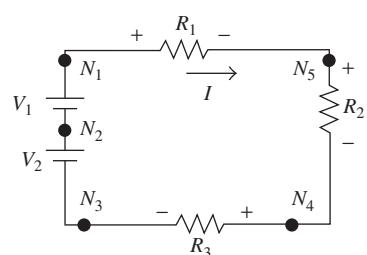
1.3.1 Kirchoff's Laws

The two Kirchoff's laws are Kirchoff's voltage and Kirchoff's current laws. Kirchoff's voltage law (KVL) states that the sum of voltages between successive nodes in a closed path in a circuit is equal to zero. Kirchoff's current law states that the algebraic sum of currents in all the branches that converge in a common node in a circuit is zero.

Kirchoff's Voltage Law. Consider the circuit in Fig. 1.3. The KVL equation for this circuit is:

$$V_1 + V_2 - IR_1 - IR_2 - IR_3 = 0 \quad (1.2)$$

$$\text{or } V_1 + V_2 = I(R_1 + R_2 + R_3) \quad (1.3)$$

FIGURE 1.3 A network having nodes N_1 to N_5 and two sources aiding each other

Consider a case when the two batteries oppose each other as shown in Fig. 1.4. Here, the KVL equation is modified as:

$$V_1 - V_2 - IR_1 - IR_2 - IR_3 = 0 \quad (1.4)$$

$$\text{or } V_1 - V_2 = I(R_1 + R_2 + R_3) \quad (1.5)$$

Kirchoff's Current Law. Consider the circuit in Fig. 1.5. For the given current directions in Fig. 1.5, to write the KCL equation at the node N , treat the currents entering the node as positive and those leaving the node as negative. Thus, the KCL equation at the node N is $I_1 + I_2 - I_{R1} - I_{R2} = 0$. In other words, $I_1 + I_2 = I_{R1} + I_{R2}$.

A parallel circuit (see Fig 1.6) behaves as a current divider. The total current (I) is divided into two branch currents— I_1 and I_2 . The current in one of the branches, say I_1 , is calculated as:

$$I_1 = \frac{IR_2}{R_1 + R_2} \quad (1.6)$$

That is, I_1 is calculated as the total current (I) multiplied by the other branch resistance (R_2) divided by the total resistance ($R_1 + R_2$). Similarly,

$$I_2 = \frac{IR_1}{R_1 + R_2} \quad (1.7)$$

Kirchoff's laws are used to analyse a multi-loop network, as shown in Fig. 1.7. The KVL equations for the two loops are:

$$V_1 = I_1(R_1 + R_3) + I_2R_3 \quad (1.8)$$

$$V_2 = I_2(R_2 + R_3) + I_1R_3 \quad (1.9)$$

Equations (1.8) and (1.9) can be used to calculate I_1 and I_2 , if V_1 , V_2 , R_1 , R_2 and R_3 are known.

EXAMPLE

Example 1.1: For the circuit in Fig. 1.7, let $V_1 = 10$ V, $V_2 = 20$ V, $R_1 = R_2 = 10$ k Ω , $R_3 = 5$ k Ω . Find I_1 and I_2 .

Solution: From Eqs. (1.8) and (1.9):

$$10 = 15I_1 + 5I_2$$

$$20 = 5I_1 + 15I_2$$

Solving these equations, we get:

$$I_1 = 0.25 \text{ mA} \quad \text{and} \quad I_2 = 1.25 \text{ mA}$$

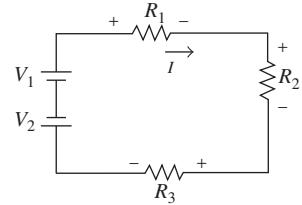


FIGURE 1.4 V_1 and V_2 oppose each other

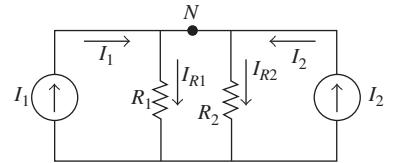


FIGURE 1.5 Circuit with two current sources

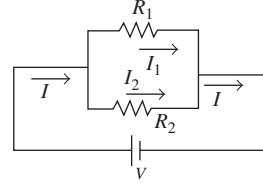


FIGURE 1.6 A parallel circuit as a current divider

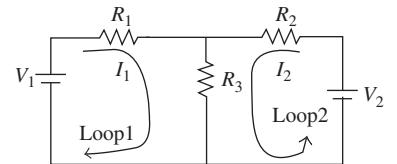


FIGURE 1.7 A two-loop network

1.3.2 The Superposition Theorem

In a linear bilateral network containing many simultaneously acting sources (either current or voltage), the superposition theorem is used to evaluate the current in a given branch or the voltage at a given node. The superposition theorem states that the total current in any branch (or voltage at any node) in a bilateral linear network equals the algebraic sum of currents (voltages) produced by each source, acting independently. Consider the two-loop network shown in Fig. 1.8(a).

The procedure to calculate the voltage at node N using the superposition theorem is:

1. Consider one source at a time and set the other source to zero (short circuit the voltage source and open circuit the current source, leaving their internal resistances).
2. Consider source V_1 and short source V_2 . The resultant circuit is as shown in Fig. 1.8(b).
3. Let $R = R_2 \parallel R_3$, The circuit reduces to that shown in Fig. 1.8(c).
4. The voltage at the node, N due to source V_1 is:

$$V_{N1} = \frac{V_1 R}{R_1 + R} \quad (1.10)$$

Now consider the other source V_2 and short V_1 as in Fig. 1.8(d). Let R' be the parallel combination of R_1 and R_3 , and $R' = R_1 \parallel R_3$. The resultant circuit is shown in Fig. 1.8(e).

5. The voltage at node N due to V_2 is:

$$V_{N2} = \frac{V_2 R'}{R_2 + R'} \quad (1.11)$$

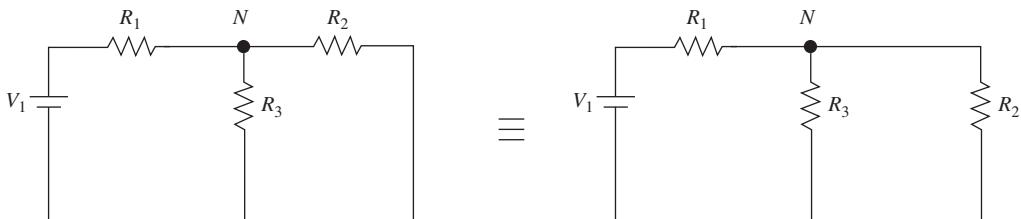


FIGURE 1.8(a) A two-loop network

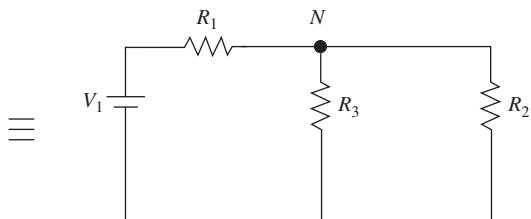


FIGURE 1.8(b) Circuit that results when V_2 is shorted

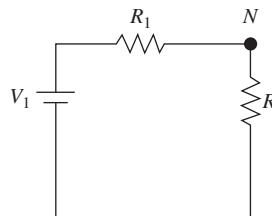


FIGURE 1.8(c) Simplified circuit of Fig. 1.8(b)

FIGURE 1.8(d) Network that results when V_1 is shorted

6. Hence, the net voltage at node N due to the two sources V_1 and V_2 is:

$$V_N = V_{N1} + V_{N2} = \frac{V_1 R}{R_1 + R} + \frac{V_2 R'}{R_2 + R'} \quad (1.12)$$

Let us consider an example to understand this principle.

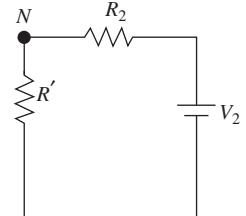


FIGURE 1.8(e) Simplified circuit of Fig. 1.8(d)

EXAMPLE

Example 1.2: For the circuit shown in Fig. 1.9(a), calculate the voltage V_N at node N , given that $V_1 = 10$ V, $V_2 = 20$ V, $R_1 = R_2 = 10$ k Ω , and $R_3 = 5$ k Ω .

Solution: To calculate V_N , consider V_1 and short V_2 , as shown Fig. 1.9(b).

$$R = \frac{5 \times 10}{5 + 10} = \frac{10}{3} \text{ k}\Omega$$

$$V_{N1} = \frac{V_1 R}{R_1 + R} = \frac{10 \times \frac{10}{3}}{10 + \frac{10}{3}} = \frac{100}{3} \times \frac{3}{40} = 2.5 \text{ V}$$

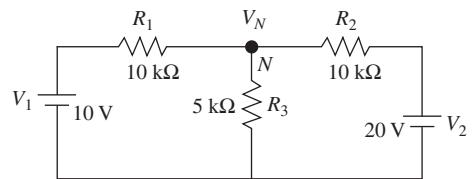
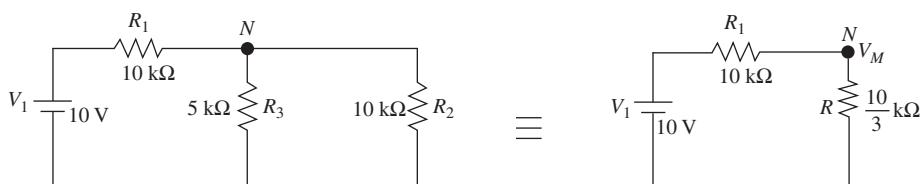
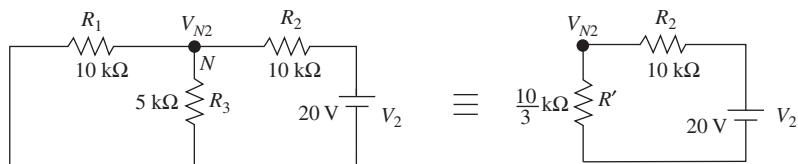


FIGURE 1.9(a) Given network

FIGURE 1.9(b) Circuit that results when V_2 is shorted

Now consider V_2 and short V_1 , as shown in Fig. 1.9(c).

FIGURE 1.9(c) Network that results when V_1 is shorted

$$R' = \frac{5 \times 10}{5 + 10} = \frac{10}{3} \text{k}\Omega \quad V_{N2} = \frac{V_2 R'}{R_2 + R'} = \frac{20 \times \frac{10}{3}}{10 + \frac{10}{3}} = \frac{200}{3} \times \frac{3}{40} = 5 \text{ V}$$

$$V_N = V_{N1} + V_{N2} = 2.5 + 5 = 7.5 \text{ V}$$

E X A M P L E

Example 1.3: For the circuit shown in Fig. 1.10(a), find the current I_3 .

Solution: To find I_3 , consider I and short V . The resultant circuit is as shown in Fig. 1.10(b).

$$I_1 = \frac{IR_2}{R_2 + R_3} = \frac{10 \times 10}{20} = 5 \text{ A}$$

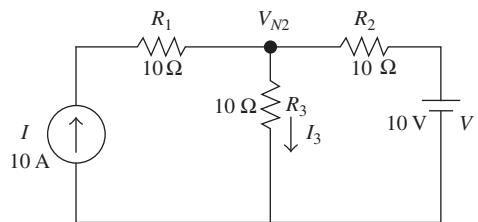


FIGURE 1.10(a) The given two-loop network

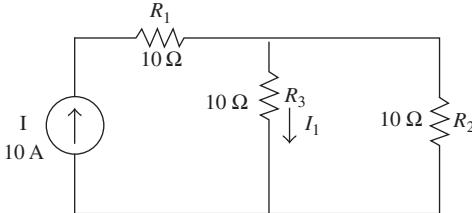


FIGURE 1.10(b) Circuit that results when V is shorted

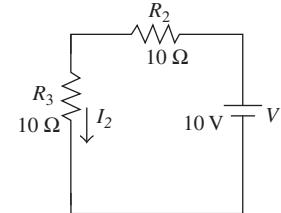


FIGURE 1.10(c) Circuit that results when I is open

Now consider the source V and open circuit I . The resultant network is as shown in Fig. 1.10(c).

$$I_2 = \frac{V}{R_2 + R_3} = \frac{10}{10 + 10} = 0.5 \text{ A} \quad I_3 = I_1 + I_2 = 5 + 0.5 = 5.5 \text{ A}$$

It is clear from the preceding discussion that a set of network equations need to be solved to find out either the current through an element in a network or the voltage across it. However, with the help of Thévenin's theorem, it is possible to simplify a two-loop linear bilateral circuit, containing a number of sources (voltage and current), to a circuit consisting of a voltage source with its internal resistance connected to the load.

1.3.3 Thévenin's Theorem

Thévenin's theorem states that any bilateral linear network consisting of voltage or current sources can be replaced by an equivalent circuit comprising a voltage source and its internal resistance.

The procedure to analyse a circuit using Thévenin's theorem is outlined below:

1. Open circuit the load and find the open-circuited voltage across the load terminals, V_{OC} . This is the value of the Thévenin voltage source, V_{th} .

2. Find the internal resistance of the Thévenin source by short circuiting the voltage source (open circuiting the current source) and looking into the open-circuited load terminals. This is the internal resistance of the Thévenin generator, R_{th} .
3. Now connect the load.
4. In the circuit shown in Fig. 1.11(a), R_L is the load and I_L is the load current. Following the procedure described above, open circuit R_L to find V_{th} . The resultant circuit is shown in Fig. 1.11(b). The Thévenin voltage source is given by:

$$V_{OC} = V_{th} = \frac{VR_3}{R_1 + R_3} \quad (1.13)$$

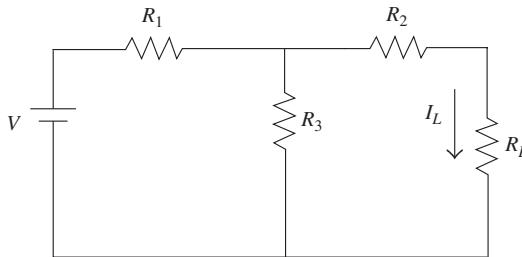


FIGURE 1.11(a) A two-loop network

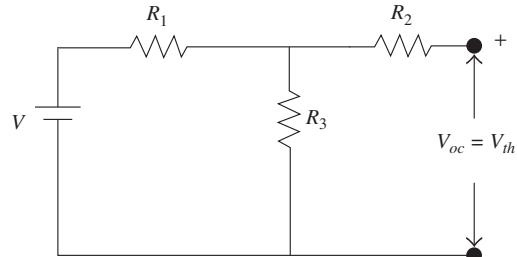
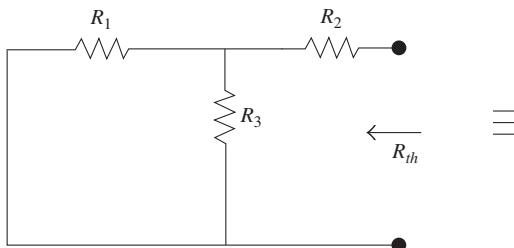


FIGURE 1.11(b) Resultant circuit when the load is open

FIGURE 1.11(c) Resultant circuit when V is shorted

To find the internal resistance of the Thévenin source, short V and find the resistance between the open-circuit load terminals. The circuit reduces to that shown in Fig. 1.11(c). The Thévenin equivalent and its internal resistance circuit is as shown in Fig. 1.11(d). From Fig. 1.11(c):

$$R_{th} = R_2 + \frac{R_1 R_3}{R_1 + R_3} \quad (1.14)$$

Therefore,

$$I_L = \frac{V_{th}}{R_{th} + R_L}$$

or

$$V_L = V_{th} \times \frac{R_L}{R_{th} + R_L} \quad (1.15)$$

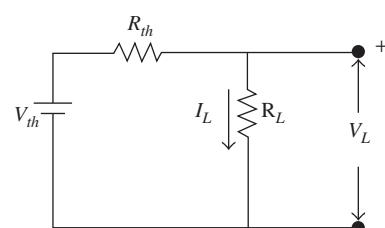


FIGURE 1.11(d) Simplified circuit of Fig. 1.11(a)

E X A M P L E

Example 1.4: Consider the circuit given in Fig. 1.12(a). Find the load current and voltage using Thévenin's theorem.

Solution: Open the load R_L and find V_{th} , as shown in Fig. 1.12(b).

$$V_{OC} = V_{th} = \frac{VR_3}{R_1 + R_3} = \frac{15 \times 5}{10 + 5} = 5 \text{ V}$$

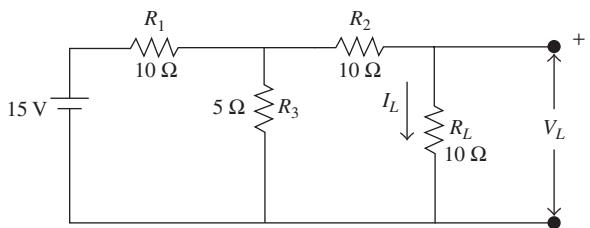


FIGURE 1.12(a) The given two-loop network

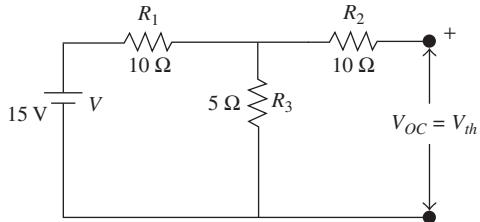


FIGURE 1.12(b) Resultant circuit when R_L is open

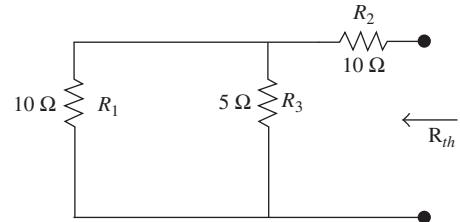


FIGURE 1.12(c) Resultant circuit when V is shorted

To find R_{th} , short the voltage source [see Fig. 1.12(c)].

$$R_{th} = R_2 + \frac{R_1 R_3}{R_1 + R_3} = 10 + \frac{10 \times 5}{10 + 5} = 10 + \frac{10}{3} = \frac{40}{3} \Omega$$

The circuit in Fig. 1.12(a) reduces to that in Fig. 1.12(d).

$$I_L = \frac{V_{th}}{R_{th} + R_L} = \frac{5}{\frac{40}{3} + 10} = \frac{5 \times 3}{70} = \frac{3}{14} \text{ A}$$

$$V_L = I_L R_L = \frac{3}{14} \times 10 = \frac{15}{7} \text{ V}$$

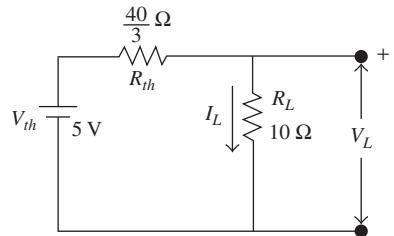


FIGURE 1.12(d) Thévenin equivalent circuit of Fig. 1.12(a)

1.3.4 Norton's Theorem

Norton's theorem states that any bilateral linear network consisting of voltage and current sources can be replaced by a current source (Norton source) and its internal resistance.

The procedure to analyse a circuit using Norton's theorem is as follows:

1. Open the load and open circuit the current source (or short circuit the voltage source) and find the internal resistance of the Norton source, R_{Norton} , by looking into the open-circuit load terminals.
2. Now short the load and find the short-circuit load current, I_{SC} . This is called I_{Norton} .
3. Represent the Norton source with its internal resistance and connect the load. Calculate I_L .

To analyse the circuit shown in Fig. 1.13(a) using Norton's theorem, open the load R_L and short V . Look into the open-circuited load terminals and find out R_{Norton} . The circuit to be considered is shown in Fig. 1.13(b).

$$R_{\text{Norton}} = R_2 + \frac{R_1 R_3}{R_1 + R_3} \quad (1.16)$$

Now short the load, consider V and find $I_{SC} = I_{\text{Norton}}$. The circuit to be considered is shown in Fig. 1.13(c). Here:

$$I = \frac{V}{R_1 + \frac{R_2 R_3}{R_2 + R_3}} \quad (1.17)$$

and

$$I_{SC} = I_{\text{Norton}} = I \times \frac{R_3}{R_2 + R_3} \quad (1.18)$$

Substituting Eq. (1.17) in Eq. (1.18):

$$\begin{aligned} I_{SC} &= \frac{V}{R_1 + \frac{R_2 R_3}{R_2 + R_3}} \times \frac{R_3}{R_2 + R_3} = \frac{VR_3}{R_1 R_2 + R_1 R_3 + R_2 R_3} \\ &= \frac{V}{R_1 + R_2 + \frac{R_1 R_2}{R_3}} \end{aligned} \quad (1.19)$$

The Norton source with its internal resistance is shown with the load connected as in Fig. 1.13(d). Here:

$$I_L = I_{\text{Norton}} \times \frac{R_{\text{Norton}}}{R_{\text{Norton}} + R_L} \quad (1.20)$$

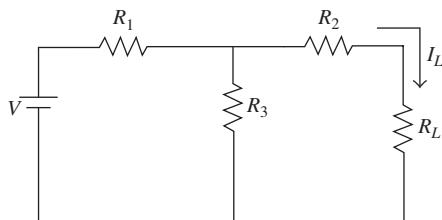


FIGURE 1.13(a) A two-loop network

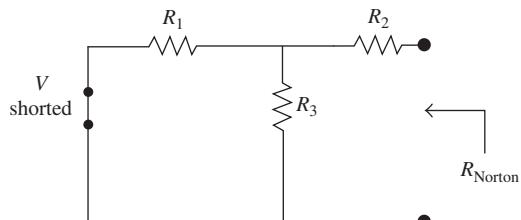


FIGURE 1.13(b) Circuit when R_L is open and V is shorted

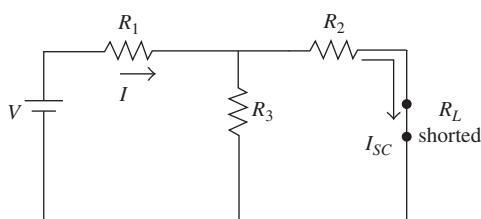


FIGURE 1.13(c) Circuit when R_L is shorted

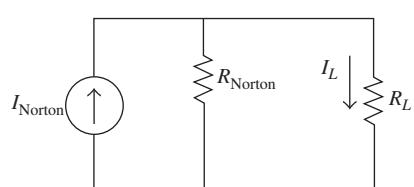


FIGURE 1.13(d) Norton source with its internal resistance and load

E X A M P L E

Example 1.5: Find the current in the 100Ω load for the circuit shown in Fig. 1.14(a), using Norton's theorem.

Solution: To find I_L , first find R_{Norton} . The circuit that enables us to calculate this value is shown in Fig. 1.14(b). Open R_L and short the 10-volt source.

$$R_{\text{Norton}} = 100 + (200||200)$$

$$= 100 + 100 = 200\Omega$$

To find out I_{SC} or I_{Norton} , short the load and find I_{SC} with the 10-volt source connected [see Fig. 1.14(c)].

$$\begin{aligned} I &= \frac{V}{R_1 + \frac{R_2 R_3}{R_2 + R_3}} \\ &= \frac{10}{200 + \frac{100 \times 200}{100 + 200}} \\ &= \frac{10 \times 300}{60000 + 20000} = \frac{3}{80} \text{ A} \end{aligned}$$

$$\begin{aligned} I_{\text{Norton}} &= I \times \frac{R_3}{R_2 + R_3} \\ &= \frac{3}{80} \times \frac{200}{200 + 100} \\ &= \frac{3}{80} \times \frac{2}{3} = 0.025 \text{ A} \end{aligned}$$

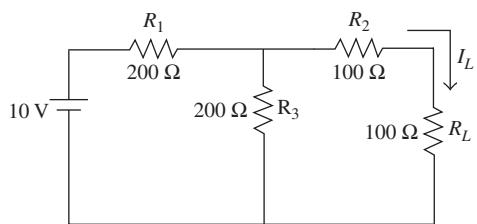


FIGURE 1.14(a) The given two-loop network

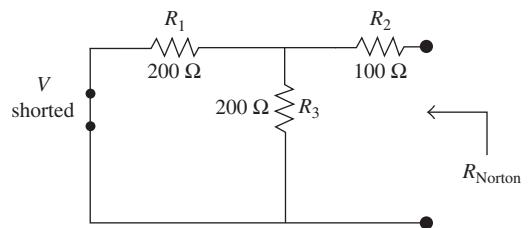


FIGURE 1.14(b) Circuit when R_L is open and V is shorted

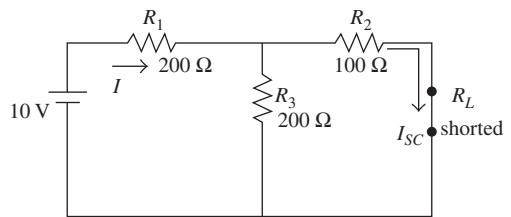


FIGURE 1.14(c) Circuit when R_L is shorted

The Norton source with load is as shown in Fig. 1.14(d). From this simplified circuit:

$$\begin{aligned} I_L &= I_{\text{Norton}} \times \frac{R_{\text{Norton}}}{R_{\text{Norton}} + R_L} \\ &= 0.025 \times \frac{200}{200 + 100} = \frac{0.05}{3} = 0.0167 \text{ A} \end{aligned}$$

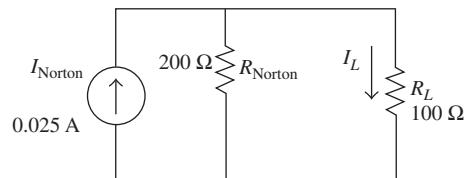


FIGURE 1.14(d) Norton source with its internal resistance and load

1.4 DEVICES, CHARACTERISTICS AND APPLICATIONS

Devices such as diodes and bipolar junction transistors (BJTs) (generally called transistors), field-effect transistors (FETs), metal oxide semiconductor field-effect transistors (MOSFETs) and complementary MOS (CMOS) devices are used both for linear and non-linear and switching applications. A different class of

devices, called relaxation devices, such as tunnel diodes, unijunction transistors (UJT), and *p–n–p–n* diodes are also used in switching applications. The characteristics and applications of some of these devices are briefly discussed here.

1.4.1 Diodes

A diode is a two-terminal device. Diodes can be of different types—a *p–n* junction diode, commonly known as a semiconductor diode; a Zener diode, which is essentially a breakdown diode; *p–n–p–n* diode; a tunnel diode and many more. The principle of working of some of these devices is described in the following subsections.

Semiconductor Diodes or *p–n* Junction Diodes.

Semiconductor diodes are either germanium or silicon diodes. These again could be classified as either signal diodes or power diodes. Signal diodes are used for low-current applications like demodulation or detection whereas power diodes are used in high-current applications such as power supplies. The semiconductor diode is schematically represented as in Fig. 1.15(a). A diode is either forward-biased or reverse-biased. For forward-biassing a diode, the positive terminal of the external battery is connected to the *p*-material (anode, *A*) and the negative terminal of the battery is connected to the *n*-material (cathode, *K*), as shown in Fig. 1.15(b). When the polarity of the battery is reversed, the diode is said to be reverse-biased [see Fig. 1.15(c)].

The V–I characteristics of Ge and Si semiconductor diodes are shown in Fig. 1.15(d). As can be seen from the figure, the forward current, I_F , in the diode is practically zero till V_r (V_r , the cut-in voltage, is 0.1 V for Ge and 0.5 V for Si), beyond which the current rises almost exponentially. However, when reverse-biased, the reverse current (I_R) almost remains constant at I_0 , called the reverse saturation current. I_0 gets doubled for every 10°C rise in temperature. The diode current I is given by the relation:

$$I = I_0(e^{V/\eta V_T} - 1) \approx I_0 e^{V/\eta V_T} \quad (1.21)$$

where I_0 is the reverse saturation current, V_T is the Volt-equivalent of temperature and η is 1 for Ge and 2 for Si. This device is mainly used as a switch. When forward-biased, it can be thought of as a closed switch and when reverse-biased, it can be considered to be an open switch.

Diodes find applications in rectifiers, clipping and clamping circuits, and, in every electronic circuit where they can be used for linear, non-linear and switching applications.

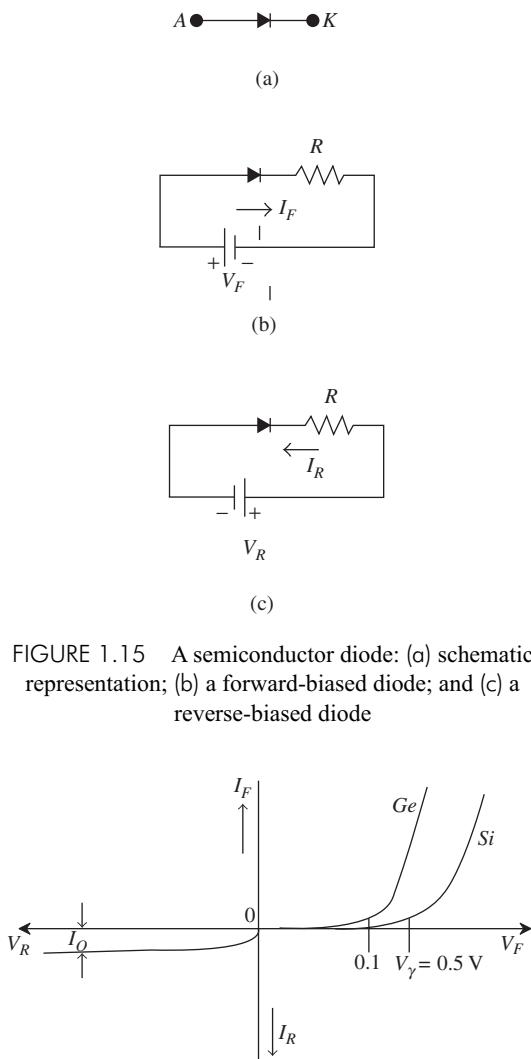


FIGURE 1.15 A semiconductor diode: (a) schematic representation; (b) a forward-biased diode; and (c) a reverse-biased diode

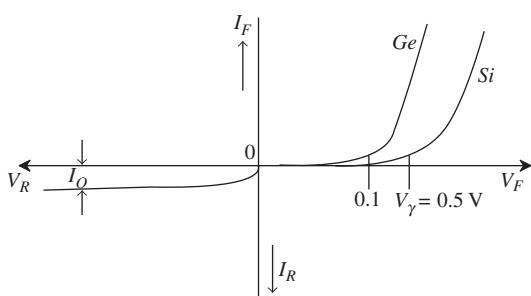


FIGURE 1.15(d) V–I characteristics of Ge and Si semiconductor diodes

Zener Diodes. A Zener diode is a breakdown diode and, when reverse-biased, conducts heavily at the breakdown voltage. Once the device is ON, the voltage between the anode and the cathode remains almost constant. Therefore, a Zener diode is normally used as a reference voltage source. This can also be used as a switch. The schematic representation and a reverse-biased Zener diode are shown in Figs. 1.16(a) and (b), respectively. The V-I characteristics of a practical and an ideal reverse-biased Zener diode are shown in Figs. 1.16(c) and (d) respectively.

When forward-biased, a Zener diode behaves like an ordinary semiconductor diode. However, when reverse-biased and when $V > V_Z$, it is a battery with voltage V_Z . At a voltage V_Z , when reverse-biased, the Zener current suddenly rises to a large value and to limit this current to a safe value, a limiting resistance, R_S is invariably included in the Zener circuit. $I_{Z\min}$ is the minimum Zener current at breakdown and $I_{Z\max}$ is the maximum permitted Zener current. A Zener diode is normally chosen based on $I_{Z\max}$, V_Z and $P_{Z\max}$, where V_Z is the Zener voltage and $P_{Z\max}$ is the dissipation in the device ($P_{Z\max} = V_Z I_{Z\max}$).

Tunnel Diodes. A tunnel diode is another two-terminal device where the p - and n -materials are heavily doped, resulting in a greatly reduced depletion region, which enables charge carriers to tunnel through it. This device exhibits a negative resistance characteristic—when the voltage across the diode increases, the diode current decreases. Tunnel diodes are used in negative resistance or relaxation oscillators. Figures 1.17(a) and (b) show a schematic representation and the V-I characteristics of a tunnel diode.

As shown in Fig. 1.17(b), I_P and I_V are the peak and valley currents, and V_P and V_V are the peak and the valley voltages, respectively. The region from points A to B is termed as the negative resistance region. However, when reverse-biased, it behaves like a resistance. The equivalent circuit of a tunnel diode is given in Fig. 1.17(c).

1.4.2 Bipolar Junction Transistors

The bipolar junction transistor, often simply called a transistor, is a three-terminal device. Transistors are classified as $n-p-n$ and $p-n-p$ transistors, represented in Figs. 1.18(a) and (b) respectively.

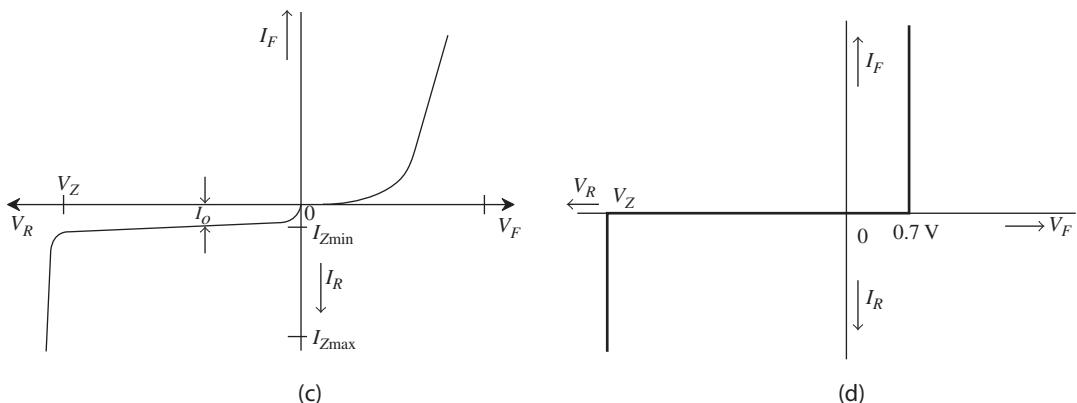


FIGURE 1.16 V-I characteristics of (c) a practical Zener diode; and (d) an ideal Zener diode

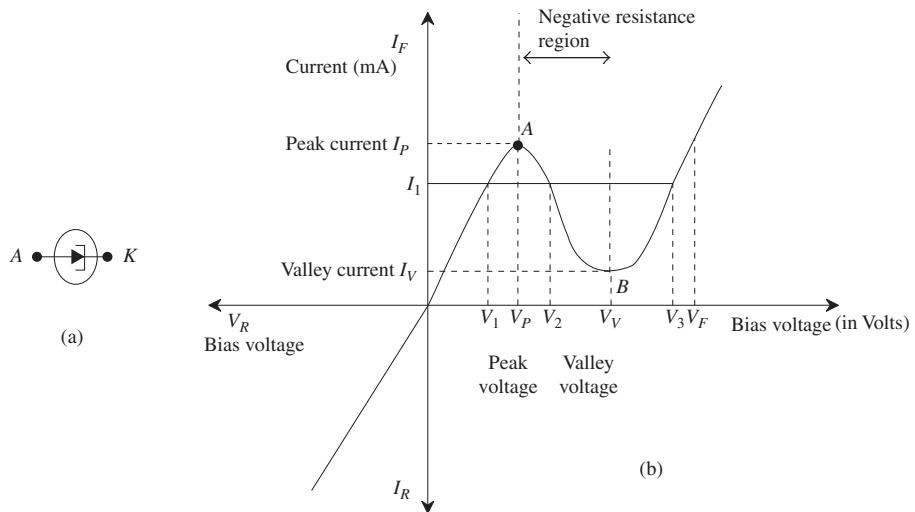


FIGURE 1.17 Tunnel diode: (a) a schematic representation; and (b) V-I characteristics of a tunnel diode

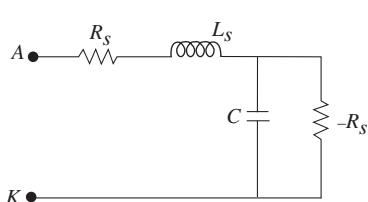
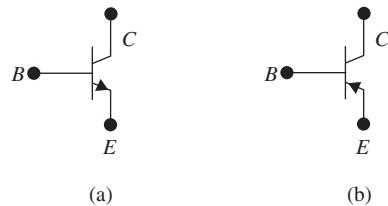
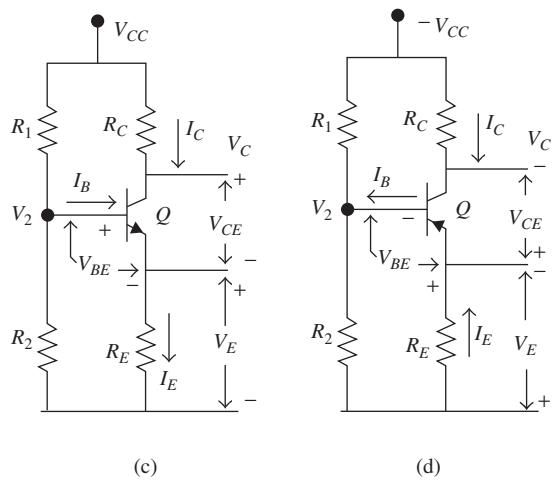


FIGURE 1.17(c) The equivalent circuit of a tunnel diode

A transistor, when used for linear or non-linear applications, is biased in the active region, that is, the base-emitter diode is forward-biased and the base-collector diode is reverse-biased. Under this condition, the device always draws current and this operation is called a class-A operation. The biasing of $n-p-n$ and $p-n-p$ transistors using a single DC source, V_{CC} , is represented in Figs. 1.18(c) and (d) respectively. We select the circuit components and supply voltage such that there is a DC collector current, I_C and a DC collector-to-emitter voltage, V_{CE} . These values specify the coordinates of the operating point, also called the Q -point.

To evaluate the coordinates of the Q -point for the circuit shown in Fig. 1.18(c), calculate V_2 using the following equations:

$$V_2 = V_{CC} \times \frac{R_2}{R_1 + R_2} \quad (1.22)$$

FIGURE 1.18 A schematic representation of bipolar junction transistors: (a) an $n-p-n$ transistor; and (b) a $p-n-p$ transistorFIGURE 1.18(c) Biasing an $n-p-n$ transistor; (d) Biasing a $p-n-p$ transistor

$$V_E = V_2 - V_{BE} \quad \text{and} \quad I_E = \frac{V_E}{R_E} \approx I_C \quad (1.23)$$

We know that

$$V_C = V_{CC} - I_C R_C \quad \text{and} \quad V_{CE} = V_{CC} - I_C (R_C + R_E) \quad (1.24)$$

The polarities of voltages and directions of currents in a *p*-*n*-*p* transistor are opposite to the polarities of voltages and directions of currents in an *n*-*p*-*n* transistor. Hence, *p*-*n*-*p* and *n*-*p*-*n* devices are called complementary devices. Once the dc conditions have been established in the circuit, we use this circuit to amplify ac signals. The purpose of an amplifier, as in a public addressing system, is essentially to amplify complex waveforms—speech signals in this case. As there are varying frequency components and varying amplitudes in such a signal, analysing the behaviour of the amplifier becomes complicated. Therefore, to simplify the analysis, a sinusoidal signal is given as an input to an amplifier and the output is obtained in terms of the input by calculating a quantity known as voltage gain. Keeping the amplitude constant, the frequency of the input signal can be varied to find out the response of the amplifier. This gives us an insight into how the amplifier responds to various frequency components.

1.4.3 Amplifiers

An amplifier refers to a circuit whose output signal is larger than the applied input signal. An amplifier may sometimes be used to drive an electromechanical device such as a relay or a loud speaker. Thus, amplifiers are required to not only have voltage gain but also power gain. Based on this consideration, amplifiers are classified as either voltage amplifiers (small-signal amplifiers) or power amplifiers (large-signal amplifiers).

Consider the output characteristics in Fig. 1.19(a) and the transfer characteristic in Fig. 1.19(b) for the CE configuration, where *Q* is the operating point. If the input sinusoidal swing is small enough to limit the operation to a linear region in the transfer characteristic (between points *X* and *Y*), the output is also sinusoidal. The device is then said to be used as a linear circuit element. If, on the other hand, the input sinusoidal swing takes the operation beyond the *XY* region, the transfer characteristic is non-linear and the output is distorted in amplitude, containing unwanted frequency terms called harmonics. The device is now said to be operated as a non-linear circuit element.

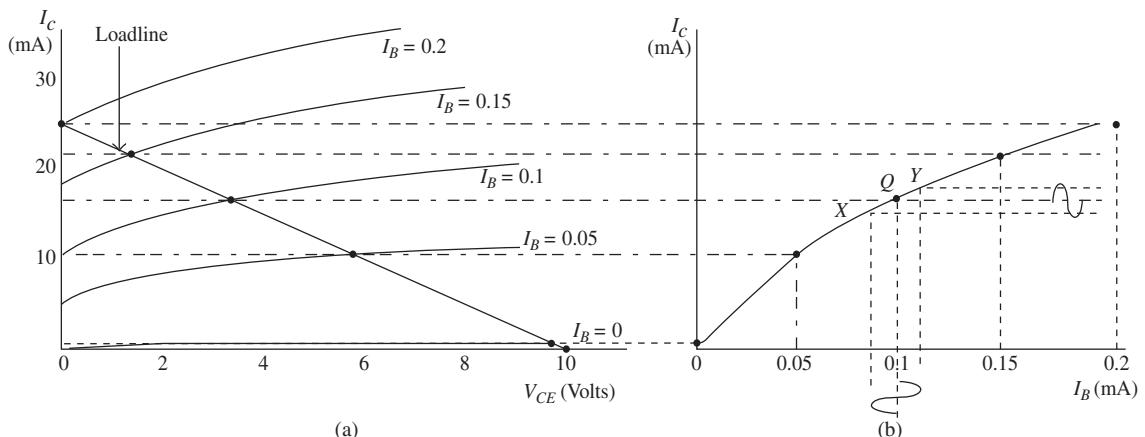


FIGURE 1.19 CE amplifier: (a) output characteristics; (b) transfer characteristic

The output of a voltage amplifier drives the input of a power amplifier. In practice, harmonic distortion is invariably present in the output of a power amplifier. To analyse a linear amplifier, we consider the small-signal low-frequency model of a device (either transistor or FET).

Input and Output Resistances of an Amplifier. Based on the type of input signal applied (voltage or current) and the type of desired output signal (voltage or current), there are four basic amplifier topologies—voltage amplifier, current amplifier, trans-conductance amplifier and trans-resistance amplifier. The first two topologies are shown in Figs. 1.20(a) and (b), respectively.

As the name suggests, in a voltage amplifier [shown in Fig. 1.20(a)], the driving signal is a voltage and the desired signal at the output is also a voltage. This amplifier, as can be seen from the figure, has an input resistance R_i and an output resistance R_o . Now the pertinent question is: Should an amplifier have a large input resistance or a small input resistance? Similarly, should the amplifier, so chosen, have a small or a large output resistance? Obviously, the requirement is dictated by the type of input signal and the desired output signal. In the present case, the driving signal is a voltage and the desired output signal is also a voltage. Hence, R_i should ideally be infinity or significantly higher than the internal resistance of the voltage source, R_S , to ensure that the entire source voltage appears at the actual input terminals of the amplifier. On the other hand, if $R_S = R_i$, then 50 per cent of the signal is lost at the input itself, thereby giving a smaller output voltage. It can be argued on similar lines that for getting a larger output voltage, R_o should be ideally zero or $R_o \ll R_L$.

Figure 1.20(b) shows the circuit for a current amplifier where the driving signal is a current and the desired signal at the output is also a current. In this case, for the entire source current to pass through the input of the amplifier, R_i should ideally be zero or $R_i < R_S$. Similarly, for the entire current in the output ($A_i I_i$) to flow through the load, R_o should be infinity or $R_o \gg R_L$.

The other two amplifier topologies are trans-conductance and trans-resistance amplifiers. Trans-conductance amplifier is one where the output current is proportional to the input voltage of the amplifier. Similarly, trans-resistance amplifier is one where the output voltage is proportional to the input current.

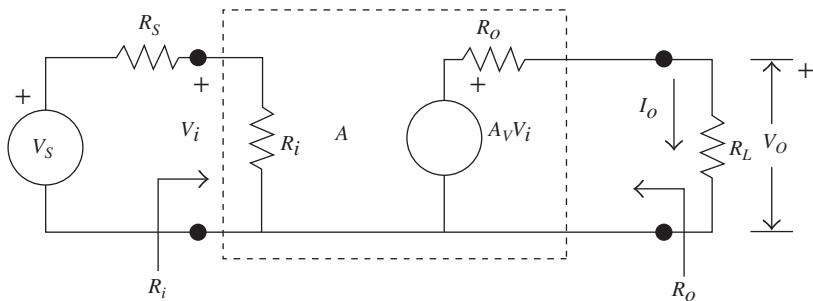


FIGURE 1.20(a) Voltage amplifier

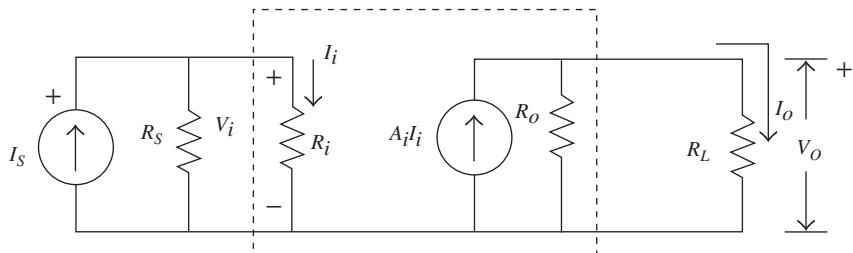


FIGURE 1.20(b) Current amplifier

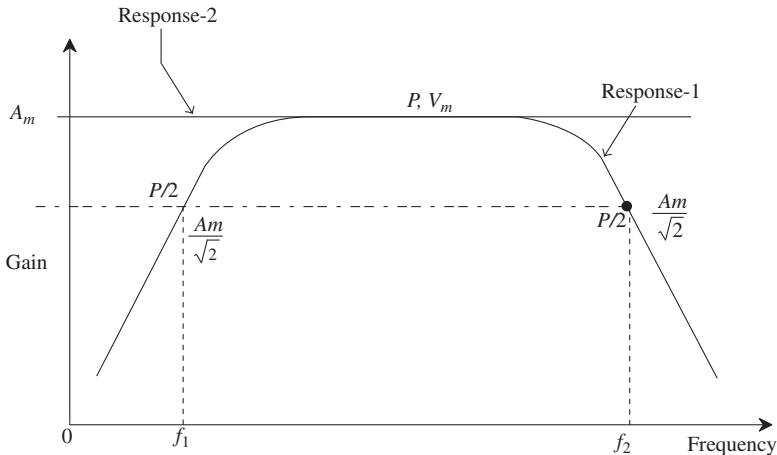


FIGURE 1.21 Frequency-response characteristic

Bandwidth. An amplifier, used for a specific application, is presumed to have the desired bandwidth. Consider the characteristic shown in Fig. 1.21.

Let P be the power in the mid-band (V_m is the voltage). Here, two frequencies, f_1 and f_2 are identified at which the power is $P/2$ (the corresponding voltage is $V_m/\sqrt{2}$) — half of the power that is available in the mid-band range, P . Hence, these two frequencies are called the half-power frequencies. As $10 \log_{10} P/(P/2) = 3$ dB, the frequencies f_1 and f_2 are also called 3-dB frequencies. The difference between these two frequencies ($f_2 - f_1$) is called the power bandwidth; that is, if the amplifier is operated within this frequency range ($f_2 - f_1$), called the bandwidth, the output remains almost constant. For frequencies below f_1 and above f_2 , the output falls off rapidly. If there are successive frequency components at the input, one corresponding to the mid-band range and the other beyond f_2 or below f_1 , the output fluctuates by a great amount and, if heard on a loud speaker, will be irritating to the human ear. Hence, it is always advisable to use the amplifier in the frequency range f_1 to f_2 . Ideally an amplifier should have a flat frequency response (Response-2). As the inter-stage coupling uses reactive elements, the response is not necessarily a flat response characteristic (Response-1). However, if direct coupling is used in an amplifier, as in an operational amplifier, one can get a flat frequency-response characteristic right from zero cycles (DC).

1.4.4 The Three Basic Amplifiers

The three basic amplifier configurations are (a) common-emitter configuration (CE); (b) common-collector configuration (CC); and (c) common-base configuration (CB). In this section, we discuss these different types of amplifier configurations and find the input resistance (R_i), the output resistance (R_O) and the voltage gain (A), which are called the performance quantities, for each configuration.

The basic amplifier circuit is shown in Fig. 1.22(a). The moment we call this circuit an amplifier, it means that it amplifies alternating voltages and the output is larger than the input. In order to establish dc conditions, we consider the dc circuit. The dc circuit is drawn from Fig. 1.22(a), by considering only the dc source and eliminating the condensers because once the condenser is charged, it behaves as an open circuit for dc. The resultant dc circuit is as shown in Fig. 1.22(b).

I_C and V_C can be evaluated using the DC circuit. Now, to evaluate the output for a given ac input (sinusoidal in the simplest case), the ac circuit is drawn. The ac circuit is drawn by short circuiting the dc source and replacing the condensers ideally by short circuits (because the condensers are chosen such that they

behave ideally as short circuits in the frequency range of operation). The resultant ac circuit of Fig. 1.22(a) is shown in Fig. 1.22(c) and the simplified circuit is shown in Fig. 1.22(d).

Using Fig. 1.22(d), the output v_o that appears across R_C cannot be evaluated. To calculate v_o , the transistor has to be replaced by its equivalent circuit. The popular method of replacing the transistor by its equivalent electrical circuit at low frequencies and under small-signal conditions is by using the h -parameter model.

***h*-Parameter Model of a Transistor.** In the analysis of transistor circuits, the transistor is required to be replaced by its equivalent electrical circuit. Consider a transistor in a two-port network as shown in Fig. 1.23(a). In the network shown in Fig. 1.23(a), let us represent V_1 and I_2 as:

$$V_1 = h_i I_1 + h_r V_2 \quad (1.25)$$

$$I_2 = h_f I_1 + h_o V_2 \quad (1.26)$$

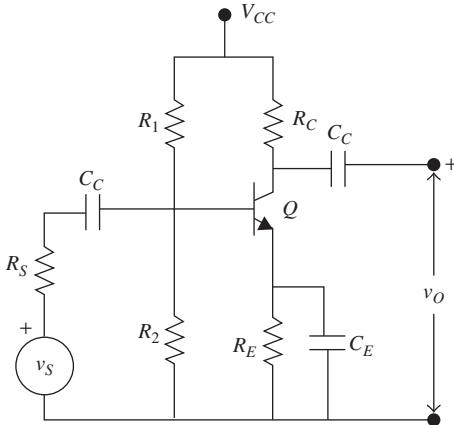


FIGURE 1.22(a) Amplifier circuit

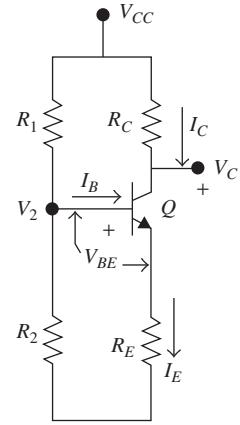


FIGURE 1.22(b) DC or biasing circuit

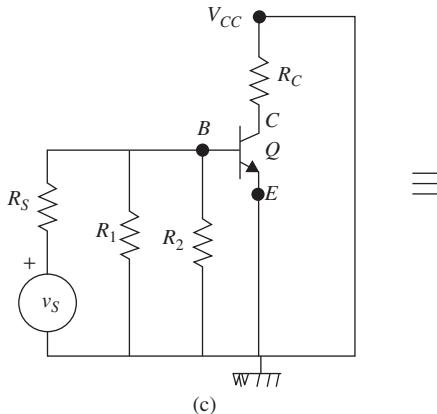


FIGURE 1.22(c) AC circuit of the amplifier in Fig. 1.22(a)

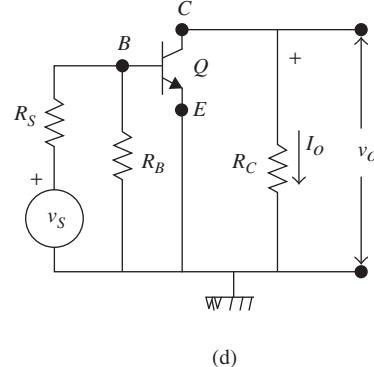


FIGURE 1.22(d) Simplified circuit of Fig. 1.22(c)

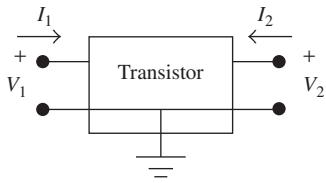


FIGURE 1.23(a) A transistor in a two-port network

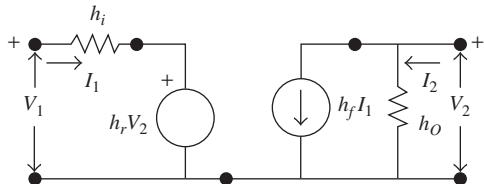


FIGURE 1.23(b) Low-frequency, small-signal model of the transistor

Using Eqs. (1.25) and (1.26), the equivalent circuit is drawn as in Fig. 1.23(b). These equations can be used to evaluate the h -parameters using the relations:

$$\text{Input resistance, } h_i = \frac{V_1}{I_1} \Big| V_2 = 0,$$

$$\text{Reverse transmission gain, } h_r = \frac{V_1}{V_2} \Big| I_1 = 0,$$

$$\text{Forward current gain, } h_f = \frac{I_2}{I_1} \Big| V_2 = 0,$$

$$\text{Output admittance, } h_o = \frac{I_2}{V_2} \Big| I_1 = 0,$$

These parameters are called h_{ie} , h_{re} , h_{fe} and h_{oe} for the common-emitter (CE) configuration; h_{ic} , h_{rc} , h_{fc} and h_{oc} for the common-collector (CC) configuration and h_{ib} , h_{rb} , h_{fb} and h_{ob} for the common-base (CB) configuration. It is possible to convert these parameters from one form to the other (see Appendix A). In the equivalent circuit in Fig. 1.23(b), assuming CE configuration, if $h_{re} V_2 \ll h_{ie} I_b$, the equivalent circuit reduces to that shown in Fig. 1.23(c). Here, if $1/h_{oe} \rightarrow \infty$, the equivalent circuit further reduces to that shown in Fig. 1.23(d).

CE Configuration. The amplifier circuit in Fig. 1.22(a) is a CE amplifier as the emitter is the common terminal between the input and the output and its ac circuit is given in Fig. 1.22(d). Replacing the transistor between the base, collector and emitter terminals by the equivalent circuit in Fig. 1.22(d) and assuming $R_B \gg h_{ie}$, the circuit reduces to that shown in Fig. 1.24(a).

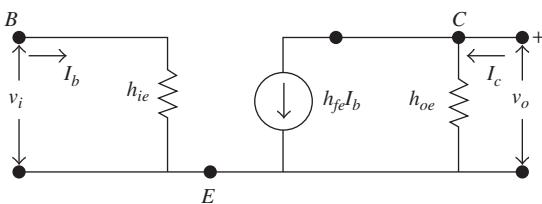


FIGURE 1.23(c) Simplified equivalent circuit of Fig. 1.23(b)

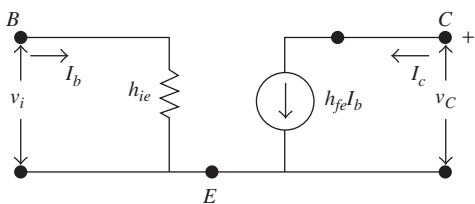


FIGURE 1.23(d) Approximate low-frequency small-signal model of the transistor

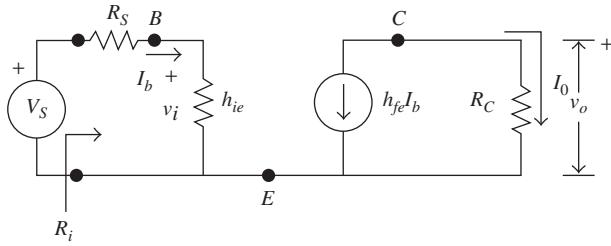


FIGURE 1.24(a) Equivalent circuit of Fig. 1.22(d)

For the circuit in Fig. 1.22(d), using the equivalent circuit in Fig. 1.24(a), v_o is calculated in terms of v_i to calculate the gain, A .

$$A = \frac{v_o}{v_i} = \frac{-h_{fe} I_b R_C}{h_{ie} I_b} = \frac{-h_{fe} R_C}{h_{ie}} \quad (1.27)$$

$$R_i = \frac{v_i}{I_b} = h_{ie} \quad (1.28)$$

Example 1.6 elucidates how these relations can be applied to real circuits.

E X A M P L E

Example 1.6: If for a transistor, $h_{ie} = 1.1 \text{ k}\Omega$, $h_{fe} = 50$, $h_{oe} = 25 \times 10^{-6} \text{ V}$ and $R_C = 2.2 \text{ k}\Omega$, find A , R_i and R_o .

Solution: Using Eqs.(1.27) and (1.28),

$$A = \frac{-50 \times 2.2 \times 10^3}{1.1 \times 10^3} = -110 \quad \text{and} \quad R_i = h_{ie} = 1.1 \text{ k}\Omega.$$

R_o , the output resistance, is infinity because when we open the load and look into the output terminals we encounter an ideal current source whose internal resistance ($1/h_{oe}$) is assumed to be infinity.

Considering h_{oe} , $R_o = 1/h_{oe} = 1/25 \times 10^{-6} = 40 \text{ k}\Omega$

Equation (1.27) gives the voltage gain of the CE amplifier. In the circuit of Fig. 1.22(a), R_E is included in series with the emitter to provide bias stability; that is, I_C and V_C remain unaltered inspite of temperature variations. However, under ac conditions, connecting a large condenser C_E in shunt with R_E ensures that the emitter is at the ground potential resulting in a CE amplifier. C_E behaves ideally as a short circuit providing a low-resistance path for the flow of an ac component of current and hence, is called the bypass condenser. A common-emitter amplifier with un-bypassed emitter resistance is shown in Fig. 1.24(b). The equivalent ac circuit of Fig. 1.24(b) is drawn in Fig. 1.24(c).

From the circuit in Fig. 1.24(c):

$$v_o = -h_{fe} I_b R_C \quad (1.29)$$

$$v_i = (h_{ie} + R_E) I_b + h_{fe} I_b R_E = [(h_{ie} + (1 + h_{fe}) R_E) I_b] \quad (1.30)$$

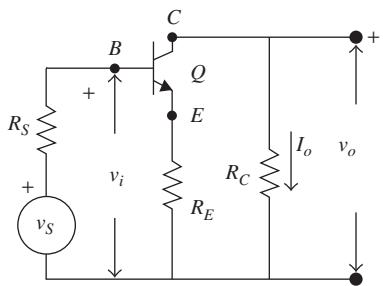


FIGURE 1.24(b) Common-emitter amplifier with un-bypassed emitter resistance

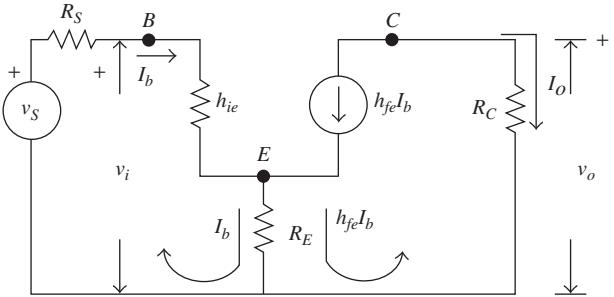


FIGURE 1.24(c) Equivalent circuit of the amplifier in Fig. 1.24(b)

From Eqs. (1.29) and (1.30), the gain is:

$$A = \frac{v_o}{v_i} = \frac{-h_{fe}I_b R_C}{[h_{ie} + (1 + h_{fe})R_E]I_b} = \frac{-h_{fe}R_C}{[h_{ie} + (1 + h_{fe})R_E]} \quad (1.31)$$

$$R_i = \frac{v_i}{I_b} = \frac{[h_{ie} + (1 + h_{fe})R_E]I_b}{I_b} = h_{ie} + (1 + h_{fe})R_E \quad (1.32)$$

EXAMPLE

Example 1.7: If for a transistor $h_{ie} = 1.1 \text{ k}\Omega$, $h_{fe} = 50$, $R_E = 1 \text{ k}\Omega$, and $R_C = 2.2 \text{ k}\Omega$, calculate the gain, input and output resistances.

Solution: Using Eqs. (1.31) and (1.32):

$$A = \frac{-50 \times 2.2 \times 10^3}{1.1 \times 10^3 + (1 + 50)1 \times 10^3} = -2.11$$

$$R_i = 1.1 + (1 + 50)1 = 52.1 \text{ k}\Omega$$

R_o , the output resistance, is infinity.

A comparison of Eqs. (1.27) and (1.31) shows that the gain in the amplifier with un-bypassed emitter resistance is very small when compared to the gain of a CE amplifier. In the CE amplifier, a part of the output is fed back to the input (ac voltage drop across R_E is the feedback signal), which reduces the actual signal at the amplifier input terminals. Thus, the CE amplifier shown in Fig. 1.24(b) is called a feedback amplifier. However, the input resistance of the amplifier in Fig. 1.24(b) is significantly larger.

A Common-collector Amplifier or an Emitter Follower. Instead of considering the emitter as the common terminal between the input and the output, let us consider an amplifier in which the collector terminal is common between the input and the output. Such an amplifier is called the common-collector amplifier [see Fig. 1.25(a)]. Though in this amplifier the collector is common between the input and the output, the fact is not obvious in the circuit shown in Fig. 1.25(a).

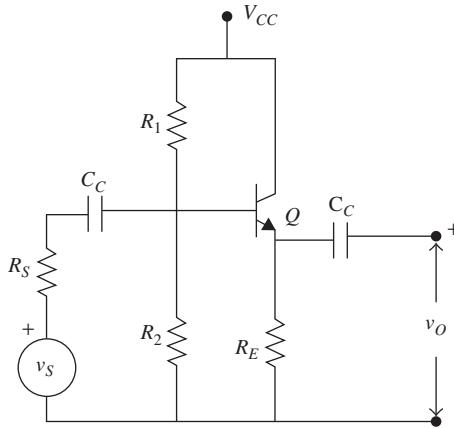


FIGURE 1.25(a) Common-collector amplifier or emitter follower

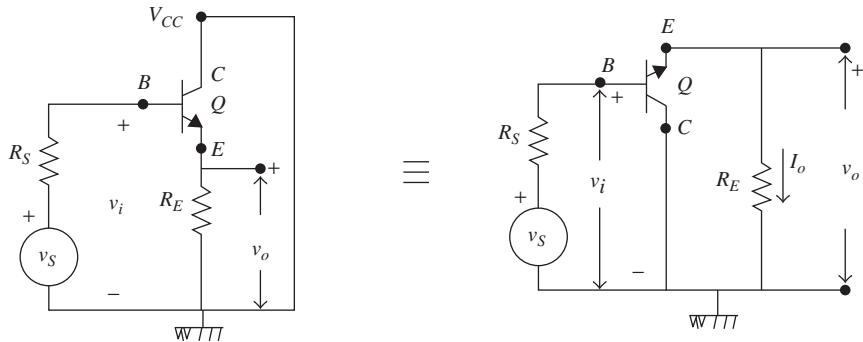


FIGURE 1.25(b) AC circuit of Fig. 1.25(a)

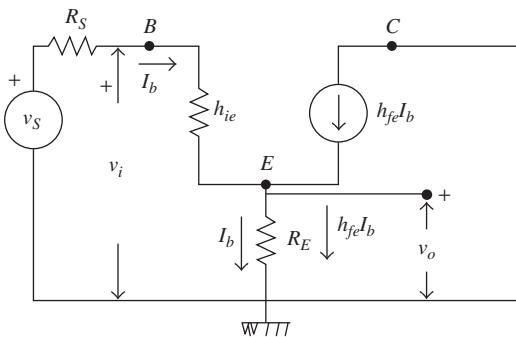


FIGURE 1.25(c) Equivalent circuit of Fig. 1.25(a)

$R_1 \parallel R_2$ is considered large and is omitted.

To calculate the gain of this amplifier, the ac circuit is drawn as shown in Fig. 1.25(b). $R_1 \parallel R_2$ is considered large and is omitted. From this circuit, it is evident that the collector is the common terminal and, hence, the name common-collector amplifier. Replacing the transistor by its equivalent circuit [see Fig. 1.25(c)], the gain, and input and output resistances are calculated.

$$v_o = (1 + h_{fe})I_b R_E \cong h_{fe} I_b R_E$$

$$v_i = [h_{ie} + (1 + h_{fe})R_E]I_b$$

$$A = \frac{v_o}{v_i} = \frac{h_{fe}I_b R_E}{[h_{ie} + (1 + h_{fe})R_E]I_b} = \frac{h_{fe}R_E}{[h_{ie} + (1 + h_{fe})R_E]} \approx 1 \quad (1.33)$$

Since, $h_{ie} \ll (1 + h_{fe})R_E$ and $1 \ll h_{fe}$,

$$R_i = h_{ie} + (1 + h_{fe})R_E \quad (1.34)$$

$$R_o = \frac{h_{ie}}{h_{fe}} \quad (1.35)$$

EXAMPLE

Example 1.8: For the emitter follower in Fig. 1.25(b), $h_{ie} = 1.1 \text{ k}\Omega$, $h_{fe} = 50$, $R_E = 1 \text{ k}\Omega$. Calculate the voltage gain, input resistance and the output resistance.

Solution: From Eq. (1.33):

$$A = \frac{h_{fe}R_E}{[h_{ie} + (1 + h_{fe})R_E]} = \frac{50 \times 1}{1.1 + (1 + 50) \times 1} = \frac{50}{52.1} = 0.96$$

From Eq. (1.34):

$$R_i = h_{ie} + (1 + h_{fe})R_E = 1.1 + (1 + 50)1 = 52.1 \text{ k}\Omega$$

From Eq. (1.35):

$$R_o = \frac{h_{ie}}{h_{fe}} = \frac{1100}{50} = 22 \Omega$$

As seen in Example 1.8, the voltage gain is unity ($A = 1$) in a common-collector amplifier. This means that the voltage at the emitter is the same as the voltage at the base and these two voltages are in the same phase. Hence, this amplifier is also called an emitter follower, i.e., the emitter follows the base.

Also, the emitter follower has a large input resistance and small output resistance. Since the voltage gain is 1 (in practice, it is less than 1), the term *amplifier* may not be appropriate here as, in principle, the output of a circuit that is called an amplifier should be larger than the input. However, this circuit is still used as a buffer amplifier to transmit the input signal to the output terminals with the same phase and with almost the same magnitude. This buffer amplifier offers several advantages. Consider the CE amplifier shown in Fig. 1.26. In this figure,

$$v_i = v_s R_i / (R_s + R_i) = v_s / 2, \quad \text{if } R_i = R_s.$$

This means, though a signal of v_s is applied at the input, only $v_s/2$ appears between the actual input terminals of the amplifier. That is, 50 per cent of the signal is lost at the input, because of the small input resistance of the amplifier. Further, $A_V v_i = A_V \times v_s / 2$. If $R_o = R_L$:

$$v_o = A_V \frac{v_s}{2} \times \frac{R_L}{R_o + R_L} = A_V \frac{v_s}{2} \times \frac{R_L}{R_L + R_L} = \frac{A_V v_s}{4}$$

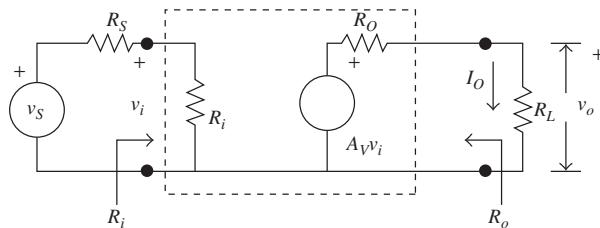


FIGURE 1.26 A CE amplifier

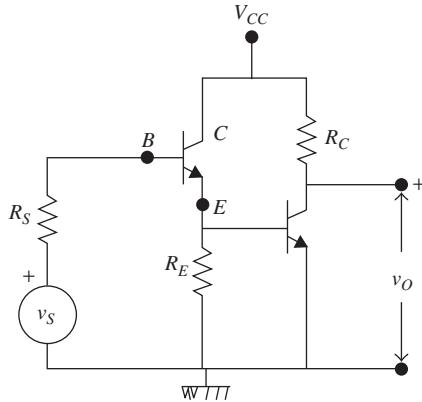


FIGURE 1.27 CC amplifier as an input stage to CE amplifier

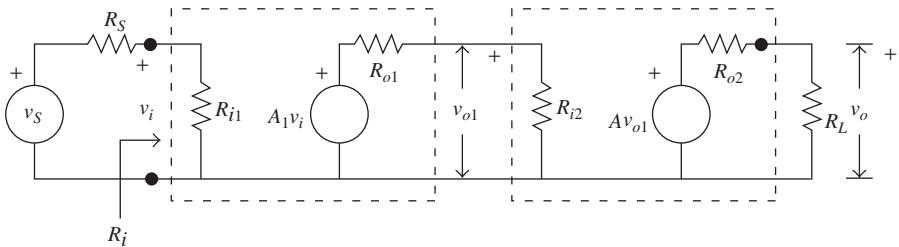


FIGURE 1.28 ac circuit of Fig. 1.27

If a CC amplifier is connected as an input stage to a CE amplifier (see Figs. 1.27 and 1.28), from Fig. 1.27 we have:

$$v_i = \frac{v_s \times R_{i1}}{R_s + R_{i1}} \approx v_s \quad (\text{since } R_{i1} \gg R_s)$$

As $A_1 = 1$, $A_1 v_i = v_s$.

$$v_{o1} = \frac{v_s \times R_{i2}}{R_{o1} + R_{i2}}$$

As $R_{o1} \ll R_{i2}$, $v_{o1} \approx v_s$.

$$A v_{o1} = A v_s$$

$$v_o = A v_s \frac{R_L}{R_{o2} + R_L} = \frac{A v_s}{2} \quad (\text{if } R_{o2} = R_L)$$

Thus, using a CC amplifier as a pre-amplifier, for the same input (v_s), the output increases from $A v_s/4$ to $A v_s/2$. Consider another CC amplifier at the output of a CE amplifier as shown in Fig. 1.29.

The output of the second stage, $A v_s$, serves as the input to the CC amplifier. The equivalent circuit is shown in Fig. 1.30. As the input to the last stage, which is an emitter follower, $v_{i2} = A v_s$, since $R_{i3} \gg R_{o2}$. Also as $A_3 = 1$,

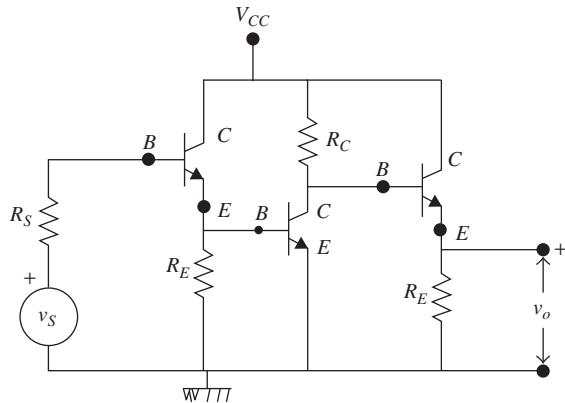


FIGURE 1.29 CE amplifier with CC amplifier at the output stage

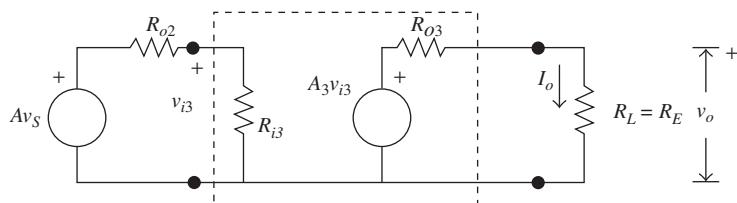


FIGURE 1.30 Equivalent circuit from Fig. 1.29

$$v_o = \frac{Av_s \times R_L}{R_{o3} + R_L} = Av_s, \quad \text{since} \quad R_L = R_E >> R_{o3}$$

Thus, the output of a CE amplifier increases from $Av_s/4$ to $Av_s/2$ to Av_s with a CC pre-amplification stage and a third output CC amplification stage, respectively. Thus the output is larger when using CC stage as a buffer amplifier. To understand this better, let us consider Example 1.9.

EXAMPLE

Example 1.9: For the circuit in Fig. 1.26, calculate the output if $V_s = 10 \text{ mV}$, $R_s = 1\text{k}\Omega$, $R_i = 1\text{k}\Omega$, $A = 100$, $R_o = 5\text{k}\Omega$ and $R_L = 5\text{k}\Omega$.

Solution:

$$V_i = \frac{10 \text{ mV} \times 1 \text{ k}\Omega}{1 \text{ k}\Omega + 1 \text{ k}\Omega} = 5 \text{ mV}$$

- (a) This means, though a signal of 10 mV is applied at the input of the amplifier, only 5 mV appears between the actual input terminals of the amplifier. That is, 50 per cent of the signal is lost at the input itself because of small input resistance of the amplifier.

Since $A = 100$, $A V_i = 100 \times 5 \text{ mV} = 500 \text{ mV}$. If $R_o = 5 \text{ k}\Omega$ and $R_I = 5 \text{ k}\Omega$:

$$V_o = AV_i \times \frac{R_L}{R_o + R_L} = 500 \text{ mV} \times \frac{5 \text{ K}}{5 \text{ K} + 5 \text{ K}} = 250 \text{ mV}$$

Though the entire output voltage of 500 mV should appear across R_L , due to appreciable output resistance, V_o is only 250 mV.

- (b) If now a CC amplifier is connected as a pre-amplifier to CE amplifier for which $R_{o1} = 20 \Omega$, $R_{i1} = 52 \text{ k}\Omega$ (see Figs. 1.27 and 1.28) the output calculated as under.

$$\text{If } V_s = 10 \text{ mV}, R_s = 1 \text{ k}\Omega, R_i = 52 \text{ k}\Omega \text{ then } V_i = \frac{10 \text{ mV} \times 52 \text{ k}\Omega}{1 \text{ k}\Omega + 52 \text{ k}\Omega} = 10 \text{ mV}$$

As $A_1 = 1$, $A_1 V_i = 10 \text{ mV}$

$$V_{o1} = 10 \times \frac{1.1 \text{ k}\Omega}{0.02 \text{ k}\Omega + 1.1 \text{ k}} \approx 10 \text{ mV}$$

As $A = 100$, $AV_{o1} = 1000 \text{ mV}$

$$V_o = 1000 \times \frac{5 \text{ k}\Omega}{5 \text{ k}\Omega + 5 \text{ k}\Omega} = 500 \text{ mV}$$

Thus, by providing a CC amplifier as a pre-amplifier, for the same input V_s ($=10 \text{ mV}$), the output now is 500 mV. Earlier it was only 250 mV.

- (c) Now consider another CC amplifier at the output of a CE amplifier, (see Fig. 1.29). We have seen that the output of the second stage is 1000 mV. This is connected as input to CC amplifier. The equivalent circuit is shown in Fig. 1.30. So, $R_{o2} = 5 \text{ K}$, $R_{i3} = 52 \text{ K}$, $V_{i3} = 1000 \text{ mV}$, $V_o = A_3 V_{i3} \approx 1000 \text{ mV}$, since $R_{o3} = 20 \Omega$, $R_E = 2 \text{ k}\Omega$. Thus, the output is significantly larger here. From these calculations, we understand the importance of a CC amplifier.

However, in many applications, even when using a transistor, a very large input resistance is needed. The input resistance of the emitter follower seen was only $52 \text{ k}\Omega$. If we want a larger input resistance, as in the case of Bootstrap sweep generator (to be discussed later), we prefer a Darlington pair, which is manufactured as a single transistor [see Fig. 1.31(a)]. The advantage of a Darlington pair is that the h_{fe} of the composite pair is the product of $h_{fe1}h_{fe2}$ and is very large. The Darlington emitter follower is shown in Fig. 1.31(b). The h_{fe} of the Darlington pair is $h_{fe} = h_{fe1}h_{fe2}$ and the input resistance of the Darlington emitter follower is $h_{fe1}h_{fe2}R_E = 50 \times 50 \times 2 \text{ k}\Omega = 5 \text{ M}\Omega$

Thus, if there is a need to derive a transistor circuit that provides large input resistance, a Darlington emitter follower is a possible answer.

Common-base Amplifier. A common-base amplifier is shown in Fig. 1.32(a). In this amplifier, we see that the base is common between the input and the output. The ac circuit is shown in Fig. 1.32(b). In this figure:

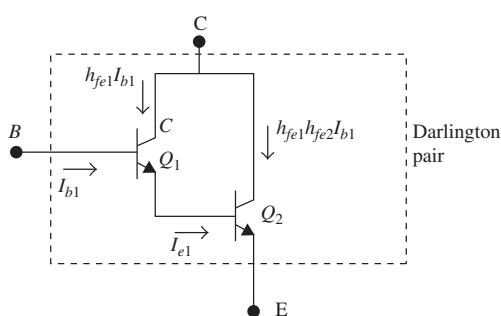


FIGURE 1.31(a) A Darlington pair

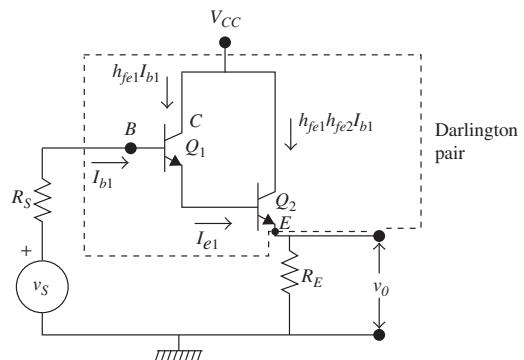


FIGURE 1.31(b) Darlington emitter follower

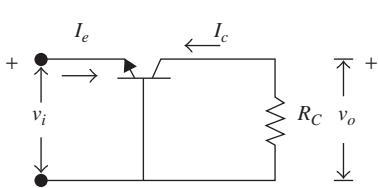


FIGURE 1.32(a) A CB amplifier

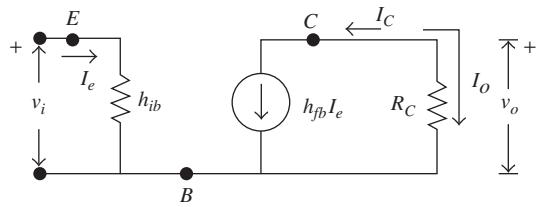


FIGURE 1.32(b) AC circuit of Fig. 1.32(a)

$$A = \frac{v_o}{v_i} = \frac{-h_{fb}R_C}{h_{ib}} \quad (1.36)$$

$$R_i = \frac{v_i}{I_e} = h_{ib} \quad (1.37)$$

$$R_o = \frac{1}{h_{ob} - \left(\frac{h_{fb}h_{rb}}{h_{ib}} \right)} \quad (1.38)$$

To understand the procedure to calculate these quantities let us consider an example.

E X A M P L E

Example 1.10: For the CB amplifier in Fig. 1.32(a) using the equivalent circuit in Fig. 1.32(b), calculate A , R_i and R_o . If, $h_{fb} = -0.991$, $R_C = 2 \text{ k}\Omega$, $h_{ib} = 14.55 \Omega$, $h_{ob} = 0.18\mu\text{V}$, $h_{rb} = 0.883 \times 10^{-4}$.

From Eq. (1.36):

$$A = \frac{v_o}{v_i} = \frac{-h_{fb}R_C}{h_{ib}} = \frac{-0.991 \times 2 \text{ k}\Omega}{14.55 \Omega} = 136.22$$

From Eq. (1.37):

$$R_i = \frac{v_i}{I_e} = 14.55 \Omega$$

From Eq. (1.38):

$$R_o = \frac{1}{h_{ob} - \left(\frac{h_{fb}h_{rb}}{h_{ib}} \right)} = \frac{1}{0.18 \times 10^{-6} - \left[\frac{(-0.991)(0.883 \times 10^{-4})}{14.55} \right]} = \frac{1000}{6.2} = 161.3 \text{ k}\Omega$$

Thus, a CB amplifier has a current gain less than 1, but has a large voltage gain, small input resistance and large output resistance. There is no phase shift in this amplifier. Table 1.1 gives the typical values of the parameters and a comparison between these three configurations.

From Table 1.1, it can be seen that both CE and CB configurations have a large voltage gain. The input resistance of the CB configuration is very small whereas that of the CC configuration is very large. The voltage gain of the CC configuration is unity whereas its current gain is large. This suggests that the CC configuration can be also used as a power amplifier. The current gain of the CB configuration is unity. The output resistance of the CC configuration is very small and that of the CB configuration is very large. Thus, it is possible to cascade these amplifier configurations to get a desired signal at the output.

TABLE 1.1 A comparison of CE, CC and CB configurations.

Parameter	CE	CB	CC
R_i	Medium ($\approx 1 \text{ k}\Omega$)	Low (20Ω)	High ($50 \text{ k}\Omega$)
R_o	Medium ($\approx 40 \text{ k}\Omega$)	Very high ($150 \text{ k}\Omega$)	Low (20Ω)
A_I	High (50)	Low (≈ 1)	High (-51)
A_V	High (≈ -200)	High (≈ 200)	Low (≈ 1)

1.4.5 Multi-stage Amplifiers

As the gain of a single-stage amplifier is limited, in order to derive a larger output voltage, there arises the need to cascade a number of amplifier stages; that is, the output of one amplifier is connected as input to the next stage, as shown in Fig. 1.33. In such a case, the overall gain of the cascaded configuration is the product of the individual gains.

$$A_V = A_{V1} \cdot A_{V2} \cdot A_{V3} \cdots A_{Vn} \quad (1.39)$$

There are three basic methods of interconnecting the output of one stage to the input of the next stage:

1. *RC* coupling: The resultant amplifier is called an *RC*-coupled amplifier.
2. Transformer coupling: The amplifier is called a transformer-coupled amplifier.
3. Direct coupling: The amplifier is called a direct-coupled (DC) amplifier.

The advantage of an *RC*-coupled amplifier is that it is simple and easy to implement. The coupling condenser blocks the dc. Consequently, only the ac signal is connected to the input of the next stage. But the disadvantage is that it has a poor low-frequency response. An *RC*-coupled amplifier and its frequency-response characteristic are shown in Figs. 1.34 and 1.35, respectively.

The mid-band gain (A_m) remains constant, whereas the gain at low frequencies and at high frequencies changes as per the relations in Eqs. (1.40) and (1.41), respectively.

$$A_l = \frac{A_m}{1 + j \frac{\omega_1}{\omega}} \quad (1.40)$$

$$\text{and } A_h = \frac{A_m}{1 + j \frac{\omega_2}{\omega}} \quad (1.41)$$

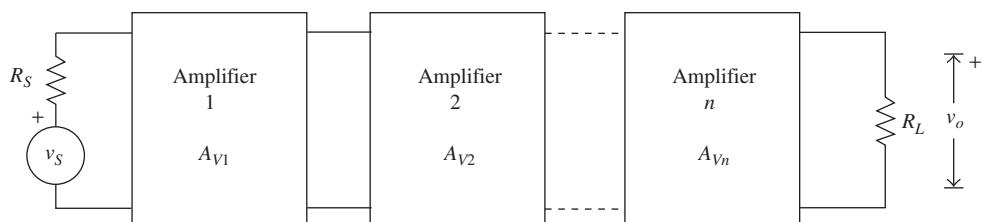
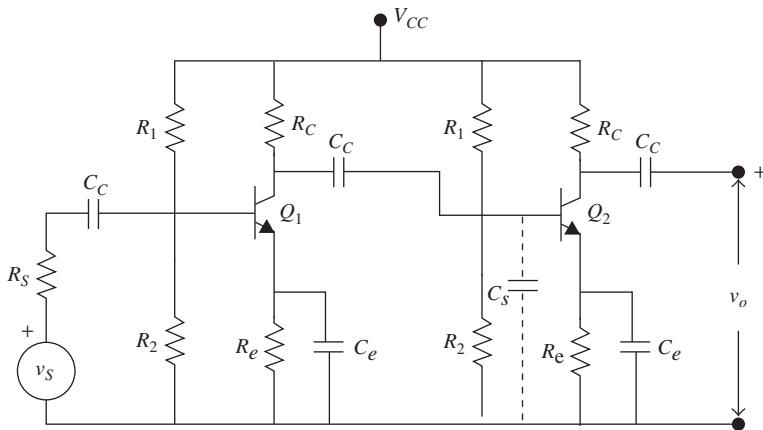


FIGURE 1.33 Cascaded amplifier configuration

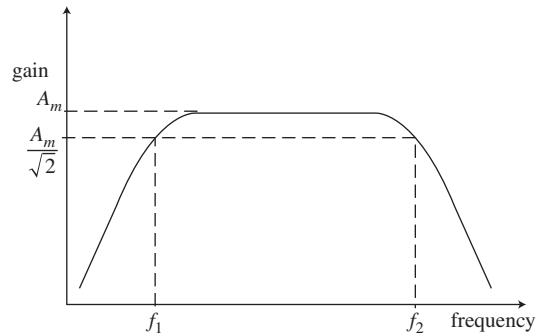
FIGURE 1.34 A two-stage RC -coupled amplifier

ω_1 is the lower half-power frequency and ω_2 is the upper half-power frequency. The low-frequency response tends to be poor because of the coupling condenser, C_C and the high-frequency response becomes poor because of the shunt condenser, C_S .

Another amplifier is the transformer-coupled amplifier shown in Fig. 1.36. In this amplifier also, the transformer blocks the dc and the output is an ac component. However, the problem is that a transformer is a lossy element. Further, when used in the audio-frequency range, it becomes bulky as the transformer is wound on an iron core. Hence, transformer coupling is not preferred in the audio-frequency range and is used only in the radio-frequency range. It should also be noted that there exists a distributed capacitance between the transformer windings which gives rise to resonance, thereby increasing the gain in a narrow frequency band.

The third type of amplifier is the direct-coupled amplifier in which the output of one stage is connected directly to the input of the next stage without using reactive elements such as capacitors and inductors [see Fig. 1.37(a)]. The advantage here is a flat frequency-response characteristic right from zero cycles (dc), as shown in Fig. 1.37(b).

In a direct-coupled amplifier, both ac and dc are coupled to the input of the next stage. So properly biasing each of the devices is necessary. Further, the output is referenced to V_C , the dc voltage at the collector. However, in many applications, the requirement is that the output should be referenced to a zero level, in which case, a single-supply dc amplifier will not do the job. Here we need a two-supply (+ve and -ve supply) DC amplifier in which it is possible to reference the output to the zero level by incorporating level translation. However, one major drawback with dc amplifiers is the problem of drift. Under quiescent conditions, let the DC voltage at the output be V_C (say 7.5 V). If for some reason, the parameters of the device change, say h_{FE} increases which leads to an increase in I_C , V_C decreases (say, 7.0 V). But any change in V_C is expected to occur only when an input signal is present. In the present situation, V_C has decreased due to an increase in h_{FE} ; this decrease in V_C , normally, could be construed as a change occurring due to a signal present at the input. However, in practice, V_C has actually reduced due to increasing h_{FE} . This problem is called drift in DC amplifiers. Temperature compensation is provided in the circuit to take care of the problem of drift to make

FIGURE 1.35 Frequency-response characteristic of an RC -coupled amplifier

the dc amplifiers the best amplifiers. For this reason, direct-coupled amplifiers are fabricated as integrated circuits, for example, operational amplifiers.

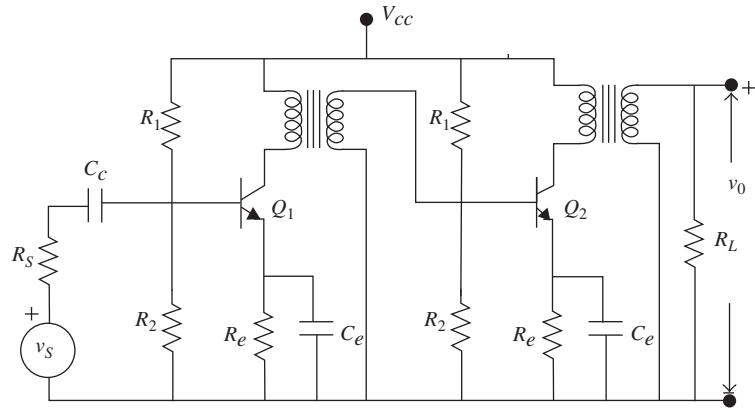


FIGURE 1.36 Two-stage transformer-coupled amplifier

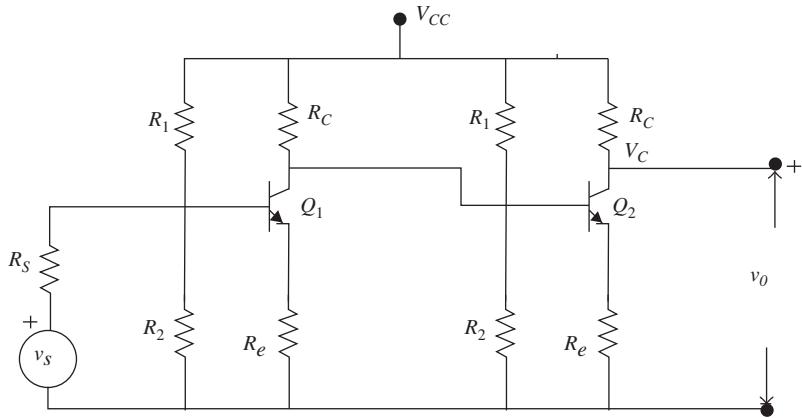


FIGURE 1.37(a) Direct-coupled amplifier

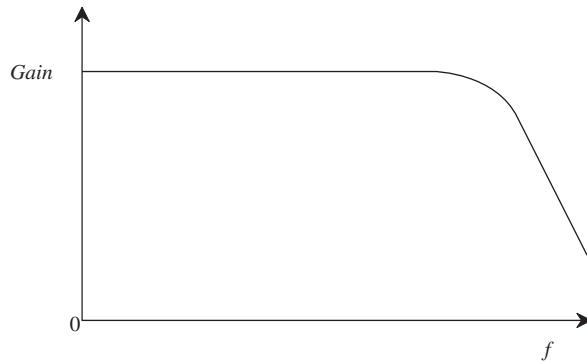


FIGURE 1.37(b) Frequency response of a direct-coupled amplifier

1.4.6 Feedback in Amplifiers

The gain of the amplifier in Fig. 1.26 is given as:

$$A = A_I \times \frac{R_L}{R_i} = -h_{fe} \times \frac{R_L}{R_S + h_{ie}} \quad (1.42)$$

As the parameters of the device, h_{fe} and h_{ie} , are temperature dependent, the gain of the amplifier is liable to change with temperature variations. However, for the gain to be stable, there is a need to provide feedback in the amplifier.

A feedback amplifier as shown in Fig. 1.38 consists of the original amplifier whose gain A is to be stabilized, a sampling network, a feedback network and a mixing arrangement at the input.

The sampled signal could be either a current or a voltage. Also the output of the β -network can either be a current or a voltage, in which case the mixing can be either shunt or series mixing. Therefore, depending on the type of sampling employed at the output and the type of mixing employed at the input, feedback amplifiers are classified as: voltage series feedback amplifier; current series feedback amplifier, voltage shunt feedback amplifier and current shunt feedback amplifier.

A voltage series feedback amplifier is schematically represented as in Fig. 1.39. Here $A = v_o/v_i$, where A is the voltage gain of the internal amplifier.

$$v_o = Av_i \quad (1.43)$$

A_f , the gain with feedback is given by:

$$\begin{aligned} A_f &= \frac{v_o}{v_s} \\ v_s &= v_i + v_f = v_i + \beta v_o = v_i + Av_i\beta = v_i(1 + A\beta) \\ A_f &= \frac{v_o}{v_s} = \frac{Av_i}{v_i(1 + A\beta)} = \frac{A}{(1 + A\beta)} = \frac{A}{D} \end{aligned} \quad (1.44)$$

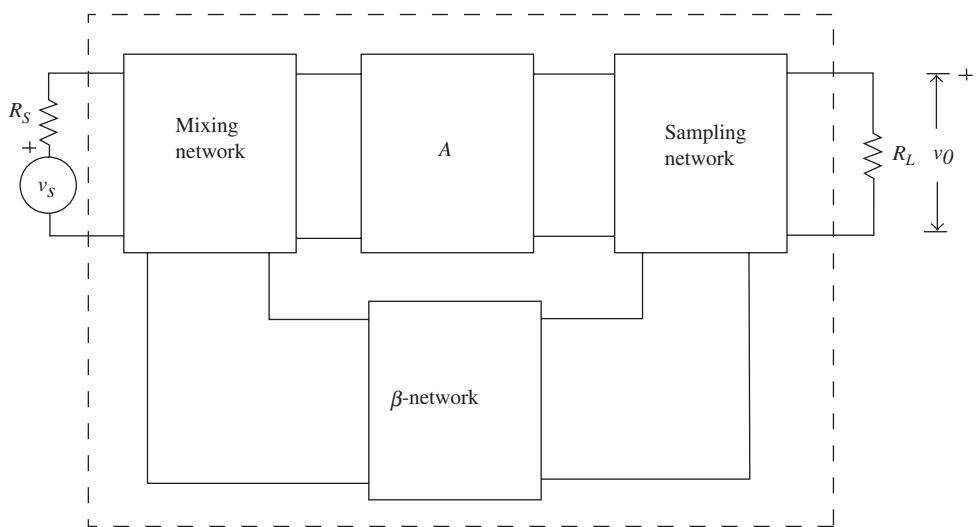


FIGURE 1.38 Schematic diagram of a feedback amplifier

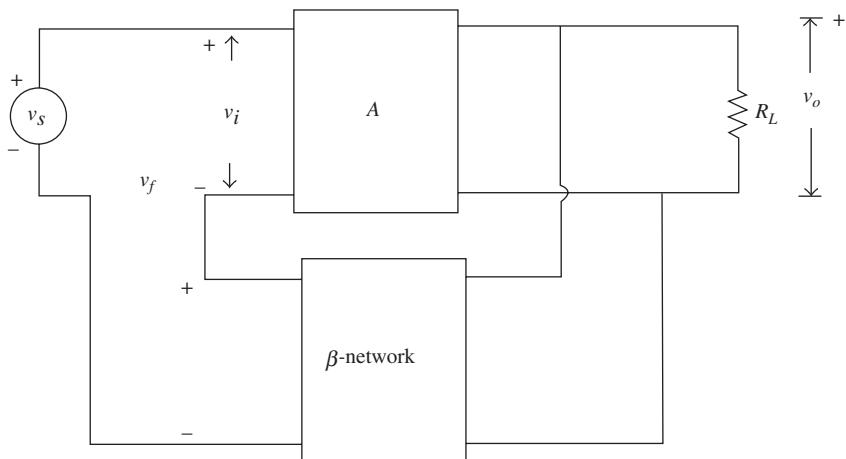


FIGURE 1.39 Voltage series feedback amplifier

where $D = (1 + A\beta)$ is called the return difference or de-sensitivity factor. From Eq. (1.44), the following may be inferred:

- If $D > 1, A_f < A$, then negative or degenerative feedback is said to be employed in the amplifier.
- If $D < 1, A_f > A$, then positive feedback is employed.
- If $A\beta \gg 1, A_f = 1/\beta$, the gain is independent of the device parameters and is solely decided by β -network. If the β -network is stable, A_f is stable.
- If $D = 0, A_f = v_o/v_s = \infty$, which means as A_f tends to infinity, v_s tends to 0.

This condition says that we derive finite output with zero input if the condition $1 + A\beta = 0$ is satisfied in the amplifier. Then the amplifier is called an oscillator. $1 + A\beta = 0$ is called the Barkhausen criterion.

1.4.7 Noise

Unwanted signals that cause random variations in the output of an electronic circuit could be termed noise. Noise can be present in a circuit mainly due to external sources or could be internally generated. Externally generated noise could be due to lightening, electrical discharges, etc. Noise can also be internally generated in a circuit due to: (i) the particle nature of electrical current; (ii) the variations in path and recombination rates; and (iii) the diffusion caused by the randomness of the charge movement. Noise can be present at all frequencies. Some of the factors that are responsible for noise in electronic circuits are briefly discussed below.

Thermal or Johnson's Noise. Thermal noise arises due to the thermal agitation of charge carriers. It is dependent on the temperature. Thermal noise due to a resistance R is given as:

$$V_n = \sqrt{4KTBR} \quad (1.45)$$

where, K = Boltzman constant = 1.38×10^{-23} J/K

T = temperature in Kelvin

B = Bandwidth in cycles

R = Resistance in ohms

When thermal noise is generated in a circuit, it can be represented by a voltage source (see Fig 1.40). In the circuit, $V_o = (V_n \times R)/(R + R) = V_n/2$. The maximum noise power ($\max P_n$) = $V_o^2/R = V_n^2/4R$. From Eq. (1.45), we know that $\max P_n = V_n^2/4R = KTB$.

Therefore, it is seen that the noise power depends on the bandwidth, B . The larger the bandwidth, larger is the noise. To reduce the thermal noise, B should be small and the operating temperature, T , low. If there is a noise power of 0.02 nW , with $B = 6 \text{ MHz}$ at 300 K and if $R = 100 \Omega$,

$$\frac{V_n^2}{R} = 2.0 \times 10^{-14} \text{ W}$$

$$V_n^2 = 2.0 \times 10^{-12}$$

$$V_n = \sqrt{2.0} \mu\text{V} = 1.41 \mu\text{V}$$

Thermal noise is present in diodes and transistors due to the bulk resistance of materials. FETs and MOSFETs have thermal noise in the conduction channel.

Shot Noise. Shot noise is present in devices due to irregular diffusion across the junction and also due to recombination effects in base and random motion of carriers in diffusion across the junctions. It is uniformly distributed over the frequency spectrum. As the current in the device increases, the noise energy also increases. Hence, at smaller collector currents, this noise is small.

Flicker Noise. Flicker noise is normally present below 1 kHz and is mainly due to charge diffusion processes and this noise varies inversely with frequency. This is minimized by suitable fabrication techniques. Thus, we see that the noise is present in a circuit either due to external sources or is internally generated. When this kind of noise is present in a circuit, we may use clipping circuits, filters, etc. to eliminate it.

1.5 OPERATIONAL AMPLIFIERS

An operational amplifier (op-amp) is a high-gain direct-coupled amplifier and, as shown in Fig. 1.41, has three basic building blocks—a differential amplifier as an input stage, dc-level shifter or level translator and an output power stage.

The differential amplifier gives an output proportional to the difference between the two inputs. As the op-amp is a direct-coupled amplifier, the output is referenced to a dc voltage. If there is a need to ensure that the output is referenced to the zero level, there arises the need for a level translator or a dc level shifter, which translates the dc voltage at the output to zero. An operational amplifier, unless otherwise warranted, needs to be balanced before it is used for an application. When the two inputs are grounded, if there is a dc voltage at the output, it is adjusted to zero. This is called balancing an op-amp. An op-amp is schematically represented as in Fig. 1.42. It has two inputs, an inverting input and a non-inverting input.

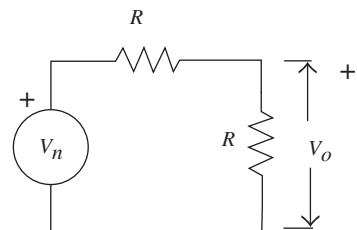


FIGURE 1.40 Noise in a resistance

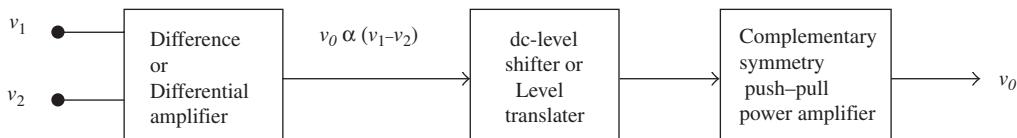


FIGURE 1.41 The basic building blocks of an operational amplifier

An op-amp, being a high-gain amplifier, may oscillate at high frequencies. To overcome this problem, frequency compensation is provided in the amplifier which reduces the gain at those frequencies. However, the most popular commercially available 741 op-amp is internally compensated. To balance 741, between pins 1 and 5, a $10\text{-k}\Omega$ potentiometer is connected and its centre tap is returned to $-V_{EE}$ source ($|V_{CC}| = |V_{EE}|$), as shown in Fig. 1.43.

The op-amp can be used in many applications. Consider the inverting amplifier shown in Fig. 1.44. Ideally an op-amp has $R_i = \infty$, $R_o = 0$, $A_V = \infty$. Since $A_V = v_o/v_i$, as $A_V \rightarrow \infty$, $v_i \rightarrow 0$. This implies that there exists a short circuit at the input. If really there exists a short circuit at the input, the entire current I should flow through this short circuit. However, we also have $R_i = \infty$, which means that there exists an open circuit between the input terminals, in which case the entire input current I now should flow through R' . These are two contradictory conditions. However, as A_V is very large, v_i is very small. Hence, for all practical purposes, the two input nodes are at the same potential. Thus, we can say there exists a virtual ground at the input and as R_i is very large, the input current I flows through R' . Hence, the equivalent circuit of inverting amplifier in Fig. 1.44 is drawn as shown in Fig. 1.45.

From the equivalent circuit in Fig. 1.45

$$v_o = -IR' \quad \text{and} \quad v_s = IR$$

$$A_f = \frac{v_o}{v_s} = \frac{-R'}{R} \quad (1.46)$$

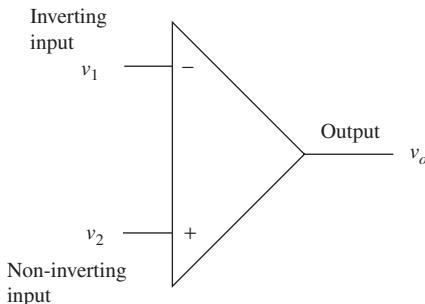


FIGURE 1.42 Schematic representation of an op-amp

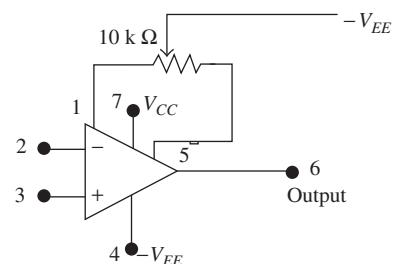


FIGURE 1.43 Balancing of the 741 op-amp

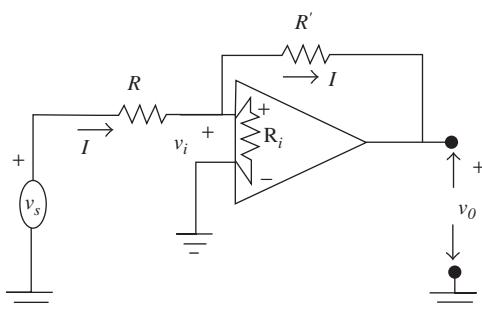


FIGURE 1.44 An op-amp as an inverting amplifier

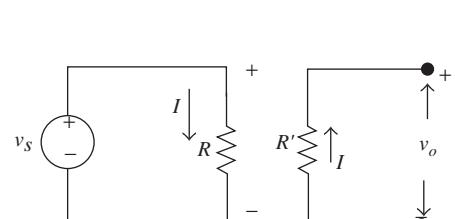


FIGURE 1.45 Simplified equivalent of Fig. 1.44

An op-amp can be used as an non-inverting amplifier, differential amplifier, subtracting amplifier, logarithmic and antilog amplifier, in active filters and in many more analogue applications. We are going to consider some of the applications later.

When an op-amp is used as a differential amplifier, the signal at the output is required to be proportional to the difference of the two input signals, v_1 and v_2 , called the difference signal, v_d . However, there appears a common mode signal, v_c which is due to the average of the two input signals, v_1 and v_2 which gives rise to an error term in the output. Therefore,

$$v_d = v_1 - v_2 \quad (1.47)$$

$$v_c = \frac{v_1 + v_2}{2} \quad (1.48)$$

$$v_o = A_d (v_1 - v_2) + A_c \left(\frac{v_1 + v_2}{2} \right) \quad (1.49)$$

Where A_d is the differential gain and A_c is the common mode gain. The second term in Eq. (1.49) in the output is due to an unwanted error signal which should ideally be zero.

The goodness of an operational amplifier—how effectively the op-amp is able to reject the unwanted common mode signal and deliver only the differential signal at the output—is given by the common mode rejection ratio (CMRR), also known as ρ . It is the figure of merit of a differential amplifier.

$$\rho = \frac{A_d}{A_c} \quad (1.50)$$

Substituting Eq. (1.50) in Eq. (1.49):

$$v_o = A_d \left[(v_1 - v_2) + \frac{A_c}{A_d} \left(\frac{v_1 + v_2}{2} \right) \right] \quad (1.51)$$

$$v_o = A_d \left(v_d + \frac{1}{\rho} v_c \right) \quad (1.52)$$

If the signal in the output due to the common mode component is to be zero, ideally, $\rho \rightarrow \infty$, then $v_o = A_d v_d$. In practice, ρ should be very large. However, the main limitation in an op-amp is its slew rate, defined as the maximum time rate-of-change of the output voltage v_o under large signal conditions.

$$S = \max \frac{dv_o}{dt} \quad (1.53)$$

The slew rate S limits the maximum frequency and amplitude to which the op-amp can respond. If $v_o = V_m \sin \omega t$, then $dv_o/dt = \omega V_m \cos \omega t$. Now, (dv_o/dt) is maximum when $\cos \omega t = 1$. Therefore, the slew rate S is given by the relation:

$$S = \frac{dv_o}{dt} \max = V_m \omega \quad (1.54)$$

The maximum amplitude at the output is:

$$V_m = \frac{S}{2\pi f} \quad (1.55)$$

If the op-amp has $S = 10 \text{ V}/\mu\text{s}$ and if $f = 1 \text{ MHz}$, then the maximum possible output voltage is:

$$V_m = \frac{\frac{10 \text{ V}}{10^{-6}}}{2\pi \times 1 \times 10^6} = \frac{10 \text{ V}}{2\pi} = 1.59 \text{ V}$$

If $f = 0.1 \text{ MHz}$:

$$V_m = \frac{\frac{10 \text{ V}}{10^{-6}}}{2\pi \times 0.1 \times 10^6} = \frac{10 \text{ V}}{0.2\pi} = 15.92 \text{ V}$$

Thus, to derive a larger output voltage we have to sacrifice bandwidth. Else, to derive larger bandwidth we have to be content with smaller output.

1.6 OSCILLATORS

Oscillators are of two types—sinusoidal and relaxation oscillators. Sinusoidal oscillators generate sinusoidal signals whereas relaxation oscillators generate an output whose amplitude changes abruptly like in sweep generators and multivibrators that we will discuss later.

A sinusoidal oscillator is essentially a feedback oscillator in which the Barkhausen condition, $1 + A\beta = 0$, is satisfied. The Barkhausen condition has an amplitude condition and a phase condition.

- (i) $|A\beta| \geq 1$ is the amplitude condition, i.e., for oscillations to build up, initially $A\beta$ is greater than 1; and $A\beta = 1$ when the amplitude reaches a predetermined level.
- (ii) The overall phase shift the signal (noise is input to the amplifier as $v_s = 0$) undergoes as it passes through the amplifier and the β -network should be 360° . That is, if the noise signal undergoes a phase shift of 180° in a CE amplifier, then an additional phase shift of 180° is required to be produced by the frequency-selective β -network. The β -network can produce this phase shift of 180° either by using LC components, in which case the oscillators are called LC oscillators (for example, Colpitts, Hartley, Clapp and tuned collector). If on the other hand, this additional phase shift of 180° is produced by RC components, the resultant oscillators are called RC oscillators (for example, RC phase shift and Wien-bridge oscillators).

LC oscillators are used in the radio frequency range. In the audio-frequency range LC oscillators are not used mainly because the size of the inductor is large. Hence, RC oscillators are preferred in the audio-frequency range. As an illustration, a Wien-bridge oscillator using an op-amp is shown in Fig. 1.46(a).

In this oscillator, if $A \geq 3$, it would generate oscillations at $f = 1/2\pi RC$. R_1 and R_2 decide the gain, A . The network in Fig. 1.46(b) determines the frequency of oscillations and is a Wien's or β -network. As X is connected to the non-inverting terminal, it means that output and input are in the same phase.

The frequency stability of oscillations depends on the Q of the tank circuit ($= 1/\omega_o CR = \omega_o L/R$). The larger the value of Q , the better the frequency stability of the oscillator. As neither LC nor RC oscillators have large Q , their frequency stability is poor. So to get stable oscillations, crystal oscillators with very large values of Q are used. Another class of oscillators is relaxation oscillators in which the output abruptly changes from one level to another. Sweep generators and multivibrators come under this category.

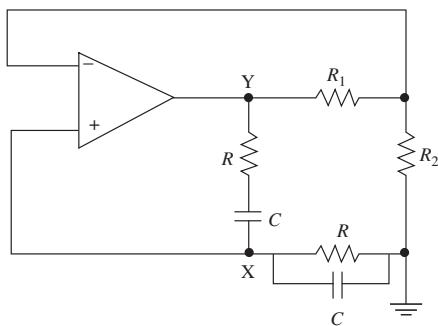


FIGURE 1.46(a) A Wien-bridge oscillator using op-amp

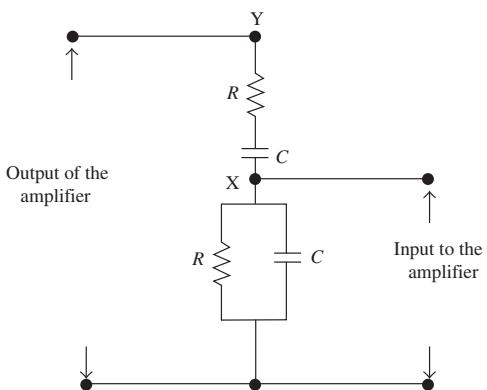


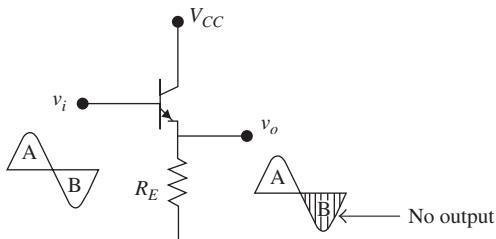
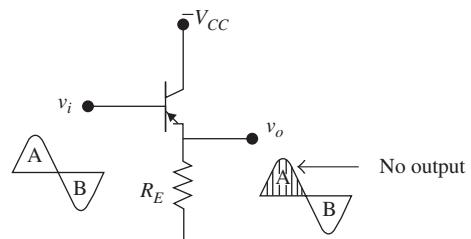
FIGURE 1.46(b) A Wien's network

1.7 CC AMPLIFIER AS A POWER AMPLIFIER

We have seen that though an emitter follower has only unity voltage gain but its current gain is $h_{fc} = |1 + h_{fe}|$. This is the configuration having the largest current gain. Hence, an emitter follower can be used as a power amplifier. Consider the emitter follower using an *n-p-n* device, as shown in Fig. 1.47(a). There is an output only during the positive going half-cycle, i.e., during the period A.

Now consider an emitter follower using a *p-n-p* transistor, as shown in Fig. 1.47(b). There is an output only during the negative going half-cycle, i.e., during the period B. If *n-p-n* and *p-n-p* devices are used in an emitter follower, so that one device takes care of one half of the input cycle period and the other device takes care of another half of the input cycle period, the resultant configuration is called a the push-pull configuration. Though the individual devices are operated under class-B condition, there is an output for the entire input cycle period. Such a power amplifier is called a class-B complementary symmetry push-pull power amplifier, as shown in Fig. 1.47(c).

However, in pure class-B operation, unless the magnitude of the input is equal to V_V of the device, there is no conduction in the device. Hence, for a short duration there is no output—the output is distorted. The resultant output of the amplifier is shown in Fig. 1.47(d). This distortion is called cross-over distortion. This can be eliminated by using a trickle-bias. In other words, a voltage of magnitude V_V is provided between the base and the emitter terminals, so that, the moment there is an input signal, there is an output. The complementary symmetry push-pull power amplifier with a trickle-bias is shown in Fig. 1.47(e).

FIGURE 1.47(a) An emitter follower using an *n-p-n* deviceFIGURE 1.47(b) An emitter follower using a *p-n-p* device

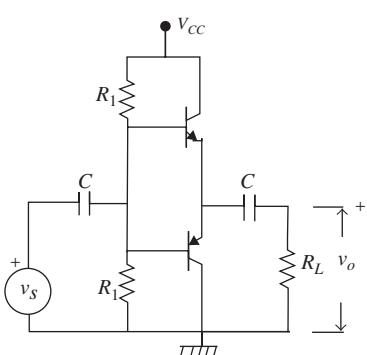


FIGURE 1.47(c) Complementary symmetry class-B push-pull power amplifier

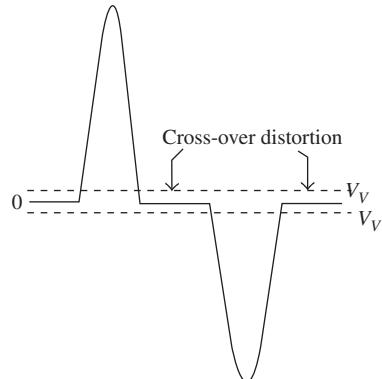


FIGURE 1.47(d) Cross-over distortion in a pure class-B amplifier

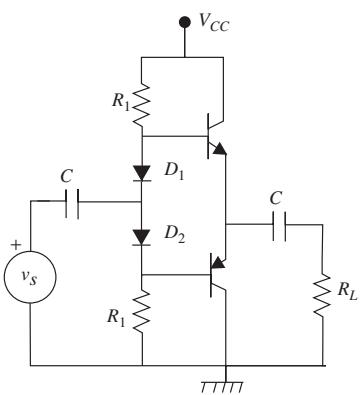


FIGURE 1.47(e) The complementary symmetry class-B push-pull amplifier with a trickle-bias

By choosing the diodes and the transistors such that the $V-I$ characteristic of the diodes is the same as the V_{BE} , V_s and I_C characteristics of the transistors, temperature compensation can be provided in the power amplifier. A complementary symmetry push-pull power amplifier is an output stage in an operational amplifier.

Another class of power amplifier is class-C power amplifier in which the operating point is located well below the cut-off, so that the transistor conducts for less than one half of the input cycle period. Consequently the output is in the form of pulses. Normally, a tuned circuit is provided in the output to select the desired frequency band. Class-C amplifiers are normally used in the radio-frequency range. They can also be used as harmonic generators.

Yet another class of power amplifier is a class-D power amplifier in which the sinusoidal signal is converted into a digital signal; and this drives the amplifier. The output of the amplifier is again in the form of pulses. For converting the signals into a sinusoidal signal at the output of the amplifier, a low-pass filter or a tuned circuit is employed. As the dissipation in the device is negligible, larger efficiency can be achieved.

1.8 MILLER'S THEOREM

Miller's theorem states that if an impedance is connected between the input and output nodes in an amplifier, having a reference node N , then this impedance can be replaced by two impedances, one connected between the input and the reference node and the other connected between the output and the reference node.

Consider an amplifier in which N is the reference node and 1 and 2 are the input and output nodes. A resistance R' is connected between nodes 1 and 2, as shown in Fig. 1.48(a).

Let I_1 be the current leaving node 1.

$$I_1 = \frac{V_1 - V_2}{R'} = \frac{V_1 \left(1 - \frac{V_2}{V_1}\right)}{R'} = \frac{V_1(1 - A_V)}{R'} = \frac{V_1}{\frac{R'}{(1 - A_V)}} = \frac{V_1}{R_1} \quad (1.56)$$

where $A_V = V_2/V_1$ is the voltage gain and

$$R_1 = \frac{R'}{(1 - A_V)} \quad (1.57)$$

Thus, if R' is removed and a resistance R_1 is connected between nodes 1 and N , the current drawn from node 1 is still I_1 , as shown in Fig. 1.48(b).

Let us now calculate I_2 using Fig. 1.48(c).

$$I_2 = \frac{V_2 - V_1}{R'} = \frac{V_2 \left[1 - \frac{V_1}{V_2} \right]}{R'} = \frac{V_2 \left[1 - \frac{1}{A_V} \right]}{R'} = \frac{V_2 \left[\frac{A_V - 1}{A_V} \right]}{R'} = \frac{V_2}{R' \times \left[\frac{A_V}{A_V - 1} \right]} = \frac{V_2}{R_2}$$

where

$$R_2 = R' \times \frac{A_V}{A_V - 1} \quad (1.58)$$

Then if R_2 is connected between node 2 and N the current drawn from node 2 is still I_2 , Fig. 1.48(d).

This suggests that we can replace R' by R_1 and R_2 . Voltage shunt feedback amplifier can be analysed using Miller's theorem. We can also see the advantage of op-amp integrator by using the Miller's theorem, when we study low-pass circuits.

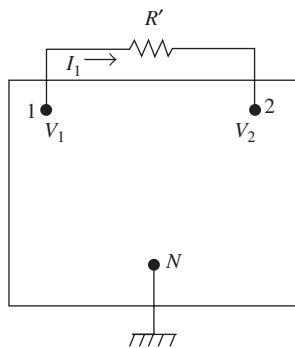


FIGURE 1.48(a) A multi-node network

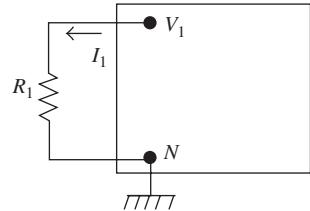


FIGURE 1.48(b) Network when R_1 is connected between 1 and N

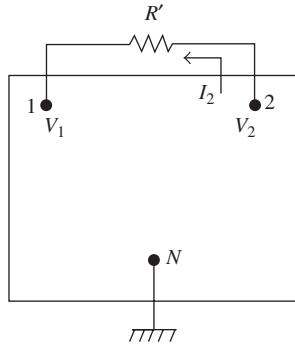


FIGURE 1.48(c) Network to calculate I_2

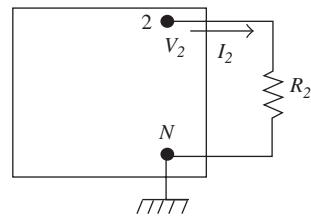


FIGURE 1.48(d) Circuit when R_2 is connected between 2 and N

1.8.1 The Dual of Miller's Theorem

The dual of the Miller's theorem states that if an impedance is connected between node 3 and the reference node N , in an amplifier then this impedance can be replaced by two impedances, one connected in series with the input and the other connected in series with the output.

Consider an amplifier in which a resistance R' is connected between node 3 and reference node N as shown in Fig. 1.49(a). Then the dual of Miller's theorem states that the resistance R' now can be replaced by two resistances, R_1 connected in series with the input node 1 and the R_2 connected in series with the output node 2 as in Fig. 1.49(b) where:

$$R_1 = R' (1 - A_I) \quad (1.59)$$

and

$$R_2 = \frac{R' (A_I - 1)}{A_I} \quad (1.60)$$

where A_I is the current gain.

Current series feedback amplifier can be analysed using the dual of the Miller's theorem. The advantage of using op-amp differentiator is seen when we study high-pass circuits.

1.9 GROUND IN A CIRCUIT

When we consider a CE amplifier, the emitter is a common terminal between the input and output, commonly referred to as the ground terminal. Consider the CE amplifier shown in Fig. 1.50(a). Let an $n-p-n$ device be used in the amplifier. V_{CC} is connected to one end of R_C and the negative terminal is connected to the ground. I_C flows downwards and V_C is positive with respect to the ground.

If on the other hand, a $p-n-p$ device is used in the amplifier circuit, the biasing is exactly opposite, as shown in Fig. 1.50(b).

$-V_{CC}$ is connected to one end of R_C and the positive end of the battery is connected to the ground. I_C flows upwards and V_C is negative with respect to the ground. This means that the directions of the currents and polarities of voltages are exactly opposite in an $n-p-n$ device when compared to a $p-n-p$ device. Hence, these two types of devices are called complementary devices. Now consider a practical case of a two-stage amplifier using $n-p-n$ devices shown in Fig. 1.51(a)

If for some reason, Q_2 needs to be replaced and the only replacement available is a $p-n-p$ device with similar characteristics, resultant circuit, when the devices are biased, is as shown in Fig. 1.51(b).

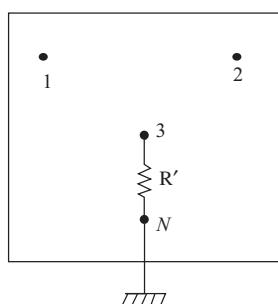


FIGURE 1.49(a) Multi-node network

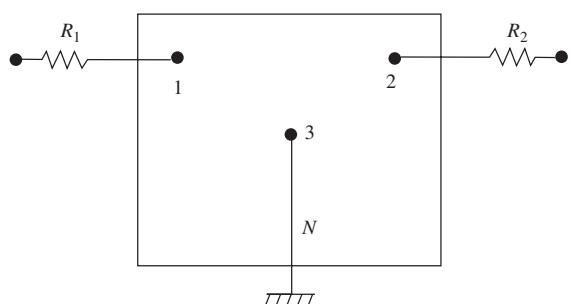


FIGURE 1.49(b) Redrawn circuit of Fig. 1.49(a) using dual of Millers theorem

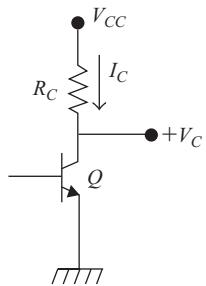


FIGURE 1.50(a) Supply voltage for biasing of an $n-p-n$ device is positive

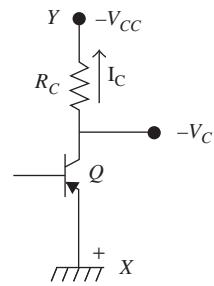


FIGURE 1.50(b) Supply voltage for biasing of a $p-n-p$ device is negative

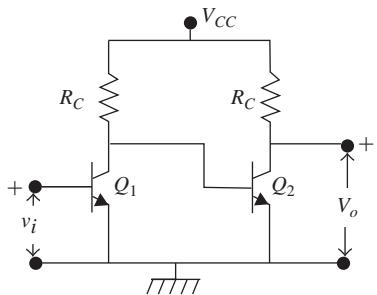


FIGURE 1.51(a) Two stage amplifier using $n-p-n$ devices

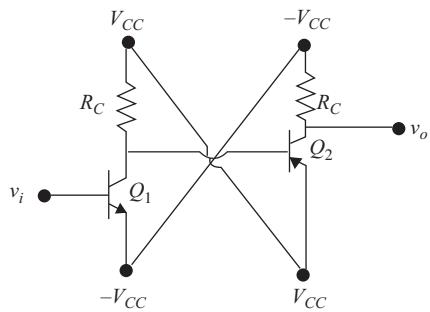


FIGURE 1.51(b) Resultant circuit with the crossovers

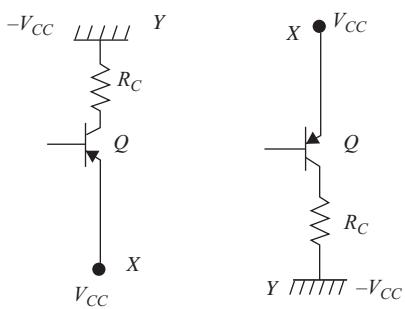


FIGURE 1.51(c) A $p-n-p$ device connected in its upside down fashion

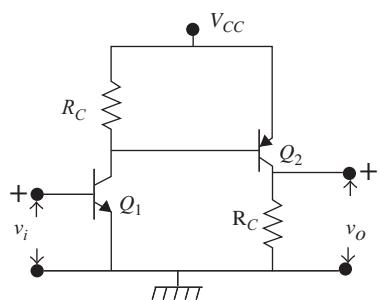


FIGURE 1.51(d) Circuit in which a $p-n-p$ device is connected in an upside down fashion

With the crossovers it is not possible to run a $+V_{CC}$ and $-V_{CC}$ bus bars and make the circuit look simple. Now consider an alternate arrangement for Fig. 1.50(b). Instead of calling point X as the ground, call point Y as the ground and connect the $p-n-p$ device in its upside down fashion as shown in Fig. 1.51(c).

Once the $p-n-p$ device Q_2 is connected in its upside down fashion, as in Fig. 1.51(d), it is possible to run a common bus bar. Thus, the ground in a circuit is nothing but an arbitrarily chosen reference terminal with respect to which we measure voltages.

1.10 STRAY CAPACITANCES IN DEVICES

The semiconductor diode is used as a switch. In a forward-biased diode, there is a diffusion capacitance C_D that depends on the forward current of the diode. However, while considering the equivalent circuit of the diode at high frequencies, this capacitance will have a negligible say. But in a reverse-biased diode, there exists a transition capacitance C_T which is inversely proportional to the diode reverse-bias voltage and is taken into consideration at high frequencies. Hence, the high-frequency equivalent circuit of a reverse-bias semiconductor diode is given in Fig. 1.52. The stray capacitances limit the switching speed. Here, R_r is the reverse resistance of the diode.

Similarly, we have stray capacitances in transistors between a pair of terminals, called inter-electrode capacitances. These influence the switching speed of the devices. These capacitances also have a role in the high-frequency response of the amplifiers.

1.11 FIELD-EFFECT TRANSISTORS

A junction field-effect transistor (JFET), also called a field-effect transistor (FET), is a voltage-controlled three-terminal device in which the current flow is essentially due to the majority carriers—either holes or electrons. Hence, this device is a unipolar device whereas a transistor is a bipolar device where the current is due to both the majority and minority carriers. The major advantage of an FET over a BJT is that it has a large input resistance. JFETs are again of two types, an *n*-channel FET and a *p*-channel FET, schematically represented in Figs. 1.53(a) and (b), respectively.

In an *n*-channel FET, the gate is made negative with respect to the source whereas in a *p*-channel FET the gate is positive with respect to the source. The small-signal low-frequency models of a JFET are shown in Figs. 1.53(c) and (d), respectively. For an FET:

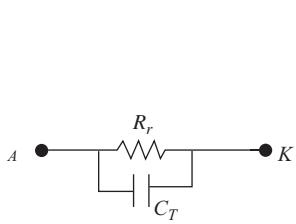


FIGURE 1.52 Stray capacitance in a reverse-biased diode

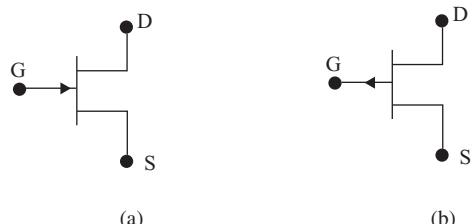


FIGURE 1.53(a) Two types of JFETs: *n*-channel FET; and (b) *p*-channel FET

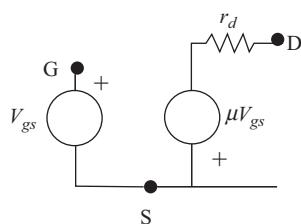


FIGURE 1.53(c) The voltage source equivalent circuit of an FET

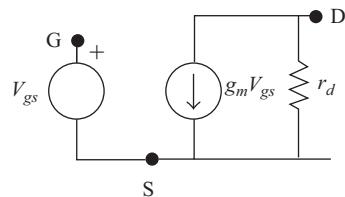


FIGURE 1.53(d) The current source equivalent circuit of an FET

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad (1.61)$$

where, I_D is the drain current, V_P is pinch-off voltage and I_{DSS} is the drain current when V_{GS} is zero. An FET can be used as a common source, common drain and common gate amplifier. A common drain amplifier is also called a source follower whose voltage gain is unity. Consider the common source amplifier shown in Fig. 1.54(a).

The equivalent circuit is as shown in Fig. 1.54(b). From Fig. 1.54(b);

$$V_o = \frac{-\mu V_{gs} R_d}{r_d + R_d}$$

$$A = \frac{V_o}{V_{gs}} = \frac{-\mu R_d}{r_d + R_d} \quad (1.62)$$

where μ is the amplification factor, r_d is the drain resistance and g_m is the trans-conductance.

The n -channel and p -channel FETs are complementary devices. If the gate is insulated from the channel, the resultant FET is called an insulated gate field-effect transistor (IGFET) or metal oxide semiconductor field-effect transistor (MOSFET). MOSFETs are again of two types—depletion type MOSFETs and enhancement type MOSFETs.

Depletion type MOSFETs are also of two types; n -channel depletion type MOSFET and p -channel depletion type MOSFET. D-MOSFETs are similar to JFETs; the only difference being the fact that V_{GS} can be positive for n -channel devices and negative for p -channel devices. The major advantage with MOSFETs over JFETs is that, as the gate is insulated, the input resistance is very high—of the order of hundreds of $M\Omega$. Enhancement type MOSFETs can either be n -channel (n -MOS) or p -channel (p -MOS) devices. A schematic representation of D-MOSFET, p -channel and n -channel enhancement MOSFETs is shown in Figs. 1.55(a), (b) and (c), respectively.

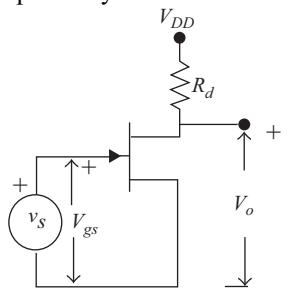


FIGURE 1.54(a) A common source amplifier

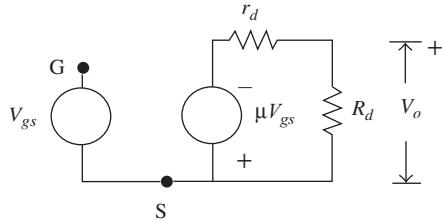


FIGURE 1.54(b) The equivalent circuit of Fig. 1.54(a)

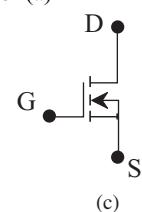
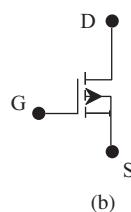
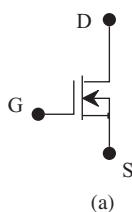


FIGURE 1.55(a) D-MOSFET; (b) p -MOS enhancement type MOSFET; and (c) n -MOS enhancement type MOSFET

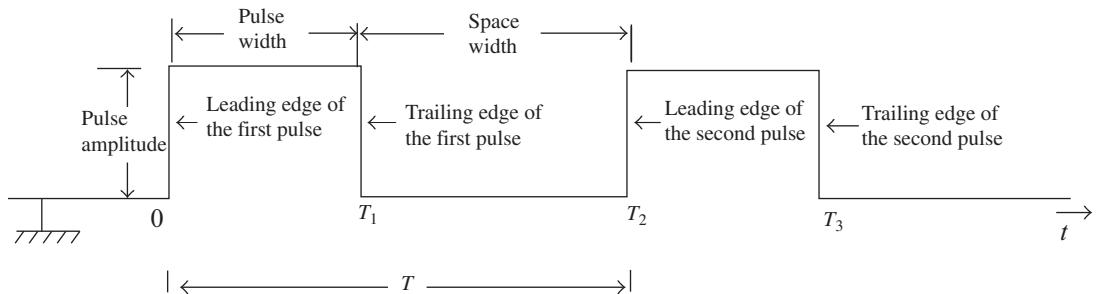


FIGURE 1.56 Ideal pulse waveforms

Where there is a specific requirement that the inputs of the devices are required not to load the outputs of the previous stages or the generator outputs, MOSFETs are used. These can also be used as switches. When we later consider logic gates the *n*-MOS and *p*-MOS gates are considered using these devices. If *n*-MOS and *p*-MOS devices are used as complementary devices, the resultant gate is called a CMOS gate.

1.12 CHARACTERISTICS OF PULSE WAVEFORMS

Consider the waveform (a pulse train) where the pulse amplitude is positive, as shown in Fig. 1.56.

The voltage level of the top of the pulse with respect to the ground is the *pulse amplitude*. The first edge of the pulse at $t = 0$ (say) is called the *leading edge*, the rising edge or positive going edge. The second edge, at $t = T_1$, is called the *trailing edge*, the falling edge or the negative going edge. The time interval from the leading or trailing edge of one pulse to the leading or trailing edge of the next pulse is the *time period* T . The reciprocal of the time period is the *pulse repetition frequency (PRF)*. The time interval from the leading edge to the trailing edge of a pulse is called the *pulse width*, *pulse duration* or *mark length (M)*. The time interval between successive pulses is called the *space width* or *space length (S)*. The ratio of pulse width to space width is the *mark-to-space ratio (M/S ratio)*. The ratio of a pulse width to a time period is called the *duty cycle* D , and is normally expressed as a percentage:

$$D = \frac{T_1}{T_1 + T_2} \times 100\% \quad \text{If } T_1 = T_2 = \frac{T}{2}, \text{ then } D = 50\% \quad (1.63)$$

The smaller the value of D , the sharper is the pulse train. The pulse train in Fig. 1.56 has flat top and sharp rising and trailing edges and may be considered to be an ideal pulse train. However, the pulses generated may not necessarily be ideal. A practical pulse may not have sharp leading and trailing edges and it may not be a flat pulse, as shown in Fig. 1.57. The pulse may have a finite rise time and fall time. In Fig. 1.57,

$V_3 = V_1 - V_2$ and $V = (V_1 + V_2)/2$, where V_1 is the maximum amplitude, V_2 is the minimum amplitude and V is the average amplitude.

As the top of the pulse is not flat and has a tilt (or sag), we define per cent tilt as:

$$\% \text{Tilt} = \frac{V_1 - V_2}{V} \times 100\% \quad (1.64)$$

Here, t_r = rise time = time taken for the voltage to change from $0.1V$ to $0.9V$ and t_f = fall time = time taken for the voltage to change from $0.9V$ to $0.1V$.

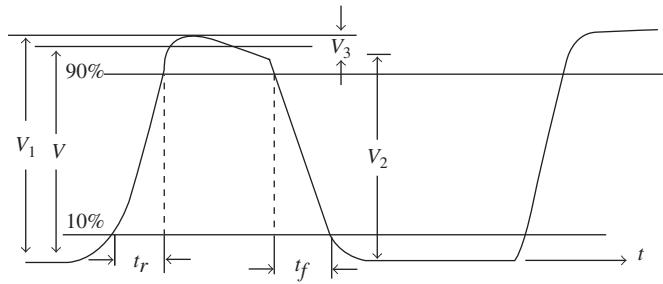


FIGURE 1.57 Practical pulse train

1.12.1 Types of Waveforms Used in Pulse Circuits

- (1) **Step voltage:** A positive step voltage waveform is shown in Fig. 1.58. It is defined as a signal that has zero amplitude for $t < 0$ and a constant amplitude V , for $t \geq 0$.

A step is represented as:

$$\begin{aligned} v(t) &= 0, & \text{for } t < 0 \\ &= V, & \text{for } t > 0 \end{aligned} \quad (1.65)$$

- (2) **Pulse waveform:** A pulse is a signal that has an amplitude V for a duration t_p and zero amplitude elsewhere. A pulse is a combination of a positive step and a delayed negative step as represented in Fig. 1.59.

A pulse waveform is represented by the relation:

$$\begin{aligned} v(t) &= V, & \text{for } 0 < t < t_p \\ &= 0, & \text{elsewhere} \end{aligned} \quad (1.66)$$

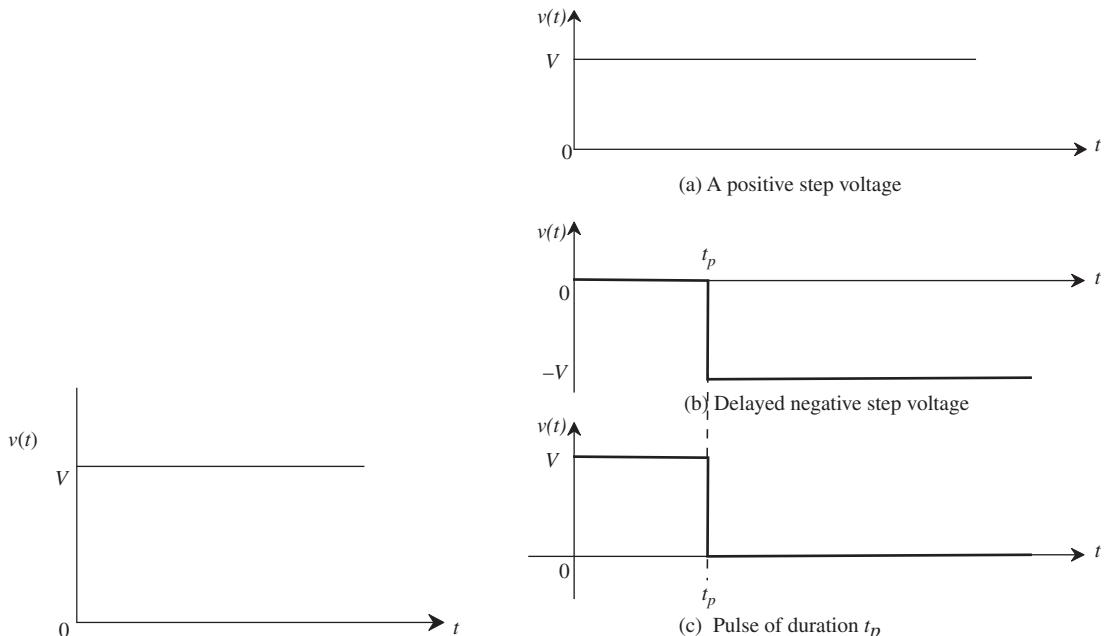


FIGURE 1.58 Step waveform

FIGURE 1.59 A pulse waveform

- (3) **Square wave:** A square wave is a periodic waveform with amplitude V' for T_1 and an amplitude V'' for T_2 and repeats itself for $T = T_1 + T_2$ with a repetitive frequency, f as shown in Fig. 1.60.

Here, $f = 1/T$. If $T_1 = T_2 = T/2$, then the square wave is called a symmetric square wave. If $T_1 \neq T_2$, then it is called an un-symmetric square wave. Fig. 1.61 is a symmetric square wave referenced to the zero level (0 V).

- (4) **Ramp waveform:** A ramp is a signal that varies linearly as a function of time. A positive ramp is shown in Fig. 1.62.

A positive ramp waveform is mathematically represented as:

$$\begin{aligned} v(t) &= 0 & \text{for } t < 0 \\ &= \alpha t & \text{for } t \geq 0 \end{aligned} \quad (1.67)$$

where, $\alpha = V/T$ is the slope.

- (5) **Exponential waveform:** A waveform which varies exponentially as a function of time with a time constant τ is shown in Fig. 1.63. This waveform is mathematically expressed as:

$$v(t) = V(1 - e^{-t/\tau}) \quad (1.68)$$

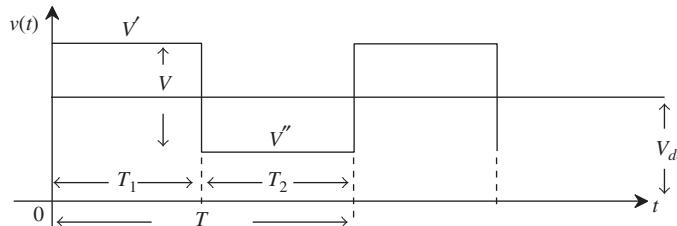


FIGURE 1.60 A square waveform referenced to V_{dc}

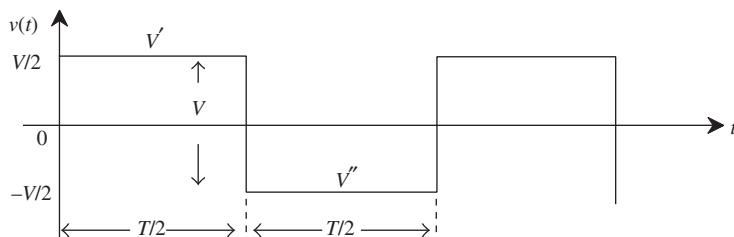


FIGURE 1.61 A symmetric square waveform referenced to the zero level

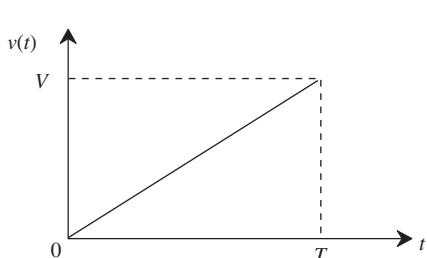


FIGURE 1.62 A positive ramp waveform

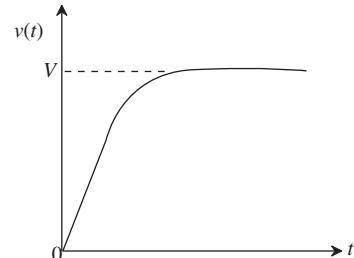


FIGURE 1.63 An exponential waveform

1.12.2 Energy Storage Elements

Capacitors and inductors are energy storage elements. A capacitor stores charge and an inductor stores current. If C is the value of the condenser then its capacitive reactance is given by $X_C = 1/j\omega C$, whose magnitude decreases with increasing frequency. Similarly, if L is the value of the inductance, its inductive reactance is given by $X_L = j\omega L$ and its magnitude increases with increasing frequency. If a voltage V_1 is connected across the capacitor terminals, the capacitor charges to V_1 . If now the connected voltage suddenly changes to V_2 the voltage across the capacitor will not change suddenly. Thus, we may say that a capacitor will not allow any sudden changes in the voltage. Similarly an inductor will not allow any sudden changes in the current.

Why do Capacitors not Allow Sudden Changes in the Voltage? A capacitor has two parallel plates with a dielectric in between. When a voltage v is applied between the two plates of the capacitor, the voltage source deposits a positive charge ($+q$) on one plate and a negative charge ($-q$) on the other plate as shown in Fig. 1.64(a).

The capacitor stores the electric charge. The charge stored on C is directly proportional to v .

$$q \propto v$$

Or

$$q = Cv \quad (1.69)$$

From Eq. (1.69):

$$C = \frac{q}{v} \quad (1.70)$$

Therefore, the capacitance C is the ratio of charge on one plate of the condenser to the applied voltage v . We have:

$$i = \frac{dq}{dt} \quad (1.71)$$

From Eq. (1.69):

$$\frac{dq}{dt} = C \frac{dv}{dt} \quad (1.72)$$

Therefore, from Eqs.(1.71) and (1.72):

$$i = C \frac{dv}{dt} \quad (1.73)$$

The relation between (dv/dt) and i is linear and is shown in Fig. 1.64(b).

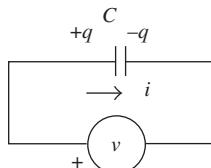


FIGURE 1.64(a) Voltage source v connected between the two plates of a capacitor

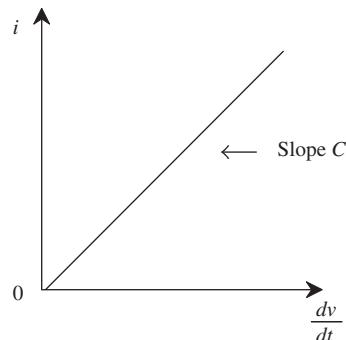


FIGURE 1.64(b) Relation between i and dv/dt

From Eq. (1.73) we have $dv/dt = i/C$. Rearranging:

$$v = \frac{1}{C} \int idt \quad (1.74)$$

Using Eqs. (1.73) and (1.74), the power P delivered to the capacitor is given by:

$$P = vi = vC \frac{dv}{dt} \quad (1.75)$$

W , the energy stored, is given by:

$$W = \int_{-\infty}^t P dt = \frac{Cv^2}{2} \quad (1.76)$$

From Eq. (1.70):

$$v^2 = \frac{q^2}{C^2} \quad (1.77)$$

Substituting Eq. (1.77) in Eq. (1.76):

$$W = \frac{q^2}{2C} \quad (1.78)$$

- (i) Let the voltage connected to C be a DC voltage, V , as shown in Fig. 1.64(c). For this, $dv/dt = 0$. From Eq. (1.73), therefore, $i = 0$. This means that the capacitor behaves as an open circuit for DC.
- (ii) Now, if the voltage across the capacitor changes abruptly as in Fig. 1.64(d), $dv/dt = \infty$.

From Eq. (1.73), $i = \infty$, which means that as $i \rightarrow \infty$ (practically impossible), we say that the capacitor will not allow any sudden changes in V . To summarize, a capacitor behaves as an open circuit for DC; and if there is a sudden change in the voltage, the capacitor will not allow any sudden changes in the voltage, behaving as a short circuit.

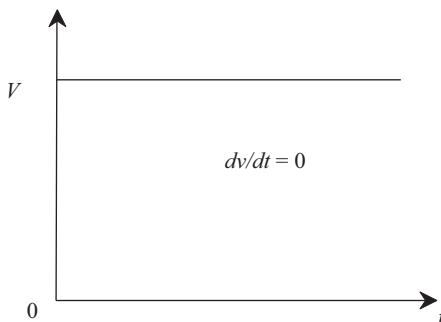


FIGURE 1.64(c) DC voltage connected to the capacitor

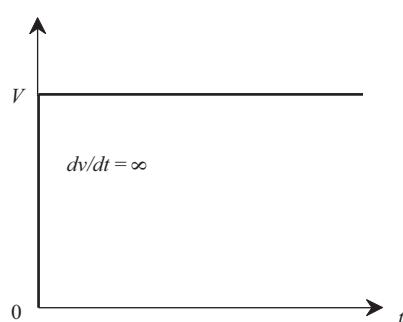


FIGURE 1.64(d) Voltage across C abruptly rises to V at $t = 0$

Why do Inductors not Allow Sudden Changes in the Current? Similarly when a battery is connected [see Fig. 1.65(a)], the voltage v in an inductor is given by:

$$v = L \frac{di}{dt} \quad (1.79)$$

and

$$i = \frac{v}{L} t \quad (1.80)$$

The relation between v and (di/dt) is shown in Fig. 1.65(b).

From Eq. (1.79), for a constant current [shown in Fig. 1.65(c)] as $di/dt = 0$, $v = 0$. This means that when the current is constant, the inductor behaves as a short circuit.

If the current abruptly changes as shown in Fig. 1.65(d), $(di/dt) = \infty$. Therefore, from Eq. (1.79), $v = \infty$, which is not physically possible. Thus, an inductor opposes sudden changes in the current. If the current abruptly changes, an inductor behaves as an open circuit.

Let us summarize the behaviour of capacitors C and inductors L based on the characteristics discussed:

- (1) A capacitor behaves as an open circuit for a constant unidirectional voltage and if there is a sudden change in voltage it causes an impulse current in the capacitor.
- (2) An inductor behaves as a short circuit for a constant unidirectional current and if the current suddenly changes, it causes an impulse voltage in the inductor. (For more details see Appendix B.)

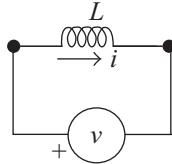


FIGURE 1.65(a)
Voltage v applied
to an inductor

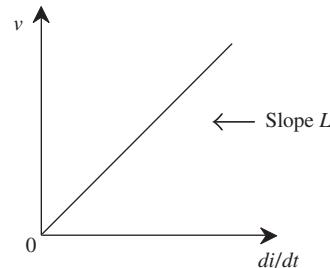
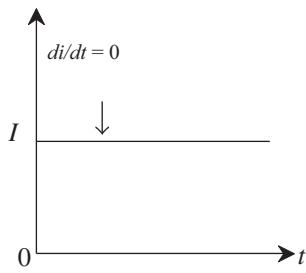
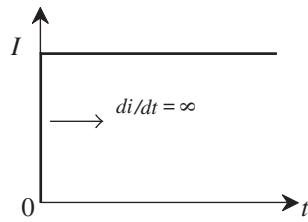


FIGURE 1.65(b) Relation
between v and (di/dt)



(c)



(d)

FIGURE 1.65(c) Constant current flowing through an inductor (d) Current in the inductor
abruptly rises to I at $t = 0$

1.13 LAPLACE TRANSFORMS

In order to find out the response of linear waveshaping circuits to the various types of inputs discussed above, we usually formulate a differential equation and solve the differential equation using Laplace transforms. The Laplace transform of any function in the time domain t is given by:

$$F(s) = L[f(t)] = \int_0^{\infty} f(t)e^{-st} dt \quad (1.81)$$

where, $s = \sigma + j\omega$. The lower limit is taken as zero instead of $-\infty$ because the convergence factor for $e^{-\sigma t}$ will diverge for $t \rightarrow -\infty$; therefore, all the information before $t = 0$ is ignored. A function is said to be Laplace transformable when:

$$\int_0^{\infty} f(t)e^{-st} dt < \infty$$

The Laplace transform permits us to go from the time domain to the frequency domain whereas the inverse Laplace transform allows us to go from the frequency domain to the time domain.

$$L^{-1}[F(s)] = f(t) = \frac{1}{2\pi} \int_{\sigma - j\omega}^{\sigma + j\omega} F(s)e^{st} ds \quad (1.82)$$

1.13.1 Basic Properties of Laplace Transformation

Property 1: The Laplace transform of the sum or difference of time functions is equal to the sum or difference of the Laplace transforms of the individual time functions.

$$L[f_1(t) + f_2(t) + \dots + f_n(t)] = F_1(s) + F_2(s) + \dots + F_n(s) \quad (1.83)$$

Property 2: The Laplace transform of the product of a constant and a time function is equal to the product of the constant and the Laplace transform of the time function.

$$L[af(t)] = aF(s) \quad (1.84)$$

Property 3: If $F_1(s)$ and $F_2(s)$ are the Laplace transforms of $f_1(t)$ and $f_2(t)$, respectively, then:

$$L[a_1f_1(t) + a_2f_2(t)] = a_1F_1(s) + a_2F_2(s)$$

where a_1 and a_2 are arbitrary constants.

Property 4: Scaling:

$$L[f(at)] = \frac{1}{a}F\left(\frac{s}{a}\right) \quad (1.85)$$

where a is an arbitrary constant.

Property 5: Time Shifting: The Laplace transform of a time function $f(t)$ delayed by time t_0 is equal to the Laplace transform of $f(t)$ multiplied by e^{-st_0} , i.e.,

$$L[f(t - t_0)] = e^{-st_0} F(s) \quad (1.86)$$

Property 6: Frequency Shifting: The multiplication of $f(t)$ by e^{-at} has the effect of replacing s by $(s + a)$ in the Laplace transform

$$L[e^{-at}f(t)] = F(s + a) \quad (1.87)$$

Property 7: Convolution: This property states that the convolution of two real functions is equal to the multiplication of their respective functions. If

$$L[f_1(t)] = F_1(s) \quad \text{and} \quad L[f_2(t)] = F_2(s)$$

By convolution, it can be written as:

$$L[f_1(t) * f_2(t)] = F_1(s)F_2(s) \quad (1.88)$$

The mathematical expression given in Eq. (1.88) is known as the convolution theorem. The word *convolve* means “to revolve continuously”. The two functions $f_1(t)$ and $f_2(t)$ are multiplied in such a way that one is continually moving with time (say λ) relative to the other. Laplace transforms are very useful for solving problems in science and engineering. Some useful Laplace transforms are given in Appendix A.

CHAPTER 2

Linear Waveslicing: High-pass Circuits

LEARNING OBJECTIVES

After reading this chapter, you will be able to:

- Derive the responses of high-pass RC and RL circuits to different types of inputs
- Describe the application of a high-pass circuit as a differentiator
- Understand the use of a double differentiator as a rate-of-rise amplifier

2.1 INTRODUCTION

Linear systems are those that satisfy both homogeneity and additivity.

(i) Homogeneity: Let x be the input to a linear system and y the corresponding output, as shown in Fig. 2.1. If the input is doubled ($2x$), then the output is also doubled ($2y$). In general, a system is said to exhibit homogeneity if, for the input nx to the system, the corresponding output is ny (where n is an integer). Thus, a linear system enables us to predict the output.

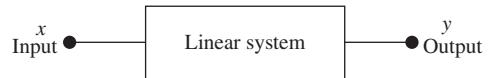


FIGURE 2.1 A linear system

(ii) Additivity: For two input signals x_1 and x_2 applied to a linear system, let y_1 and y_2 be the corresponding output signals. Further, if $(x_1 + x_2)$ is the input to the linear system and $(y_1 + y_2)$ the corresponding output, it means that the measured response will just be the sum of its responses to each of the inputs presented separately. This property is called additivity. Homogeneity and additivity, taken together, comprise the principle of superposition.

(iii) Shift invariance: Let an input x be applied to a linear system at time t_1 . If the same input is applied at a different time instant t_2 , the two outputs should be the same except for the corresponding shift in time. A linear system that exhibits this property is called a shift-invariant linear system. All linear systems are not necessarily shift invariant.

A circuit employing linear circuit components, namely, R , L and C can be termed a linear circuit. When a sinusoidal signal is applied to either RC or RL circuits, the shape of the signal is preserved at the output, with a change in only the amplitude and the phase. However, when a non-sinusoidal signal is transmitted through a linear network, the form of the output signal is altered. The process by which the shape of a non-sinusoidal signal passed through a linear network is altered is called linear waveslicing. We study the response of high-pass RC and RL circuits to different types of inputs in the following sections.

2.2 HIGH-PASS CIRCUITS

Figures 2.2(a) and 2.2(b) represent high-pass RC and RL circuits, respectively.

Consider the high-pass RC circuit shown in Fig. 2.2(a). The capacitor offers a low reactance ($X_C = 1/j\omega C$) as the frequency increases; hence, the output is large. Consequently, high-frequency signals are passed to the output with negligible attenuation whereas, at low frequencies, due to the large reactance

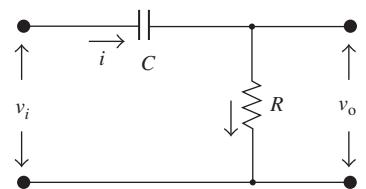


FIGURE 2.2(a) A high-pass RC circuit

offered by the condenser, the output signal is small. Similarly, in the circuit shown in Fig. 2.2(b), the inductive reactance $X_L (= j\omega L)$ increases with frequency, leading to a large output. At low frequencies, the reactance of the inductor X_L becomes small; hence, the output is small. Therefore, the circuits in Figs. 2.2(a) and (b) are called high-pass circuits. In the case of L , X_L is directly proportional to frequency; and in the case of C , X_C is inversely proportional to frequency. C and L may therefore be called inverse circuit elements. Thus, in the high-pass circuit of Fig. 2.2(a), C appears as a series element; and in the high-pass circuit of Fig. 2.2(b), L appears as a shunt element. The time constant τ is given by: $\tau = RC = L/R$.

What will be the response if different types of inputs such as sinusoidal, step, pulse, square wave, exponential and ramp are applied to a high-pass circuit?

2.2.1 Response of the High-pass RC Circuit to Sinusoidal Input

Let us consider the response of a high-pass RC circuit, shown in Fig. 2.2(a) when a sinusoidal signal is applied as the input. Here:

$$v_o = v_i \frac{R}{R + \frac{1}{j\omega C}} \quad (2.1)$$

$$\left| \frac{v_o}{v_i} \right| = \frac{R}{\sqrt{R^2 + \left(\frac{1}{\omega C} \right)^2}} = \frac{R}{R \sqrt{1 + \left(\frac{1}{\omega CR} \right)^2}} = \frac{1}{\sqrt{1 + \left(\frac{1}{\omega CR} \right)^2}}$$

$$\text{Let } \omega_1 = \frac{1}{CR} = \frac{1}{\tau} \quad (2.2)$$

where, $\tau = RC$, the time constant of the circuit.

$$\left| \frac{v_o}{v_i} \right| = \frac{1}{\sqrt{1 + \left(\frac{\omega_1}{\omega} \right)^2}} = \frac{1}{\sqrt{1 + \left(\frac{T}{\tau} \right)^2}} \quad (2.3)$$

The signal undergoes a phase change and the phase angle, θ , is given by:

$$\theta = \tan^{-1} (\omega_1/\omega) = \tan^{-1} (T/\tau)$$

At $\omega = \omega_1$:

$$\left| \frac{v_o}{v_i} \right| = \frac{1}{\sqrt{2}} = 0.707$$

Hence, f_1 is the lower half-power frequency of the high-pass circuit. The expression for the output for the circuits in Figs. 2.2(a) and (b) is the same as given by Eq. (2.3). Figure 2.3(a) shows a typical frequency-response curve for a sinusoidal input to a high-pass circuit. The frequency response and the phase

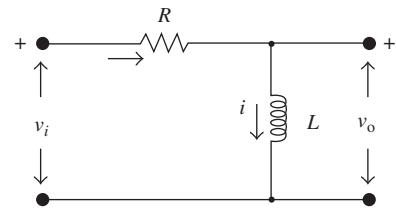


FIGURE 2.2(b) A high-pass RL circuit

shift of the circuit shown in Fig. 2.2(a) are plotted in Figs. 2.3(b) and 2.3(c), respectively, for different values of τ .

From Fig. 2.3(b), it is seen that as the half-power frequency decreases for larger values of τ , the gain curve shows a sharper rise. From Fig. 2.3(c), it is seen that if $T/\tau > 20$, the phase angle approaches approximately 90° .

2.2.2 Response of the High-pass RC Circuit to Step Input

A step voltage, shown in Fig. 2.4(a), is represented mathematically as:

$$\left. \begin{array}{ll} v_i = 0 & \text{for } t < 0 \\ v_i = V & \text{for } t \geq 0 \end{array} \right\} \quad (2.4)$$

As discussed in Chapter 1, a step is a sudden change in voltage, say at an instant $t = 0$, from say zero to V , in which case, it is called a positive step. The voltage change could also be from zero to $-V$, in which case it is called a negative step. This is an important signal in pulse and digital circuits. For instance, consider an *n-p-n* transistor in the CE mode. Assume that $V_{BE} = 0$. Then, the voltage at the collector is approximately V_{CC} . Now if a battery with voltage V_σ is connected so that $V_{BE} = V_\sigma$, as the device is switched ON, the voltage at the collector which earlier was V_{CC} , now falls to $V_{CE(\text{sat})}$. This means a negative step is generated at the collector. However, if the transistor is initially turned ON so that the voltage at its collector is $V_{CE(\text{sat})}$ and V_{BE} is made zero, then as the transistor is switched OFF, the voltage at its collector rises to V_{CC} . A positive step is now generated at its collector.

For a step input, let the output voltage be of the form:

$$v_o = B_1 + B_2 e^{-t/\tau} \quad (2.5)$$

where, $\tau = RC$, the time constant of the circuit.

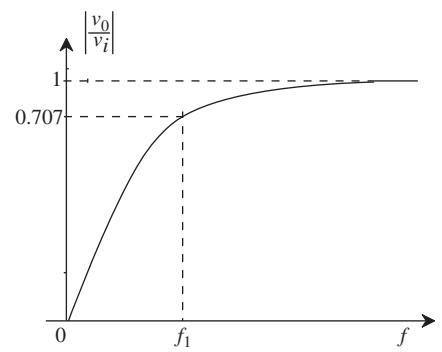


FIGURE 2.3(a) A typical frequency response curve for a sinusoidal input

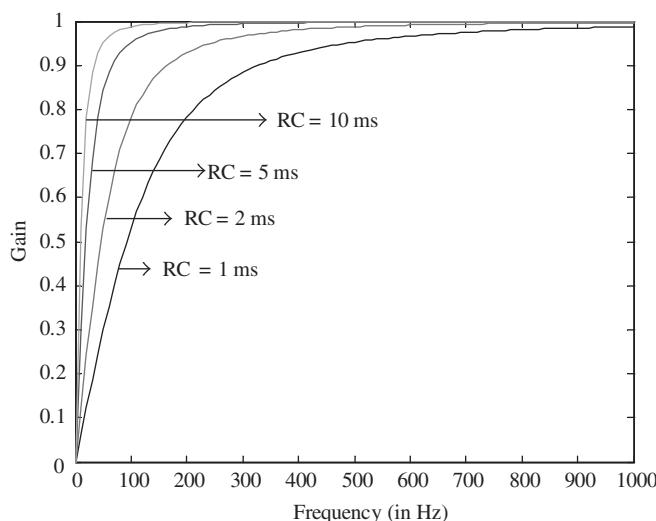
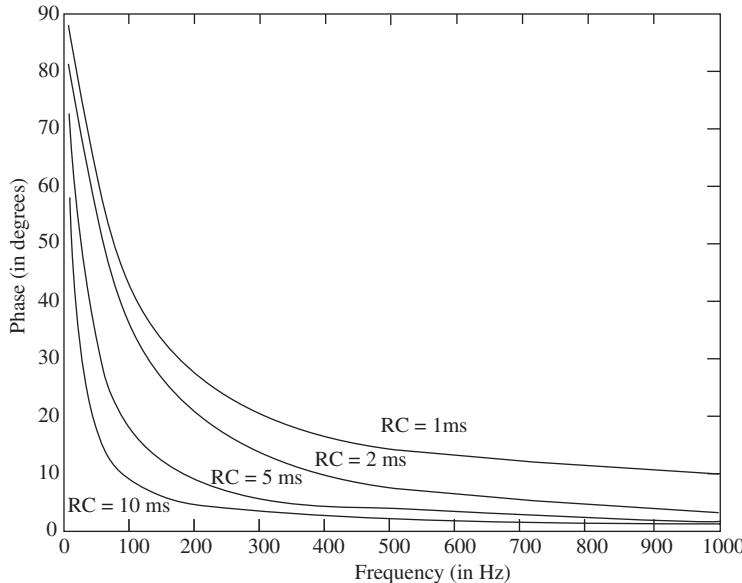


FIGURE 2.3(b) The frequency-response curve for different values of τ

FIGURE 2.3(c) Phase versus frequency curve for different values of τ

B_1 is the steady-state value of the output voltage because as $t \rightarrow \infty$, $v_o \rightarrow B_1$.

Let the final value of this output voltage be called v_f . Then:

$$v_f = B_1 \quad (2.6)$$

B_2 is determined by the initial output voltage. At $t = 0$, when the step voltage is applied, the change at the output is the same as the change at the input, because a capacitor is connected between the input and the output. Hence,

$$v_i = v_o = B_1 + B_2 \quad (2.7)$$

Therefore,

$$B_2 = v_i - B_1$$

Using Eq. (2.6):

$$B_2 = v_i - v_f \quad (2.8)$$

Substituting the values of B_1 and B_2 from Eqs. (2.6) and (2.8) respectively in Eq. (2.5), the general solution is given by the relation:

$$v_o = v_f + (v_i - v_f) e^{-t/\tau} \quad (2.9)$$

For a high-pass RC circuit, let us calculate v_i and v_f . As the capacitor blocks the dc component of the input, $v_f = 0$. Since the capacitor does not allow sudden voltage changes, a change in the voltage of the input signal is necessarily accompanied by a corresponding change in the voltage of the output signal. Hence, at $t = 0+$ when the input abruptly rises to V , the output also changes by V .

Therefore, $v_i = V$.

Substituting the values of v_f and v_i in Eq. (2.9):

$$v_o(t) = V e^{-t/\tau} \quad (2.10)$$

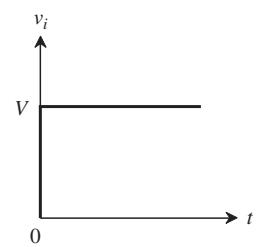


FIGURE 2.4(a) Step voltage

If

$$x = \frac{t}{\tau} \quad (2.11)$$

$$\frac{v_o(t)}{V} = e^{-x} \quad (2.12)$$

$v_0(t)/V$ for x varying from 0 to 5 is shown in Table 2.1. The response of the circuit is plotted in Fig. 2.4(b).

At $t = 0$, when a step voltage V is applied as input to the high-pass circuit, as the capacitor will not allow any sudden changes in voltage, it behaves as a short circuit. Hence, the input voltage V appears at the output. As the input remains constant, the charge on the capacitor discharges exponentially with the time constant τ . After approximately 5τ , when τ is small, the output reaches the steady-state value. As τ becomes large, it takes a longer time for the charge on the capacitor to decay; hence, the output takes longer to reach the steady-state value. In general, the response of the circuit to different types of inputs is obtained by formulating the differential equation and solving for the output.

For the circuit in Fig. 2.2(a):

$$v_i = \frac{1}{C} \int idt + v_o \quad (2.13)$$

But $v_o = iR$

$$i = \frac{v_o}{R} \quad (2.14)$$

$$\therefore v_i = \frac{1}{RC} \int v_o dt + v_o \quad (2.15)$$

For a step input, put $v_i = V$ and $RC = \tau$. Taking Laplace transforms:

$$\frac{V}{s} = \frac{v_o(s)}{s\tau} + v_o(s) \left(1 + \frac{1}{s\tau}\right) = \frac{V}{s} \quad v_o(s) \left(s + \frac{1}{\tau}\right) = V$$

$$v_o(s) = \frac{V}{\left(s + \frac{1}{\tau}\right)} \quad (2.16)$$

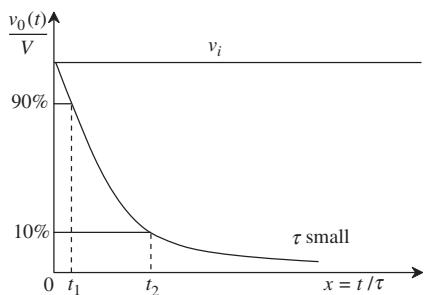


FIGURE 2.4(b) The response of a high-pass circuit to step input

TABLE 2.1 $v_o(t)/V$ as a function of x

x	$\frac{v_o(t)}{V}$
0.0	1
0.5	0.607
1.0	0.368
2.0	0.135
3.0	0.050
4.0	0.018
5.0	0.007

Taking Laplace inverse:

$$v_o(t) = V e^{-t/\tau} \quad (2.17)$$

Fall time (t_f): When a step voltage V is applied to a high-pass circuit, the output suddenly changes as the input and then the capacitor charges to V . Once the capacitor C is fully charged, it behaves as an open circuit for the dc input signal. Hence, in the steady-state, the output should be zero. However, the output does not reach this steady-state instantaneously; there is some time delay before the voltage on the capacitor decays and reaches the steady-state value. The time taken for the output voltage to fall from 90 per cent of its initial value to 10 per cent of its initial value is called the fall time. It indicates how fast the output reaches its steady-state value. The output voltage at any instant, in the high-pass circuit is given by Eq. (2.17). At $t = t_1$, $v_o(t_1) = 90\%$ of $V = 0.9$ V. Therefore,

$$0.9 = e^{-t_1/\tau} \quad e^{t_1/\tau} = 1/0.9 = 1.11 \quad t_1/\tau = \ln(1.11)$$

$$t_1 = \tau \ln(1.11) = 0.1\tau$$

At $t = t_2$, $v_o(t) = 10\%$ of $V = 0.1$ V. Hence,

$$0.1 = e^{-t_2/\tau} \quad e^{t_2/\tau} = 1/0.1 = 10 \quad t_2 = \tau \ln(10) = 2.3\tau$$

The fall time is calculated as:

$$t_f = t_2 - t_1 = 2.3\tau - 0.1\tau = 2.2\tau \quad (2.18)$$

The lower half-power frequency of the high-pass circuit is:

$$f_1 = \frac{1}{2\pi RC} \quad (2.19)$$

$$\tau = RC = \frac{1}{2\pi f_1} \quad (2.20)$$

$$t_f = 2.2\tau = \frac{2.2}{2\pi f_1} = \frac{0.35}{f_1} \quad (2.21)$$

Hence, the fall time is inversely proportional to f_1 , the lower half-power frequency. As f_1 , is inversely proportional to τ , the shape of the signal at the output changes with τ .

E X A M P L E

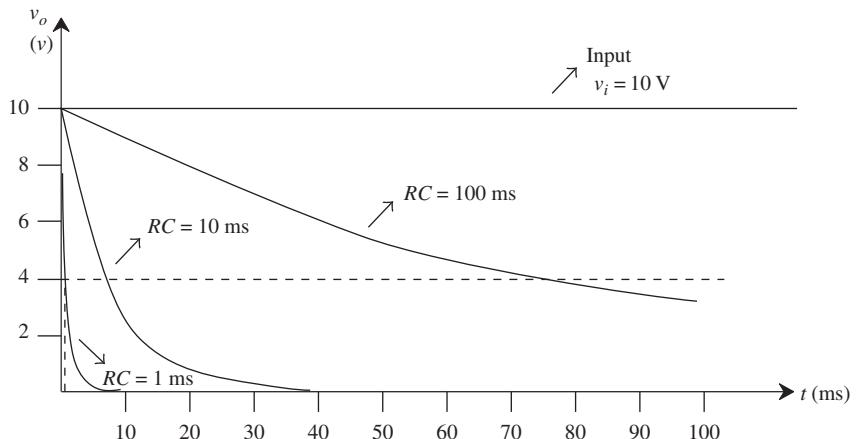
Example 2.1: A 10-Volt step input is applied to a high-pass RC circuit. Plot the response of the circuit when

- (i) $RC = 1$ ms
- (ii) $RC = 10$ ms
- (iii) $RC = 100$ ms.

Solution: Here, we use the expression for the response to a step input in Eq. (2.17) and calculate the output voltage for different values of time constants (as shown in the Table 2.2) and plot the response, as shown in Fig. 2.5.

TABLE 2.2 The output voltage for different time constants

Time t (ms)	$v_o = 10 e^{-t/\tau}$ (Volts)		
	$\tau = 1$ ms	$\tau = 10$ ms	$\tau = 100$ ms
0	10	10	10
1	3.68	9	9.9
2	1.35	8.18	9.8
4	0.18	6.7	9.6
5	—	6.06	9.512
10	—	3.68	9
20	—	1.35	8.18
40	—	0.18	6.7
100	—	—	3.68

FIGURE 2.5 The response of the high-pass circuit to a step input for different values of τ

To visualize the response of the high-pass circuit for different time constants, consider Example 2.1. It is evident from this example that the output decays exponentially to zero more rapidly when the time constant becomes smaller. This response tells us that the smaller the value of τ , the sharper the response of a high-pass circuit; resulting in a narrower pulse. The width of the pulse increases with an increase in τ .

2.2.3 Response of the High-pass RC Circuit to Pulse Input

A positive pulse is mathematically represented as the combination of a positive step followed by a delayed negative step i.e., $v_i = V_u(t) - V_u(t - t_p)$ where, t_p is the duration of the pulse as shown in Fig. 2.6.

To understand the response of a high-pass circuit to this pulse input, let us trace the sequence of events following the application of the input signal.

At $t = 0$, v_i abruptly rises to V . As a capacitor is connected between the input and output, the output also changes abruptly by the same amount. As the input remains constant, the output decays exponentially to V_1 at $t = t_p$. Therefore,

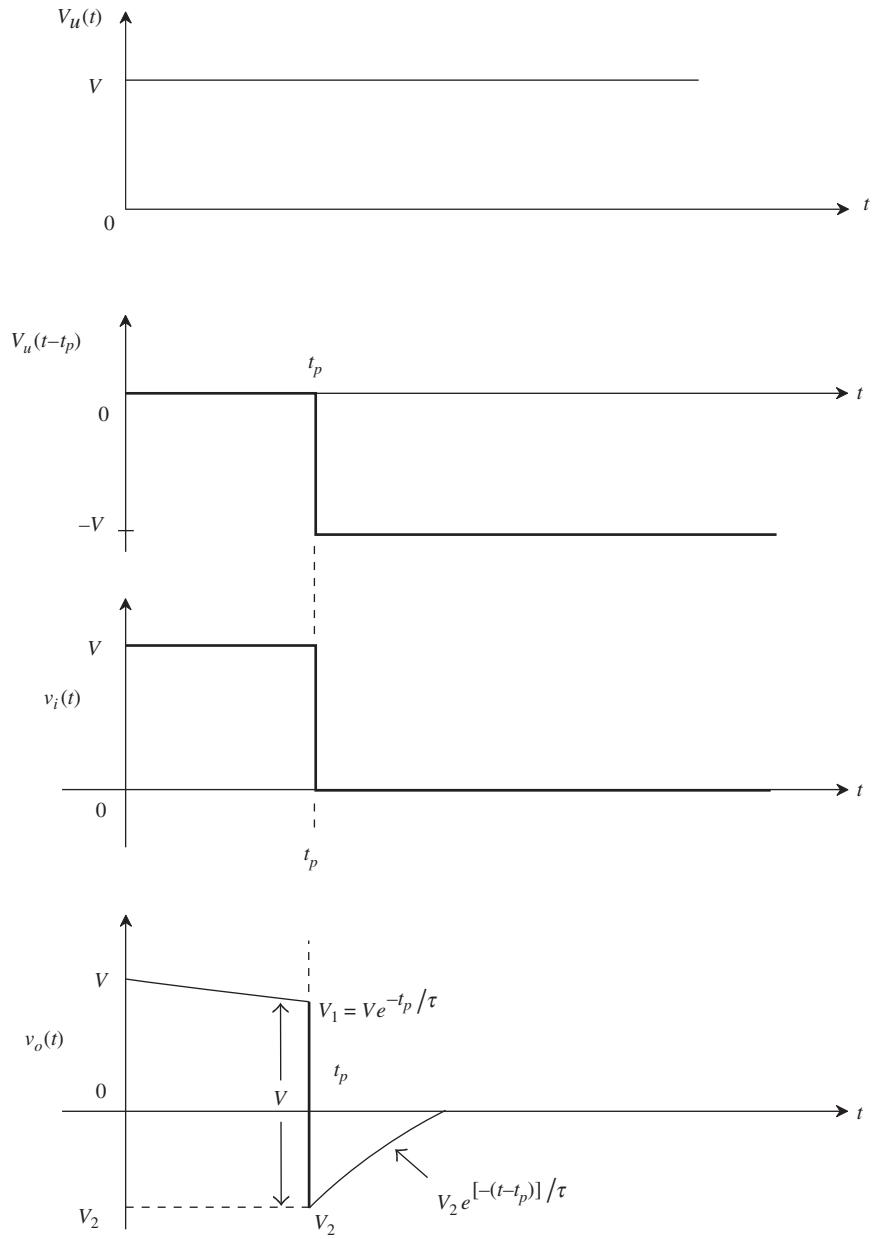


FIGURE 2.6 Pulse input and output of a high-pass circuit

$$V_1 = V e^{-t_p/\tau} \quad (2.22)$$

At $t = t_p$, the input abruptly falls by V , v_o also falls by the same amount. In other words, $v_o = V_1 - V$. Since V_1 is less than V ; v_o is negative and its value is V_2 and this decays to zero exponentially. For $t > t_p$,

$$v_o = V_2 e^{[-(t-t_p)/\tau]} = (V_1 - V) e^{[-(t-t_p)/\tau]} \quad (2.23)$$

Substituting Eq. (2.22) in Eq. (2.23):

$$v_o = V(e^{-t_p/\tau} - 1) e^{[-(t-t_p)]/\tau} \quad (2.24)$$

The response of high-pass circuits with different values of τ to pulse input is plotted in Fig. 2.7. As is evident from the preceding discussion, when a pulse is passed through a high-pass circuit, it gets distorted. Only when the time constant τ is very large, the shape of the pulse at the output is preserved, as can be seen from Fig. 2.7(b). However, as shown in Fig. 2.7(c), when the time constant τ is neither too small nor too large, there is a tilt (also called a sag) at the top of the pulse and an undershoot at the end of the pulse. If $\tau \ll t_p$, as in Fig. 2.7(d), the output comprises a positive spike at the beginning of the pulse and a negative spike at the end of the pulse. In other words, a high-pass circuit converts a pulse into spikes by employing a small time constant; this process is called peaking.

If the distortion is to be negligible, τ has to be significantly larger than the duration of the pulse. In general, there is an undershoot at the end of the pulse. The larger the tilt (for small τ), the larger the undershoot and the smaller the time taken for this undershoot to decay to zero. The area above the reference level (A_1) is the same as the area below the reference level (A_2). Let us verify this using Fig. 2.8.

Area A_1 : For $0 < t < t_p$:

$$\begin{aligned} v_o &= Ve^{-t/\tau} \\ A_1 &= \int_0^{t_p} Ve^{-t/\tau} dt = [-V\tau e^{-t/\tau}]_0^{t_p} \\ A_1 &= [-V\tau e^{-t_p/\tau} + V\tau] = V\tau(1 - e^{-t_p/\tau}) \end{aligned} \quad (2.25)$$

Similarly,

$$\begin{aligned} A_2 &= \int_{t_p}^{\infty} V(e^{-t_p/\tau} - 1)e^{-(t-t_p)/\tau} dt = \int_{t_p}^{\infty} [Ve^{-t/\tau} - Ve^{-(t-t_p)/\tau}] dt \\ &= \left[\frac{Ve^{-t/\tau}}{\frac{-1}{\tau}} \right]_{t_p}^{\infty} - \left[V \frac{1}{\frac{-1}{\tau}} e^{-(t-t_p)/\tau} \right]_{t_p}^{\infty} \end{aligned}$$

$$A_2 = [V\tau e^{-t_p/\tau} - V\tau] = -V\tau(1 - e^{-t_p/\tau}) \quad (2.26)$$

From Eqs. (2.25) and (2.26) it is evident that

$$|A_1| = |A_2| \quad (2.27)$$

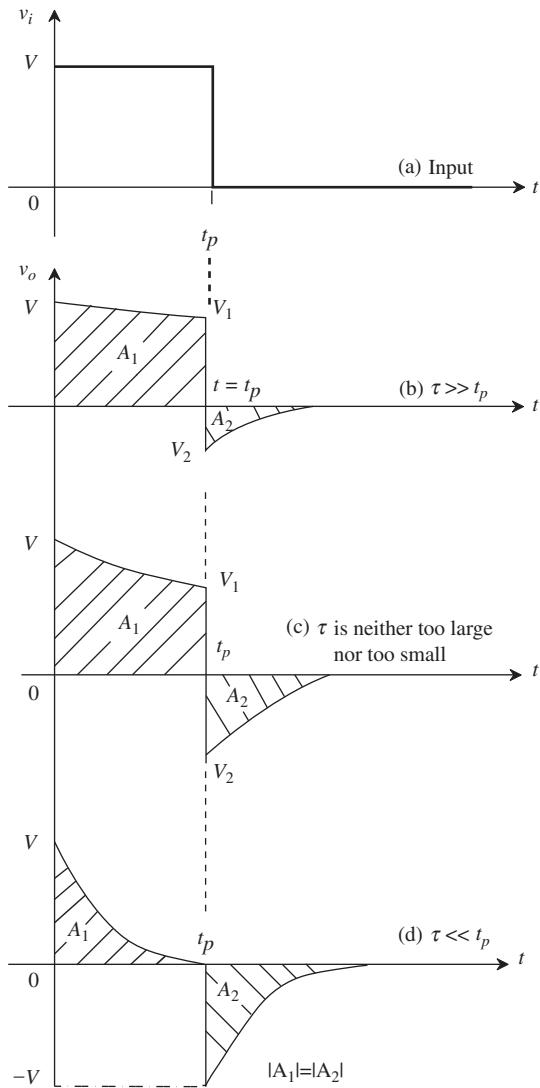


FIGURE 2.7 The response of a high-pass circuit to a pulse input

EXAMPLE

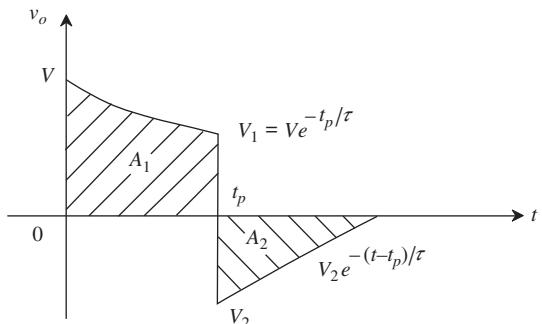
Example 2.2: A pulse of amplitude 10 V and duration 10 μ s is applied to a high-pass RC circuit. Sketch the output waveform indicating the voltage levels for (i) $RC = t_p$, (ii) $RC = 0.5t_p$ and (iii) $RC = 2t_p$.

Solution: (i) When $RC = t_p = \tau$

At $t = t_p$

$$V_1 = 10 e^{-(10 \times 10^{-6})/(10 \times 10^{-6})} = 10^{-1} = 3.678 \text{ V}$$

$$v_{o1} = 10 e^{-t/(10 \times 10^{-6})} \quad \text{for } t < t_p$$

FIGURE 2.8 The calculation of A_1 and A_2

$$v_o(t > t_p) = (V_1 - 10)e^{-(t-10 \times 10^{-6})/(10 \times 10^{-6})} = -6.322 e^{-(t-10 \times 10^{-6})/(10 \times 10^{-6})}$$

(ii) When $RC = \tau = 0.5t_p$

At $t = t_p$

$$V_1 = 10 e^{-(10 \times 10^{-6})/(0.5 \times 10 \times 10^{-6})} = 10e^{-2} = 1.35 \text{ V}$$

$$v_{o1} = 10 e^{-t/(0.5 \times 10 \times 10^{-6})} \quad \text{for } t < t_p$$

$$v_o(t > t_p) = -8.65 e^{-(t-10 \times 10^{-6})/(0.5 \times 10 \times 10^{-6})}$$

(iii) When $RC = \tau = 2t_p$

At $t = t_p$

$$V_1 = 10 e^{(-10 \times 10^{-6})/(2 \times 10 \times 10^{-6})} = 10e^{-0.5} = 6.05 \text{ V}$$

$$v_{o1} = 10 e^{-t/(2 \times 10 \times 10^{-6})} \quad \text{for } t < t_p$$

$$v_o(t > t_p) = -3.935 e^{-(t-10 \times 10^{-6})/(2 \times 10 \times 10^{-6})}$$

Based on these results, the output waveforms are sketched as in Fig. 2.9(a), (b) and (c) corresponding to cases (i), (ii) and (iii), respectively.

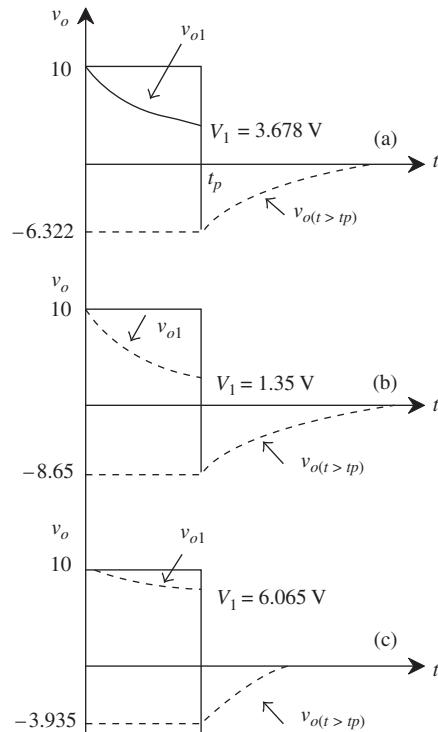


FIGURE 2.9(b) The response of a high-pass circuit for different values of τ

From Example 2.2, it is seen that when τ is large, the amplitude distortion in the output is minimal, i.e., the shape of the signal is almost preserved in the output. As the value of τ decreases, the charge on the capacitor decreases by a larger amount during the period the input remains constant. Consequently, the output is distorted. If τ decreases still further, it can be seen that the output contains positive and negative spikes. The shape of the signal in the output is essentially decided by the time constant of the circuit.

2.2.4 Response of the High-pass RC Circuit to Square-wave Input

A waveform that has a constant amplitude, say, V' for a time T_1 and has another constant amplitude, V'' for a time T_2 , and which is repetitive with a time $T = (T_1 + T_2)$, is called a square wave. In a symmetric square wave, $T_1 = T_2 = T/2$. Figure 2.10 shows typical input-output waveforms of the high-pass circuit when a square wave is applied as the input signal.

As the capacitor blocks the DC, the DC component in the output is zero. Thus, as expected, even if the signal at the input is referenced to an arbitrary dc level, the output is always referenced to the zero level. It can be proved that whatever the dc component associated with a periodic input waveform, the dc level of the steady-state output signal for the high-pass circuit is always zero as shown in Fig. 2.10. To verify this statement, we write the KVL equation for the high-pass circuit:

$$v_i = \frac{q}{C} + v_o \quad (2.28)$$

where, q is the charge on the capacitor. Differentiating with respect to t :

$$\frac{dv_i}{dt} = \frac{1}{C} \frac{dq}{dt} + \frac{dv_o}{dt} \quad (2.29)$$

$$\text{But } i = \frac{dq}{dt}$$

Substituting this condition in Eq. (2.29):

$$\frac{dv_i}{dt} = \frac{i}{C} + \frac{dv_o}{dt}$$

Since $v_o = iR$, $i = v_o/R$ and $RC = \tau$. Therefore,

$$\therefore \frac{dv_i}{dt} = \frac{v_o}{\tau} + \frac{dv_o}{dt} \quad (2.30)$$

Multiplying by dt and integrating over the time period T we get:

$$\int_0^T dv_i = [v_i]_0^T = v_i(T) - v_i(0) \quad (2.31)$$

$$\int_0^T \frac{v_o}{\tau} dt = \frac{1}{\tau} \int_0^T v_o dt \quad (2.32)$$

$$\int_0^T dv_o = [v_o]_0^T = v_o(T) - v_o(0) \quad (2.33)$$

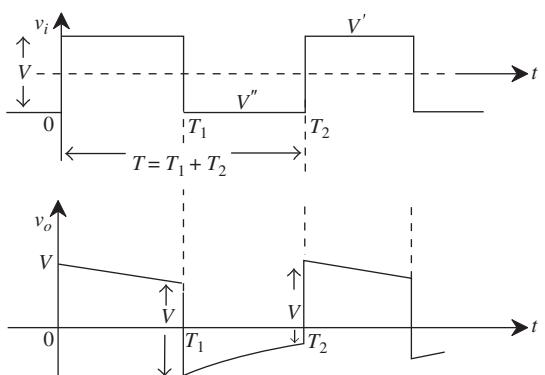


FIGURE 2.10 A typical steady-state output of a high-pass circuit with a square wave as input

From Eqs. (2.30), (2.31), (2.32) and (2.33):

$$v_i(T) - v_i(0) = \frac{1}{\tau} \int_0^T v_o dt + [v_o(T) - v_o(0)] \quad (2.34)$$

Under steady-state conditions, the output and the input waveforms are repetitive with a time period T . Therefore, $v_i(T) = v_o(T)$ and $v_i(0) = v_o(0)$. Hence, from Eq. (2.34):

$$\int_0^T v_o dt = 0 \quad (2.35)$$

As the area under the output waveform over one cycle represents the DC component in the output, from Eq. (2.35) it is evident that the DC component in the steady-state is always zero. Now let us consider the response of the high-pass RC circuit for a square-wave input for different values of the time constant τ , as shown in Fig. 2.11.

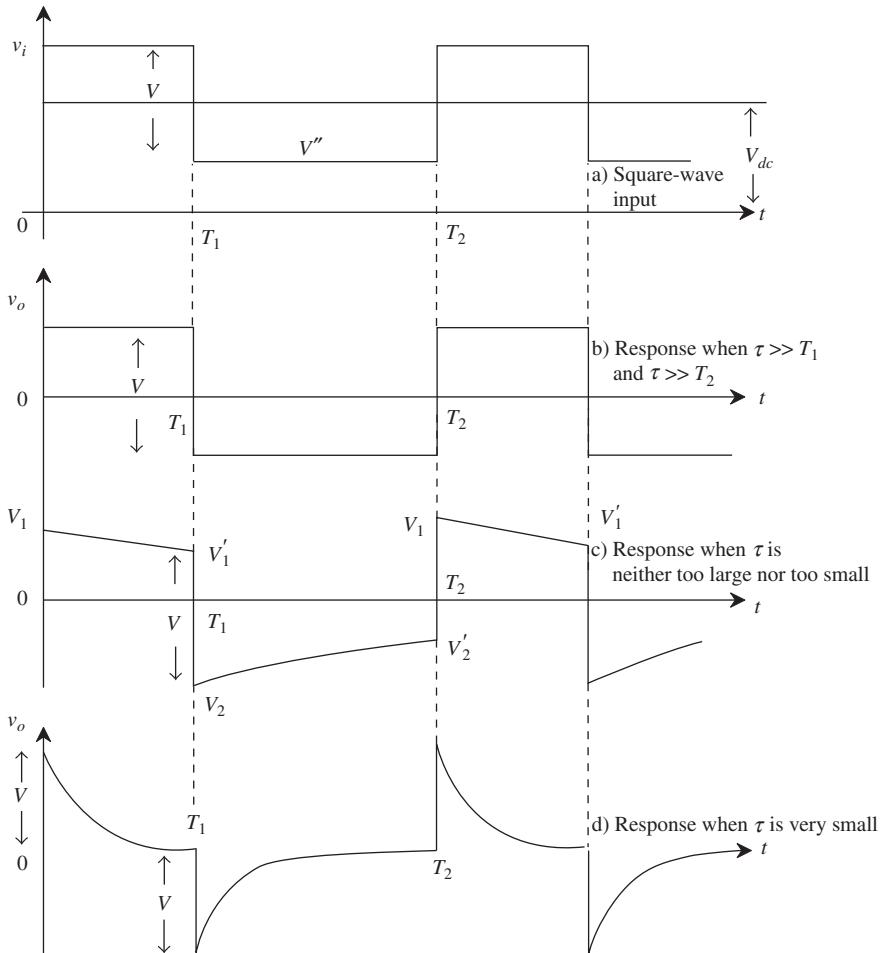


FIGURE 2.11 The response of a high-pass circuit for a square-wave input

As is evident from the waveform in Fig. 2.11(b), there is no appreciable distortion in the output if τ is large. The output is almost the same as the input except for the fact that there is no DC component in the output. As τ decreases, as in Fig. 2.11(c), there is a tilt in the positive duration (amplitude decreases from V_1 to V_1' during the period 0 to T_1) and there is also a tilt in the negative duration (amplitude increases from V_2 to V_2' during the period T_1 to T_2). A further decrease in the value of τ [see Fig. 2.11(d)] gives rise to positive and negative spikes. There is absolutely no resemblance between the signals at the input and the output. However, this condition is imposed on high-pass circuits to derive spikes. In case a pulse is required to trigger another circuit, we see that the pulses obtained either at the rising edge (positive spike) or at the trailing edge (negative spike) may be used to edge trigger a flip-flop, as discussed in later chapters in the book. Let us consider the typical response of the high-pass circuit for a square-wave input shown in Fig. 2.12.

From Fig. 2.12 and using Eq. (2.17) we have:

$$\begin{aligned} V_1' &= V_1 e^{-T_1/\tau} \quad \text{and} \quad V_1' - V_2 = V \\ V_2' &= V_2 e^{-T_2/\tau} \quad \text{and} \quad V_1 - V_2' = V \end{aligned} \quad (2.36)$$

For a symmetric square wave $T_1 = T_2 = T/2$. And, because of symmetry:

$$V_1 = -V_2 \quad \text{and} \quad V_1' = -V_2' \quad (2.37)$$

From Eq. (2.36):

$$V_1' - V_2 = V$$

But

$$V_1' = V_1 e^{-T_1/\tau}$$

Therefore,

$$V_1 e^{-T_1/\tau} - V_2 = V \quad (2.38)$$

From Eq. (2.37):

$$V_1 = -V_2$$

Substituting in Eq. (2.38):

$$V_1 e^{-T_1/\tau} + V_1 = V \quad V_1(1 + e^{-T_1/\tau}) = V$$

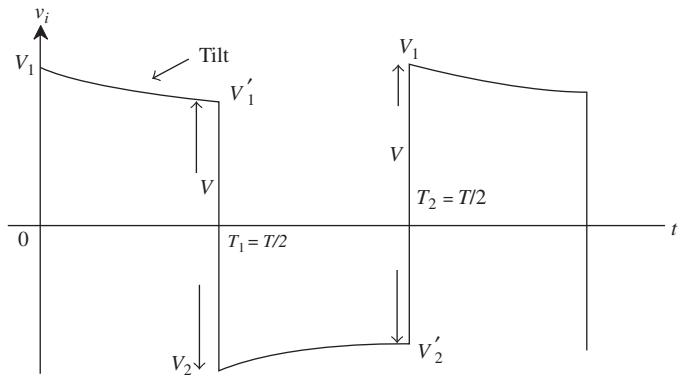


FIGURE 2.12 The typical response of a high-pass RC circuit for a square-wave input

Thus,

$$V_1 = \frac{V}{1 + e^{-T_1/\tau}} \quad (2.39)$$

For a symmetric square wave, as $T_1 = T_2 = T/2$, Eq. (2.39) is written as:

$$V_1 = \frac{V}{1 + e^{-T/2\tau}} \quad (2.40)$$

But

$$V'_1 = V_1 e^{-T/2\tau} = \frac{V}{(1 + e^{-T/2\tau})} \times e^{-T/2\tau} \quad (2.41)$$

There is a tilt in the output waveform. The percentage tilt, P , is defined as:

$$P = \frac{V_1 - V'_1}{\frac{V}{2}} \times 100\% \quad (2.42)$$

$$P = \frac{\frac{V}{1 + e^{-T/2\tau}} - \frac{V e^{-T/2\tau}}{1 + e^{-T/2\tau}}}{\frac{V}{2}} \times 100\% = \frac{V}{1 + e^{-T/2\tau}} \frac{[1 - e^{-T/2\tau}]}{\frac{V}{2}} \times 100\%$$

$$P = \frac{(1 - e^{-T/2\tau})}{(1 + e^{-T/2\tau})} \times 200\% \quad (2.43)$$

If $T/2\tau \ll 1$,

$$e^{-T/2\tau} = 1 - \frac{T}{2\tau} \quad (2.44)$$

Therefore,

$$P = \frac{1 - \left(1 - \frac{T}{2\tau}\right)}{1 + \left(1 - \frac{T}{2\tau}\right)} \times 200\% = \frac{\frac{T}{2\tau}}{2 - \frac{T}{2\tau}} \times 200\% \cong \frac{T}{2\tau} \times 100\% \text{ since } \frac{T}{2\tau} \ll 1$$

Thus, for a symmetrical square wave:

$$P = \frac{T}{2\tau} \times 100\%, \quad (2.45)$$

Equation (2.45) tells us that the smaller the value of τ when compared to the half-period of the square wave ($T/2$), the larger is the value of P . In other words, distortion is large with small τ and is small with large τ . The lower half-power frequency, $f_1 = 1/2\pi\tau$.

Therefore,

$$\frac{1}{2\tau} = \pi f_1$$

Putting in Eq. (2.45)

$$P = \pi f_1 T \times 100\%$$

Therefore,

$$P = \frac{\pi f_1}{f} \times 100\% \quad \text{since } T = \frac{1}{f} \quad (2.46)$$

Let us calculate and plot the response by taking specific examples.

EXAMPLE

Example 2.3: A 10 Hz square wave whose peak-to-peak amplitude is 2 V is fed to an amplifier. Calculate and plot the output waveform if the lower 3-dB frequency is 0.3 Hz.

Solution: Let C be the condenser through which the signal is connected to the amplifier, having an input resistance R , as shown in Fig. 2.13(a). This is essentially the high-pass circuit in Fig. 2.1(a).

The lower 3-dB frequency $f_1 = 0.3$ Hz

Input frequency is $f = 10$ Hz

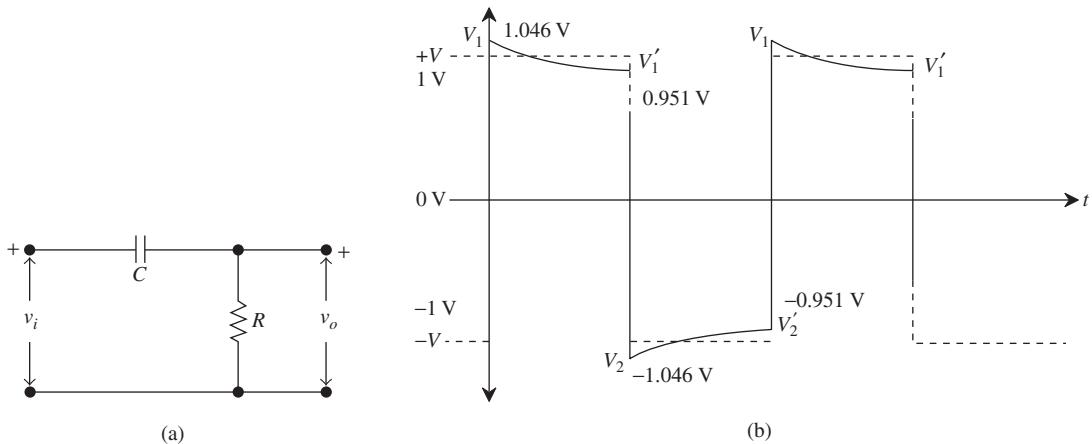


FIGURE 2.13(a) The coupling network and (b) The response of the circuit

$$\tau = RC = \frac{1}{2\pi f_1} = \frac{1}{2\pi(0.3)} = 0.53 \text{ s}$$

$$T = \frac{1}{f} = \frac{1}{10} = 0.1 \text{ s}$$

Therefore,

$$\frac{T}{2} = 0.05 \text{ s}$$

$$V_1 = \frac{V}{1 + e^{-T/2\tau}} = \frac{2}{1 + e^{-0.05/0.53}} = 1.046 \text{ V} \quad V_1' = V_1 e^{-T/2\tau} = 1.046 e^{-0.05/0.53} = 0.951 \text{ V}$$

$$V_1 = -V_2 \quad \text{and} \quad V'_1 = -V'_2$$

$$V_1 = |V_2| = 1.046 \text{ V} \quad V'_1 = |V'_2| = 0.951 \text{ V}$$

The response of the circuit is shown in Fig. 2.13(b).

EXAMPLE

Example 2.4: A 20-Hz symmetrical square wave, shown in Fig. 2.14(a), with peak-to-peak amplitude of 2 V is impressed on a high-pass circuit shown in Fig. 2.1(a) whose lower 3-dB frequency is 10 Hz. Calculate and sketch the output waveform. What is the peak-to-peak output amplitude of the above waveform?

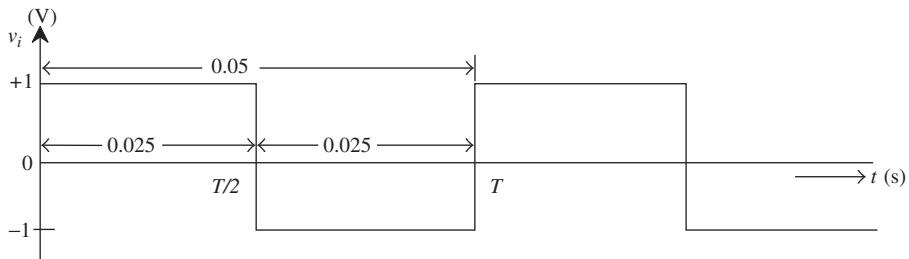


FIGURE 2.14(a) Input to the high-pass circuit

Solution: The lower 3-dB frequency:

$$f_1 = \frac{1}{2\pi RC} = 10 \text{ Hz} \quad RC = \tau = \frac{1}{2\pi f_1} = \frac{1}{2\pi \times 10} = 0.0159 \text{ s}$$

Input signal frequency $f = 20 \text{ Hz}$

$$\text{Time period of the input } T = \frac{1}{f} = \frac{1}{20} = 0.05 \text{ s}$$

$$\frac{T}{2} = \frac{0.05}{2} = 0.025 \text{ s}$$

Therefore, τ is small compared to $T/2$; so the capacitor charges and discharges appreciably in each half-cycle. Since the input is a symmetrical square wave, $V_1 = -V_2$, i.e., $|V_1| = |V_2|$, $V'_1 = -V'_2$ i.e., $|V'_1| = |V'_2|$. The peak-to-peak input = 2 V. Hence,

$$V_1 = \frac{V}{1 + e^{(-T/2)/\tau}} = \frac{2}{1 + e^{-0.025/0.0159}} = 1.656 \text{ V} \quad V_2 = -V_1 = -1.656 \text{ V}$$

Peak-to-peak value of output = $V_1 - V_2 = 3.312 \text{ V}$.

$$V'_1 = V_1 e^{(-T/2)/\tau} = 1.656 e^{-(0.025/0.0159)} = 0.344 \text{ V}$$

$$V'_1 = -V'_2 = 0.344 \text{ V}$$

The output is plotted in Fig. 2.14(b).

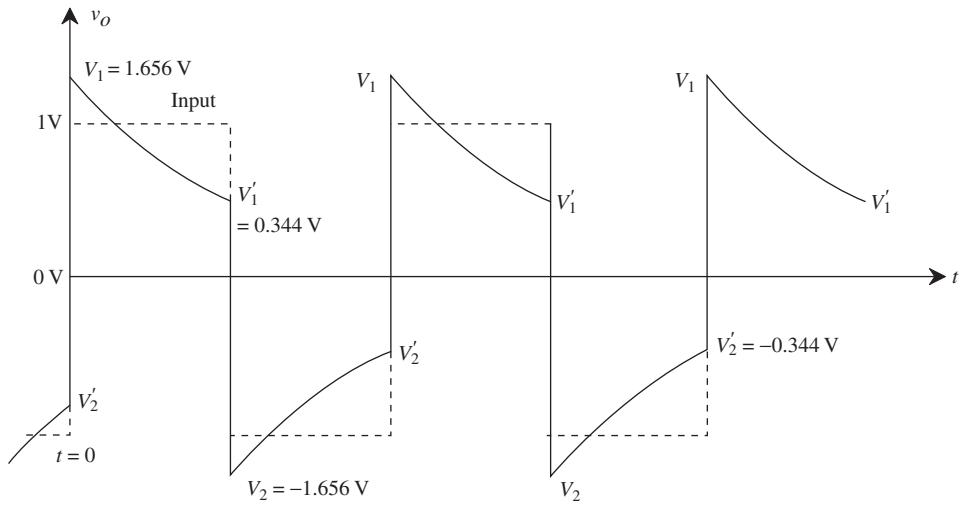


FIGURE 2.14(b) Output of the high-pass circuit for the given input

E X A M P L E

Example 2.5: An unsymmetric square wave has a peak-to-peak amplitude of 2 V and is referenced to the zero level. The duration of the positive section is 0.2 s, and of the negative section is 0.4 s. If this waveform is applied as input to the high-pass circuit shown in Fig. 2.2(a) whose time constant is 0.4 s, what are the steady-state maximum and minimum values of the output waveform? Prove that the area under the positive section is equal to the area under the negative section of the output waveform.

Solution: Given $T_1 = 0.2$ s, $T_2 = \tau = 0.4$ s

The steady-state output waveform is drawn by calculating V_1 , V_1' , V_2 and V_2' .

At

$$t = 0^-, \quad v_o = V_2' \quad \text{and at } t = 0^+, \quad v_o = V_1$$

For $0 < t < T_1$, $v_o = V_1 e^{-t/\tau}$

$$\text{At } t = T_1, \quad v_o = V_1' = V_1 e^{-T_1/\tau} = V_1 e^{-0.2/0.4} = 0.606 V_1$$

For $T_1 < t < (T_1 + T_2)$, $v_o = V_2 e^{-T_2/\tau}$

$$\text{At } t = T_2, \quad v_o = V_2' = V_2 e^{-T_2/\tau} = V_2 e^{-0.4/0.4} = 0.367 V_2$$

The peak-to-peak input is 2 V.

$$\begin{aligned} V_1' - V_2 &= 2 & 0.606 V_1 - V_2 &= 2 \\ V_1 - V_2' &= 2 & V_1 - 0.367 V_2 &= 2 \end{aligned}$$

Solving the above equations, $V_1 = 1.628$ V and $V_2 = -1.016$ V.

$$V_1' = 0.606 \times 1.628 = 0.986 \text{ V} \quad \text{and} \quad V_2' = -0.367 \times 1.106 = -0.372 \text{ V}.$$

The area under positive swing of output:

$$A_1 = \int_0^{T_1} V_1 e^{-t/\tau} dt = V_1 \tau (1 - e^{-T_1/\tau}) = 1.628 \times 0.4 (1 - e^{-0.2/0.4}) = 0.256 \text{ V-s}$$

The area under the negative swing of output is:

$$A_2 = \int_{T_1}^{T_2} |V_2| e^{-(t-T_1)/\tau} dt = |V_2| \tau (1 - e^{-T_2/\tau}) = 1.016 \times 0.4 (1 - e^{-0.4/0.4}) = 0.256 \text{ V-s}$$

Thus, $A_1 = A_2$. The output waveform is shown in Fig. 2.15.

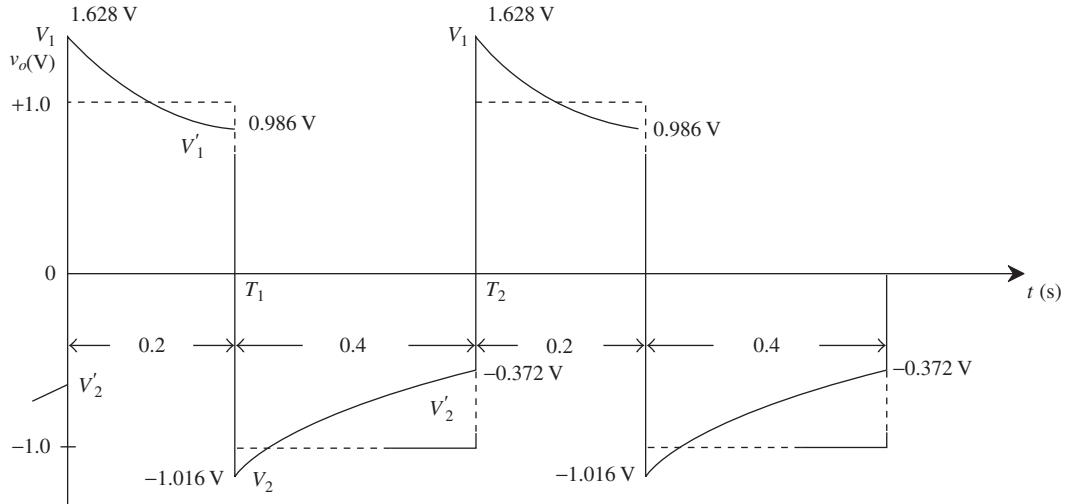


FIGURE 2.15 The output of the high-pass circuit for the specified input

2.2.5 Response of the High-pass RC Circuit to Exponential Input

When a pulse is applied as input to an amplifier, it may while appearing at the actual input terminals of the amplifier, have a finite rise time. The result is that the input to the amplifier is no longer a pulse with sharp rising edge, but an exponential. We would now like to know the response of the high-pass circuit to this exponential input. If the input to the high-pass circuit in Fig. 2.2(a) is an exponential of the form:

$$v_i = V(1 - e^{-t/\tau_1}), \quad (2.47)$$

where, τ_1 is the time constant of the circuit that has generated the exponential signal as shown in Fig. 2.16(a).

From Eq. (2.30), we know:

$$\frac{dv_i}{dt} = \frac{v_o}{\tau} + \frac{dv_o}{dt}$$

As $v_i = V(1 - e^{-t/\tau_1})$,

$$\frac{dv_i}{dt} = \frac{V}{\tau_1} e^{-t/\tau_1} \quad (2.48)$$

Substituting Eq. (2.48) in Eq. (2.30):

$$\frac{V}{\tau_1} e^{-t/\tau_1} = \frac{v_o}{\tau} + \frac{dv_o}{dt} \quad (2.49)$$

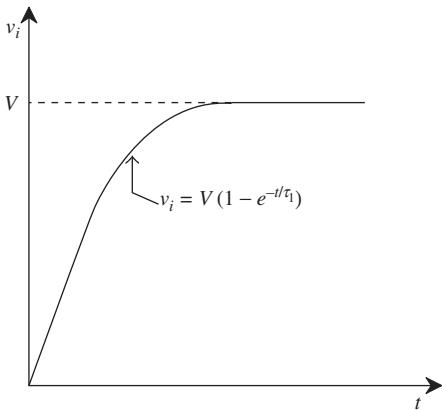


FIGURE 2.16(a) Exponential input

Taking Laplace transforms:

$$\frac{V}{\tau_1} \frac{1}{\left(s + \frac{1}{\tau_1}\right)} = \frac{v_o(s)}{\tau} + sv_o(s)$$

where, τ is the time constant of the high-pass circuit.

$$\frac{V}{\tau_1} \frac{1}{\left(s + \frac{1}{\tau_1}\right)} = v_o(s) \left(s + \frac{1}{\tau}\right)$$

Therefore,

$$v_o(s) = \frac{\frac{V}{\tau_1}}{\left(s + \frac{1}{\tau_1}\right) \left(s + \frac{1}{\tau}\right)} \quad (2.50)$$

Case 1: $\tau \neq \tau_1$

Applying partial fractions, Eq. (2.50) can be written as:

$$v_o(s) = \frac{A}{\left(s + \frac{1}{\tau_1}\right)} + \frac{B}{\left(s + \frac{1}{\tau}\right)} = \frac{\frac{V}{\tau_1}}{\left(s + \frac{1}{\tau_1}\right) \left(s + \frac{1}{\tau}\right)} \quad (2.51)$$

Therefore,

$$\frac{V}{\tau_1} = A \left(s + \frac{1}{\tau}\right) + B \left(s + \frac{1}{\tau_1}\right) \quad (2.52)$$

Put $s = -1/\tau_1$ in Eq. (2.52).

$$\frac{V}{\tau_1} = A \left(\frac{-1}{\tau_1} + \frac{1}{\tau}\right) \quad \text{or} \quad A = \frac{\frac{V}{\tau_1}}{\left(\frac{1}{\tau} - \frac{1}{\tau_1}\right)} = \frac{V}{\left(\frac{\tau_1}{\tau} - 1\right)}$$

Now put $s = -1/\tau$ in Eq. (2.52). Then:

$$\frac{V}{\tau_1} = B \left(\frac{1}{\tau_1} - \frac{1}{\tau}\right)$$

Therefore,

$$B = \frac{-V}{\left(\frac{\tau_1}{\tau} - 1\right)} \quad (2.53)$$

Substituting the values of A and B in Eq. (2.51):

$$v_o(s) = \frac{V}{\left(\frac{\tau_1}{\tau} - 1\right) \left(s + \frac{1}{\tau_1}\right)} - \frac{V}{\left(\frac{\tau_1}{\tau} - 1\right) \left(s + \frac{1}{\tau}\right)} = \frac{V}{\left(\frac{\tau_1}{\tau} - 1\right)} \left[\frac{1}{\left(s + \frac{1}{\tau_1}\right)} - \frac{1}{\left(s + \frac{1}{\tau}\right)} \right]$$

Taking inverse Laplace transform:

$$v_o(t) = \frac{V}{\left(\frac{\tau_1}{\tau} - 1\right)} (e^{-t/\tau_1} - e^{-t/\tau}) \quad (2.54)$$

This is the expression for the output voltage where $\tau \neq \tau_1$.

Let $t/\tau_1 = x$ and $\tau/\tau_1 = n$. For $n \neq 1$, i.e., $\tau \neq \tau_1$, we have from Eq. (2.54):

$$v_o(t) = \frac{V}{\left(\frac{1}{n} - 1\right)} (e^{-x} - e^{-x/n}) \quad \text{since } \frac{t}{\tau_1} \times \frac{\tau_1}{\tau} = \frac{x}{n} = \frac{t}{\tau}$$

Therefore,

$$v_o(t) = \frac{Vn}{(1-n)} (e^{-x} - e^{-x/n}) = \frac{Vn}{(n-1)} (e^{-x/n} - e^{-x}) \quad (2.55)$$

If $\tau \gg \tau_1$, the second term in the Eq. (2.55) is small when compared to the first. Thus,

$$v_o(t) \cong \frac{Vn}{(n-1)} e^{-x/n} = \frac{Vn}{(n-1)} e^{-t/\tau} \quad (2.56)$$

Case 2 : $\tau = \tau_1$, that is, $n = 1$.

$$v_o(s) = \frac{\frac{V}{\tau}}{\left(s + \frac{1}{\tau}\right)\left(s + \frac{1}{\tau}\right)} = \frac{\frac{V}{\tau}}{\left(s + \frac{1}{\tau}\right)^2}$$

Taking Laplace inverse:

$$v_o(t) = \frac{V}{\tau} t e^{-t/\tau} \quad (2.57)$$

As $t/\tau = x = t/\tau_1$ and $\tau/\tau_1 = n = 1$:

$$v_o(t) = V x e^{-x} \quad (2.58)$$

The response of the circuit is plotted for different values of n in Fig. 2.16(b).

From the response in Fig. 2.16(b), it is seen that near the origin the output follows the input. Also, the smaller the value of n ($= \tau/\tau_1$ is small), the smaller is the output peak and the shorter is the duration of the pulse. As n increases, the peak becomes larger and the duration of the pulse becomes longer. Hence, the choice of n is based on the amplitude and duration of the pulse required for a specific application. The maximum output occurs when $(dv_o/dt) = 0$. From Eq. (2.55):

$$\frac{d}{dt} \left[V \frac{n}{n-1} (e^{-x/n} - e^{-x}) \right] = 0$$

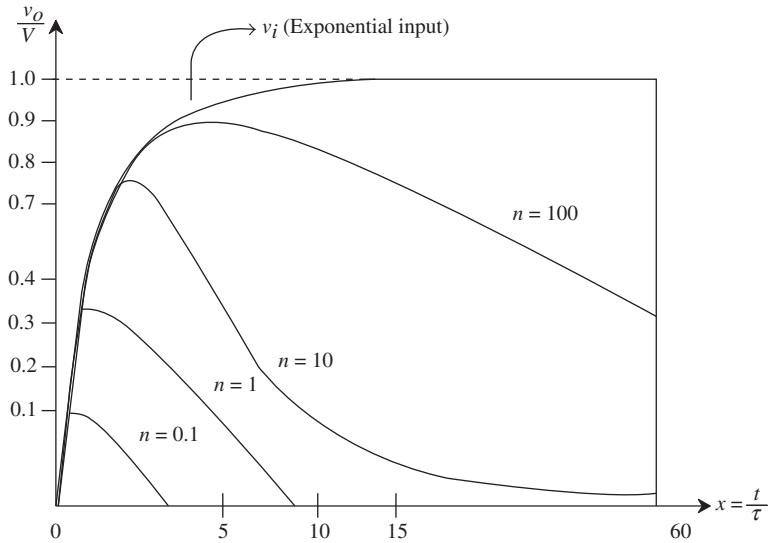


FIGURE 2.16(b) The response of a high-pass circuit to an exponential input

$$V \frac{n}{n-1} \left[\left(\frac{-1}{n} \right) \left(\frac{1}{\tau} \right) e^{-x/n} - e^{-x} \left(\frac{-1}{\tau} \right) \right] = 0$$

$$V \frac{n}{n-1} \left[\left(\frac{e^{-x}}{\tau} - \frac{e^{-x/n}}{n\tau} \right) \right] = 0 \quad e^{-x} = \frac{e^{-x/n}}{n}$$

$$n = e^{x \left(1 - \frac{1}{n} \right)} = e^{\left(\frac{x(n-1)}{n} \right)}$$

$$\ln n = \frac{x(n-1)}{n}$$

$$x = \frac{n}{n-1} \ln n \quad (2.59)$$

Since $x = t/\tau$, from Eq. (2.59), the time taken to rise to the peak t_p is given by:

$$t_p = \tau \frac{n}{n-1} \ln n$$

From Eq. (2.59):

$$-x = \frac{-n}{n-1} \ln n = \ln \left[n^{n/(1-n)} \right] \quad (2.60)$$

To obtain the maximum value of the output, substitute this value of $-x$ from Eq. (2.60) in the expression for $v_o(t)$ in Eq. (2.55).

$$\begin{aligned}
v_o(\max) &= \frac{Vn}{n-1} \exp \left[\frac{1}{n} \ln n^{[n/(1-n)]} - \ln n^{[n/(1-n)]} \right] \\
&= V \frac{n}{n-1} \exp \left[\ln n^{[1/(1-n)]} - \ln n^{[n/(1-n)]} \right] \\
&= V \frac{n}{n-1} \left[n^{[1/(1-n)]} - n^{[n/(1-n)]} \right] = \frac{V}{n-1} \left[n^{1+[1/(1-n)]} - n^{1+[n/(1-n)]} \right] \\
&= \frac{V}{n-1} \left[n^{(2-n)/(1-n)} - n^{1/(1-n)} \right] = \frac{V}{n-1} \left[(n-1)^{1/(1-n)} \right] = V n^{1/(1-n)} \quad \text{for } n \neq 1 \\
\frac{v_o(\max)}{V} &= n^{1/(1-n)} \quad \text{for } n \neq 1
\end{aligned} \tag{2.61}$$

From the waveforms in Fig. 2.16(b) and the subsequent mathematical relations derived, it is seen that, if an exponential signal is applied as an input to a high-pass circuit, the output is a pulse whose duration depends on $n (= \tau/\tau_1)$, where τ_1 is the time constant of the previous circuit that has generated the exponential signal and τ is the time constant of the high-pass circuit under consideration. The smaller the value of n , the smaller the duration of this output pulse and also the smaller its amplitude. As n increases, the duration as well as the amplitude of this output pulse increases. Hence, depending on our requirement, we adjust the value of n .

Example 2.6 elucidates the procedure to calculate the output when an exponential input is applied to the high-pass circuit in Fig. 2.1(a).

EXAMPLE

Example 2.6: An exponential input of $10 \left(1 - e^{-t/10 \times 10^{-3}} \right)$ is applied to a high-pass RC circuit. Plot the response when (i) $RC = 10$ ms and (ii) $RC = 20$ ms.

Solution:

(i) $\tau = 10$ ms and τ_1 as specified is $\tau = \tau_1 = 10$ ms

We know that when $\tau = \tau_1$:

$$v_o = \frac{V}{\tau} t e^{-t/\tau} = \frac{10}{10 \times 10^{-3}} t e^{-t/10 \times 10^{-3}} = 1000 t e^{-t/10 \times 10^{-3}}$$

The output is calculated for t ranging from 0 to 50 ms and is shown in Table 2.3.

(ii) When $\tau_1 \neq \tau$, the output voltage is calculated and is shown in Table 2.4. $\tau = 20$ ms and $\tau_1 = 10$ ms

$$v_o = \frac{V}{\left[\frac{\tau_1}{\tau} - 1 \right]} \left(e^{-t/\tau_1} - e^{-t/\tau} \right) = \frac{10}{\left(\frac{10 \times 10^{-3}}{20 \times 10^{-3}} \right) - 1} \left(e^{-t/10 \times 10^{-3}} - e^{-t/20 \times 10^{-3}} \right)$$

TABLE 2.3 The output of the high-pass circuit for the given exponential input when $\tau = \tau_1$

t (in ms)	$v_o = 1000 \times t \times e^{t/10 \times 10^{-3}}$ (Volts)
0	0
1	0.904
2	1.637
3	2.22
4	2.68
5	3.03
6	3.29
7	3.476
8	3.59
9	3.66
10	3.678
15	3.346
20	2.7
50	0.336

TABLE 2.4 The output of the high-pass circuit when $\tau_1 \neq \tau$

Time (t) ms	$v_o = \frac{10}{\left(\frac{10 \times 10^{-3}}{20 \times 10^{-3}} - 1\right)} \left(e^{-t/10 \times 10^{-3}} - e^{-t/20 \times 10^{-3}} \right)$ (Volts)
0	0
1	0.92
2	1.722
3	2.414
4	2.9746
5	3.456
6	3.856
7	4.173
8	4.426
9	4.632
10	4.79
15	4.987
20	4.65
25	4.09
50	1.5

The input and the output waveforms are as shown in Fig. 2.17.

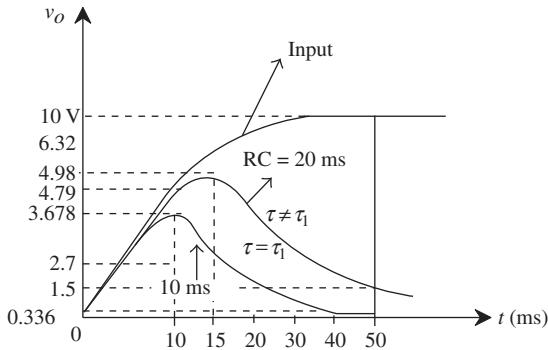


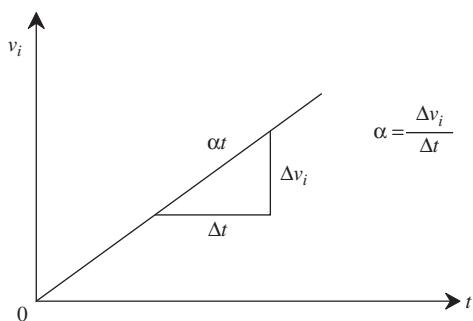
FIGURE 2.17 The input to and the output of the high-pass circuit

2.2.6 Response of the High-pass RC Circuit to Ramp Input

Ramp is a waveform in which the voltage increases linearly with time, for $t > 0$, and is zero for $t < 0$. It is used to move the spot in a CRO linearly with time along the x -axis. This type of waveform is generated by sweep circuits which we shall study later. However, if a ramp is applied as an input to a high-pass circuit, there could be deviation from linearity in the output. We can calculate and plot the output for different values of τ to understand how it influences the output. Let the input to the high-pass circuit be $v_i = \alpha t$ where, α is the slope, as shown in Fig. 2.18(a).

For the high-pass circuit, we have:

$$\begin{aligned} v_i &= \frac{1}{\tau} \int v_o dt + v_o \\ \alpha t &= \frac{1}{\tau} \int v_o dt + v_o \end{aligned} \quad (2.62)$$



Taking Laplace transforms:

$$\frac{\alpha}{s^2} = \frac{1}{s\tau} v_o(s) + v_o(s) = v_o(s) \left(1 + \frac{1}{s\tau} \right)$$

Multiplying throughout by s :

$$\frac{\alpha}{s} = v_o(s) \left(s + \frac{1}{\tau} \right) \quad (2.63)$$

Therefore,

$$v_o(s) = \frac{\alpha}{s \left(s + \frac{1}{\tau} \right)} = \frac{A}{s} + \frac{B}{\left(s + \frac{1}{\tau} \right)}$$

FIGURE 2.18(a) Ramp input

From which, $A = \alpha\tau$ and $B = -\alpha\tau$

$$v_o(s) = \frac{\alpha\tau}{s} - \frac{\alpha\tau}{\left(s + \frac{1}{\tau}\right)} = \alpha\tau \left[\frac{1}{s} - \frac{1}{\left(s + \frac{1}{\tau}\right)} \right]$$

Taking Laplace inverse:

$$v_o(t) = \alpha\tau \left(1 - e^{-t/\tau} \right) \quad (2.64)$$

If $t/\tau \ll 1$:

$$e^{-t/\tau} = 1 - \frac{t}{\tau} + \frac{t^2}{2\tau^2}$$

$$\text{Therefore, } v_o(t) = \alpha\tau \left(1 - 1 + \frac{t}{\tau} - \frac{t^2}{2\tau^2} \right)$$

$$v_o(t) = \alpha t \left(1 - \frac{t}{2\tau} \right) \quad (2.65)$$

The output falls away from the input, as shown in Fig. 2.18(b). From the waveforms in Fig. 2.18(b), we see that for the output to be the same as the input, $\tau \gg T$ (the duration of the ramp). As the value of τ decreases, not only the amplitude of the output decreases but also the signal now is an exponential. The output falls away from the input. So, the choice of τ is dictated by the specific application. Transition error defines deviation from linearity and is given by:

$$e_t = \frac{v_i - v_o}{v_i} \quad (2.66)$$

At $t = T$, $v_i = \alpha T$ and $v_o = \alpha T [1 - (T/2\tau)]$. Therefore,

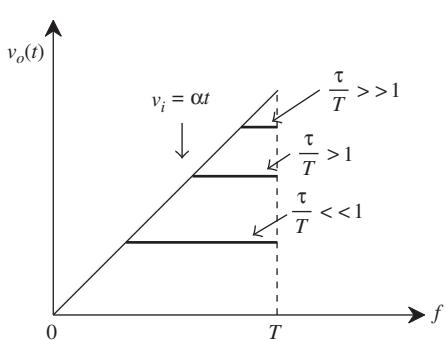


FIGURE 2.18(b) The response of a high-pass circuit to ramp input

$$e_t = \frac{\alpha T - \alpha T \left(1 - \frac{T}{2\tau} \right)}{\alpha T} = \frac{\frac{\alpha T^2}{2\tau}}{\alpha T} = \frac{T}{2\tau} \quad (2.67)$$

Thus,

$$e_t = \frac{T}{2\tau} = \pi f_1 T \quad \text{as } \frac{1}{2\tau} = \pi f_1 \quad (2.68)$$

The transmission error, e_t describes how faithfully the signal is transmitted to the output. As the input is a ramp and if the output falls away from the input, e_t specifies the deviation from linearity. Let us try to plot the output by considering an example.

EXAMPLE

Example 2.7: A ramp is applied to an RC differentiator, [see Fig. 2.1(a)]. Draw to scale the output waveform for the following cases: (i) $T = RC$, (ii) $T = 0.5RC$, (iii) $T = 10RC$.

Solution:

From Eq. (2.64):

$$v_o = \alpha \tau \left(1 - e^{-t/\tau}\right) \quad v_o = V \left(\frac{\tau}{T}\right) \left(1 - e^{-t/\tau}\right) \quad \text{as} \quad \alpha = \frac{V}{T}$$

The peak of the output will occur at $t = T$.

$$v_o(\text{peak}) = V \left(\frac{\tau}{T}\right) \left(1 - e^{-T/\tau}\right)$$

(i) When $T = \tau$, $(\tau/T) = 1$ and $(T/\tau) = 1$

$$v_o(\text{peak}) = V(1) \left(1 - e^{-1}\right) = 0.632 \text{ V}$$

(ii) When $T = 0.5\tau$

$$\left(\frac{T}{\tau}\right) = 0.5 \quad \text{and} \quad \left(\frac{\tau}{T}\right) = 2$$

$$v_o(\text{peak}) = V(2) \left(1 - e^{-0.5}\right) = 0.788 \text{ V}$$

(iii) When $T = 10\tau$

$$\left(\frac{T}{\tau}\right) = 10 \quad \left(\frac{\tau}{T}\right) = 0.1$$

$$v_o(\text{peak}) = V(0.1) \left(1 - e^{-10}\right) = V(0.1) \left(1 - 0.000045\right) = 0.1 \text{ V}$$

The response is plotted in Fig. 2.19.

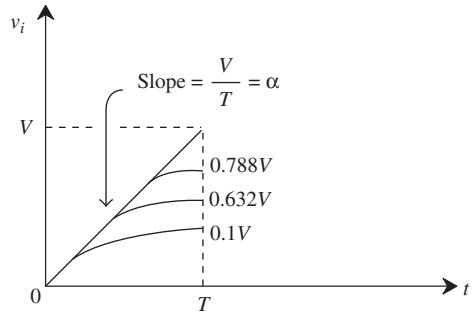


FIGURE 2.19 The response of the high-pass circuit to ramp input

2.3 DIFFERENTIATORS

Sometimes, a square wave may need to be converted into sharp positive and negative spikes (pulses of short duration). By eliminating the positive spikes, we can generate a train of negative spikes and vice-versa. The pulses so generated may be used to trigger a multivibrator. In such cases, a differentiator is used. If in a circuit, the output is a differential of the input signal, then the circuit is called a differentiator.

2.3.1 A High-pass RC Circuit as a Differentiator

If the time constant of the high-pass RC circuit, shown in Fig. 2.1(a), is much smaller than the time period of the input signal, then the circuit behaves as a differentiator. If T is to be large when compared to τ , then the frequency must be small. At low frequencies, X_C is very large when compared to R . Therefore, the voltage drop across R is very small when compared to the drop across C .

$$v_i = \frac{1}{C} \int idt + iR$$

But $iR = v_o$ is small. Therefore,

$$v_i = \frac{1}{C} \int idt \quad \text{or} \quad v_i = \frac{1}{\tau} \int v_o dt \quad (\text{since } i = V_o/R)$$

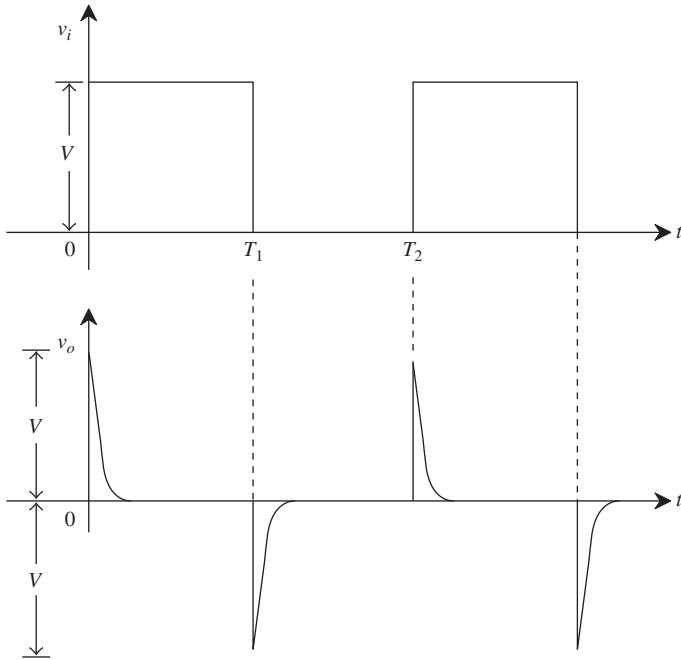


FIGURE 2.20 The output of a differentiator

Differentiating:

$$\begin{aligned} \frac{dv_i}{dt} &= \frac{v_o}{\tau} \\ v_o &= \tau \frac{dv_i}{dt} \end{aligned} \quad (2.69)$$

Therefore,

$$v_o \propto \frac{dv_i}{dt} \quad (2.70)$$

Thus, from Eq. (2.70), it can be seen that the output is proportional to the differential of the input signal, as shown in Fig. 2.20. If the input $v_i(t) = V_m \sin \omega t$:

$$v_o(t) \approx RC \left[\frac{d}{dt} (V_m \sin \omega t) \right]$$

$$v_o(t) \approx V_m \frac{\omega}{\omega_1} \cos \omega t \quad \text{where } \omega_1 = \frac{1}{RC}$$

We have from Eq. (2.3):

$$\left| \frac{v_o}{v_i} \right| = \frac{1}{\sqrt{1 + \left(\frac{\omega_1}{\omega} \right)^2}} \quad \text{and} \quad \theta = \tan^{-1}(\omega_1/\omega)$$

When $\theta = 90^\circ$, the sine function at the input becomes a cosine function at the output, as is required in a differentiator. When $\omega_1/\omega = 100$, $\theta = 89.4^\circ$ which is nearly equal to 90° . Hence, a high-pass circuit behaves as a good differentiator only when $RC \ll T$, and the output is a co-sinusiodally varying signal if the input is

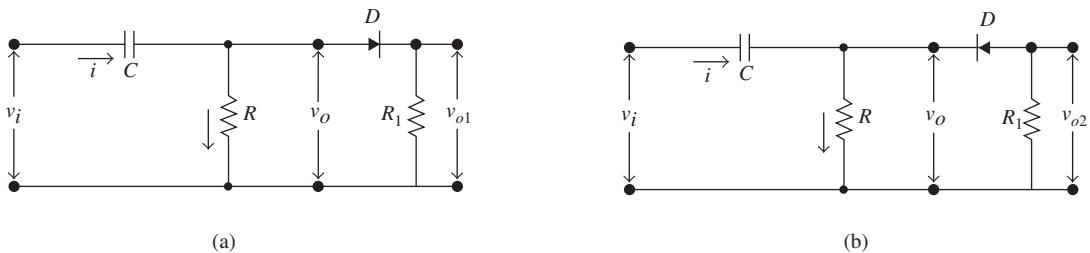


FIGURE 2.21(a) The differentiator circuit when : negative spikes are eliminated in the output; and (b) positive spikes are eliminated in the output

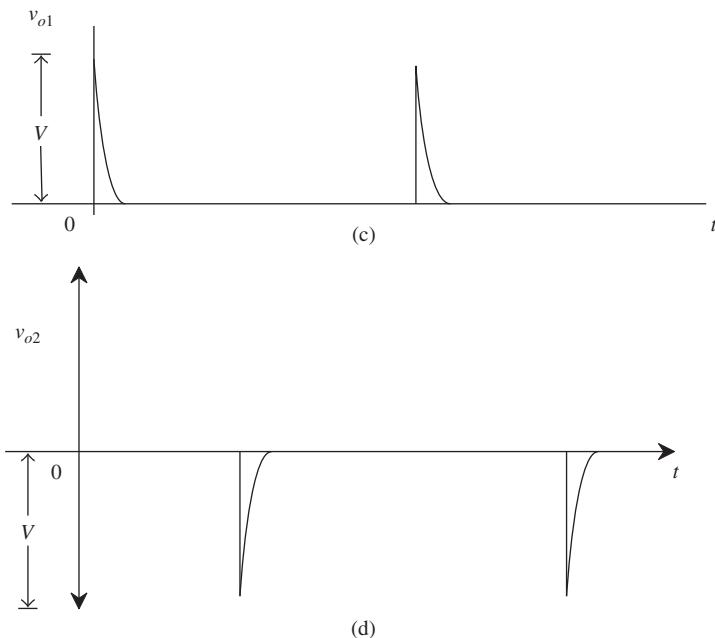


FIGURE 2.21(c) The output of a differentiator showing: positive spikes only; and (d) negative spikes only

a sine wave. If the input is a square wave, the output is in the form of positive and negative spikes, as shown in Fig. 2.20.

The output of the differentiator in Fig. 2.20 contains both positive and negative spikes. If only positive spikes are needed to trigger a multivibrator (to be considered later), we use the circuit shown in Fig. 2.21(a). Here, since D conducts only when the input spikes are positive, the negative spikes are eliminated. Alternately, if only negative spikes are needed, the positive spikes are eliminated using the circuit in Fig. 2.21(b), since D conducts only when the input spikes are negative. The output of the circuit in Fig. 2.21(a) is shown in Fig. 2.21(c). Similarly, the output of the circuit in Fig. 2.21(b) is shown in Fig. 2.21(d).

2.3.2 An Op-amp as a Differentiator

An operational amplifier, commonly known as an op-amp, can be used as a differentiator, as shown in Fig. 2.22(a).

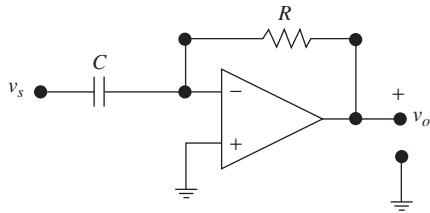


FIGURE 2.22(a) Op-amp as a differentiator

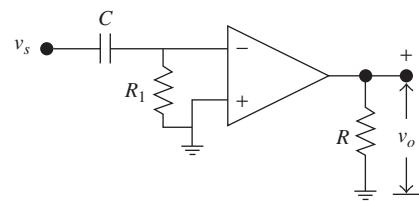


FIGURE 2.22(b) The op-amp differentiator circuit resulting from the use of Miller's theorem

From Miller's theorem:

$$Z_1 = \frac{Z'}{1 - A} \quad \text{and} \quad Z_2 = \frac{Z' A}{A - 1}$$

where A is the gain of the amplifier. The resistance, R , appears between the input and output terminals of the op-amp. Using Miller's theorem, R can be replaced by R_1 and R_2 as $R_1 = R/(1 - A)$ is small since A is large; and $R_2 = RA/(A - 1) = R$ since A is large. Hence, the op-amp circuit can be redrawn as shown in Fig. 2.22(b).

For a good differentiator, $\tau (= R_1 C)$ should be small. As R_1 is a very small value of resistor (since A is large), an op-amp differentiator behaves as a better differentiator when compared to a simple RC differentiator, without physically reducing the value of R .

2.3.3 Double Differentiators

The circuit in Fig. 2.23 is called a double differentiator as we have two high-pass differentiating circuits. In the figure, A is the gain of the inverting amplifier. Here, $R_1 C_1 = \tau_1$ and $R_2 C_2 = \tau_2$ are small when compared to the time period of the input signal.

Let the input to the circuit be a ramp, i.e., $v_i = \alpha t$. From Eq. (2.64), the output of the first high-pass $R_1 C_1$ circuit for the ramp input is:

$$v_1 = \alpha \tau_1 (1 - e^{-t/\tau_1}) \quad (2.71)$$

Therefore, the output voltage of the amplifier v is written as:

$$v = -A \alpha \tau_1 (1 - e^{-t/\tau_1}) \quad (2.72)$$

where, A is the amplifier gain. It can be seen from Eq. (2.72) that v has phase inversion. The output of the first high-pass circuit, which is an exponential, is the input to the second differentiator. We know from Eq. (2.55) that the output of this second differentiator is a pulse.

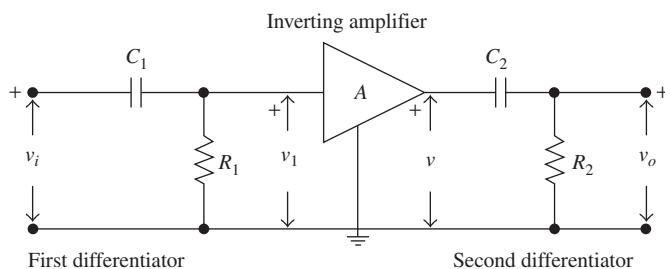


FIGURE 2.23 A double differentiator

$$v_o = -A\alpha\tau_1 \frac{n}{n-1} (e^{-x/n} - e^{-x})$$

where $n = \tau_2/\tau_1$ and $x = t/\tau_1$. So,

$$v_o = A\alpha\tau_1 \frac{n}{n-1} (e^{-x} - e^{-x/n}) \quad (2.73)$$

Therefore,

$$v_o = v \frac{n}{n-1} (e^{-x} - e^{-x/n}) \quad (2.74)$$

For $n = 1$

$$v_o = vx e^{-x} = A\alpha\tau (t/\tau) e^{-t/\tau} = A\alpha t e^{-t/\tau} \quad (2.75)$$

The ramp voltage which is input to the double differentiator is converted to a pulse. The response is plotted in Fig. 2.24. From Eq. (2.75), the output for $\tau = \tau_1 = \tau_2$ is given as:

$$v_o = A\alpha t e^{-t/\tau} \quad (2.76)$$

From Eq. (2.72) the output of the amplifier v is given as:

$$v = -A\alpha\tau_1 (1 - e^{-t/\tau_1})$$

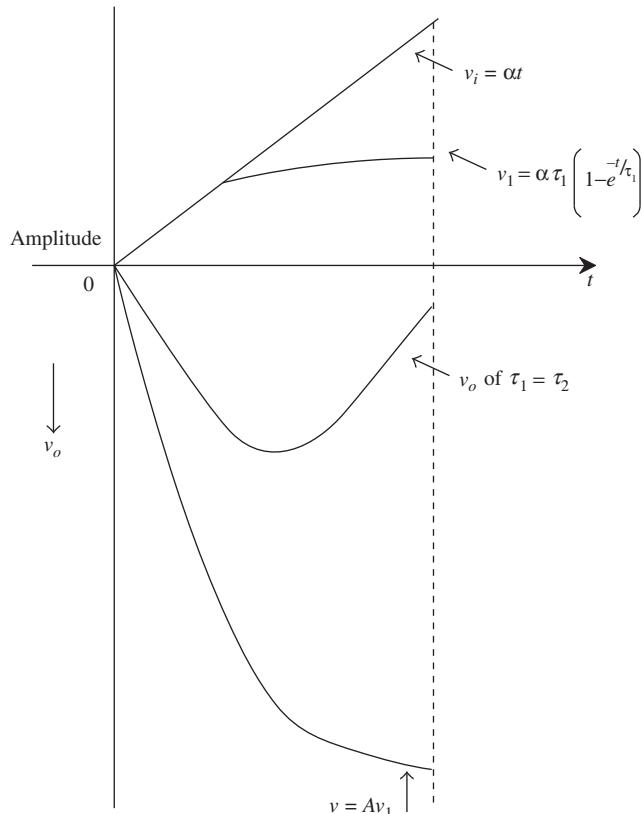


FIGURE 2.24 The response of a double differentiator to a ramp input

The initial slope of this output is:

$$\frac{dv}{dt} \Big|_{t=0} = A\alpha \quad (2.77)$$

From Eq. (2.71), we have:

$$v_1 = \alpha\tau (1 - e^{-t/\tau})$$

The initial slope of the output of the first differentiator (input to the amplifier) is:

$$\frac{dv_1}{dt} \Big|_{t=0} = \alpha \quad (2.78)$$

We see from Eqs. (2.77) and (2.78), the initial slope of the input to the amplifier v_1 is α , whereas the initial slope of the amplifier output v is $A\alpha$. The output rises much faster than the input, as shown in Fig. 2.24. Hence, the amplifier is called a rate-of-rise amplifier. At this point, it is relevant to talk about a comparator. A circuit that compares the input with a reference and tells us the instant at which the input has reached the reference level is called a comparator. One such simple and practical comparator is a diode comparator. Sometimes a circuit needs to be activated the moment the input reaches a predetermined level. The diode comparator will not be able to do this job. Thus, the output of the diode comparator is given as the input to the double differentiator. As the output of the double differentiator is a pulse whose amplitude and duration can be controlled, this output can activate the desired circuit. We discuss this aspect in greater details in later chapters.

2.4 THE RESPONSE OF A HIGH-PASS RL CIRCUIT TO STEP INPUT

A high-pass RL circuit is represented in Fig. 2.2(b). If a step of magnitude V is applied, let us find the response. Writing the KVL equation:

$$v_i = iR + L \frac{di}{dt} \quad (2.79)$$

$$v_o = L \frac{di}{dt} \quad (2.80)$$

Therefore, from Eq. (2.80)

$$\frac{di}{dt} = \frac{v_o}{L} \quad di = \frac{1}{L} v_o dt \quad i = \frac{1}{L} \int v_o dt$$

As $v_i = V$, Eq. (2.79) can also be written as:

$$V = \frac{R}{L} \int v_o dt + v_o$$

Applying Laplace transforms:

$$\begin{aligned} \frac{V}{s} &= \left(\frac{1}{s\tau} + 1 \right) v_o(s) \quad \text{where } \tau = \frac{L}{R} \\ V &= \left(s + \frac{1}{\tau} \right) v_o(s) \quad v_o(s) = \frac{V}{\left(s + \frac{1}{\tau} \right)} \end{aligned}$$

Taking Laplace inverse:

$$v_o(t) = V e^{-t/\tau} \quad (2.81)$$

Similarly, the response of this circuit is evaluated for other inputs. This high-pass circuit is used as a differentiator if $L/R \ll T$. Since $v_o = L di/dt$, and $i \approx v_i/R$:

$$v_o = \frac{L}{R} \frac{dv_i}{dt} \quad (2.82)$$

S O L V E D P R O B L E M S

Example 2.8: The output of a step generator has an amplitude of 10 V and rise-time of 1.1 ns. When this is applied as an input to a high-pass circuit with $R = 100 \Omega$ [see Fig 2.25(a)], there appears across R a pulse of amplitude 1 V. Find the value of the capacitance.

Solution:

The response of the circuit in Fig. 2.25(a) is shown in Fig. 2.25(b).

Rise time of step input $t_r = 2.2 \tau_1 = 1.1$ ns

Therefore, the time constant of the exponential input:

$$\tau_1 = \frac{1.1}{2.2} = 0.5 \text{ ns}$$

The maximum value of the output is:

$$v_o(\max) = v_i n^{1/(1-n)} = 1 \text{ V}$$

$$10n^{1/(1-n)} = 1 \quad \text{or}$$

$$n = 0.14$$

$$n = \frac{\tau}{\tau_1} = 0.14$$

$$\tau = n\tau_1 = 0.14 \times 0.5 \text{ ns} = 0.07 \text{ ns}$$

$$\tau = RC = 0.07 \times 10^{-9} \text{ s}$$

Therefore,

$$C = \frac{0.07 \times 10^{-9}}{100} = 0.7 \text{ pF}$$

Example 2.9: A limited ramp from a generator rises linearly to V_s in a time period $T_s = 0.1 \mu\text{s}$ and remains constant for $2 \mu\text{s}$. This signal is applied to a differentiating circuit whose time constant is $0.01 \mu\text{s}$. The resultant pulse at the output of the differentiator has a maximum value of 15 V. What is the peak amplitude of the ramp at the output of the generator?

Solution:

$$RC = \tau = 0.01 \mu\text{s} = 0.01 \times 10^{-6} \text{ s}$$

$$v_o(\max) = 15 \text{ V}$$

$$v_o(t) = \alpha \tau \left(1 - e^{-T_s/\tau} \right)$$

$$\alpha \tau = v_o(\max) = 15 \text{ V}$$

$$\alpha = \frac{15}{\tau} = \frac{15}{0.01 \times 10^{-6}} \text{ V/s}$$

$$T_s = 0.1 \mu\text{s}$$

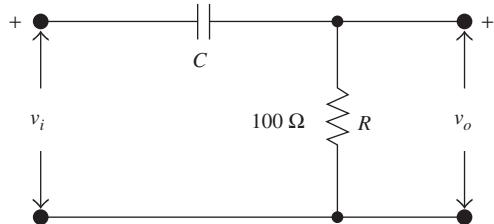


FIGURE 2.25(a) The given coupling circuit

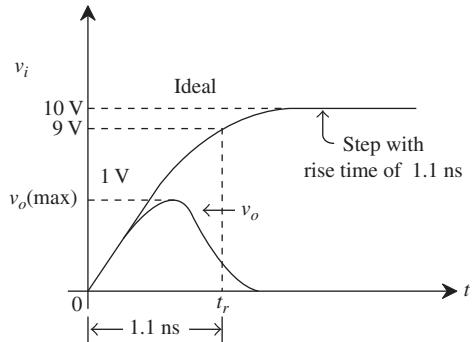


FIGURE 2.25(b) The response of the circuit

The peak value of the ramp from the generator is:

$$V_s = \alpha T_s = \frac{15}{0.01 \times 10^{-6}} \times 0.1 \times 10^{-6} = 150 \text{ V}$$

The input and output are plotted in Fig. 2.26.

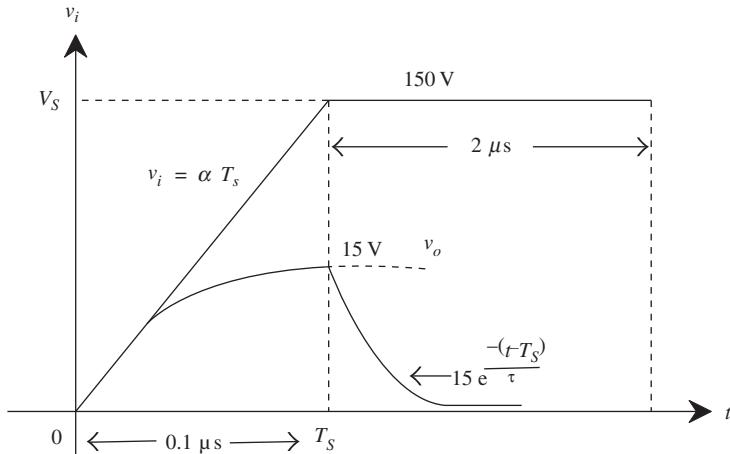


FIGURE 2.26 The input and the output for the specified conditions

Example 2.10: The input to a high-pass RC circuit in Fig. 2.2(a) is periodic and trapezoidal as indicated in Fig. 2.27(a). Given that $T_1 = 1 \text{ ms}$ and $T_2 = 1.5 \text{ ms}$ and $\tau = 10 \text{ ms}$, find and sketch the steady-state output.

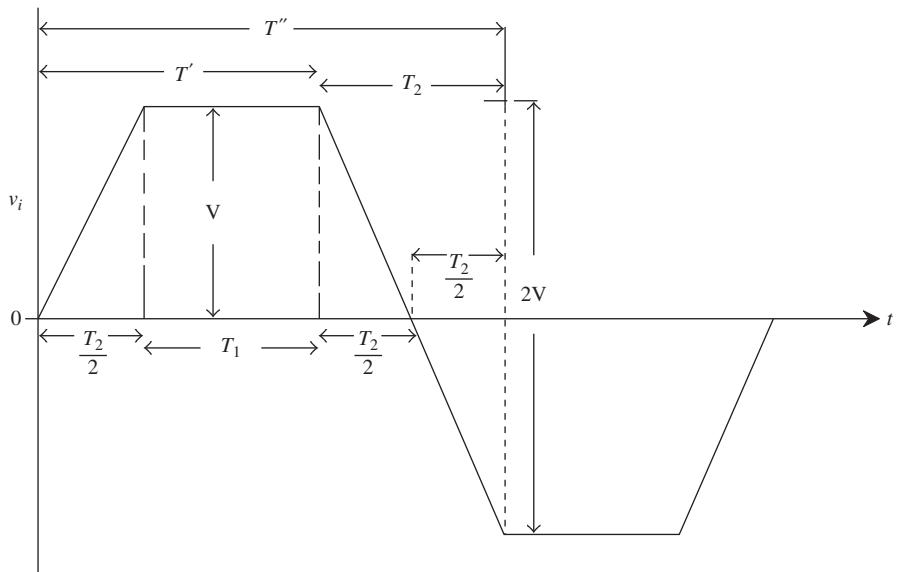


FIGURE 2.27(a) The given input to the high-pass circuit

Solution:

Given that $\tau = 10 \text{ ms}$, $T_1 = 1 \text{ ms}$ and $T_2 = 1.5 \text{ ms}$

As the time constant τ is very large when compared to $T_2/2$, upto $T_2/2$, the output follows the input and at $T_2/2$ let this value be V_1 . As the input is now constant at V , output decays exponentially to V'_1 at $T' (= T_2/2 + T_1)$.

$$V'_1 = V_1 e^{-T_1/\tau} = V_1 e^{-1/10} = V_1 e^{-0.1} = 0.905 V_1 \quad (1)$$

Beyond T' the input is a negative ramp. The output also falls linearly as the input. At T'' let the output be V_2 . Once again as the input remains constant, the output decays to V'_2 .

$$V'_2 = V_2 e^{-T_1/\tau} = V_2 e^{-1/10} = V_2 e^{-0.1} = 0.905 V_2 \quad (2)$$

$$V_2 = V'_1 - \alpha \tau \left(1 - e^{-T_2/\tau} \right)$$

We have $\alpha = 2V/T_2$

$$V_2 = V'_1 - \frac{2}{1.5} (10) \left(1 - e^{-0.15} \right) = V'_1 - \frac{2}{1.5} (10)(0.14) \\ V_2 = V'_1 - 1.87 \quad (3)$$

$$V_1 = V'_2 + \alpha \tau \left(1 - e^{-T_2/\tau} \right) = V'_2 + \frac{2}{1.5} (10) \left(1 - e^{-T_2/10} \right)$$

$$V_1 = V'_2 + 1.87 \quad (4)$$

Solving (3) and (4) using (1) and (2)

$$V_2 = 0.905 V_1 - 1.87 \quad (5)$$

$$V_1 = 0.905 V_2 + 1.87 \quad (6)$$

By solving Eqs. (5) and (6)

$$V_1 = 0.983 \text{ V}, \quad V_2 = -0.983 \text{ V} \quad V'_1 = 0.889 \text{ V}, \quad V'_2 = -0.889 \text{ V}.$$

The output is plotted in Fig. 2.27(b).

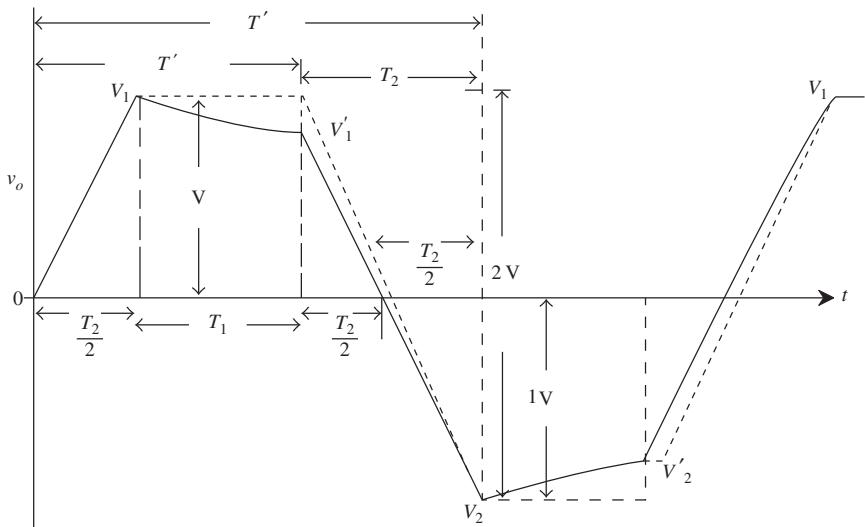


FIGURE 2.27(b) The output of the high-pass circuit to the input in Fig. 2.27(a)

In fact, there is no need for these elaborate calculations since when τ is large, V_1 is approximately equal to 1 V. Similarly V_2 is approximately equal to -1 V. These calculations are necessary only when τ is small.

Example 2.11: Show that the ratio $(v_o/V)_{\max} = 0.368$ if $n = 1$ for an exponential input to the high-pass RC circuit [see Fig. 2.2(a)].

Solution: The output of a high-pass RC circuit for an exponential input when $n = 1$ is given by:

$$v_o = Vxe^{-x}$$

where $x = t/\tau$

$$\therefore \frac{v_o}{V} = xe^{-x}$$

To find the max value of v_o/V differentiate v_o/V with respect to x and equate it to zero.

$$\frac{d}{dx} \left(\frac{v_o}{V} \right) = xe^{-x}(-1) + e^{-x} = 0 \quad \therefore x = 1$$

Therefore,

$$\left(\frac{v_o}{V} \right)_{\max} = 1 \times e^{-1} = 0.368$$

Example 2.12: A 20-V step of 2.2 ns rise time is applied to an inductor L from a generator of 100Ω internal resistance as shown in Fig. 2.28. The pulse across the inductor attains amplitude of 4.4 V. Find the value of inductance, L .

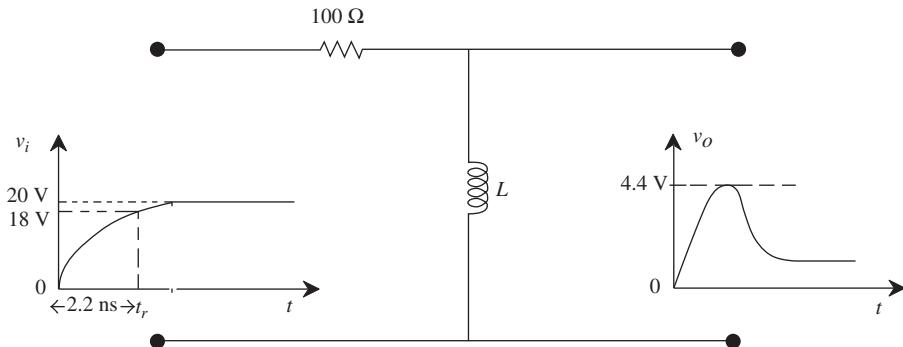


FIGURE 2.28 Circuit with the input and output waveforms

Solution: Output is taken across inductor, hence it is a high-pass circuit.

Rise time of the step input $= 2.2 \times 10^{-9}$ s

$$v_i(\max) = 20 \text{ V} \quad \tau = \frac{L}{R} = \frac{L}{100}$$

Therefore, Rise time of the input, $t_r = 2.2\tau_1$

$$\therefore \tau_1 = \frac{\text{Rise time}}{2.2} = \frac{2.2 \times 10^{-9}}{2.2} = 10^{-9} \text{ s}$$

The max output voltage is = 4.4 V.

The output is also shown in Fig. 2.28.

$$\therefore \left(\frac{v_o}{v_i} \right)_{\max} = \frac{4.4}{20} = 0.22 \quad \left(\frac{v_o}{v_i} \right)_{\max} = n^{1/1-n} = 0.22 \quad \therefore n = 0.33$$

$$n = \frac{\tau}{\tau_1} \quad \therefore \tau = n\tau_1 = 0.33 \times 10^{-9} \text{ s}$$

$$\tau = \frac{L}{R} \quad \therefore L = \tau R = 0.33 \times 10^{-9} \times 100 = 33 \times 10^{-9} \text{ H}$$

Example 2.13: A 20-kHz square wave is applied to a RC differentiating circuit of Fig. 2.1(a). With $R = 4 \text{ k}\Omega$, it produces the output with a tilt of 5 per cent. Calculate the value of the capacitor and lower 3-dB frequency.

Solution: Tilt in the output for a square-wave input is:

$$P = \frac{\pi f_1}{f}$$

Lower 3-dB frequency

$$f_1 = \frac{Pf}{\pi} = \frac{0.05 \times 20 \times 10^3}{\pi} = 318.3 \text{ Hz}$$

$$\text{Also } f_1 = \frac{1}{2\pi RC}$$

$$C = \frac{1}{2\pi f_1 R} = \frac{1}{2\pi \times 318.3 \times 4 \times 10^3} = 125 \text{ nF}$$

Example 2.14: The input signal shown in Fig. 2.29(a) is applied to a RC high-pass circuit in Fig. 2.2(a), whose time constant is 0.4 ms. Draw the output waveform and mark all voltages, assuming that the capacitor is initially uncharged.

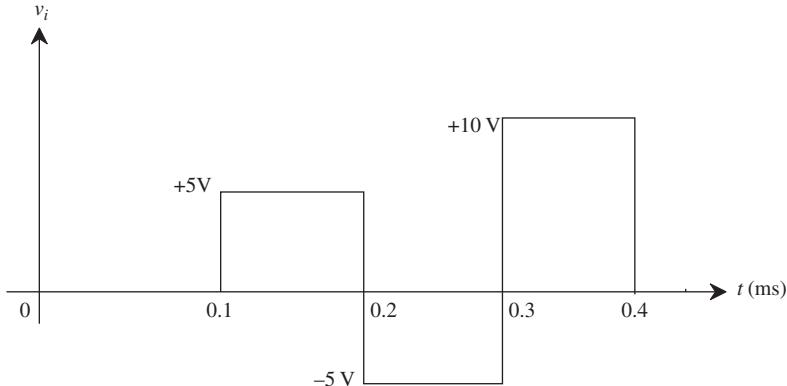


FIGURE 2.29(a) The input to the high-pass circuit

Solution: For $t < 0.1 \text{ ms}$, $v_i = 0$, $v_o = 0$

At $t = 0.1 \text{ ms}$, the input suddenly rises to $+5 \text{ V}$, the output also changes by the same amount as the capacitor acts as a short circuit.

For $0.1 < t < 0.2$, v_i remains constant at 5 V . Therefore, v_o decays exponentially with the time constant 0.4 ms .

At $t = 0.2 \text{ ms}$,

$$v_o = 5e^{(-0.1 \times 10^{-3})/(0.4 \times 10^{-3})} = 3.894 \text{ V}$$

At $t = 0.2 \text{ ms}$ the input suddenly drops by 10 V , v_o also falls by the same amount.

$$v_o (t = 0.2 \text{ ms}) = 3.894 - 10 = -6.106 \text{ V}$$

For $0.2 \text{ ms} < t < 0.3 \text{ ms}$, v_i remains at -5 V . Hence, v_o decays exponentially with the time constant 0.4 ms .

At $t = 0.3 \text{ ms}$

$$v_o = -6.106 e^{(-0.1 \times 10^{-3})/(0.4 \times 10^{-3})} = -4.755 \text{ V}$$

At $t = 0.3 \text{ ms}$, input suddenly rises by 15 V . The output also changes by the same amount.

$$v_o (t = 0.3 \text{ ms}) = -4.755 + 15 = 10.245 \text{ V}$$

For $0.3 \text{ ms} < t < 0.4 \text{ ms}$, v_i remains constant at 10 V . Hence, v_o will decay exponentially with the time constant 0.4 ms .

At $t = 0.4 \text{ ms}$,

$$v_o = 10.245 e^{0.1 \times 10^{-3}/0.4 \times 10^{-3}} = 7.979 \text{ V}$$

The output waveform is shown in Fig. 2.29(b).

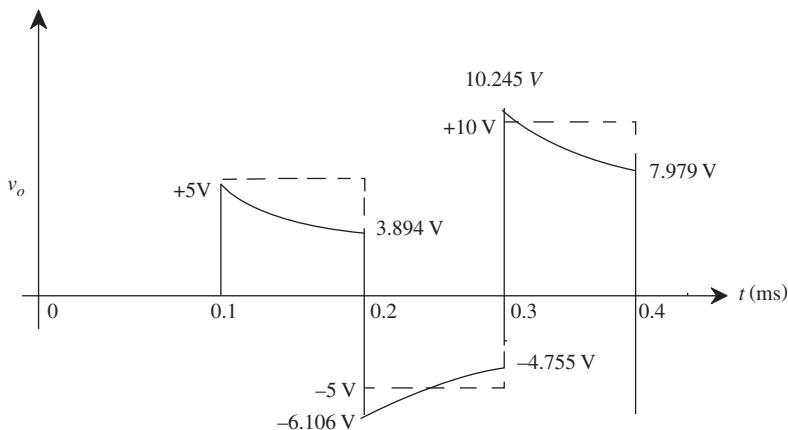


FIGURE 2.29(b) The output of the high-pass circuit

Example 2.15: Design a RC differentiator circuit for a square-wave input having time period 2 ms and 20 V amplitude, as shown in Fig. 2.30(a). It is required to have output of 12 V . Assume $R_S = 40 \Omega$ and $R_L = 400 \Omega$.

Solution: The desired circuit is shown in Fig. 2.30(b).

At $t = 0$, v_i suddenly jumps from 0 to 20 V . As the capacitor acts as a short circuit, v_o rises only by 12 V , because of the drop across R_S .

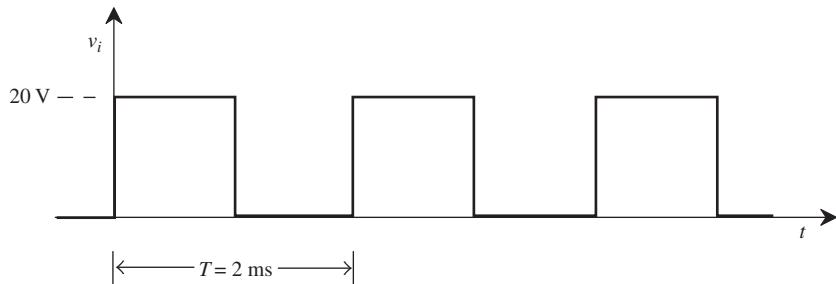


FIGURE 2.30(a) The input to the circuit

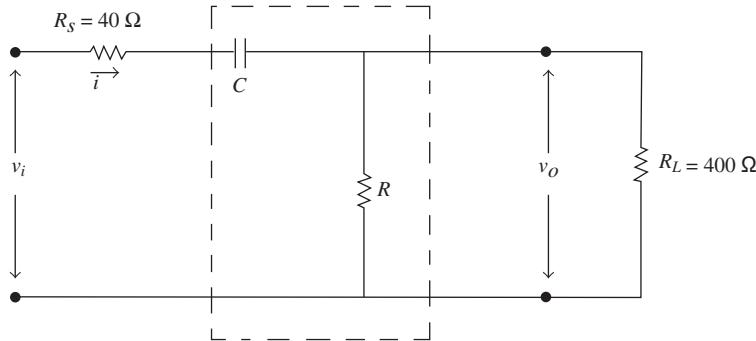


FIGURE 2.30(b) The desired circuit

At $t = 0+$, $v_i = 20$ V, and $v_o = 12$ V.

Hence, $i = (v_i - v_o)/R_S = (20 - 12)/40 = 0.2$ A.

$$\therefore v_o = i \left(\frac{R \times R_L}{R + R_L} \right) = 0.2 \times \left(\frac{R \times 400}{R + 400} \right) \quad 12 = 0.2 \left(\frac{400R}{R + 400} \right) \quad 60 = \left(\frac{400R}{R + 400} \right)$$

$$\therefore R = 70.588 \Omega$$

For the differentiating circuit the condition required is $\tau \ll T$ or $R_{eq}C \ll T$, where, the total resistance of the input side is R_{eq} .

$$R_{eq} = R + 40 = 70.588 + 40 = 110.588 \Omega \quad C \ll (T/R_{eq}) \quad C \ll \frac{2 \times 10^{-3}}{110.588} = 18 \mu\text{F}$$

Example 2.16: A 1000-Hz triangular wave having peak-to-peak amplitude of 10 V, shown in Fig. 2.31(a), is applied to a high-pass RC circuit with $R = 1 \text{ M}\Omega$ and $C = 10 \text{ pF}$. Calculate the peak-to-peak amplitude of the voltage across the resistor and draw the waveform to scale.

Solution: Given that

$$f = 1000 \text{ Hz} \quad \therefore T = \frac{1}{1000} = 1 \text{ ms}$$

$$\tau = RC = 1 \times 10^6 \times 10 \times 10^{-12} = 10 \times 10^{-6} \text{ s} = 0.01 \text{ ms}$$

As $\tau \ll T$, the high-pass circuit behaves as a differentiator. Hence, the output is $v_o = RC(dv_i/dt)$. Therefore, $0 < t < \frac{T}{4}$ and $v_i = \frac{5}{T/4}t$.

$$\therefore v_o = 10 \times 10^{-6} \frac{d}{dt} \left(\frac{5}{T/4}t \right) = 10 \times 10^{-6} \times \frac{5 \times 4}{1 \times 10^{-3}} \quad \therefore v_o \left(\frac{T}{4} \right) = 0.2 \text{ V}$$

Upto $T/4$, the output is 0.2 V. For $T/4 < t < T/2$,

$$v_i = \frac{-5}{T/4}t \quad v_o \left(\frac{T}{2} \right) = 10 \times 10^{-6} \frac{d}{dt} \left(\frac{-5}{T/4}t \right) = 10 \times 10^{-6} \times \frac{-5 \times 4}{1 \times 10^{-3}} = -0.2 \text{ V}$$

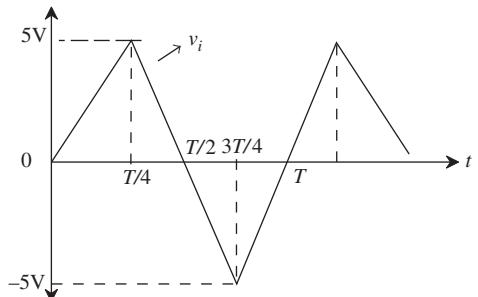


FIGURE 2.31(a) Input

From $T/4$ to $T/2$ the output is -0.2 V. At $T/2$ the input becomes negative. So from $T/2$ to $3T/4$

$$v_i = -(-\alpha t) = \frac{5}{T/4} t \quad v_o \left(\frac{3T}{4} \right) = 10 \times 10^{-6} \frac{d}{dt} \left(\frac{5}{T/4} t \right) = 10 \times 10^{-6} \times \frac{5 \times 4}{1 \times 10^{-3}} = 0.2 \text{ V}$$

At $3T/4$, the output is $+0.2$ V. For $3T/4 < t < T$,

$$v_i = \frac{-5}{T/4} t$$

$$\begin{aligned} v_o(T) &= 10 \times 10^{-6} \frac{d}{dt} \left(\frac{-5t}{T/4} \right) \\ &= 10 \times 10^{-6} \times \frac{-5 \times 4}{1 \times 10^{-3}} \\ &= -0.2 \text{ V} \end{aligned}$$

From $3T/4$ to T , the output is -0.2 V

Beyond T the output is once again $+0.2$ V as the the input is positive and so on.

The output waveform is shown in Fig. 2.31(b).

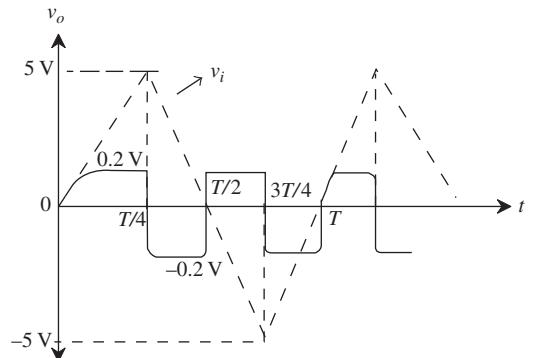


FIGURE 2.31(b) Output

Example 2.17: A signal $v_i = Ve^{-t/\tau}$ is applied to a double differentiator, shown in Fig. 2.32(a). Find the output if $\tau = R_1 C_1 = R_2 C_2$. Plot the response and find the value of $t > 0$ at which v_o is maximum. The amplifier has a gain A .

Solution: Assume $R_1 = R_2 = R$ and $C_1 = C_2 = C$

$$R_1 C_1 = R_2 C_2 = \tau$$

Assume the capacitor is initially uncharged.

Therefore, the Laplace transformed circuit is as shown in Fig. 2.32(b).

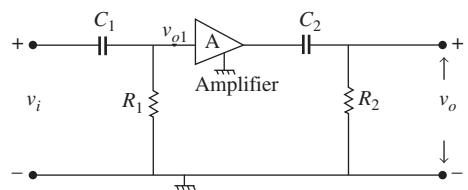


FIGURE 2.32(a) Given high-pass circuit

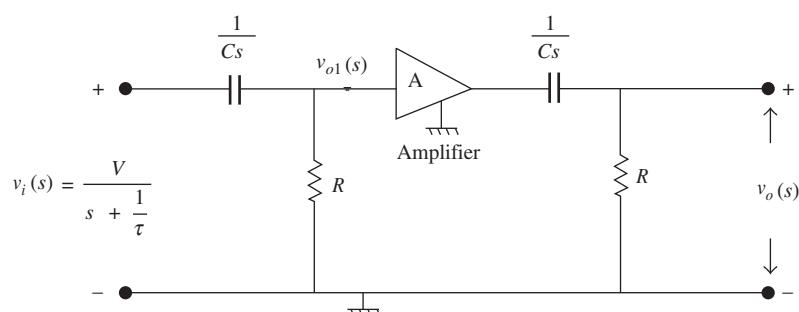


FIGURE 2.32(b) Laplace transform version of Fig. 2.30(a)

The output $v_{o1}(s) = \frac{VRCs}{\left(s + \frac{1}{\tau}\right)(RCs + 1)} = \frac{V\tau s}{\left(s + \frac{1}{\tau}\right)(\tau s + 1)} = \frac{V\tau s}{\left(s + \frac{1}{\tau}\right)\left(s + \frac{1}{\tau}\right)\tau} = \frac{Vs}{\left(s + \frac{1}{\tau}\right)^2}$

$$\therefore v_o(s) = A \left[\frac{\frac{v_{o1}(s)}{Cs}}{\frac{1}{Cs} + R} \right] R = \frac{Av_{o1}(s)CsR}{1 + RCs} = \frac{Av_{o1}(s)\tau s}{1 + \tau s}$$

$$\frac{Av_{o1}(s)\tau s}{\left(s + \frac{1}{\tau}\right)\tau} = \frac{AVs \times s}{\left(s + \frac{1}{\tau}\right)\left(s + \frac{1}{\tau}\right)^2} = \frac{AVs^2}{\left(s + \frac{1}{\tau}\right)^3}$$

Taking Laplace inverse,

$$\therefore v_o(t) = AVe^{-t/\tau} \left(1 - \frac{t}{\tau}\right)^2$$

The minimum value of $v_o(t)$ occurs only at $t = \tau$.

Therefore $v_o(t)_{\min} = 0$

To find the max value of $v_o(t)$, make

$$\frac{dv_o(t)}{dt} = 0 = AVe^{(-t/\tau)} 2 \left[1 - \frac{t}{\tau}\right] \times \left(\frac{-1}{\tau}\right) + A \left(1 - \frac{t}{\tau}\right)^2 ve^{(-t/\tau)} \times \left(\frac{-1}{\tau}\right)$$

$$0 = AV \left(1 - \frac{t}{\tau}\right) e^{-t/\tau} \left(\frac{-1}{\tau}\right) \left[2 + \left(1 - \frac{t}{\tau}\right)\right]$$

$$\therefore \left(1 - \frac{t}{\tau}\right) = -2 \quad \frac{\tau - t}{\tau} = -2 \quad \therefore t = 3\tau$$

The maximum value of $v_o(t)$ occurs at $t = 3\tau$.

Calculating the output at $t = 3\tau$,

$$v_o = AVe^{-3} (1 - 3)^2 = (4)AV(0.05) = 0.2AV.$$

The output is shown in Fig. 2.32(c).

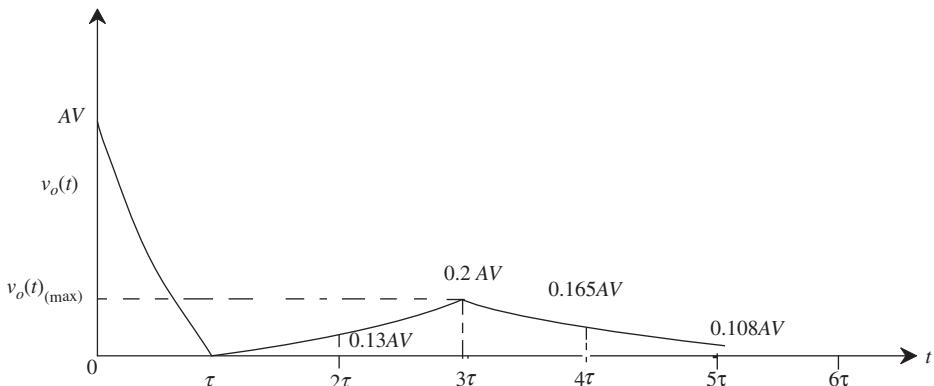


FIGURE 2.32(c) Output of the given circuit

SUMMARY

- Linear systems are those that obey homogeneity and additivity.
- Homogeneity and additivity taken together comprise the principle of superposition.
- The process by which the shape of a non-sinusoidal signal, when passed through a linear network, is altered is called linear waveshaping.
- Only a sinusoidal signal can preserve its form when transmitted through a linear high-pass network. All other signals undergo distortion in shape.
- A high-pass circuit attenuates all low-frequency signals and transmits only signals of high frequency.
- If C of the high-pass RC circuit is replaced by L and if $L/R = RC$, then all the results of the RC circuits are valid for the RL circuits as well.
- A step voltage is one, which has a value zero for all times $t < 0$, and remains at V for all times $t \geq 0$.
- Fall time is defined as the time taken by the output waveform to fall from 90 per cent to 10 per cent of its initial value.
- The fall time is directly proportional to the time constant and inversely proportional to the lower cut-off frequency.
- The voltage across a capacitor cannot change instantaneously if the current through it remains finite.
- A waveform which is zero for $t < 0$, and which increases linearly with time for $t > 0$ is called a ramp.
- The transmission error, e_t for a ramp input is defined as the difference between the input and the output divided by the input.
- For most applications, the steady-state condition is reached approximately at $t = 5\tau$.
- A pulse may be treated as the sum of a positive step followed by a delayed negative step of the same amplitude.
- A periodic waveform which maintains itself at one constant level V' for a time T_1 , and then changes abruptly to another level V'' and remains constant at that level for a time T_2 , and repeats itself with a period $T = T_1 + T_2$ is called a square wave. If $T_1 = T_2 = T/2$, it is called a symmetric square wave.
- The lower cut-off frequency of a high-pass circuit is given by $f_1 = 1/2\pi RC$.
- The capacitor in the high-pass circuit blocks the dc component of the input. Hence, no dc component is present in the output.
- The process of converting pulses into spikes by means of a circuit of a very short time constant is called peaking.
- The output of a high-pass circuit excited by a square-wave input exhibits a tilt when the time constant of the circuit is not very high.
- A high-pass circuit acts as a differentiator if the time constant of the circuit is very small as compared to the time period of the input signal.
- When a high-pass circuit is used as an ideal differentiator, the phase shift between the input and the output is 90° .
- It is more convenient to introduce initial conditions in an integrator than in a differentiator.
- For double differentiation, two high-pass networks with small time constants are connected in a cascade.
- The current through an inductor cannot change instantaneously when a finite voltage is applied across it.

MULTIPLE CHOICE QUESTIONS

- 1) The process by which the shape of a non-sinusoidal signal when transmitted through a linear network is altered is called:
- Non-linear waveshaping
 - Peaking
 - Linear waveshaping
 - Clamping
- 2) The lower half-power frequency of a high-pass circuit is:
- $\frac{1}{2\pi LC}$
 - $\frac{1}{2\pi RC}$
 - $\frac{1}{2\pi\sqrt{LC}}$
 - $\frac{1}{2\pi\sqrt{RC}}$
- 3) The fall time of a high-pass circuit is:
- $\frac{0.35}{f_1}$
 - $\frac{1}{2\pi LC}$
 - 22τ
 - $\frac{35}{f_1}$
- 4) A dc component is associated with a periodic input waveform applied to a high-pass circuit. The dc component in the output is:
- ∞
 - 0
 - $2v_i$
 - Finite value
- 5) If the shape of the square wave is to be preserved in the output of a high-pass circuit, then the percentage tilt should be:
- a) ∞
b) 0
c) 50%
d) 100%
- 6) An exponential signal $v_i = V(1 - e^{-t/\tau_1})$ is applied to high-pass circuit. When $n = \tau/\tau_1$ is small, the output is:
- Larger in duration, smaller in amplitude
 - Shorter in duration, smaller in amplitude
 - Larger in duration, larger in amplitude
 - Shorter in duration, larger in amplitude
- 7) An exponential signal $v_i = V(1 - e^{-t/\tau_1})$ is applied to a high-pass circuit when $n = \tau/\tau_1$ is large. The output is:
- Larger in duration, smaller in amplitude
 - Shorter in duration, smaller in amplitude
 - Larger in duration, larger in amplitude
 - Shorter in duration, larger in amplitude
- 8) When a ramp is applied to a high-pass circuit, the transmission error is given as:
- $\frac{T}{2\tau}$
 - $\frac{T}{\tau}$
 - 2τ
 - τ^2
- 9) When a high-pass circuit is used as differentiator, it means that the output is:
- Same as the input
 - Integral of the input
 - Differential of the input
 - None of the above
- 10) A double differentiator is called:
- An RC -coupled amplifier
 - A feedback amplifier
 - A rate-of-rise amplifier
 - A tuned amplifier

SHORT ANSWER QUESTIONS

- What is a linear network? Explain the working of a high-pass RC circuit.
- What is meant by linear waveshaping?
- Obtain the expression for the lower cut-off frequency of a high-pass RC circuit.
- Define fall time of a high-pass circuit for a step input.
- Specify the condition for which a high-pass circuit behaves as a differentiator and draw the input and output waveforms.

6. Draw the circuit of a double differentiator.
7. Define per cent tilt.
8. Draw the output of a high-pass circuit for a ramp input when the time constant τ is: (i) very small, and (ii) very large when compared to the time period of the input signal.

9. Plot the response of a high-pass circuit for $\tau = 0.1T$, $\tau = T$ and $\tau = 10T$ when the input is a square wave.

10. Derive the condition under which high-pass RC circuit behaves as a peaking circuit.
11. Explain why a double differentiator is called a rate-of-rise amplifier.

LONG ANSWER QUESTIONS

1. A positive step input of magnitude V is applied to high-pass RC circuit at $t = 0$. Derive the expression for the output voltage and also calculate the fall time and show that the fall time is $0.35/f_1$ where f_1 is the lower cut-off frequency.
2. A pulse is applied as an input to a high-pass RC circuit. Derive the expression for the output voltage.
3. Derive the expression for per cent tilt, 'P' when a square wave is the input to a high-pass RC circuit.
4. Prove that, for any periodic input waveform, the average level of the steady-state output signal from the high-pass RC circuit is always zero.

5. The input to a high-pass circuit is an exponential $v_i = V(1 - e^{-t/\tau_1})$. Derive the expression for its output voltage:
(i) When $\tau = \tau_1$ and (ii) when $\tau \neq \tau_1$ where, τ is the time constant of high-pass RC circuit.
6. The input to a high-pass circuit is a ramp $v_i = \alpha t$. Obtain the expression for the output voltage and also calculate the transmission error, e_t and show that e_t is proportional to the lower cut-off frequency.
7. Show how a high-pass circuit having a time constant smaller than the time period of an input signal behaves as a differentiator.
8. What is a double differentiator? Show that a double differentiator is a rate-of-rise amplifier.

UNSOLVED PROBLEMS

1. A ramp shown in Fig. 2p.1 is applied to a high-pass RC circuit. Draw to scale the output waveform for the cases: (i) $T = RC$, (ii) $T = 0.2 RC$, (iii) $T = 5 RC$.

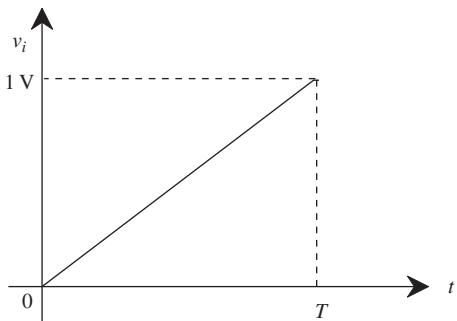


FIGURE 2p.1 A ramp as input

2. A waveform shown in Fig. 2p.2 is applied as input to a RC high pass circuit whose time constant is 250 ps. If the maximum output

voltage across the resistor is 50 V, what is the peak value of the input waveform?

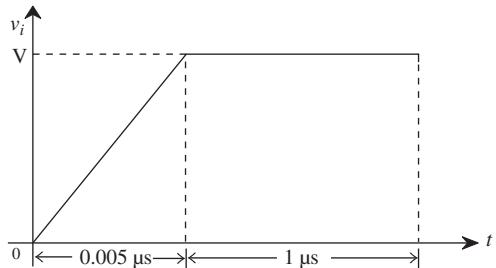


FIGURE 2p.2 Input to the high-pass RC circuit

3. A limited ramp shown in Fig. 2p.3(a) is applied to a RC high-pass circuit of Fig. 2.2(a). The time constant of the RC circuit is 2 ms. Calculate the maximum value of the output voltage and the output at the end of the input waveform.

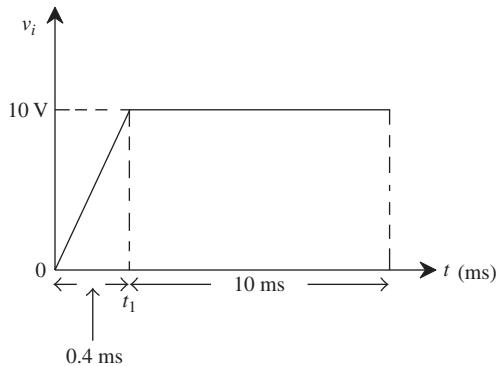


FIGURE 2p.3 Input to the high-pass circuit

4. The periodic waveform shown in Fig. 2p.4 is applied to an RC differentiating circuit whose time constant is $10 \mu\text{s}$. Sketch the output and calculate the maximum and minimum values of the output voltage with respect to the ground.

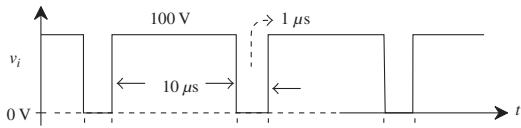


FIGURE 2p.4 Periodic square wave as an input to the high-pass circuit

5. The periodic ramp voltage as shown in Fig. 2p.5 is applied to a high-pass RC circuit. Find equations from which to determine the steady-state output waveform when $T_1 = T_2 = RC$.

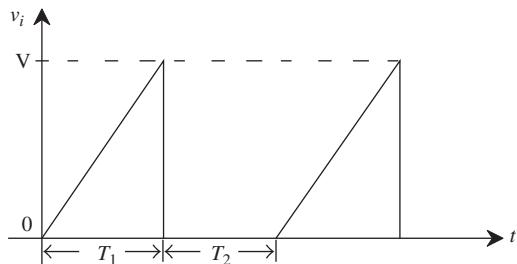


FIGURE 2p.5 A periodic ramp as input

6. A square wave of pulse width 2 ms and peak amplitude of 12 V as shown in Fig. 2p.6 is applied to high-pass RC circuit with time constant 4 ms. Plot the first four cycles of the output waveform.

$$T/2 = 2 \text{ ms}$$

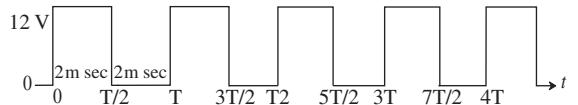


FIGURE 2p.6 Symmetric square wave as an input

7. A 20-Hz symmetric square wave, referenced to zero volts, and with a peak-to-peak amplitude of 10 V is fed to an amplifier through the coupling network shown in Fig. 2p.7. Calculate and plot the output waveform when the lower 3-dB frequency is: (i) 0.6 Hz, (ii) 6 Hz, (iii) 60 Hz.

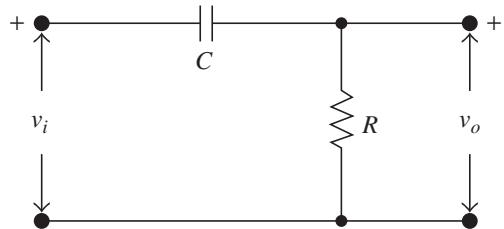


FIGURE 2p.7 The given coupling network

8. A square wave is applied as input to an amplifier through a coupling condenser of $10 \mu\text{F}$. The amplifier has input resistance of $10 \text{k}\Omega$. Determine the lowest frequency if the tilt is not to exceed 10 per cent.
9. A pulse of 10 V amplitude and duration 1 ms is applied to a high-pass RC circuit with $R = 20 \text{k}\Omega$ and $C = 0.5 \mu\text{F}$. Plot the output waveform to scale and calculate the per cent tilt in the output.
10. The input to the high-pass circuit shown in Fig. 2.2(a) is the waveform shown in Fig. 2p.8. Calculate and plot the output waveform to scale, given that $RC = \tau = 0.1 \text{ ms}$.

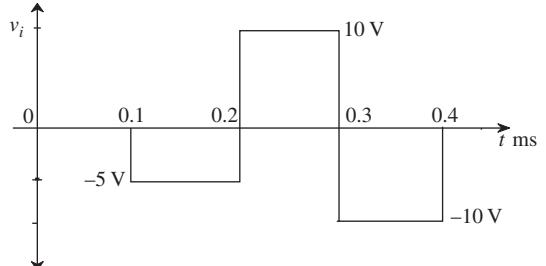


FIGURE 2p.8 Input to the high-pass circuit

11. A pulse of 10-Volt amplitude with a pulse width of 0.5 ms, as shown in Fig. 2p.9, is applied to a high-pass RC circuit of Fig. 2.1(a), having time constant 10 ms. Sketch the output waveform and determine the per cent tilt in the output.

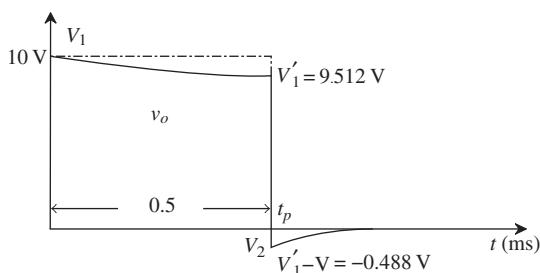


FIGURE 2p.9 Input and output of the high-pass circuit

12. A high-pass RC circuit is desired to pass a 3-ms sweep (ramp input) with less than 0.4 per cent transmission error. Calculate the highest possible value of the lower 3-dB frequency.
13. A symmetric square wave with $f = 500$ Hz shown in Fig. 2p.10 is fed to an RC high-pass network of Fig. 2.1(a). Calculate and plot the transient and the steady-state response if: (a) $\tau = 5 T$ and (b) $\tau = T/20$.

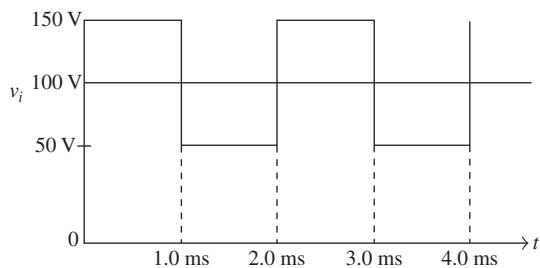


FIGURE 2p.10 Input to the coupling network

14. A current pulse of amplitude 5 A in Fig. 2p.11 is applied to a parallel RC combination shown in Fig. 2p.12. Plot to scale the waveforms of the current flowing through the capacitor for the cases: (i) $t_p = 0.1 RC$ (ii) $t_p = RC$, (iii) $t_p = 5RC$.

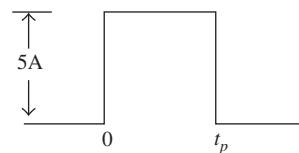


FIGURE 2p.11 The given input to the circuit

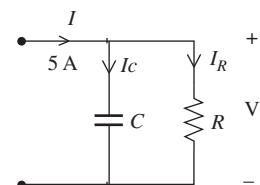


FIGURE 2p.12 The given circuit

15. Draw the output waveform if the waveform shown in Fig. 2p.13 is applied at the input of the RC circuit shown in Fig. 2p.14.

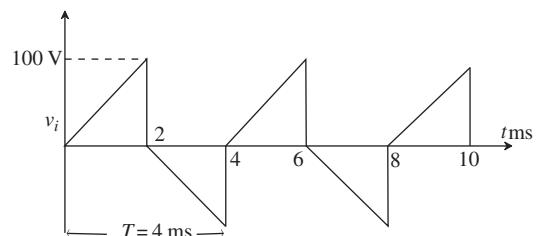


FIGURE 2p.13 The input to the high-pass circuit in Fig. 2p.13

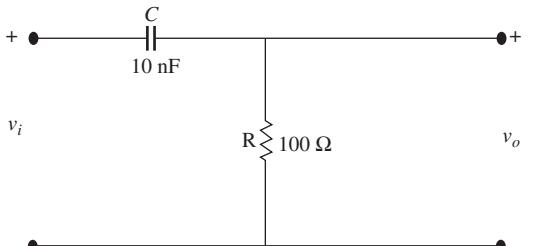


FIGURE 2p.14 The given high-pass circuit

Linear Waveshaping: Low-pass Circuits, Attenuators and RLC Circuits

LEARNING OBJECTIVES

After reading this chapter, you will be able to:

- Derive the expressions and plot the responses of low-pass RC and RL circuits to different types of inputs, namely, sinusoidal, step, pulse, square-wave, exponential and ramp
- Describe the application of a low-pass circuit as an integrator
- Understand the principles of working of uncompensated and compensated attenuators
- Realize the response of RLC circuits to step input

3.1 INTRODUCTION

A low-pass circuit is one which gives an appreciable output for low frequencies and zero or negligible output for high frequencies. In this chapter, we essentially consider low-pass RC and RL circuits and their responses to different types of inputs. Also, we study attenuators that reduce the magnitude of the signal to the desired level. Attenuators which give an output that is independent of frequency are studied. One application of such a circuit is as a CRO probe. Further, the response of the RLC circuit to step input is considered and its output under various conditions such as under-damped, critically damped and over-damped conditions is presented. The application of an RLC circuit as a ringing circuit is also considered.

3.2 LOW-PASS CIRCUITS

Low-pass circuits derive their name from the fact that the output of these circuits is larger for lower frequencies and vice-versa. Figures 3.1(a) and (b) represent a low-pass RC circuit and a low-pass RL circuit, respectively.

In the RC circuit, shown in Fig. 3.1(a), at low frequencies, the reactance of C is large and decreases with increasing frequency. Hence, the output is smaller for higher frequencies and vice-versa. Similarly, in the RL circuit shown in Fig. 3.1(b), the inductive reactance is small for low frequencies and hence, the output is large at low frequencies. As the frequency increases, the inductive reactance increases; hence, the output decreases.

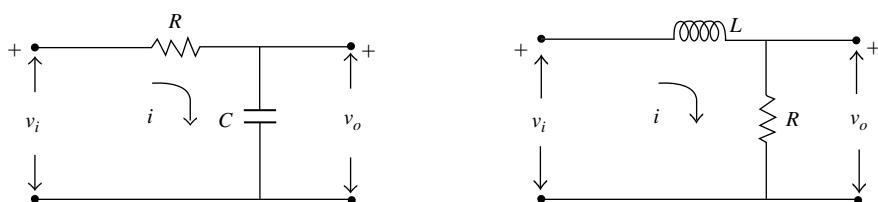


FIGURE 3.1(a) A low-pass RC circuit; and (b) a low-pass RL circuit

Therefore, these circuits are called low-pass circuits. Let us consider the response of these low-pass circuits to different types of inputs.

3.2.1 The Response of a Low-pass RC Circuit to Sinusoidal Input

For the circuit given in Fig. 3.1(a), if a sinusoidal signal is applied as the input, the output v_o is given by the relation:

$$v_0 = v_i \frac{\frac{1}{j\omega C}}{R + \frac{1}{j\omega C}} \quad \frac{v_o}{v_i} = \frac{1}{1 + j\omega CR}$$

$$\left| \frac{v_o}{v_i} \right| = \frac{1}{\sqrt{1 + (\omega CR)^2}} = \frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega_2} \right)^2}} = \frac{1}{\sqrt{1 + \left(\frac{\tau}{T} \right)^2}} \quad (3.1)$$

where, $\omega_2 = 1/CR = 1/\tau$. From Eq. (3.1), the phase shift θ the signal undergoes is given as:

$$\theta = \tan^{-1}(\omega/\omega_2) = \tan^{-1}(\tau/T)$$

Figure 3.2(a) shows a typical frequency vs. gain characteristic. Hence, f_2 is the upper half-power frequency. At $\omega = \omega_2$,

$$\left| \frac{v_o}{v_i} \right| = \frac{1}{\sqrt{2}} = 0.707$$

Figure 3.2(b) shows the variation of gain with frequency for different values of τ . As is evident from the figure, the half-power frequency, f_2 , increases with the decreasing values of τ , the time constant. The sinusoidal signal undergoes a change only in the amplitude but its shape remains preserved.

Figure 3.2(c) shows the variation of θ as a function of frequency. As (τ/T) becomes large, θ approaches 90° . This characteristic can be appreciated when we talk about an integrator later.

3.2.2 The Response of a Low-pass RC Circuit to Step Input

Let a step voltage be applied as the input to the low-pass RC circuit shown in Fig. 3.1(a). The output v_o can be obtained by using Eq. (2.9) as shown in Fig. 3.3. We have $RC = \tau$.

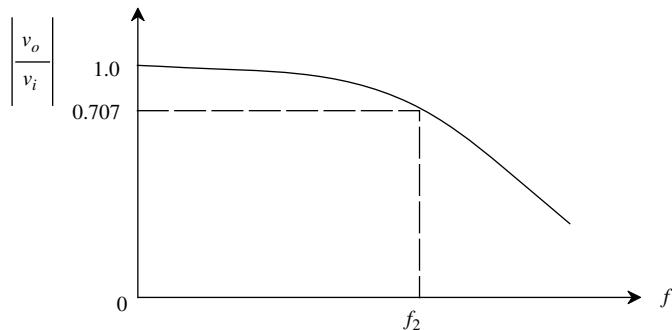
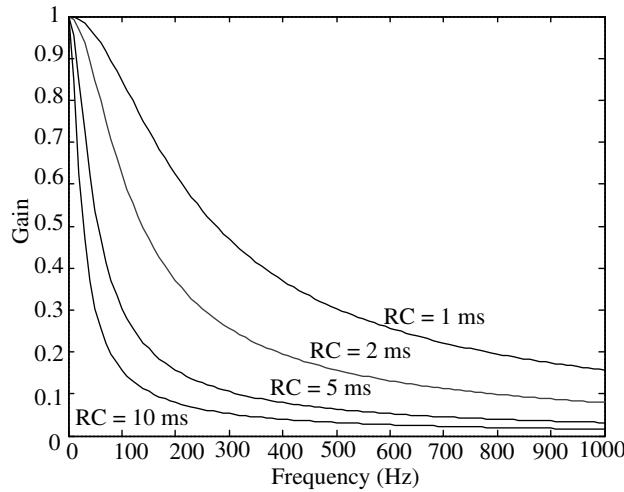
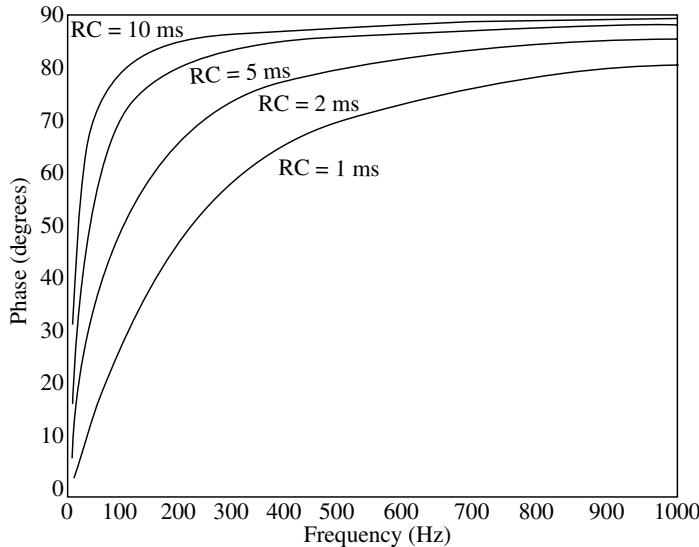


FIGURE 3.2(a) Typical frequency-vs-gain characteristic of a low-pass circuit to sinusoidal input

FIGURE 3.2(b) Gain-vs-frequency curves for different values of τ FIGURE 3.2(c) Phase-vs-frequency curves for different values of τ

$$v_o(t) = v_f + (v_i - v_f) e^{-t/\tau}$$

Here, $v_f = V$ and $v_i = 0$. Therefore,

$$v_o(t) = V - V e^{-t/\tau} = V (1 - e^{-t/\tau}) \quad (3.2)$$

As $t \rightarrow \infty$, $v_o(t) \rightarrow V$.

Initially, as the capacitor behaves as a short circuit, the output voltage is zero. As the capacitor charges, the output reaches the steady-state value of V in a time interval that is dependent on the time constant, τ .

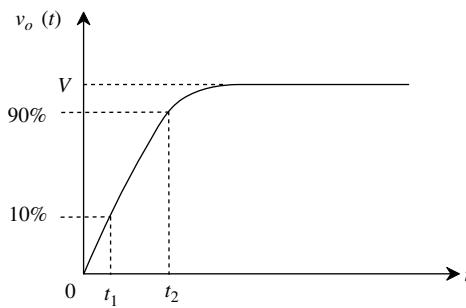


FIGURE 3.3 The response of a low-pass circuit to step input

On the other hand, the output of Eq. (3.2) can also be obtained by solving the following differential equation. From Fig. 3.1(a), For $v_i = V$:

$$V = v_i = Ri + \frac{1}{C} \int i dt \quad (3.3)$$

We know that $(1/C) \int i dt = v_o$

$$\frac{i}{C} = \frac{dv_o}{dt} \quad \text{or} \quad i = C \frac{dv_o}{dt} \quad (3.4)$$

From Eqs. (3.3) and (3.4):

$$V = RC \frac{dv_o}{dt} + v_o \quad V = \tau \frac{dv_o}{dt} + v_o \quad (3.5)$$

Taking Laplace transforms:

$$\frac{V}{s} = \tau s v_o(s) + v_o(s) = v_o(s) [\tau s + 1] = v_o(s) \tau \left(s + \frac{1}{\tau} \right), \quad \text{Hence} \quad v_o(s) = \frac{\frac{V}{\tau}}{s \left(s + \frac{1}{\tau} \right)}$$

Resolving into partial fractions:

$$\frac{\frac{V}{\tau}}{s \left(s + \frac{1}{\tau} \right)} = \frac{A}{s} + \frac{B}{\left(s + \frac{1}{\tau} \right)} \quad \frac{V}{\tau} = A \left(s + \frac{1}{\tau} \right) + Bs$$

Putting $s = 0$:

$$\frac{V}{\tau} = \frac{A}{\tau} \quad \text{or} \quad A = V$$

Putting $s = -1/\tau$

$$\frac{V}{\tau} = B \left(-\frac{1}{\tau} \right) \quad \text{or} \quad B = -V$$

Therefore,

$$v_o(s) = \frac{V}{s} - \frac{V}{\left(s + \frac{1}{\tau} \right)}$$

Taking the Laplace inverse:

$$v_o(t) = V - V e^{-t/\tau} = V (1 - e^{-t/\tau}) \quad (3.6)$$

Now, for the circuit in Fig. 3.1(b):

$$v_i = L \frac{di}{dt} + iR \quad (3.7)$$

$$v_o = iR \quad i = \frac{v_o}{R} \quad \frac{di}{dt} = \frac{1}{R} \frac{dv_o}{dt} \quad v_i = \frac{L}{R} \frac{dv_o}{dt} + v_o \quad V = \tau \frac{dv_o}{dt} + v_o$$

Applying the Laplace transform:

$$\frac{V}{s} = \tau sv_o(s) + v_o(s) = v_o(s)(1 + s\tau) = v_o(s)\tau \left(s + \frac{1}{\tau}\right) \quad v_o(s) = \frac{\frac{V}{\tau}}{s \left(s + \frac{1}{\tau}\right)}$$

$$v_o(t) = V(1 - e^{-t/\tau}) \quad (3.8)$$

From Eq. (3.8), it may be seen that the output reaches the steady-state value faster for smaller values of τ . Similarly, when τ is large, it takes a longer time for the output to reach the steady-state value.

Rise time: The time taken for the output to reach 90 per cent of its final value from 10 per cent of its final value is called the rise time. Using Eq. (3.8) to calculate the rise time for this circuit:

$$\frac{v_o}{V} = 1 - e^{-t/\tau}$$

From Fig. 3.3 at $t = t_1$, $v_o = 0.1V$. Therefore,

$$0.1 = 1 - e^{-t_1/\tau}$$

$$e^{-t_1/\tau} = 0.9$$

$$t_1 = 0.1\tau \quad (3.9)$$

Similarly at $t = t_2$, $v_o = 0.9V$:

$$0.9 = 1 - e^{-t_2/\tau} \quad e^{-t_2/\tau} = 0.1$$

$$t_2 = 2.3\tau \quad (3.10)$$

Using Eqs. (3.9) and (3.10), rise time is given as:

$$t_r = t_2 - t_1 = 2.3\tau - 0.1\tau = 2.2\tau \quad (3.11)$$

Also

$$f_2 = 1/2\pi RC$$

$$RC = \tau = \frac{1}{2\pi f_2}$$

Therefore,

$$t_r = 2.2\tau = \frac{2.2}{2\pi f_2} = \frac{0.35}{f_2} \quad (3.12)$$

Let a step voltage V_σ be applied to a low-pass circuit. The output does not reach the steady-state value V_σ instantaneously as desired. Rather, it takes a finite time delay for the output to reach V_σ , depending on the value of the time constant of the low-pass circuit employed. If this output is to drive a transistor from the OFF to the ON state, this change of state does not occur immediately, because the output of the low-pass circuit takes some time to reach V_σ . The transistor is thus said to be switched from the OFF state into the ON state only when the voltage at the output of the low-pass circuit is 90 per cent of V_σ . If this time delay is to be small, τ should be small. On the contrary, if the output is to be ramp, τ should be large. This is elucidated by Example 3.1.

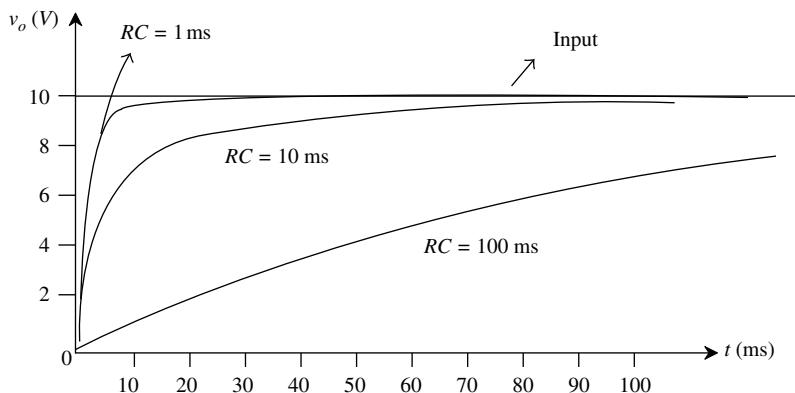
EXAMPLE

Example 3.1: A 10-Volt step input is applied to a low-pass RC circuit. Plot the response of the circuit when: (a) $RC = 1$ ms, (b) $RC = 10$ ms and (c) $RC = 100$ ms.

Solution: For a step input, the output voltage is $v_o = V(1 - e^{-t/\tau})$. Using this expression, the output voltage for different values of the time constant is shown in the Table 3.1. The waveforms are shown in Fig. 3.4.

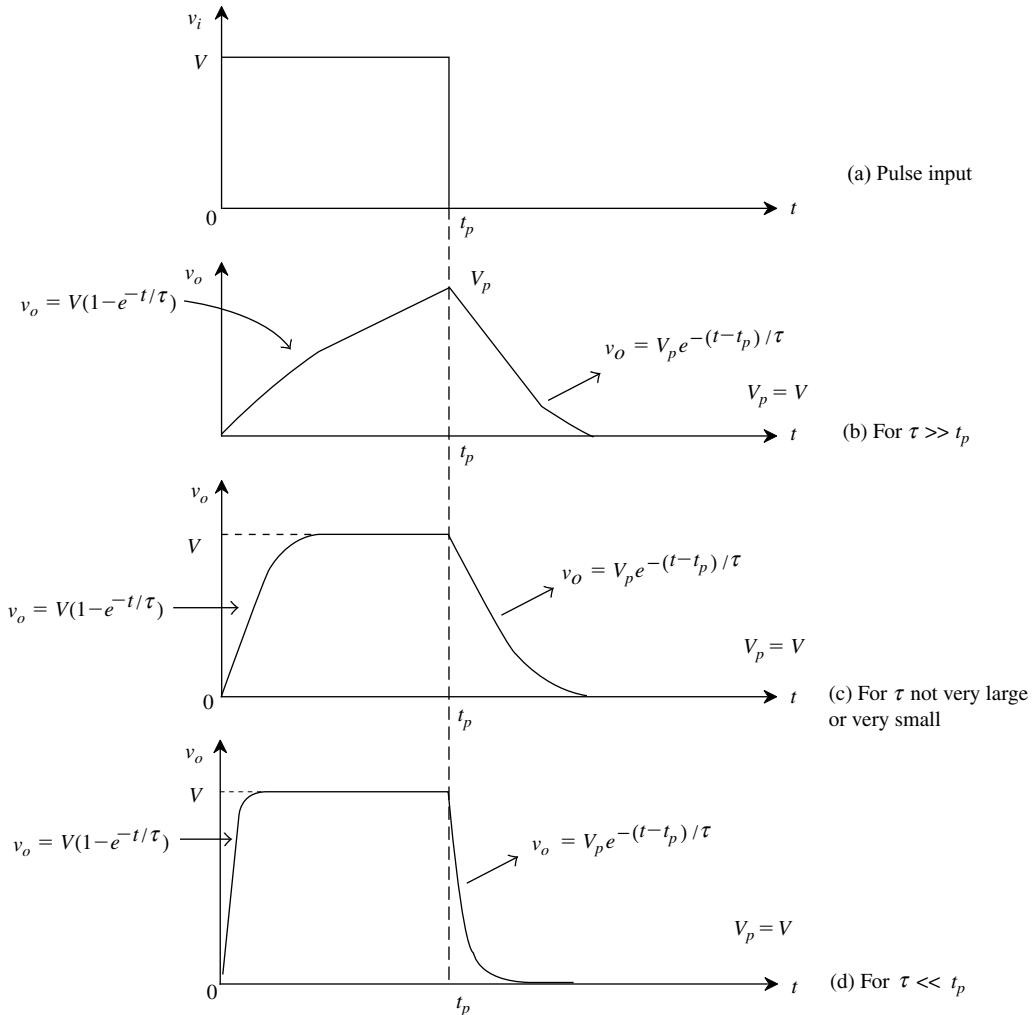
TABLE 3.1 The output of a low-pass circuit for different values of τ

t (ms)	$v_o = 10(1 - e^{-t/\tau})$ Volts		
	$\tau = 1$ ms	$\tau = 10$ ms	$\tau = 100$ ms
0	0	0	0
1	6.32	0.951	0.1
2	8.65	1.812	0.2
4	9.82	3.3	0.4
5	9.932	3.934	0.488
6	9.975	4.51	0.582
10	9.999	6.32	0.951
20	10	8.646	1.812
40	10	9.82	3.3
100	10	9.999	6.32
1000	10	10	9.999

FIGURE 3.4 The response of a low-pass circuit for different values of τ for a step input

3.2.3 The Response of a Low-pass RC Circuit to Pulse Input

Let the input to the low-pass circuit be a positive pulse of duration t_p and amplitude V as shown in Fig. 3.5(a). If this positive pulse is applied to drive an $n-p-n$ transistor from the OFF state into the ON state, the transistor will be switched ON only after a time delay. Similarly, at the end of the pulse, the transistor will not be switched immediately into the OFF state, but will take a finite time delay. To know how quickly it is possible to switch a transistor from one state to the other, we have to consider the response of a low-pass circuit to the pulse input. During the period 0 to t_p , the input is a step and the output is given by Eq. (3.8). At $t = t_p$ the input falls and the output decays exponentially as given in Eq. (3.13).

FIGURE 3.5 Response of a low-pass circuit for the pulse input for varying τ

$$v_o(t > t_p) = V_p e^{-(t-t_p)/\tau} \quad (3.13)$$

For $v_i = V$, the output for different values of τ is plotted in Fig. 3.5. It is seen here that the shape of the pulse at the output is preserved if the time constant of the circuit is much smaller than t_p , i.e., $\tau \ll t_p$. However, if a ramp is to be generated during the period of the pulse, τ is chosen such that $\tau \gg t_p$. The method to compute the output is illustrated in Example 3.2.

EXAMPLE

Example 3.2: An ideal pulse of amplitude 10 V is fed to an RC low-pass integrator circuit. The width of the pulse is $3\mu s$. Draw the output waveforms for the following upper 3-dB frequencies: (a) 30 MHz, (b) 3 MHz and (c) 0.3 MHz.

Solution: Consider the low-pass circuit in Fig. 3.1(a).

(a) At $f_2 = 30$ MHz

We know that $f_2 = 1/2\pi RC$

$$\tau = RC = \frac{1}{2\pi f_2} = \frac{1}{2\pi \times 30 \times 10^6} = 5.3 \text{ ns}$$

$$t_r = 2.2\tau = 2.2 \times 5.3 \times 10^{-9} = 11.67 \text{ ns}$$

At $t = t_p$,

$$V_p = V(1 - e^{-t_p/\tau}) = 10(1 - e^{-3 \times 10^{-6}/5.3 \times 10^{-9}}) = 10 \text{ V}$$

The output is plotted in Fig. 3.6(a).

(b) At $f_2 = 3$ MHz

$$\tau = RC = \frac{1}{2\pi f_2} = \frac{1}{2\pi \times 3 \times 10^6} = 53 \text{ ns}$$

$$t_r = 2.2\tau = 2.2 \times 53 \times 10^{-9} = 116.6 \text{ ns}$$

At $t = t_p$,

$$V_p = V(1 - e^{-t_p/\tau}) = 10(1 - e^{-3 \times 10^{-6}/53 \times 10^{-9}}) = 10 \text{ V}$$

The output is plotted in Fig. 3.6(b).

(c) At $f_2 = 0.3$ MHz

$$\tau = RC = \frac{1}{2\pi f_2} = \frac{1}{2\pi \times 0.3 \times 10^6} = 530 \text{ ns}$$

$$t_r = 2.2\tau = 2.2 \times 530 \times 10^{-9} = 1.166 \mu\text{s}$$

At $t = t_p$,

$$V_p = V(1 - e^{-t_p/\tau})$$

Therefore,

$$V_p = 10(1 - e^{-3 \times 10^{-6}/530 \times 10^{-9}}) = 9.96 \text{ V}$$

The output is plotted in Fig. 3.6(c).

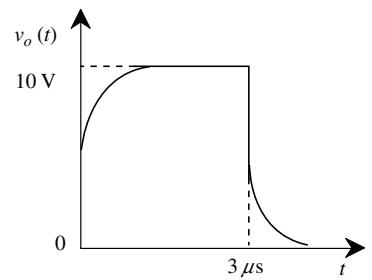


FIGURE 3.6(a) Output waveform at $f_2 = 30$ MHz

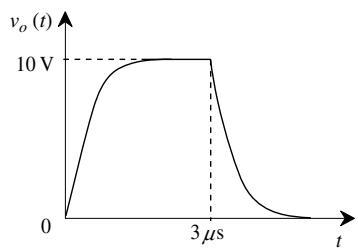


FIGURE 3.6(b) Output waveform at $f_2 = 3$ MHz

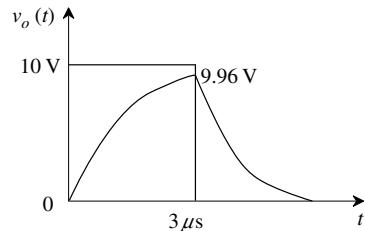


FIGURE 3.6(c) The output waveform at $f_2 = 0.3$ MHz

3.2.4 The Response of a Low-pass RC Circuit to a Square-wave Input

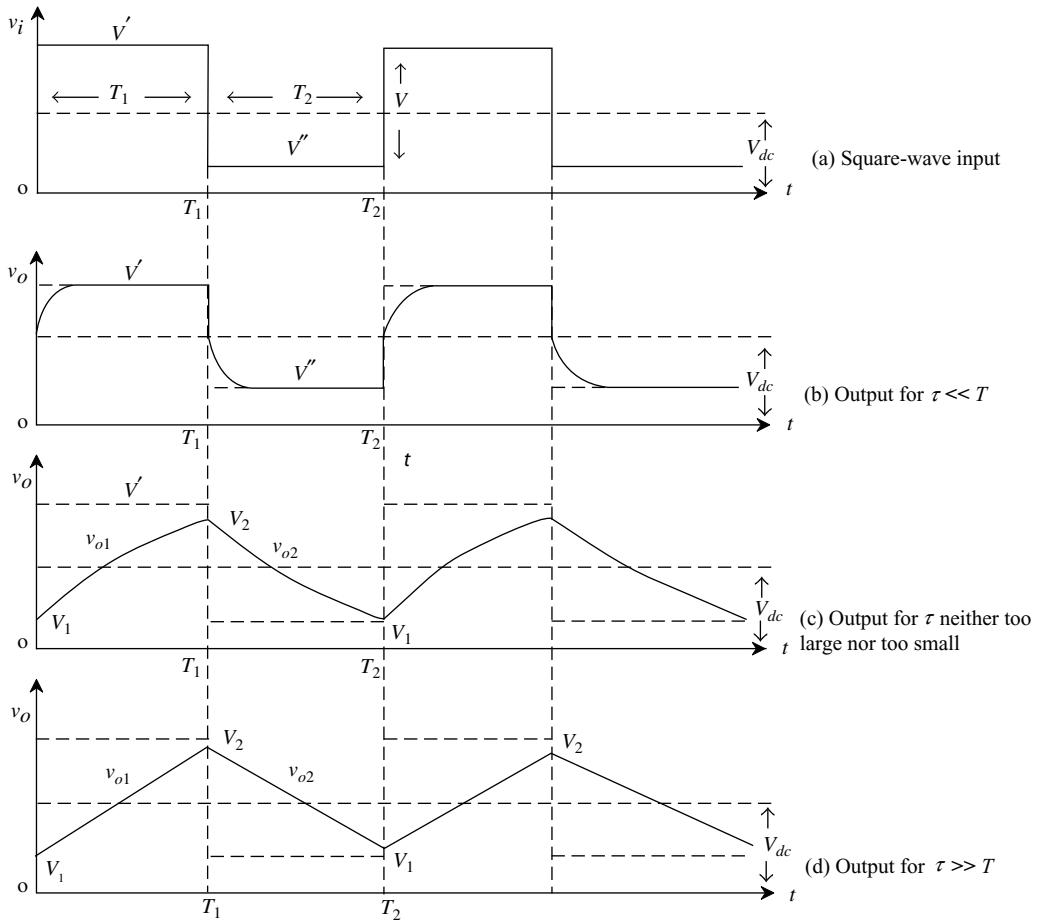
Let the input to the low-pass circuit be a square wave as shown in Fig. 3.7 (a).

We have from Eq. (2.9):

$$v_{o1}(t) = v_f + (v_i - v_f)e^{-t/\tau}$$

From Fig. 3.7(c), at $t = T_1$, $v_{o1} = V_2$ and $v_i = V_1$ and $v_f = V'$. Therefore:

$$v_{o1}(T_1) = V_2 = V' + (V_1 - V')e^{-T_1/\tau} \quad (3.14)$$

FIGURE 3.7 The response of the low-pass circuit to a square-wave input for different values of τ

Again, at $t = T_2$, $V_{o2} = V_1$ and we have $v_i = V_2$, $V_f = V''$

$$v_{o2}(T_2) = V_1 = V'' + (V_2 - V'')e^{-T_2/\tau} \quad (3.15)$$

If the input is a symmetric square wave:

$$T_1 = T_2 = \frac{T}{2} \quad (3.16)$$

Also

$$V' = -V'' = \frac{V}{2} \quad \text{and} \quad V_2 = -V_1 \quad (3.17)$$

Using Eqs. (3.14) and (3.17):

$$V_2 = \frac{V}{2} + \left(-V_2 - \frac{V}{2} \right) e^{-T/2\tau} \quad V_2 \left(1 + e^{-T/2\tau} \right) = \frac{V}{2} \left(1 - e^{-T/2\tau} \right)$$

$$V_2 = \frac{V}{2} \frac{(1 - e^{-T/2\tau})}{(1 + e^{-T/2\tau})} \quad (3.18)$$

$$\therefore V_2 = \frac{V}{2} \tanh \frac{T}{4\tau} \quad (3.19)$$

Using Eqs. (3.17) and (3.19), it is possible to calculate V_2 and V_1 and plot the output waveforms as given in Figs. 3.7(c) and (d), respectively.

If $\tau \ll T$, then the wave shape is maintained. And if $\tau \gg T$, the wave shape is highly distorted, but the output of the low-pass circuit is now a triangular wave. So it is possible to derive a triangular wave from a square wave by choosing τ to be very large when compared to $T/2$ of the symmetric square wave. Let us consider an example.

EXAMPLE

Example 3.3: A symmetric square wave, whose peak-to-peak amplitude is 4 V and whose average value is zero is applied to a low-pass RC circuit shown in Fig. 3.1(a). The time constant equals the half-period of the square wave. Find the peak-to-peak output voltage of waveform.

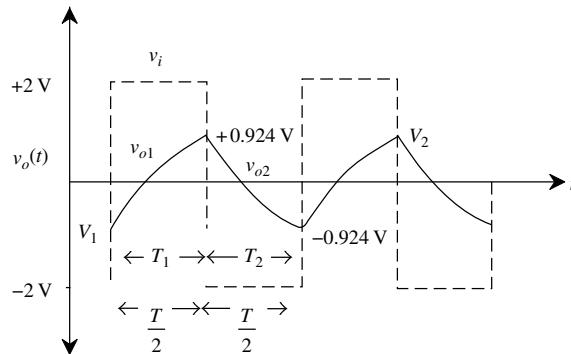


FIGURE 3.8 The input and output waveforms at $RC = T/2$

Solution: As the input is a symmetric square wave, we have:

$$T_1 = T_2 = \frac{T}{2}, \quad V_1 = -V_2 \quad \text{and} \quad V' = V'' = \frac{V}{2} \quad v_{o1} = V' + (V_1 - V') e^{-t/\tau}$$

At $t = T_1$:

$$V_2 = V' + (V_1 - V') e^{-T_1/\tau} = \frac{V}{2} + \left(-V_2 - \frac{V}{2}\right) e^{-(T/2)(2/T)}$$

where $\tau = T/2$.

$$V_2 = \frac{4}{2} + \left(-V_2 - \frac{4}{2}\right) e^{-1} = 2 + (-V_2 - 2)e^{-1} = 2 - 0.368 V_2 - 0.736 = 0.924 V$$

The peak-to-peak output voltage = $2 \times 0.924 = 1.848$ V. V_2 can also directly be calculated using Eq. 3.19.

The input and output are plotted as shown in Fig. 3.8.

EXAMPLE

Example 3.4: The periodic waveform applied to an RC low-pass circuit in Fig. 3.1(a), is a square wave with $T_1 = 0.1$ s, $T_2 = 0.2$ s and time constant $= 0.1$ s, [see Fig. 3.9(a)]. Calculate the output voltages and draw the output waveform.

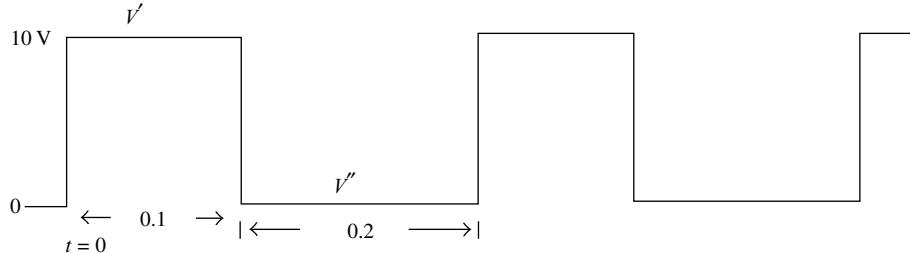


FIGURE 3.9(a) The given input waveform

Solution: The capacitor charges and discharges to the same level for each cycle.

$$RC = \tau = 0.1 \text{ s}, \quad T_1 = 0.1 \text{ s}, \quad T_2 = 0.2 \text{ s}$$

At $0 < t < 0.1$ s, $v_f = V' = 10 \text{ V}$ and $v_i = V_2$

$$v_{o1} = 10 - (10 - V_2)e^{-t/\tau}$$

At $t = 0.1$ s:

$$v_{o1} = V_1 = 10 - (10 - V_2)e^{-0.1/0.1} = 10 - (10 - V_2)0.368$$

$$V_1 = 6.32 + 0.368V_2 \quad (1)$$

For $0.1 < t < 0.3$ s, $v_f = V'' = 0 \text{ V}$ and $v_i = V_1$

$$v_{o2} = 0 - (0 - V_1)e^{-(t-0.1)/\tau}$$

At $t = 0.3$ s:

$$v_{o2} = V_2 = 0 - (0 - V_1)e^{-0.2/0.1} = 0 - (0 - V_1)0.135$$

$$V_2 = 0.135V_1 \quad (2)$$

Substitute Eq. (2) in Eq. (1) to get the values of V_1 :

$$V_1 = 6.32 + 0.368 \times 0.135V_1 \quad V_1(1 - 0.05) = 6.32 \quad 0.95V_1 = 6.32 \quad V_1 = 6.65 \text{ V}$$

From Eq.(2),

$$V_2 = 0.135 \times 6.65 = 0.898 \text{ V}$$

The input and output waveforms are plotted in Fig. 3.9(b).

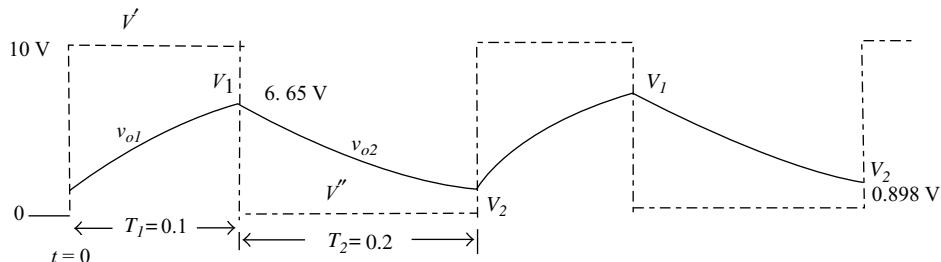


FIGURE 3.9(b) The input and output waveforms of the low-pass circuit

3.2.5 The Response of a Low-pass RC Circuit to Exponential Input

An exponential input, as shown in Fig. 3.10, is applied to the low-pass circuit in Fig. 3.1(a). The input waveform is described by the equation:

$$v_i = V(1 - e^{-t/\tau_1}) \quad (3.20)$$

where τ_1 is the time constant of the circuit that generated this exponential signal. For the low-pass circuit, we have:

$$v_i = \tau \frac{dv_o}{dt} + v_o \quad (3.21)$$

Using Eq.(3.20):

$$\begin{aligned} V(1 - e^{-t/\tau_1}) &= \tau \frac{dv_o}{dt} + v_o \\ V - Ve^{-t/\tau_1} &= \tau \frac{dv_o}{dt} + v_o \end{aligned} \quad (3.22)$$

Case 1: When $\tau \neq \tau_1$

Applying Laplace transforms:

$$\frac{V}{s} - \frac{V}{\left(s + \frac{1}{\tau_1}\right)} = s\tau v_o(s) + v_o(s) = v_o(s)(1 + s\tau) = v_o(s)\tau \left(s + \frac{1}{\tau}\right)$$

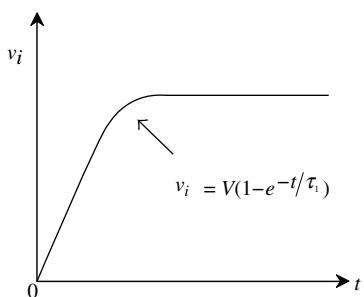
Therefore,

$$v_o(s) = \frac{\frac{V}{\tau}}{s\left(s + \frac{1}{\tau}\right)} - \frac{\frac{V}{\tau}}{\left(s + \frac{1}{\tau}\right)\left(s + \frac{1}{\tau_1}\right)} \quad (3.23)$$

Let

$$X = \frac{\frac{V}{\tau}}{s\left(s + \frac{1}{\tau}\right)} \quad \text{and} \quad Y = \frac{\frac{V}{\tau}}{\left(s + \frac{1}{\tau}\right)\left(s + \frac{1}{\tau_1}\right)}$$

Resolving X into partial fractions:



$$\frac{\frac{V}{\tau}}{s\left(s + \frac{1}{\tau}\right)} = \frac{A}{s} + \frac{B}{\left(s + \frac{1}{\tau}\right)}$$

Therefore,

$$\frac{V}{\tau} = A(s + 1/\tau) + Bs$$

Putting $s = 0, A = V$

Putting $s = -1/\tau, B = -V$

Therefore,

$$X = \frac{V}{s} - \frac{V}{\left(s + \frac{1}{\tau}\right)} \quad (3.24)$$

FIGURE 3.10 The exponential input applied

Resolving Y into partial fractions:

$$\frac{\frac{V}{\tau}}{\left(s + \frac{1}{\tau}\right)\left(s + \frac{1}{\tau_1}\right)} = \frac{C}{\left(s + \frac{1}{\tau}\right)} + \frac{D}{\left(s + \frac{1}{\tau_1}\right)} \quad \frac{V}{\tau} = C\left(s + \frac{1}{\tau}\right) + D\left(s + \frac{1}{\tau_1}\right)$$

Putting $s = -1/\tau$

$$\frac{V}{\tau} = D\left(-\frac{1}{\tau} + \frac{1}{\tau_1}\right) \quad V = D\left(\frac{\tau}{\tau_1} - 1\right) \quad D = \frac{V}{\left(\frac{\tau}{\tau_1} - 1\right)}$$

and

$$C = -\frac{V}{\left(\frac{\tau}{\tau_1} - 1\right)}$$

Therefore,

$$Y = \frac{\frac{V}{\left(\frac{\tau}{\tau_1} - 1\right)}}{\left(s + \frac{1}{\tau}\right)} - \frac{\frac{V}{\left(\frac{\tau}{\tau_1} - 1\right)}}{\left(s + \frac{1}{\tau_1}\right)} \quad (3.25)$$

Hence,

$$v_o(s) = \frac{V}{s} - \frac{V}{\left(s + \frac{1}{\tau}\right)} - \frac{\frac{V}{\left(\frac{\tau}{\tau_1} - 1\right)}}{\left(s + \frac{1}{\tau}\right)} + \frac{\frac{V}{\left(\frac{\tau}{\tau_1} - 1\right)}}{\left(s + \frac{1}{\tau_1}\right)} \quad (3.26)$$

Taking the Laplace inverse, the solution of the differential Eq. (3.26) is:

$$v_o(t) = V - Ve^{-t/\tau} - \frac{V}{\left(\frac{\tau}{\tau_1} - 1\right)}e^{-t/\tau} + \frac{V}{\left(\frac{\tau}{\tau_1} - 1\right)}e^{-t/\tau_1}$$

$$v_o(t) = V - Ve^{-t/\tau} \left[\frac{\frac{\tau}{\tau_1}}{\left(\frac{\tau}{\tau_1} - 1\right)} \right] + \frac{V}{\left(\frac{\tau}{\tau_1} - 1\right)}e^{-t/\tau_1} \quad (3.27)$$

$$\text{Let } n = \frac{\tau}{\tau_1} \quad \text{and} \quad x = \frac{t}{\tau_1} \quad (3.28)$$

$$v_o(t) = V \left[1 - \frac{n}{(n-1)}e^{-x/n} + \frac{e^{-x}}{(n-1)} \right] \quad (3.29)$$

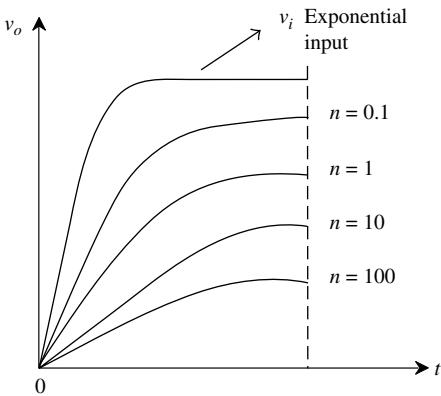


FIGURE 3.11 The input and output of a low-pass RC circuit

much the output deviates. Figure 3.11 shows the deviation of the output for different values of n ($= \tau/\tau_1$).

Now let t_{r1} be the rise time of the exponential input $t_{r1} = 2.2\tau_1$ [using Eq. (3.11)], and let t_{r2} be the rise time of the low-pass circuit $t_{r2} = 2.2\tau$. Thus, the rise time of the output t_r is given approximately as:

$$t_r = 1.05 \sqrt{t_{r1}^2 + t_{r2}^2} = 1.05 \left\{ t_{r1}^2 \left(1 + \frac{t_{r2}^2}{t_{r1}^2} \right) \right\}^{1/2} = 1.05 t_{r1} \sqrt{1 + \eta^2} \quad (3.31)$$

where, $\eta = t_{r2}/t_{r1}$. If t_{r1} and t_{r2} are the rise times of the circuit that has generated the exponential input and of the low-pass circuit respectively, then Eq. (3.31) gives the rise time of the output of the low-pass circuit. Let us consider Example 3.5.

E X A M P L E

Example 3.5: An exponential input of $10(1 - e^{-t/10 \times 10^{-3}})$ Volts is applied to a low-pass RC circuit in Fig. 3.1(a). Plot the response for (i) $RC = 10$ ms and (ii) $RC = 20$ ms.

Solution:

Case 1: $\tau = 10$ ms and τ_1 as specified is $\tau_1 = \tau = 10$ ms

When the time constant of both input and the low-pass RC circuit are equal ($n = 1$), the output voltage is:

$$v_o(t) = V [1 - (1 + x)e^{-x}] = 10 \left[1 - \left(1 + \frac{t}{\tau} \right) e^{-t/\tau} \right]$$

The output is calculated for different values of τ and is presented in Table 3.2.

Case 2: $\tau = 20$ ms

When the time constant of input, τ_1 and that of a low-pass circuit, τ are not equal ($n = 2$) the output voltage is:

$$v_o(t) = V \left[1 - \frac{1}{(1-n)} e^{-x} - \frac{n}{(n-1)} e^{-x/n} \right] = 10 \left[1 - \frac{1}{(1-2)} e^{-t/\tau_1} - \frac{2}{(2-1)} e^{-t/\tau} \right]$$

Similarly, repeating for the case $\tau = \tau_1$.

Case 2: When $\tau = \tau_1$

$$v_o(s) = \frac{V}{s} - \frac{V}{\left(s + \frac{1}{\tau} \right)} - \frac{\frac{V}{\tau}}{\left(s + \frac{1}{\tau} \right)^2}$$

$$v_o(t) = V [1 - (1 + x)e^{-x}] \quad (3.30)$$

- (i) Here, if $\tau \leq \tau_1$, the output is similar to the input.
- (ii) If $\tau > \tau_1$, then the output deviates from the input.

The choice of τ depends on the requirement. If τ is small, the distortion is negligible. However, if τ is decided by the circuit components at the input of an amplifier—over which there is no control—we can only predict as to how

much the output deviates. Figure 3.11 shows the deviation of the output for different values of n ($= \tau/\tau_1$).

TABLE 3.2 The output of a low-pass circuit for different values of t when $n = 1$ (i.e. $\tau = \tau_1 = 10$ ms)

t (ms)	$v_i = 10(1 - e^{-t/\tau_1})$ (V)	$10 \left[1 - \left(1 + \frac{t}{\tau}\right) e^{-t/\tau} \right]$ (V)
0	0	0
1	0.952	0.046
2	1.81	0.175
4	3.3	0.615
5	3.93	0.90
6	4.51	1.22
10	6.32	2.642
20	8.647	5.94
40	9.82	9.08
100	10	9.995

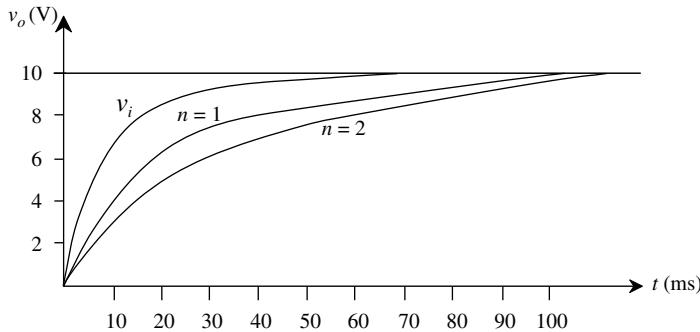
$$v_o(t) = 10 \left[1 + e^{-t/\tau_1} - 2e^{-t/\tau} \right]$$

The output for $n = 2$ is presented in Table 3.3

The output when $n = 2$ is presented in Table 3.3. The waveforms for case 1 ($n = 1$) and case 2 ($n = 2$) are shown in Fig. (3.12).

TABLE 3.3 The output of a low-pass circuit when $n = 2$ (i.e. $\tau_1 = 10$ ms and $\tau = 20$ ms)

t (ms)	$v_i = 10(1 - e^{-t/\tau_1})$ (V)	$v_o(t) = 10[1 + e^{-t/\tau_1} - 2e^{-t/\tau}]$ (V)
0	0	0
1	0.952	0.024
2	1.8	0.09
4	3.3	0.328
6	4.51	0.671
8	5.51	1.09
10	6.32	1.55
15	7.77	2.78
20	8.647	3.99
25	9.18	5.1
30	9.50	6.03
35	9.7	6.826
40	9.82	7.474
45	9.89	8.002
50	9.93	8.42
60	9.97	9.07
70	9.99	9.40
80	10	9.64
90	10	9.78
100	10	10

FIGURE 3.12 The response of the low-pass circuit for $n = 1$ and for $n = 2$

3.2.6 The Response of a Low-pass RC Circuit to Ramp Input

The ramp input signal is described by the relation $v_i = \alpha t$. We have from Eq. (3.21) that $v_i = \tau (dv_o/dt) + v_o$.

Therefore,

$$\alpha t = \tau \frac{dv_o}{dt} + v_o \quad (3.32)$$

Applying Laplace transforms:

$$\begin{aligned} \frac{\alpha}{s^2} &= v_o(s) (1 + s\tau) \\ \frac{\alpha}{s^2} &= v_o(s) \tau \left(s + \frac{1}{\tau} \right) \quad \text{or} \quad v_o(s) = \frac{\alpha}{s^2 \left(s + \frac{1}{\tau} \right) \tau} = \frac{\frac{\alpha}{\tau}}{s^2 \left(s + \frac{1}{\tau} \right)} \end{aligned}$$

Resolving into partial fractions and solving:

$$\frac{\alpha}{s^2 \left(s + \frac{1}{\tau} \right)} = \frac{A}{s} + \frac{B}{s^2} + \frac{C}{\left(s + \frac{1}{\tau} \right)} \quad (3.33)$$

$$\frac{\alpha}{\tau} = As \left(s + \frac{1}{\tau} \right) + B \left(s + \frac{1}{\tau} \right) + Cs^2 \quad (3.34)$$

Put $s = 0, B = \alpha$

Put $s = -1/\tau, C = \alpha\tau$

To get the value of A , from Eq. (3.34):

$$\frac{\alpha}{\tau} = As^2 + \frac{As}{\tau} + Bs + \frac{B}{\tau} + Cs^2 \quad \frac{\alpha}{\tau} = (A + C)s^2 + \left(\frac{A}{\tau} + B \right)s + \frac{B}{\tau}$$

Equating the coefficients of s^2 on both sides:

$$A + C = 0$$

Therefore, $A = -C$. As $C = \alpha\tau, A = -\alpha\tau$.

Substituting the values of A , B and C :

$$v_o(s) = \frac{-\alpha\tau}{s} + \frac{\alpha}{s^2} + \frac{\alpha\tau}{\left(s + \frac{1}{\tau}\right)}$$

Taking the Laplace inverse:

$$v_o(t) = -\alpha\tau + \alpha t + \alpha\tau e^{-t/\tau} \quad (3.35)$$

$$v_o(t) = \alpha \left[t - \tau (1 - e^{-t/\tau}) \right] \quad (3.36)$$

At $t = T$:

$$v_o(T) = \alpha \left[T - \tau \left(1 - e^{-T/\tau} \right) \right] \quad (3.37)$$

Case 1: If $\tau \ll T$, then the deviation of the output from the input is very small since $e^{-T/\tau} \approx 0$.

$$v_o(t) = \alpha(T - \tau) \quad (3.38)$$

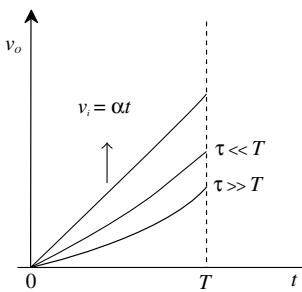
Case 2: If $\tau \gg T$, then $e^{-T/\tau}$ can be expanded as series. The response is plotted in Fig. 3.13.

$$\begin{aligned} v_o(t) &= \alpha \left[T - \tau \left(\frac{T}{\tau} - \frac{T^2}{2\tau^2} \right) \right] \\ &= \alpha \left[T - T + \frac{T^2}{2\tau} \right] = \frac{\alpha T^2}{2\tau} \end{aligned} \quad (3.39)$$

The response is plotted in Fig. 3.13. When a ramp is applied as input to a low-pass circuit, the output deviates from the input. The transmission error, e_t , is calculated as:

$$e_t = \frac{v_i - v_o}{v_i} = \frac{\alpha T - \alpha(T - \tau)}{\alpha T}$$

$$e_t = \frac{\tau}{T} \quad (3.40)$$



$$f_2 = \frac{1}{2\pi\tau} \quad \tau = \frac{1}{2\pi f_2}$$

Therefore,

$$e_t = \frac{1}{2\pi f_2} \times \frac{1}{T} \quad (3.41)$$

FIGURE 3.13 The response of a low-pass circuit to a ramp input

Transmission error defines deviation from linearity. Thus, the smaller the value of e_t , the more linear the output. Let us consider an Example 3.6.

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Example 3.6: A limited ramp, shown Fig. 3.14(a) (the pulse rises linearly and reaches V at T and remains at V beyond T), is applied to the low-pass RC circuit in Fig. 3.1(a). Plot the output waveforms when (a) $T = \tau$, (b) $T = 0.3\tau$ and (c) $T = 6\tau$.

Solution: For a low-pass circuit, $v_o(t) = \alpha(t - \tau) + \alpha \tau e^{-t/\tau}$, where $\alpha = V/\tau$.

$$\text{At } t = T, v_o(T) = \alpha(T - \tau) + \alpha \tau e^{-T/\tau}$$

(i) $T = \tau$

$$v_o(T) = \alpha(\tau - \tau) + \alpha \tau e^{-\tau/\tau} = \alpha \tau e^{-1}$$

$$v_o(T) = \frac{V}{\tau} \tau \times 0.368 = 0.368V$$

Beyond T , the output varies exponentially and reaches V

The output is as shown in Fig. 3.14(b).

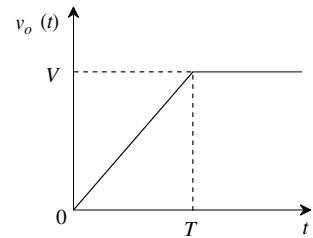


FIGURE 3.14(a) The given input waveform

(ii) $T = 0.3\tau$

$$v_o(T) = \alpha(0.3\tau - \tau) + \alpha \tau e^{-0.3\tau/\tau}$$

$$\begin{aligned} &= \frac{V}{0.3\tau}(-0.7\tau) + \frac{V}{0.3\tau}\tau e^{-0.3} \\ &= \frac{-0.7}{0.3}V + \frac{0.74}{0.3}V \end{aligned}$$

$$v_o(T) = 0.133V$$

The output is as shown in Fig. 3.14(c).

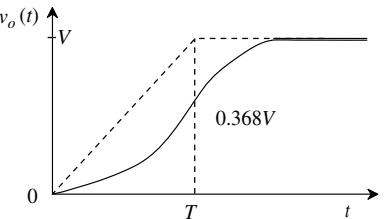


FIGURE 3.14(b) The output waveform for $T = \tau$

(iii) $T = 6\tau$

$$v_o(T) = \alpha(6\tau - \tau) + \alpha \tau e^{-6\tau/\tau}$$

$$= \frac{V}{6\tau}(5\tau) + \frac{V}{6\tau}\tau e^{-6}$$

$$v_o(T) = 0.833V$$

The output is as in Fig. 3.14(d).

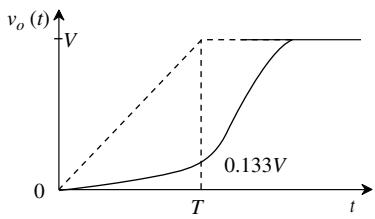


FIGURE 3.14(c) The output waveform for $T = 0.3\tau$

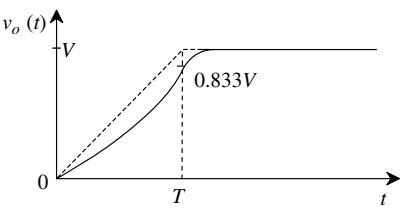


FIGURE 3.14(d) The output waveform for $T = 6\tau$

3.2.7 A Low-pass RC Circuit as an Integrator

For the low-pass RC circuit in Fig. 3.1(a) to behave as an integrator, $\tau \gg T$. For T to be small when compared to τ , the frequency has to be high. At high frequencies, X_C is very small when compared to R . Therefore, the voltage drop across R is very large when compared to the drop across C . Hence, $v_i \cong iR$.

$$v_i = iR + \frac{1}{C} \int i \, dt$$

Since,

$$\frac{1}{C} \int i \, dt \ll iR \quad \text{and} \quad v_i \cong iR \quad i = \frac{v_i}{R}$$

Therefore,

$$v_o = \frac{1}{C} \int i \, dt = \frac{1}{RC} \int v_i \, dt = \frac{1}{\tau} \int v_i \, dt \quad (3.42)$$

The output is proportional to the integral of the input signal. Hence, a low-pass circuit with a large time constant produces an output that is proportional to the integral of the input. If the input to the circuit is $v_i(t) = V_m \sin \omega t$, From Eq. (3.42):

$$v_o(t) \approx \omega_2 \int_0^t V_m \sin \omega t \, dt \quad v_o(t) \approx -V_m \frac{\omega_2}{\omega} \cos \omega t$$

where $\omega_2 = 1/RC = 1/\tau$. For the low-pass circuit, we know:

$$\left| \frac{v_o}{v_i} \right| = \frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega_2} \right)^2}}.$$

The phase shift θ is given by:

$$\theta = \tan^{-1}(\omega/\omega_2)$$

When $\theta = 90^\circ$, the sine function at the input becomes a cosine function at the output, as is required in an integrator. When $\omega/\omega_2 = 100$, $\theta = 89.4^\circ$ which is nearly equal to 90° . Hence, only when $RC \gg T$, a low-pass RC circuit behaves as a good integrator and the output is a sinusoidally varying signal if the input is a sine wave. For a low-pass circuit, to behave as a reasonably good integrator, $\omega/\omega_2 \geq 20$.

3.2.8 An Op-amp as an Integrator

Let us now consider an op-amp integrator [see Fig. 3.15(a)]. From Eqs. (1.57) and (1.58) (Miller's theorem), we have:

$$Z_1 = \frac{Z'}{1 - A} \quad \text{and} \quad Z_2 = \frac{Z'A}{A - 1}$$

where A is the gain of the amplifier. If the capacitance C appears between the input and output terminals of the op-amp as shown in Fig. 3.15(a), then using Miller's theorem, C can be replaced by Z_1 and Z_2 .

$$Z' = X_C \quad Z_1 = \frac{Z'}{1 - A} = \frac{X_C}{1 - A} = \frac{1}{\omega C(1 - A)}$$

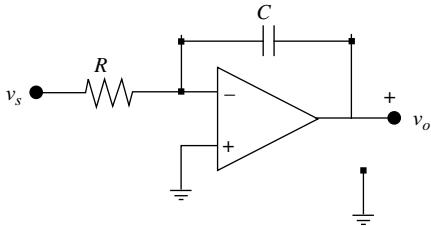


FIGURE 3.15(a) An op-amp as an integrator

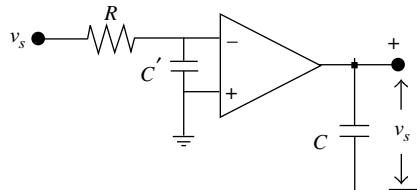


FIGURE 3.15(b) The op-amp integrator circuit using Miller's theorem

$$X'_c = \frac{1}{\omega C'} \quad \text{where } C' = C(1 - A)$$

$$Z_2 = \frac{Z'A}{A-1} = \frac{X_C A}{A-1} = \frac{1.A}{\omega C(A-1)} = \frac{1}{\omega C \left(1 - \frac{1}{A}\right)}$$

$$X''_C = 1/\omega C'' \text{ where } C'' = (1 - 1/A)C \approx C \text{ since } A \text{ is large.}$$

Hence, the integrator circuit is redrawn as shown in Fig. 3.15(b).

At the input of the amplifier, there appears a very large value of C' , which is called the Miller effect capacitor, resulting in a large value of τ , even while using a normal value of C .

Whereas in the case of a simple RC integrator, the physical value of C has to be very large to make τ large. An op-amp integrator is, therefore, a better integrator when compared to a simple RC integrator.

3.2.9 Low-pass RL Circuits

Consider the low-pass RL circuit in Fig. 3.1(b). For this low-pass circuit, $v_o = R/L \int v_i dt$. This circuit can also be used as an integrator when the time constant $L/R \gg T$. The major limitations of high-pass and low-pass RL circuits are:

- 1) For a large value of inductance, an iron-cored inductor has to be used. As such it is bulky and occupies more space.
- 2) Inductors are more lossy elements, when compared to capacitors. So, it is possible to get ideal capacitors, but not ideal inductors.

3.3 ATTENUATORS

An attenuator is a circuit that reduces the amplitude of the signal by a finite amount. A simple resistance attenuator is represented in Fig. 3.16. The output of the attenuator shown in Fig. 3.16 is given by the relation:

$$v_o = v_i \times \frac{R_2}{R_1 + R_2} = \alpha v_i$$

From this equation, it is evident that the output is smaller than the input, which is the main purpose of an attenuator—to reduce the amplitude of the signal. Attenuators are used when the signal amplitude is very large. Let us measure a voltage, say, 5000 V, using a CRO; such a large voltage may not be handled by the

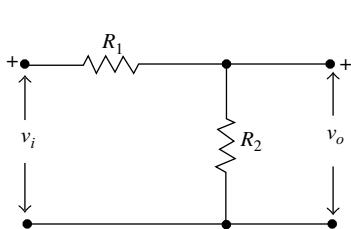


FIGURE 3.16 A resistance attenuator

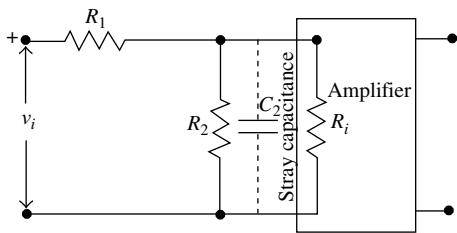


FIGURE 3.17(a) The attenuator output connected to amplifier input

amplifier in a CRO. Therefore, to be able to measure such a voltage we first attenuate the voltage by a known amount, say by a factor of 10 ($\alpha = 0.1$), so that the voltage that is actually connected to the CRO is only 500 V. The output of the attenuator is thus reduced depending on the choice of R_1 and R_2 .

3.3.1 Uncompensated Attenuators

If the output of an attenuator is connected as input to an amplifier with a stray capacitance C_2 and input resistance R_i , as shown in Fig. 3.17(a).

Consider the parallel combination of R_2 and R_i . If the amplifier input is not to load the attenuator output, then R_i should always be significantly greater than R_2 . The attenuator circuit is now shown in Fig. 3.17(b).

Reducing the two-loop network into a single-loop network by Thévenizing:

$$V_{Th} = v_i \times \frac{R_2}{R_1 + R_2} = \alpha v_i \quad \text{where} \quad \alpha = \frac{R_2}{R_1 + R_2}$$

and

$$R_{th} = R_1 \parallel R_2$$

Hence, the circuit in Fig. 3.17(b) reduces to that shown in Fig. 3.17(c).

When the input αv_i is applied to this low-pass RC circuit, the output will not reach the steady-state value instantaneously. If, for the above circuit, $R_1 = R_2 = 1 \text{ M}\Omega$ and $C_2 = 20 \text{ nF}$, the rise time is:

$$t_r = 2.2 R_{th} C_2 = 2.2 \times 0.5 \times 10^6 \times 20 \times 10^{-9}$$

$$t_r = 22 \text{ ms}$$

This means that after a time interval of approximately 22 ms after the application of the input αv_i to the circuit, the output reaches the steady-state value. This is an abnormally long delay. An attenuator of this type is called an uncompensated attenuator, i.e., its output is dependent on frequency.

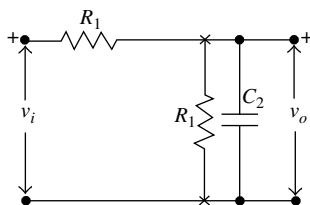


FIGURE 3.17(b) The attenuator, considering the stray capacitance at the amplifier input

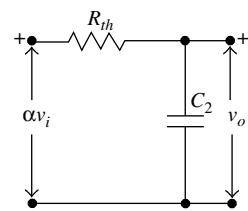


FIGURE 3.17(c) An uncompensated attenuator

3.3.2 Compensated Attenuators

To make the response of the attenuator independent of frequency, the capacitor C_1 is connected across R_1 . This attenuator now is called a compensated attenuator shown in Fig. 3.18(a). This circuit in Fig. 3.18(a) is redrawn as shown in Fig. 3.18(b).

In Figs. 3.18(a) and (b), R_1 , R_2 , C_1 , C_2 form the four arms of the bridge. The bridge is said to be balanced when $R_1C_1 = R_2C_2$, in which case no current flows in the branch xy . Hence, for the purpose of computing the output, the branch xy is omitted. The resultant circuit is shown in Fig. 3.18(c).

When a step voltage with $v_i = V$ is applied as an input, the output is calculated as follows: At $t = 0+$, the capacitors do not allow any sudden changes in the voltage; as the input changes, the output should also change abruptly, depending on the values of C_1 and C_2 .

$$v_o(0^+) = V \frac{C_1}{C_1 + C_2} \quad (3.43)$$

Thus, the initial output voltage is determined by C_1 and C_2 . As $t \rightarrow \infty$, the capacitors are fully charged and they behave as open circuits for dc. Hence, the resultant output is:

$$v_o(\infty) = V \frac{R_2}{R_1 + R_2} \quad (3.44)$$

Perfect compensation is obtained if, $v_o(0^+) = v_o(\infty)$. From this using Eqs. 3.43 and 3.44 we get:

$$\frac{C_1}{C_1 + C_2} V = V \frac{R_2}{R_1 + R_2} \quad (3.45)$$

and the output is αv_i .

$$C_1 R_1 = C_2 R_2 \quad \text{or}$$

$$C_1 = (R_2/R_1)C_2 = C_p \quad (3.46)$$

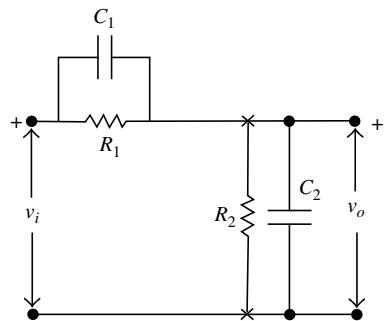


FIGURE 3.18(a) A compensated attenuator

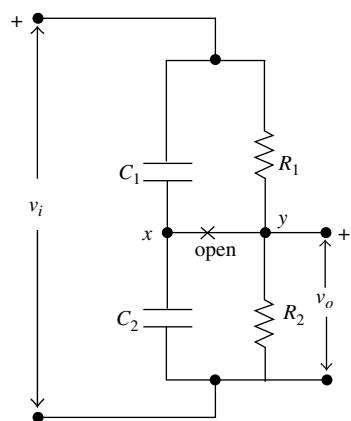


FIGURE 3.18(b) Redrawn circuit of Fig 3.18(a)

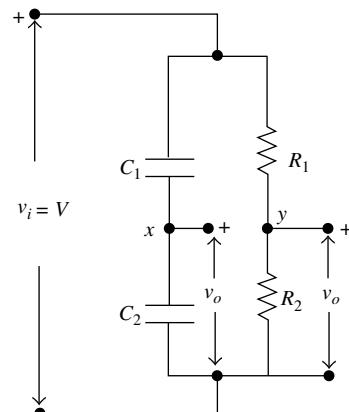


FIGURE 3.18(c) The compensated attenuator open-circuiting the xy branch

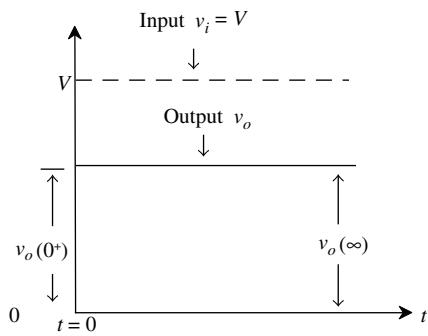


FIGURE 3.19(a) A perfectly compensated attenuator ($C_1 = C_2$)

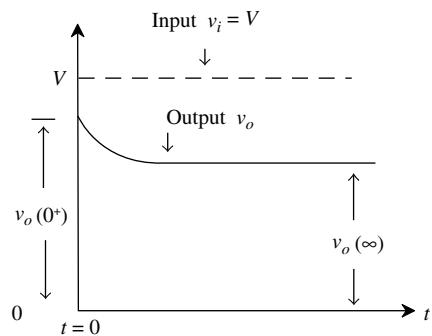


FIGURE 3.19(b) An over-compensated attenuator ($C_1 > C_2$)

Let us consider the following circuit conditions:

- When $C_1 = C_p$, the attenuator is a perfectly compensated attenuator.
- When $C_1 > C_p$, it is an over-compensated attenuator.
- When $C_1 < C_p$, it is an under-compensated attenuator.

The response of the attenuator to a step input under these three conditions is shown in Figs. 3.19(a), (b) and (c), respectively.

In the attenuator circuit, as at $t = 0+$, the capacitors C_1 and C_2 behave as short circuits, the current must be infinity. But impulse response is impossible as the generator, in practice, has a finite source resistance, not ideally zero. Now consider the compensated attenuator with source resistance R_s [see Fig. 3.19(d)].

If the xy loop is open for a balanced bridge, Thévenizing the circuit, the Thévenin voltage source and its internal resistance v_i' and R' are calculated using Fig. 3.19(e).

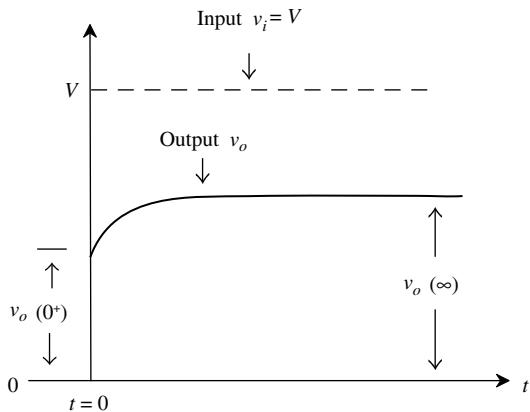


FIGURE 3.19(c) An under-compensated attenuator ($C_1 < C_2$)

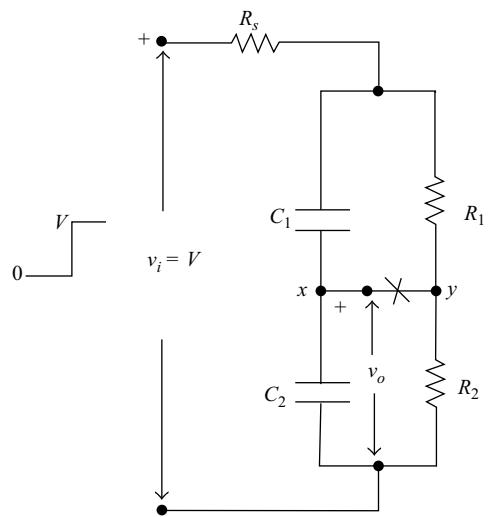


FIGURE 3.19(d) The attenuator taking the source resistance into account

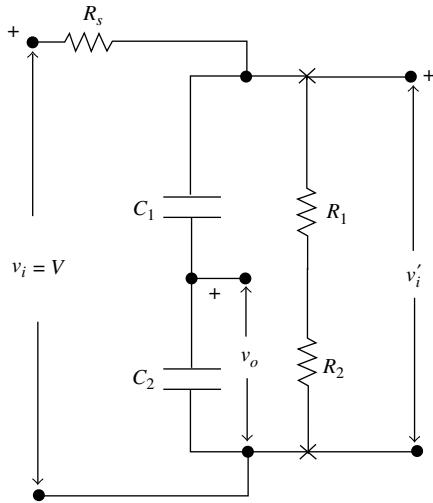


FIGURE 3.19(e) The circuit used to calculate the Thévenin voltage source and its internal resistance

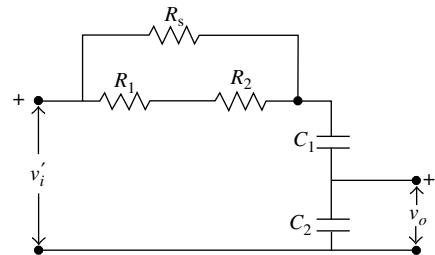


FIGURE 3.19(f) Redrawn circuit of Fig. 3.19(e)

The value of Thévenin voltage source is:

$$v'_i = \frac{v_i(R_1 + R_2)}{R_s + R_1 + R_2}$$

and its internal resistance is:

$$R' = \frac{R_s(R_1 + R_2)}{R_s + R_1 + R_2}$$

The above circuit now reduces to that shown in Fig. 3.19(f). Usually $R_s \ll (R_1 + R_2)$, hence, $R_s \parallel (R_1 + R_2) \approx R_s$. Thus the circuit in Fig. 3.19(f) reduces to that shown in Fig. 3.19(g).

This is a low-pass circuit with time constant $\tau_s = R_s C_s$, where C_s is the series combination of C_1 and C_2 ; $C_s = C_1 C_2 / (C_1 + C_2)$. The output of the attenuator is an exponential with time constant τ_s ; and if τ_s is small, the output almost follows the input. Alternately, consider the situation when a step voltage V from a source having R_s as its internal resistance, is connected to a circuit which has C_2 between its output terminals, [see Fig. 3.19(h)].

This being a low-pass circuit (can also be termed as an uncompensated attenuator), with time constant $\tau = R_s C_2$, its output will be an exponential with rise time t_r , where

$$t_r = 2.2 \tau = 2.2 R_s C_2. \quad (3.47)$$

Now consider the compensated attenuator, shown in Fig. 3.19(g), where the internal resistance of the source R_s is taken into account. The time constant of this circuit is $\tau_s (= R_s C_s)$ and the rise time τ'_r is:

$$\tau'_r = 2.2 R_s C_s \text{ where } C_s = C_1 C_2 / (C_1 + C_2)$$

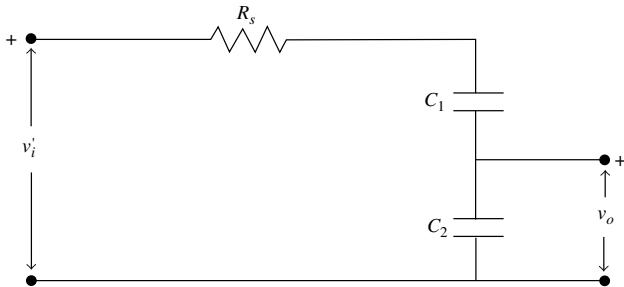


FIGURE 3.19(g) The final reduced circuit of a compensated attenuator

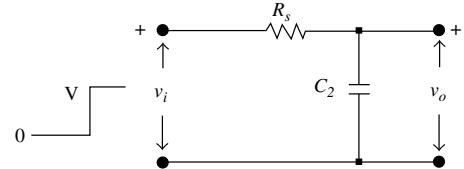


FIGURE 3.19(h) A low-pass circuit (uncompensated attenuator)

$$t'_r = 2.2 \frac{R_s C_1 C_2}{C_1 + C_2} \quad (3.48)$$

From Eqs. (3.47) and (3.48):

$$(t'_r/t_r) = [C_1/(C_1 + C_2)] = \alpha$$

where α is the attenuation constant, which tells us by what amount the signal is reduced at the output.

$$t'_r = \alpha t_r \quad (3.49)$$

If $\alpha = 0.5$:

$$t'_r = 0.5 t_r \quad (3.50)$$

From Eq. (3.50), it is seen that the output signal from a compensated attenuator has a negligible rise time when compared to the output signal from an un-compensated attenuator. It means that the step voltage, V is more faithfully reproduced at the output of a compensated attenuator, which is its main advantage.

A perfectly compensated attenuator is sometimes used to reduce the signal amplitude when the signal is connected to a CRO to display a waveform. A typical CRO probe may be represented as in Fig. 3.20. Example 3.7 helps to further elucidate and elaborate the functioning of the attenuator circuit.

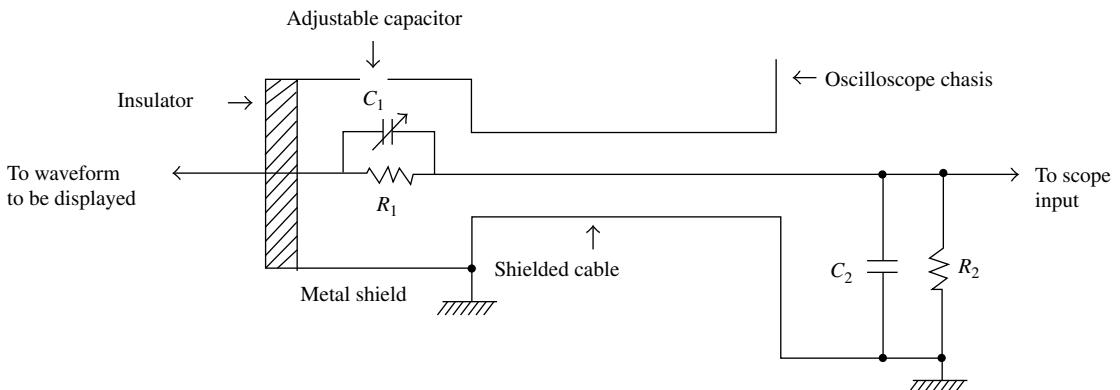


FIGURE 3.20 A typical CRO probe

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Example 3.7: Calculate the output voltages and draw the waveforms when (a) $C_1 = 75 \text{ pF}$, (b) $C_1 = 100 \text{ pF}$, (c) $C_1 = 50 \text{ pF}$ for the circuit shown in Fig. 3.21(a). The input step voltage is 50 V.

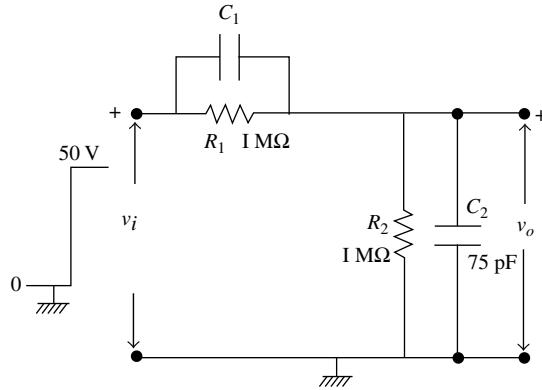


FIGURE 3.21(a) The given attenuator circuit

Solution: For perfect compensation, $R_1 C_1 = R_2 C_2$. Here $R_1 = R_2$.

(a) When $C_1 = 75 \text{ pF}$, then the attenuator is perfectly compensated. The rise time of the output waveform is zero.

$$\text{Attenuation, } \alpha = \frac{R_2}{R_1 + R_2} = \frac{1}{1+1} = 0.5$$

$$v_o(0+) = v_o(\infty) = \alpha v_i = 0.5 \times 50 = 25 \text{ V}$$

(b) When $C_1 = 100 \text{ pF}$, then the attenuator is over-compensated, hence $v_o(0^+) > v_o(\infty)$.

The output at $t = 0^+$,

$$v_o(0+) = v_i \times \frac{C_1}{C_1 + C_2} = 50 \times \frac{100}{100 + 75} = 28.6 \text{ V}$$

The output at $t = \infty$,

$$v_o(\infty) = v_i \times \frac{R_2}{R_1 + R_2} = 50 \times \frac{1}{1+1} = 25 \text{ V}$$

From Fig. 3.21(b):

$$R = \frac{R_1 R_2}{R_1 + R_2} \quad \text{and} \quad C = C_1 + C_2$$

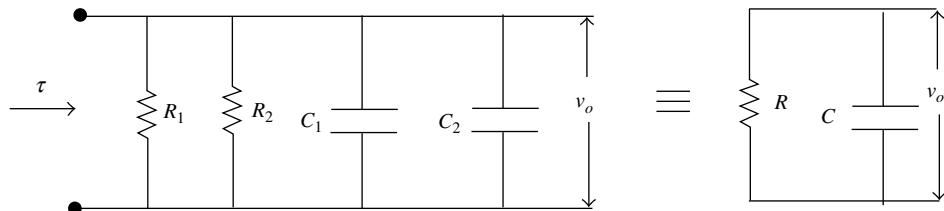


FIGURE 3.21(b) The equivalent circuit to get the time constant for the decay of the overshoot

Time constant τ_1 with which the overshoot at $t = 0^+$ decays to the steady-state value is:

$$\tau_1 = \frac{R_1 R_2}{R_1 + R_2} (C_1 + C_2) = \frac{1 \times 1}{1 + 1} \times 10^6 \times (100 + 75) \times 10^{-12} = 87.5 \mu\text{s}$$

Fall time $t_f = 2.2 \tau_1 = 2.2 \times 87.5 \times 10^{-6} = 192.5 \mu\text{s}$

(c) When $C_1 = 50 \text{ pF}$, then the attenuator is under-compensated.

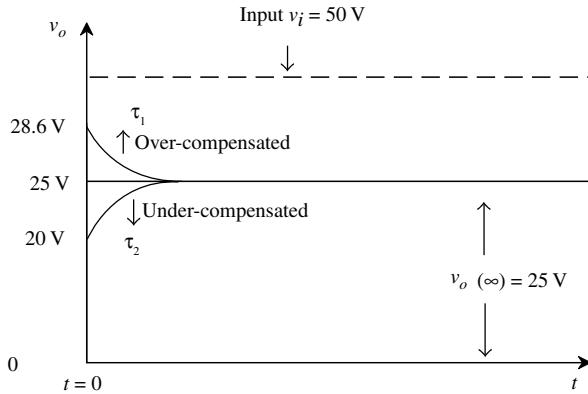


FIGURE 3.21(c) The input and output responses

The output at $t = 0^+$:

$$v_o(0^+) = v_i \times \frac{C_1}{C_1 + C_2} = 50 \times \frac{50}{50 + 75} = 20 \text{ V}$$

The output at $t = \infty$:

$$v_o(\infty) = v_i \times \frac{R_2}{R_1 + R_2} = 50 \times \frac{1}{1 + 1} = 25 \text{ V}$$

The time constant, τ_2 , with which the output rises to the steady-state value is:

$$\tau_2 = \frac{R_1 R_2}{R_1 + R_2} (C_1 + C_2) = \frac{1 \times 1}{1 + 1} \times 10^6 \times (50 + 75) \times 10^{-12} = 62.5 \mu\text{s}$$

Rise time, $t_r = 2.2 \tau_2$

$$t_r = 2.2 \times 62.5 \times 10^{-6} = 137.5 \mu\text{s}$$

The output responses are plotted in Fig. 3.21(c).

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Example 3.8: For the circuit shown in Fig. 3.22(a), calculate and draw the output response. Determine the rise time, the magnitude of the overshoot and the time constant when the output decays to the final value.

Solution: Here $R_1 = R_2$. For perfect compensation, $C_1 = C_2$, but in the figure $C_1 > C_2$. So the attenuator is over-compensated. Also, R_s is not equal to zero, the step input of 2 V will not appear at the input of the attenuator with zero rise time. The input to the attenuator is:

$$v'_i = v_i \times \frac{R_1 + R_2}{R_1 + R_2 + R_s} = 2 \times \frac{1 + 1}{1 + 1 + 0.01} = 2 \times \frac{2}{2.01} = 1.99 \text{ V}$$

The rise time, t_r of this input is:

$$t_r = 2.2 [R_s || (R_1 + R_2)] \frac{C_1 C_2}{C_1 + C_2} = 2.2 \left(\frac{0.01 \times 2}{0.01 + 2} \right) \left(\frac{30 \times 20}{30 + 20} \right) \times 10^{-6} = 0.26 \mu\text{s}$$

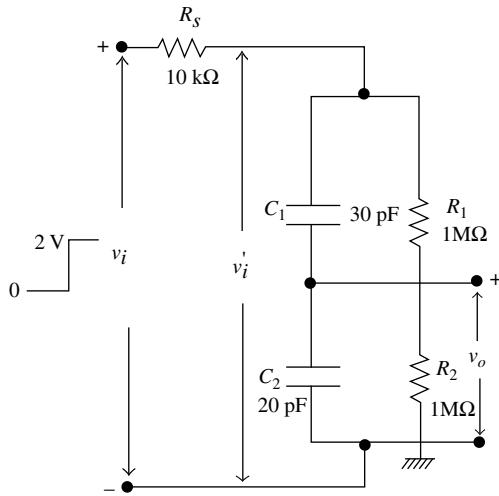


FIGURE 3.22(a) The given attenuator circuit

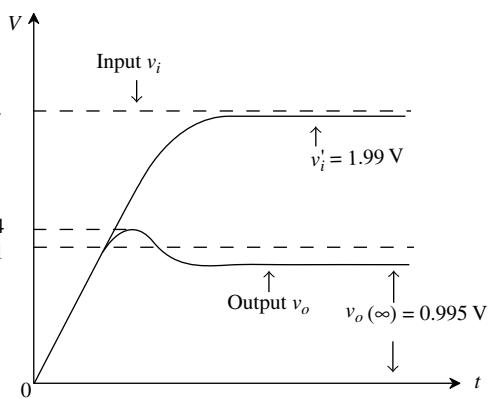


FIGURE 3.22(b) The response of the attenuator circuit

Initial response:

$$v_o(0^+) = v_i' \times \frac{C_1}{C_1 + C_2} = 1.99 \times \frac{30}{30 + 20} = 1.194 \text{ V}$$

Final response:

$$v_o(\infty) = v_i' \times \frac{R_2}{R_1 + R_2} = 1.99 \times \frac{1}{1 + 1} = 0.995 \text{ V}$$

Fall time:

$$t_f = 2.2 \left(\frac{R_1 R_2}{R_1 + R_2} \right) (C_1 + C_2) = 2.2 \left(\frac{1 \times 1}{1 + 1} \right) \times 10^6 \times (30 + 20) \times 10^{-12} = 55 \mu\text{s}$$

$$\text{Overshoot} = v_o(0^+) - v_o(\infty) = 1.194 - 0.995 = 0.199 \text{ V}$$

The response is shown in Fig. 3.22(b).

3.4 RLC CIRCUITS

RLC circuits behave altogether differently when compared to either RL or RC circuits. RLC circuits are resonant circuits. These can be either series resonant circuits or parallel resonant circuits. A parallel RLC circuit is used as a tank circuit in an oscillator to generate oscillations (this is the feedback network that produces the phase shift of 180°). The RLC circuit is also used in tuned amplifiers to select a desired frequency band at the output. When a sinusoidal signal is applied as input to a series RLC circuit [see Fig. 3.23(a)], the frequency-vs-current characteristic is as shown in Fig. 3.23(b).

At resonance: $X_L = X_C$

$$\omega_o L = 1/\omega_o C$$

$$f_o = \frac{1}{2\pi\sqrt{LC}} \quad (3.51)$$

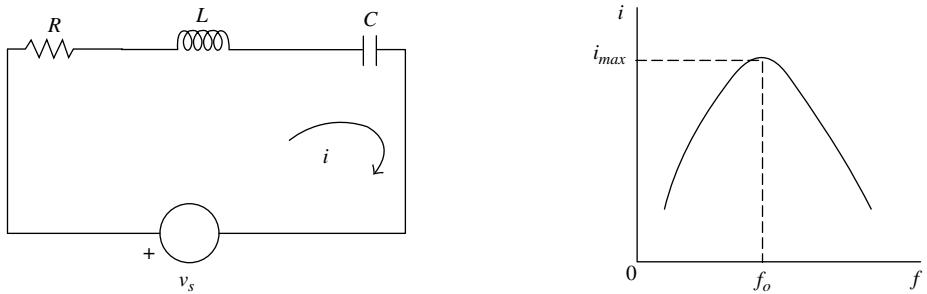


FIGURE 3.23(a) An RLC series circuit with sinusoidal input; (b) the frequency-vs-current characteristic

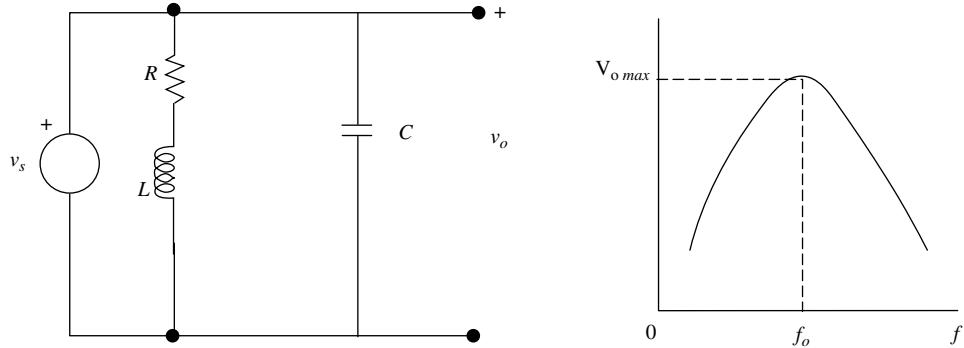


FIGURE 3.23(c) A parallel RLC resonant circuit with sinusoidal input; (d) the frequency-vs-voltage characteristic

At resonance, the impedance is minimum, purely resistive and equal to R . The current at the resonant frequency, f_o is maximum, termed i_{\max} . Let us now consider a parallel resonant circuit [see Fig. 3.23(c)] and its frequency-vs- v_o characteristic, shown in Fig. 3.23(d). In the parallel resonant circuit, the impedance is maximum at resonance and hence, the voltage is maximum at f_o . The figure of merit of a tuned circuit, denoted by Q , is given as:

$$Q = \omega_o R C = \frac{(\omega_o L)}{R}$$

The larger the value of Q , the sharper the response characteristic of the tuned circuit.

3.4.1 The Response of the RLC Parallel Circuit to a Step Input

Consider the RLC circuit shown in Fig. 3.24(a). Applying Laplace transforms, the above circuit is redrawn shown in Fig. 3.24(b). The impedance of the parallel combination of Ls and $1/Cs$ is:

$$Z_p(s) = \frac{Ls \left(\frac{1}{Cs} \right)}{Ls + \frac{1}{Cs}} \quad (3.52)$$

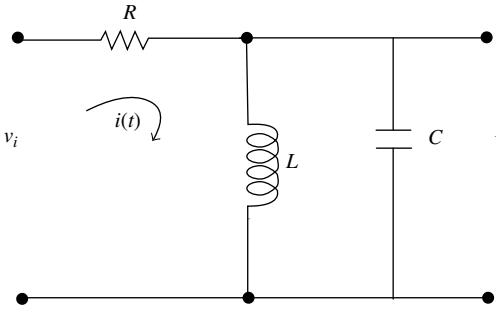


FIGURE 3.24(a) RLC parallel circuit

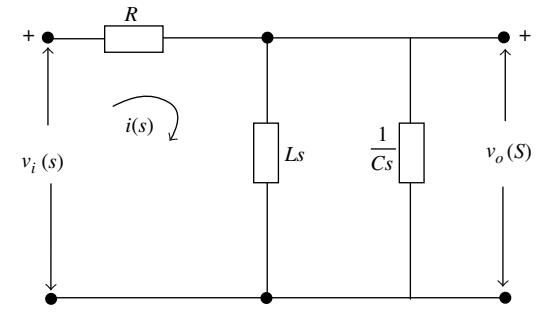


FIGURE 3.24(b) The Laplace circuit of Fig. 3.24(a)

Multiplying the numerator and denominator by Cs we get:

$$Z_p(s) = \frac{Ls}{LCs^2 + 1} \quad v_o(s) = \frac{v_i(s) \times Z_p(s)}{R + Z_p(s)} = v_i(s) \frac{\frac{Ls}{LCs^2 + 1}}{R + \frac{Ls}{LCs^2 + 1}} \\ v_o(s) = v_i(s) \frac{Ls}{RLCs^2 + Ls + R}$$

Therefore,

$$\frac{v_o(s)}{v_i(s)} = \frac{Ls}{RLCs^2 + Ls + R} \quad (3.53)$$

The characteristic equation is:

$$RLCs^2 + Ls + R = 0 \quad (3.54)$$

The roots of this characteristic equation are:

$$s_1, s_2 = \frac{-L + \sqrt{L^2 - 4(RLC)R}}{2RLC} = \frac{-L}{2RLC} \pm \sqrt{\frac{L^2}{4R^2L^2C^2} - \frac{4R^2LC}{4R^2L^2C^2}} \\ s_1, s_2 = \frac{-1}{2RC} \pm \sqrt{\frac{1}{4R^2C^2} - \frac{1}{LC}} \quad s_1, s_2 = \frac{-1}{2RC} \pm \sqrt{\frac{1}{(2RC)^2} - \frac{1}{LC}} \quad (3.55)$$

Let K , the damping constant, be given by:

$$K = \frac{1}{2R} \sqrt{\frac{L}{C}} \quad (3.56)$$

From Eq. (3.51), the resonant frequency of the tank circuit is:

$$f_o = \frac{1}{2\pi\sqrt{LC}} \\ T_o = \frac{1}{f_o} = 2\pi\sqrt{LC} \quad (3.57)$$

From Eqs. (3.56) and (3.57):

$$\frac{K}{T_o} = \frac{1}{2R} \sqrt{\frac{L}{C}} \times \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi \times 2RC}$$

Therefore,

$$\frac{1}{2RC} = \frac{2\pi K}{T_o} \quad (3.58)$$

Putting Eq. (3.58) in Eq. (3.55):

Therefore,

$$s_1, s_2 = \frac{-2\pi K}{T_o} \pm \sqrt{\left(\frac{2\pi K}{T_o}\right)^2 - \frac{1}{LC}} = \frac{-2\pi K}{T_o} \pm \frac{2\pi K}{T_o} \times \sqrt{1 - \frac{4R^2C^2}{LC}}$$

From Eq. (3.56) we have:

$$\frac{4R^2C}{L} = \frac{1}{K^2}$$

Therefore,

$$\begin{aligned} s_1, s_2 &= \frac{-2\pi K}{T_o} \pm \frac{2\pi K}{T_o} \times \sqrt{1 - \frac{1}{K^2}} = \frac{-2\pi K}{T_o} \pm \frac{2\pi K}{T_o} \times \sqrt{\frac{K^2 - 1}{K^2}} \\ s_1, s_2 &= \frac{-2\pi K}{T_o} \pm \frac{2\pi K}{T_o K} \times \sqrt{-1(1 - K^2)} = \frac{-2\pi K}{T_o} \pm \frac{j2\pi}{T_o} \sqrt{1 - K^2} \end{aligned} \quad (3.59)$$

From Eq. (3.53):

$$\frac{v_o(s)}{v_i(s)} = \frac{Ls}{RLCs^2 + Ls + R}$$

For unit step voltage as input:

$$\begin{aligned} \frac{v_o(s)}{V} &= \frac{Ls}{RLCs^2 + Ls + R} \quad \frac{V_o(s)}{V} = \frac{L}{RLCs^2 + LS + R} \\ \frac{v_o(s)}{V} &= \frac{L}{RLC \left(s^2 + \frac{1}{RC}s + \frac{1}{LC} \right)} = \frac{1}{RC} \left[\frac{1}{(s - s_1)(s - s_2)} \right] \end{aligned}$$

Applying partial fractions:

$$\frac{v_o(s)}{V} = \left[\frac{A}{(s - s_1)} + \frac{B}{(s - s_2)} \right] = \frac{1}{RC} \left[\frac{1}{(s - s_1)(s - s_2)} \right] \quad \frac{1}{RC} = A(s - s_2) + B(s - s_1)$$

Putting $s = s_1$

$$\frac{1}{RC} = A(s_1 - s_2) \quad A = \frac{1}{RC(s_1 - s_2)}$$

Putting $s = s_2$

$$\frac{1}{RC} = -B(s_1 - s_2) \quad B = \frac{-1}{RC(s_1 - s_2)}$$

$$\frac{v_o(s)}{V} = \frac{1}{RC(s_1 - s_2)} \left[\frac{1}{(s - s_1)} - \frac{1}{(s - s_2)} \right]$$

Applying inverse Laplace transform to both sides, we get:

$$\frac{v_o(t)}{V} = \frac{1}{RC(s_1 - s_2)} (e^{s_1 t} - e^{s_2 t}) \quad (3.60)$$

From Eq. (3.59):

(i) If $K = 0$:

$$s_1, s_2 = \pm \frac{j2\pi}{T_o} \quad (3.61)$$

$$s_1 - s_2 = \frac{j2\pi}{T_o} - \left(-\frac{j2\pi}{T_o} \right) = \frac{j4\pi}{T_o} = \frac{2j2\pi}{T_o} \quad (3.62)$$

Using Eq. (3.60):

$$\frac{v_o(t)}{V} = \frac{1}{RC} \frac{2\pi}{T_o} \frac{(e^{(j2\pi/T_o)t} - e^{-(j2\pi/T_o)t})}{2j} \quad (3.63)$$

$$\frac{v_o(t)}{V} = \frac{1}{2\pi RC} \left[\sin \left(\frac{2\pi}{T_o} \times t \right) \right]$$

Let

$$x = \frac{t}{T_o} \quad (3.64)$$

Therefore,

$$\frac{v_o(t)}{V} = \frac{1}{2\pi RC} \left[\sin (2\pi x) \right] \quad (3.65)$$

If we substitute the value of T_o from Eq. (3.57) in Eq. (3.65):

$$\frac{v_o(t)}{V} = \frac{2\pi \sqrt{LC}}{2RC\pi} \left[\sin (2\pi x) \right] = \frac{1}{R} \times \sqrt{\frac{L}{C}} \times \sin (2\pi x)$$

$$\frac{v_o(t)}{V} = 2K \sin (2\pi x) \quad (3.66)$$

Thus, $K \rightarrow 0$, as $R \rightarrow \infty$. Here, K can not be zero as assumed ideally, since $R = \infty$ means open-circuiting the resistance R in the circuit shown in Fig. 3.24(a), which is absurd because the excitation is not connected to the circuit when $R = \infty$. However, R can be made very large, in which case K becomes very small, though not zero as expected. The output has a smaller amplitude but is oscillatory in nature, as seen from Eq. (3.66). Thus, when a step is applied as input to the RLC circuit in Fig. 3.24(a), with $K = 0$ (practically very small), the response is un-damped oscillations, as shown in Fig. 3.24(c).

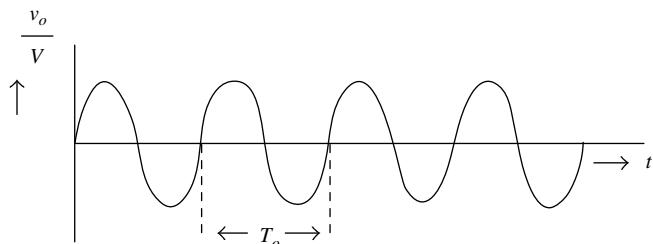


FIGURE 3.24(c) The response to $K = 0$

(ii) If $K < 1$, it is a case of under-damping as shown in Fig. 3.24(d). For this condition, from Eq. (3.59):

$$s_1, s_2 = \frac{-2\pi K}{T_o} \pm \frac{j2\pi}{T_o} \sqrt{1 - K^2}$$

$$s_1 = \frac{-2\pi K}{T_o} + \frac{j2\pi}{T_o} \sqrt{1 - K^2} \quad s_2 = \frac{-2\pi K}{T_o} - \frac{j2\pi}{T_o} \sqrt{1 - K^2}$$

Therefore,

$$s_1 - s_2 = \frac{-2\pi K}{T_o} + \frac{j2\pi}{T_o} \sqrt{1 - K^2} + \frac{2\pi K}{T_o} + \frac{j2\pi}{T_o} \sqrt{1 - K^2}$$

$$s_1 - s_2 = \frac{j4\pi}{T_o} \sqrt{1 - K^2} \quad (3.67)$$

Multiply and divide Eq. (3.67) by K and substitute $K/T_o = 1/4\pi RC$ in it. The resultant equation is:

$$\frac{1}{RC(s_1 - s_2)} = \frac{K}{j\sqrt{1 - K^2}}$$

From Eq. (3.60):

$$\frac{v_o(t)}{V} = \frac{K}{j\sqrt{1 - K^2}} \times (e^{(a+jb)t} - e^{(a-jb)t})$$

where

$$a = \frac{-2\pi K}{T_o} \quad \text{and} \quad b = \frac{2\pi}{T_o} \sqrt{1 - K^2}$$

$$\frac{v_o(t)}{V} = \frac{K}{j\sqrt{1 - K^2}} \times e^{at} (e^{jbt} - e^{-jbt}) = \frac{K}{j\sqrt{1 - K^2}} \times e^{at} 2j \sin bt$$

$$\frac{v_o(t)}{V} = \frac{2K}{\sqrt{1 - K^2}} \times e^{at} \sin bt = \frac{2K}{\sqrt{1 - K^2}} \times e^{-2\pi Kt/T_o} \times \sin \left(\frac{2\pi t}{T_o} \sqrt{1 - K^2} \right)$$

$$\frac{v_o(t)}{V} = \frac{2K}{\sqrt{1 - K^2}} \times e^{-2\pi Kx} \times \sin \left(2\pi x \sqrt{1 - K^2} \right) \quad (3.68)$$

The output response is an under-damped sinusoidal waveform. The oscillations die down after a few cycles, as shown in Fig. 3.24(d).

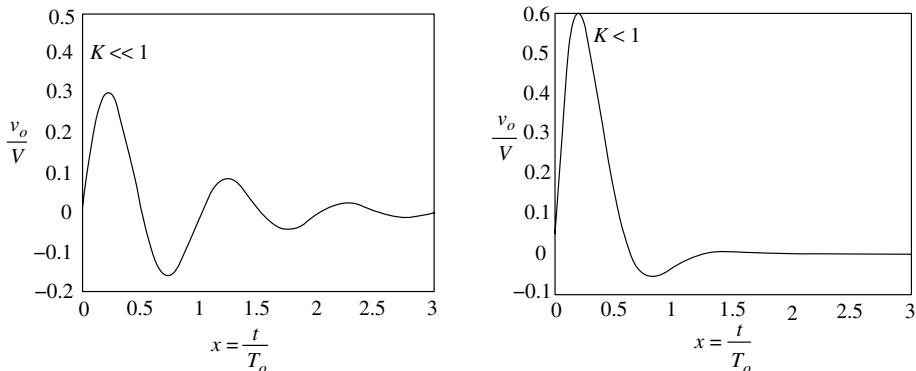


FIGURE 3.24(d) The response to $K < 1$

(iii) If $K = 1$, it is a case of critical damping. If we substitute the K value in the Eq. (3.59), then the roots are $s_1 = s_2 = -2\pi/T_o$. The roots are equal and real.

If the input is a step voltage:

$$\frac{v_o(s)}{V} = \frac{1}{RC(s - s_1)(s - s_2)}$$

Here,

$$s_1 = s_2 = \frac{-2\pi}{T_o}$$

Therefore,

$$\frac{v_o(s)}{V} = \frac{1}{RC(s - s_1)^2}$$

Applying inverse Laplace transform on both sides:

$$\frac{v_o(t)}{V} = \frac{1}{RC} \times te^{s_1 t} = \frac{1}{RC} \times te^{(-2\pi/T_o) \times t} = \frac{1}{RC} \times te^{-2\pi x}$$

where $x = t/T_o$:

$$\frac{v_o(t)}{V} = \frac{4\pi}{4\pi RC} \times te^{-2\pi x}$$

Here:

$$\frac{T_o}{K} = 4\pi RC \quad \frac{v_o(t)}{V} = \frac{4\pi t}{T_o} \times e^{-2\pi x} = \frac{4\pi Kt}{T_o} \times e^{-2\pi x}$$

$$\frac{v_o(t)}{V} = 4\pi K x e^{-2\pi x} \quad (3.69)$$

$$\frac{v_o(t)}{V} = 4\pi x e^{-2\pi x} \quad \text{since } K = 1 \quad (3.70)$$

The output response is shown in Fig. 3.24(e).

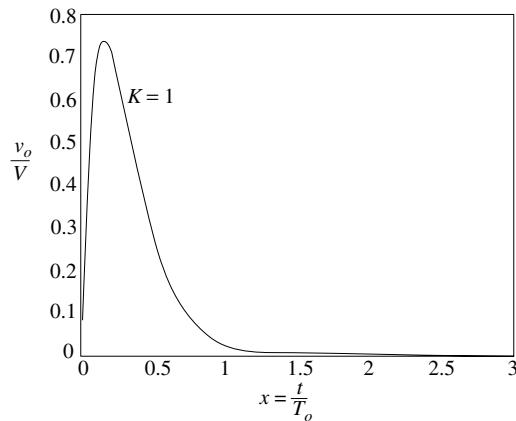


FIGURE 3.24(e) The response to $K = 1$

(iv) If $K > 1$, it is a case of over-damping. If $K > 1$, then the roots, from Eq. (3.59), are:

$$s_1, s_2 = \frac{-2\pi K}{T_o} \pm \frac{2\pi K}{T_o} \times \sqrt{1 - \frac{1}{K^2}}$$

Using the binomial expansion for $\sqrt{(1 - 1/K^2)}$, we get:

$$\left[1 - \frac{1}{2} \times \frac{1}{K^2} + \frac{\frac{1}{2} \times \frac{-1}{2}}{K^4} \dots \right]$$

Neglecting the higher order terms, the binomial expansion is reduced to $(1 - 1/2K^2)$.

$$s_1, s_2 = \frac{-2\pi K}{T_o} \pm \frac{2\pi K}{T_o} \times \left(1 - \frac{1}{2K^2} \right)$$

$$s_1 = \frac{-2\pi K}{T_o} + \frac{2\pi K}{T_o} - \frac{2\pi K}{T_o 2K^2} = \frac{-\pi}{T_o K}$$

$$s_2 = \frac{-2\pi K}{T_o} - \frac{2\pi K}{T_o} + \frac{2\pi K}{T_o 2K^2} = \frac{-4\pi K}{T_o} + \frac{\pi}{T_o K} = \frac{-\pi}{T_o} \times \frac{(4K^2 - 1)}{K}$$

As

$$K > 1, (4K^2 - 1) \approx 4K^2$$

$$s_2 = \frac{-\pi}{T_o} \times \frac{4K^2}{K} = \frac{-4\pi K}{T_o}$$

$$s_1 - s_2 = \frac{-\pi}{T_o K} + \frac{4\pi K}{T_o} = \frac{\pi}{T_o} \left(\frac{4K^2 - 1}{K} \right) \approx \frac{\pi}{T_o} \times \frac{4K^2}{K} = \frac{4K\pi}{T_o}$$

As

$$\frac{K}{T_o} = \frac{1}{4\pi RC}$$

Therefore,

$$s_1 - s_2 = \frac{4\pi}{4\pi RC} = \frac{1}{RC}$$

From Eq. (3.60):

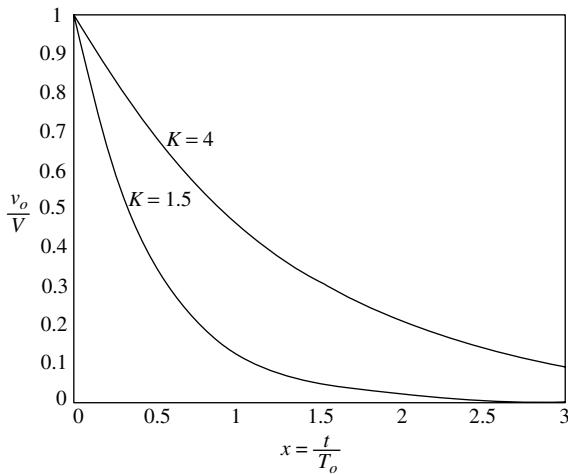
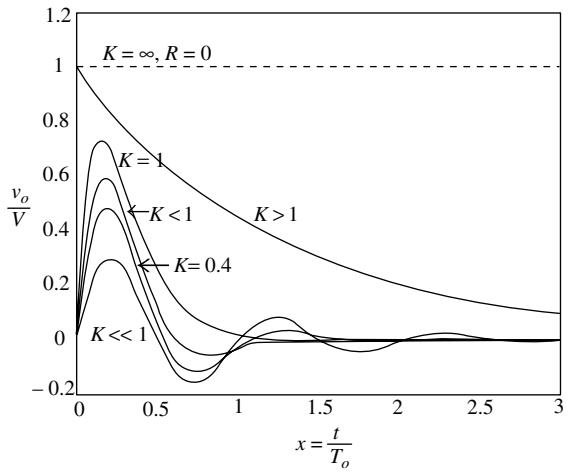
$$\begin{aligned} \frac{v_o(t)}{V} &= \frac{1}{RC(s_1 - s_2)} (e^{s_1 t} - e^{s_2 t}) = \frac{1}{RC \times \frac{1}{RC}} (e^{(-\pi/T_o K) \times t} - e^{(-4\pi K/T_o) \times t}) \\ \frac{v_o(t)}{V} &= (e^{-\pi x/K} - e^{-4\pi K x}) = e^{-\pi x/K} - e^{(-\pi x/K) \times 4K^2} \end{aligned} \quad (3.71)$$

As $4K^2 \gg 1$

Therefore,

$$\frac{v_o(t)}{V} \approx e^{-\pi x/K} \quad (3.72)$$

$$KT_0 = \frac{1}{2R} \sqrt{\frac{L}{C}} (2\pi \sqrt{LC}) = (\pi L/R) \quad (3.73)$$

FIGURE 3.24(f) The response to $K > 1$ FIGURE 3.24(g) The response of an RLC parallel circuit for different values of K

Substituting Eq. (3.73) in Eq. (3.72):

$$\frac{v_o(t)}{V} \approx e^{-Rt/L} \quad (3.74)$$

The response is plotted in Fig. 3.24(f).

(v) From Fig. 3.24(a), if $R = 0$, the input step V is directly available at the output. From Eq. (3.56), $R = 0$ means $K = \infty$. Figure 3.24(g) shows a comparison of the response of an RLC parallel circuit for different values of K .

3.4.2 The Response of the RLC Series Circuit to a Step Input

Consider a series RLC circuit, shown in Fig. 3.25(a). Applying Laplace transforms, the circuit in Fig. 3.25(a) can be redrawn as shown in Fig. 3.25(b). The total impedance $Z(s)$ in this circuit is given by the relation:

$$Z(s) = R + Ls + \frac{1}{Cs}$$

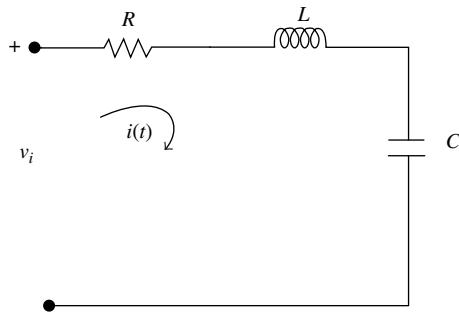


FIGURE 3.25(a) An RLC series circuit

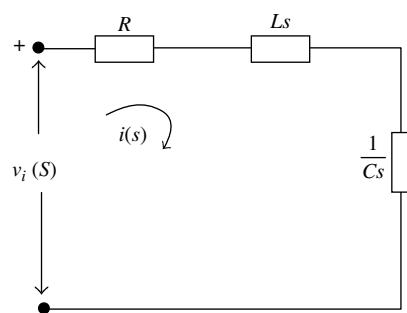


FIGURE 3.25(b) The Laplace circuit of Fig. 3.25(a)

Therefore,

$$i(s) = \frac{v_i(s)}{Z(s)} = \frac{v_i(s)}{R + Ls + \frac{1}{Cs}} \quad (3.75)$$

$$v_i(s) = i(s) \left(R + Ls + \frac{1}{Cs} \right) = \frac{i(s)}{Cs} \left(LCs^2 + RCs + 1 \right) \quad (3.76)$$

But

$$v_o(s) = \frac{i(s)}{Cs} \quad (3.77)$$

Substituting Eq. (3.77) in Eq. (3.76):

$$v_i(s) = v_o(s) \left(LCs^2 + RCs + 1 \right)$$

$$v_o(s) = \frac{v_i(s)}{LC \left(s^2 + \frac{R}{L}s + \frac{1}{LC} \right)} \quad (3.78)$$

For a step input V , from Eq. 3.75

$$i(s) = \frac{\frac{V}{s}}{R + Ls + \frac{1}{Cs}} = \frac{V}{L \left(s^2 + \frac{R}{L}s + \frac{1}{LC} \right)} \quad (3.79)$$

The characteristic equation is:

$$s^2 + \frac{R}{L}s + \frac{1}{LC} = 0 \quad (3.80)$$

The roots of this characteristic equation are:

$$s_1, s_2 = \frac{-\frac{R}{L} \pm \sqrt{\left(\frac{R}{L}\right)^2 - \frac{4}{LC}}}{2} = -\frac{R}{2L} \pm \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}} \quad (3.81)$$

1. If either $(R/2L)^2 > 1/LC$ or $R > 2\sqrt{L/C}$, then both the roots are real and different, the circuit is over-damped.
2. If either $(R/2L)^2 = 1/LC$ or $R = 2\sqrt{L/C}$, then both the roots are real and equal, the circuit is critically damped.
3. If either $(R/2L)^2 < 1/LC$ or $R < 2\sqrt{L/C}$, then both the roots are complex conjugate to each other; the circuit is under-damped. We have from Eq. (3.79):

$$i(s) = \frac{V}{L \left(s^2 + \frac{R}{L}s + \frac{1}{LC} \right)}$$

Applying partial fractions:

$$\left[\frac{A}{(s - s_1)} + \frac{B}{(s - s_2)} \right] = \frac{V}{L} \left[\frac{1}{(s - s_1)(s - s_2)} \right] \quad \frac{V}{L} = A(s - s_2) + B(s - s_1)$$

Putting $s = s_1$:

$$\frac{V}{L} = A(s_1 - s_2) \quad A = \frac{V}{L(s_1 - s_2)}$$

Putting $s = s_2$:

$$\frac{V}{L} = -B(s_1 - s_2) \quad B = \frac{-V}{L(s_1 - s_2)} \quad i(s) = \frac{V}{L(s_1 - s_2)} \left[\frac{1}{(s - s_1)} - \frac{1}{(s - s_2)} \right]$$

Taking Laplace inverse:

$$i(t) = \frac{V}{L(s_1 - s_2)} [e^{s_1 t} - e^{s_2 t}] \quad (3.82)$$

Case 1: For over-damped circuit, $(R/2L)^2 > 1/LC$

$$s_1 - s_2 = 2\sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}}$$

Let

$$P = \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}} \quad s_1 - s_2 = 2P$$

From Eq. (3.82), we get:

$$i(t) = \frac{V}{2PL} (e^{s_1 t} - e^{s_2 t}) \quad (3.83)$$

Case 2: For a critically damped circuit, $(R/2L)^2 = 1/LC$

Therefore,

$$s_1, s_2 = -\frac{R}{2L} \quad I(s) = \frac{V}{L} \left[\frac{1}{\left(s + \frac{R}{2L}\right)^2} \right]$$

Applying inverse Laplace transform on both sides, we get,

$$i(t) = \frac{V}{L} t (e^{(-R/2L) \times t}) \quad (3.84)$$

Case 3: For an under-damped circuit, $(R/2L)^2 < 1/LC$

Therefore,

$$s_1, s_2 = -\frac{R}{2L} \pm \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}} = -\frac{R}{2L} \pm \left\{ -\left[\frac{1}{LC} - \left(\frac{R}{2L}\right)^2 \right] \right\}^{1/2} = -\frac{R}{2L} \pm jM$$

where,

$$M = \left\{ \left[\frac{1}{LC} - \left(\frac{R}{2L}\right)^2 \right] \right\}^{1/2} \quad s_1 - s_2 = -\frac{R}{2L} + jM + \frac{R}{2L} + jM = 2jM$$

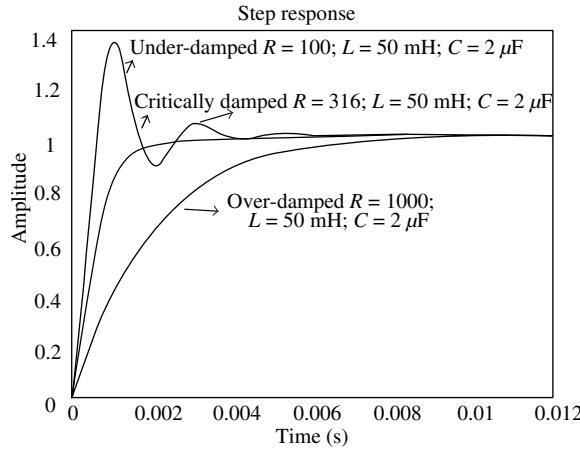


FIGURE 3.25(c) The step response of an RLC series circuit

From Eq. (3.82), we get:

$$i(t) = \frac{V}{2LjM} (e^{s_1 t} - e^{s_2 t}) = \frac{V}{2LjM} (e^{-Rt/2L} e^{jMt} - e^{-Rt/2L} e^{-jMt}) = \frac{V}{LM} e^{(-Rt/2L)} \left(\frac{e^{jMt} - e^{-jMt}}{2j} \right)$$

$$i(t) = \frac{V}{ML} (e^{(-R/2L) \times t}) \sin Mt \quad (3.85)$$

The step response is plotted using Eqs. (3.83), (3.84) and (3.85) in Fig. 3.25(c). For the under-damped condition, we see that there are damped oscillations.

3.4.3 RLC Ringing Circuits

The circuit [see Fig. 3.24(a)], for $K < 1$, gives rise to damped oscillations. This means that the amplitude of the oscillations reduces with every cycle, causing the oscillations to die down ultimately. This circuit is called a ringing circuit. From Eq. (3.68) we have:

$$\frac{v_o}{V} = \frac{2K}{\sqrt{1 - K^2}} \cdot e^{-2\pi Kx} \sin 2\pi \sqrt{(1 - K^2)} x$$

where

$$x = \frac{t}{T_o}$$

The amplitude of (v_o/V) is $(2K/\sqrt{1 - K^2}) \cdot e^{-2\pi Kx}$ and is at the maximum when $e^{-2\pi Kx} = 1$, when its value is $2K/\sqrt{1 - K^2}$. As $K < 1$, this value is $2K$. This amplitude reduces to $1/e$ of the maximum value of $2K$ in n cycles, when $2\pi Kx = 1$.

$$\frac{v_o}{V} = 2K \cdot e^{-1} \approx 2K \times \frac{1}{e} \quad \text{if } 2\pi Kx = 1$$

If $2\pi Kx = 1$, the amplitude decreases to $1/e$ of the initial value. If we know the value of Q , we can find the number of cycles for which the circuit rings before the magnitude reduces to $1/e$ of the initial value. Let the amplitude reduce to $1/e$ of the initial value after n cycles, at t_1 . At $t = t_1 = nT_o$, $x_1 = nT_o/T_o = n$, when $2\pi K x_1 = 1$.

$$Q = \omega_0 CR \quad \omega_0 = 2\pi f_0 = \frac{2\pi}{T_0} \quad Q = \frac{2\pi}{T_0} CR$$

But

$$T_0 = 2\pi\sqrt{LC} \quad (3.86)$$

Therefore,

$$Q = \frac{2\pi CR}{2\pi\sqrt{LC}} = R\sqrt{\frac{C}{L}} \quad (3.87)$$

But

$$K = \frac{1}{2R}\sqrt{\frac{L}{C}} \quad (3.88)$$

Therefore,

$$R\sqrt{\frac{C}{L}} = \frac{1}{2K} \quad (3.89)$$

From Eqs. (3.87) and (3.89):

$$Q = \frac{1}{2K} \quad (3.90)$$

$$2KQ = 1$$

Also:

$$2\pi Kx_1 = 1 \quad 2KQ = 2\pi Kx_1 \quad Q = \pi x_1 = \pi n \quad n = Q/\pi$$

If

$$Q = 20 \quad n = 20/3.14 \approx 6 \text{ cycles} \quad (3.91)$$

The circuit will ring for 6 cycles before the amplitude reduces to 37 per cent of its initial value, as shown in Fig. 3.26.

As K becomes smaller, though the amplitude of the output signal decreases, the oscillations continue for more number of cycles. In a sinusoidal oscillator with an LC tank circuit, when the power (V_{CC}) is switched ON, oscillations develop if $K < 1$ and this condition is sustained as a positive feedback is employed in these oscillators.

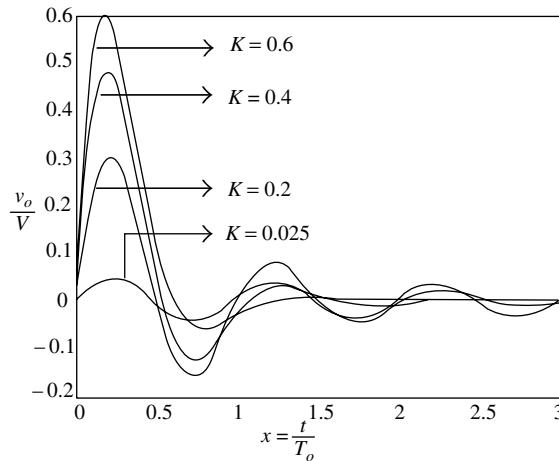


FIGURE 3.26 The output of the ringing circuit for $K < 1$

S O L V E D P R O B L E M S

Example 3.9: The periodic ramp with $T_1 = T_2 = \tau/2$ shown in Fig. 3.27(a) is applied to a low-pass RC circuit. Find the equations to determine the steady-state output waveform. The initial voltage on the condenser is V_1 . Find the maximum and minimum value of the voltage and plot the waveform.

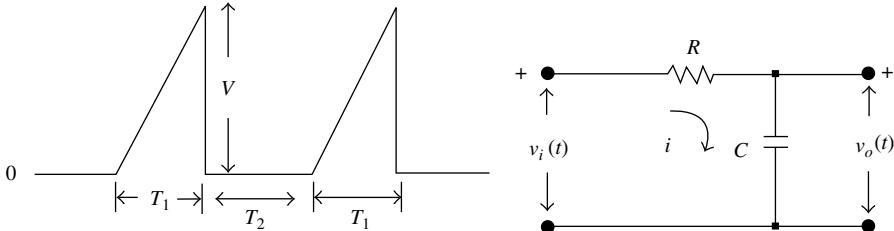


FIGURE 3.27(a) The given periodic ramp input; (b) the given RC circuit

Solution:

From Eq. (3.35), we have the output for a low-pass RC circuit to ramp input as:

$$v_o(t) = -\alpha\tau + \alpha t + \alpha\tau e^{-t/\tau}$$

If there is an initial voltage of V_1 on C , Eq. (3.35) gets modified as:

$$v_o(t) = -\alpha\tau + \alpha t + \alpha\tau e^{-t/\tau} + V_1 e^{-t/\tau}$$

For the ramp input, the slope $\alpha = V/T_1$

Therefore,

$$v_o(t) = \frac{V}{T_1}t - \frac{V}{T_1}\tau(1 - e^{-t/\tau}) + V_1 e^{-t/\tau} \quad (1)$$

The capacitor charges from V_1 to V_2 in time T_1 . During T_2 , when the input is zero, the capacitor discharges from V_2 to V_1 .

Given

$$T_1 = T_2 = \frac{\tau}{2}$$

At

$$t = T_1, v_o(t) = V_2$$

Using (1)

$$V_2 = \frac{V}{T_1} \times T_1 - \frac{V}{T_1} \times 2T_1(1 - e^{-0.5}) + V_1 e^{-0.5} = -V + (V_1 + 2V)e^{-0.5} \quad (2)$$

When the ramp input is reduced to zero V_2 decays to V_1 .

Therefore,

$$V_1 = V_2 e^{-T_2/\tau} = V_2 e^{-0.5} \quad (3)$$

Substituting (2) in (3)

$$V_1 = \left[-V + (V_1 + 2V)e^{-0.5} \right] e^{-0.5} \quad V_1(1 - e^{-1}) = V(-e^{-0.5} + 2e^{-1})$$

$$V_1 = \frac{V(-e^{-0.5} + 2e^{-1})}{1 - e^{-1}} = 0.21 \text{ V}$$

From (2)

$$V_2 = -V + (V_1 + 2V)e^{-0.5} = -V + V(0.21 + 2)0.606 \quad V_2 = 0.34 \text{ V}$$

The minimum value of the output occurs when $dv_o(t)/dt = 0$.

$$v_o(t) = \alpha t + V_1 e^{-t/\tau} - \alpha \tau (1 - e^{-t/\tau}) \quad \frac{dv_o(t)}{dt} = \alpha - \frac{V_1}{\tau} \times e^{-t/\tau} - \frac{\alpha \tau}{\tau} e^{-t/\tau} = 0$$

$$\frac{V}{T_1} - \frac{V_1}{2T_1} e^{-t/\tau} - \frac{V}{T_1} e^{-t/\tau} = 0 \quad \frac{V}{T_1} - e^{-t/\tau} \left(\frac{V_1}{2T_1} + \frac{V}{T_1} \right) = 0$$

$$(V_1 + 2V)e^{-t/\tau} = 2V \quad e^{-t/\tau} = \frac{2V}{(V_1 + 2V)} = \frac{2V}{0.21V + 2V} = 0.905 \quad \frac{t}{\tau} = 0.10$$

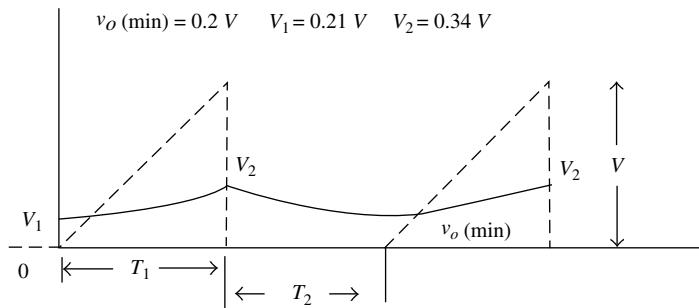


FIGURE 3.27(c) The output waveform

At $t = 0.10\tau$, v_o is $v_o(\min)$. Substituting this value in $v_o(t)$,

$$v_o(t) = \frac{V}{T_1}t - \frac{V}{T_1}\tau(1 - e^{-t/\tau}) + V_1 e^{-t/\tau}$$

$$v_o(\min) = V \times 2 \times 0.10 - 2V(1 - 0.905) + 0.21V \times 0.905 = 0.2 \text{ V}$$

The output waveform is shown in Fig. 3.27(c).

Example 3.10: Prove that an RC circuit, shown in Fig. 3.28, behaves as a reasonably good integrator if $RC \gg 20T$, where T is the period of an input, $E_m \sin \omega t$.

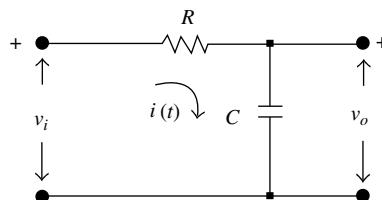


FIGURE 3.28 The given low-pass RC circuit in which $RC \gg 20T$

Solution: We have:

$$\frac{dv_o}{dt} + \frac{v_o}{\tau} = \frac{v_i}{\tau}$$

If the time constant (RC) is very large compared to T then:

$$\frac{dv_o}{dt} = \frac{v_i}{\tau} \quad v_o = \frac{1}{\tau} \int v_i dt \quad v_i = E_m \sin \omega t$$

$$v_o = \frac{1}{\tau} \int E_m \sin \omega t dt = \frac{-E_m}{\tau} \cos \omega t$$

$$v_o = \frac{\frac{1}{j\omega C}}{R + \frac{1}{j\omega C}} v_i = \frac{v_i}{1 + j\omega \tau} = \frac{E_m \sin \omega t}{1 + j\omega \tau}$$

$$|v_o| = \frac{E_m}{\sqrt{1 + \omega^2 \tau^2}} = \frac{E_m}{\sqrt{1 + \left(\frac{\tau}{T}\right)^2}}$$

And the phase angle $\theta = \tan^{-1}(\omega/\omega_2) = \tan^{-1}(\tau/T)$.

Given that $\tau \gg 20T$:

$$\frac{\tau}{T} \gg 20$$

At $\tau = 20T$,

$$\theta = \tan^{-1} 20 = 87.14^\circ$$

If $\tau \gg T$, θ will be nearly 90° . The sinusoidal signal undergoes a phase change of 90° , as required in an integrator.

Example 3.11: For the circuit shown in Fig. 3.29, find:

- The expression for the voltage across the capacitor at each stage.
- The rise time of the output in terms of the time constant.
- The ratio of the rise time of the combination of the three sections to the rise time of a single section.

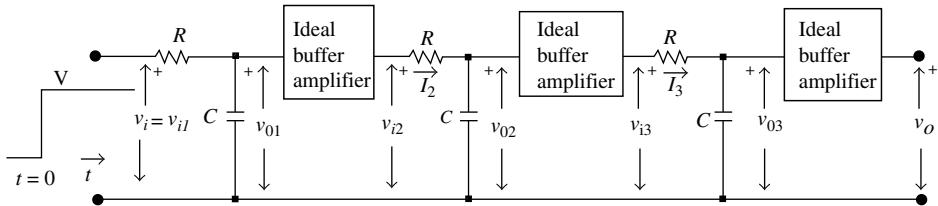


FIGURE 3.29 Cascaded low-pass RC circuits

Solution:

- Time constant $\tau = RC$

Stage 1:

$$\text{Input} = v_{i1} = V \quad \text{Output} = v_{o1} = V(1 - e^{-t/\tau})$$

Stage 2:

$$\text{Input} = v_{i2} = v_{o1} = V(1 - e^{-t/\tau}) \quad \text{Output} = v_{o2}$$

We have,

$$I_2 = \frac{v_{i2} - v_{o2}}{R} \quad \frac{C dv_{o2}}{dt} = \frac{v_{i2} - v_{o2}}{R} \quad \frac{dv_{o2}}{dt} = -\frac{v_{o2}}{RC} + \frac{v_{i2}}{RC} \quad \frac{dv_{o2}}{dt} + \frac{v_{o2}}{\tau} = \frac{v_{i2}}{\tau}$$

Therefore,

$$v_{o2} = V \left(1 - e^{-t/\tau} - \frac{t}{\tau} e^{-t/\tau} \right)$$

Stage 3:

$$\text{Input} = v_{i3} = v_{o2} = V \left(1 - e^{-t/\tau} - \frac{t}{\tau} e^{-t/\tau} \right) \quad \text{Output} = v_{o3} = v_o$$

We have,

$$I_3 = \frac{v_{i3} - v_o}{R}$$

$$C \frac{dv_o}{dt} = \frac{v_{i3} - v_o}{R} \Rightarrow \frac{dv_o}{dt} = \frac{v_{i3} - v_o}{RC} = \frac{v_{i3} - v_o}{\tau} \quad \frac{dv_o}{dt} + \frac{v_o}{\tau} = \frac{v_{i3}}{\tau}$$

Therefore,

$$v_o = V \left(1 - e^{-t/\tau} - \frac{t}{\tau} e^{-t/\tau} - \frac{t^2}{2(\tau)^2} e^{-t/\tau} \right)$$

- (b) Rise time is the time taken for the waveform to rise from 10 per cent to 90 per cent of its max value V . Here, let at $t = t_2$, v_o reach 90 per cent of V . Therefore, at 90% of V , $V_o/V = 0.9$

$$0.9 = \left(1 - e^{-t_2/\tau} - \frac{t_2}{\tau} e^{-t_2/\tau} - \frac{t_2^2}{2(\tau)^2} e^{-t_2/\tau} \right) = 1 - \left(1 + \frac{t_2}{\tau} + \frac{t_2^2}{2(\tau)^2} \right) e^{-t_2/\tau}$$

Therefore

$$0.1 = \left(1 + \frac{t_2}{\tau} + \frac{t_2^2}{2(\tau)^2} \right) e^{-t_2/\tau}$$

The rise time of the cascaded network is calculated by finding t_2 and t_1 . As the above equation is transcendental equation,* we should go for trial and error method to get the value of t_2 . The value of t_2/τ at which, LHS value = RHS value, is the value we will take into account to calculate t_2 .

Let us start with $t_2/\tau = 1$

$$0.1 = \left(1 + 1 + \frac{1^2}{2} \right) e^{-1} = 0.919$$

$LHS \neq RHS$

If $t_2/\tau = 3$

$$0.1 = \left(1 + 3 + \frac{3^2}{2} \right) e^{-3} = 0.423$$

$LHS \neq RHS$

If $t_2/\tau = 5$

$$0.1 = \left(1 + 5 + \frac{5^2}{2} \right) e^{-5} = 0.1246$$

$LHS \neq RHS$

If $t_2/\tau = 6$

$$0.1 = \left(1 + 6 + \frac{6^2}{2} \right) e^{-6} = 0.061$$

*Typically, equations of the form $x = \exp(x)$ and $x = \sin(x)$ are called transcendental equations. To find the solution of a transcendental equation one may use a graphical method or a numerical method.

LHS \neq *RHS*It means that the value of t_2/τ lies between 5 and 6. If $t_2/\tau = 5.5$

$$0.1 = \left(1 + 5.5 + \frac{5.5^2}{2}\right) e^{-5.5} = 0.088$$

LHS \neq *RHS*If $t_2/\tau = 5.3$

$$0.1 = \left(1 + 5.3 + \frac{5.3^2}{2}\right) e^{-5.3} = 0.10$$

LHS = *RHS*

$$t_2 = 5.3\tau$$

Let at $t = t_1, v_o$ reach 10% of V 10 % of V is:

$$0.1 = 1 \left(1 - e^{-t_1/\tau} - \frac{t_1}{\tau} e^{-t_1/\tau} - \frac{t_1^2}{2\tau^2} e^{-t_1/\tau}\right) = 1 - \left(1 + \frac{t_1}{\tau} + \frac{t_1^2}{2(\tau)^2}\right) e^{-t_1/\tau}$$

$$0.9 = \left(1 + \frac{t_1}{\tau} + \frac{t_1^2}{2(\tau)^2}\right) e^{-t_1/\tau}$$

The value of t_1/τ for which *LHS* = *RHS* is the value we will take into account to calculate t_1 .Let us start with $t_1/\tau = 1$

$$0.9 = \left(1 + 1 + \frac{1^2}{2}\right) e^{-1} = 0.919$$

LHS \neq *RHS*If $t_1/\tau = 2$

$$0.9 = \left(1 + 2 + \frac{2^2}{2}\right) e^{-2} = 0.676$$

LHS \neq *RHS*It means that the value of t_1/τ lies between 1 and 2.If $t_1/\tau = 1.5$

$$0.9 = \left(1 + 1.5 + \frac{1.5^2}{2}\right) e^{-1.5} = 0.808$$

LHS \neq *RHS*If $t_1/\tau = 1.1$

$$0.9 = \left(1 + 1.1 + \frac{1.1^2}{2}\right) e^{-1.1} = 0.90$$

LHS = *RHS*

$$\therefore t_1 = 1.1\tau$$

$$\text{Rise time} = t_2 - t_1 = 5.3\tau - 1.1\tau = 4.2\tau$$

(c) The rise time of three stages = 4.2τ

Rise timing single stage = 2.2τ

Ratio of the rise time of three stages to a single stage is equal to $4.2\tau/2.2\tau = 1.9$.

Example 3.12: An oscilloscope test probe shown in Fig. 3.30(a) has a cable capacitance of 50 pF . The input impedance of oscilloscope is $1 \text{ M}\Omega$ in parallel with 5 pF . Find the value of:

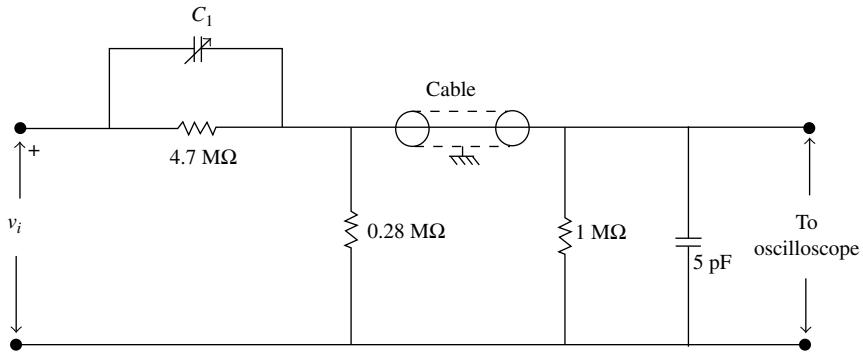


FIGURE 3.30(a) An attenuator probe

- (i) The capacitor for better performance;
- (ii) Attenuation of the probe;
- (iii) The input impedance of the compensated probe.

Solution: The input resistance of the oscilloscope = $R_i = 1 \text{ M}\Omega$

The capacitance of the oscilloscope = $C = 5 \text{ pF}$

The cable capacitance $C_b = 50 \text{ pF}$

The given circuit can be redrawn as shown in Fig. 3.30(b).

$$R_2 = 0.28 \text{ M}\Omega \parallel 1 \text{ M}\Omega = 0.2187 \text{ M}\Omega$$

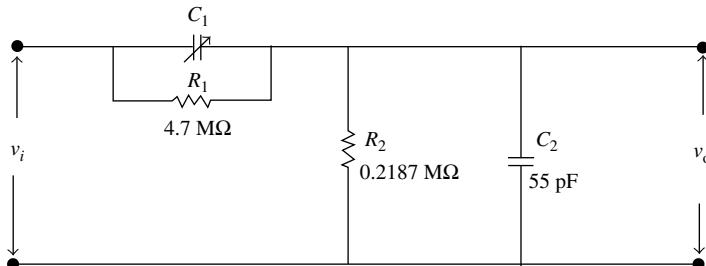


FIGURE 3.30(b) Equivalent circuit redrawn for Fig. 3.30(a)

- (i) In an attenuator the condition for perfect compensation is:

$$R_1 C_1 = R_2 C_2$$

$$\therefore C_1 = \frac{R_2 C_2}{R_1} = \frac{0.2187 \times 10^6 \times 55 \times 10^{-12}}{4.7 \times 10^6} = 2.559 \text{ pF}$$

The value of capacitor C_1 for better performance is $C = 2.559 \text{ pF}$.

$$(ii) \text{ The attenuation of the probe } \alpha = \frac{R_2}{R_1 + R_2} = \frac{0.2187 \times 10^6}{(4.7 + 0.2187) 10^6} = 0.044$$

$$(iii) \text{ The input impedance } Z_i = R_1 + R_2 = 4.7 \times 10^6 + 0.2187 \times 10^6 = 4.9187 \times 10^6 \Omega$$

Example 3.13: An ideal pulse generator produces a pulse of $250 \mu\text{s}$ duration with amplitude of 10 V and the duty cycle is 25 per cent. Find the amplitude, rise time, fall time after passing through the network shown in Fig. 3.31(a).

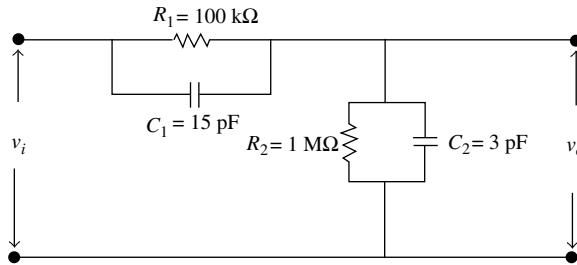


FIGURE 3.31(a) The given attenuator network

Solution: The network given is an attenuator with $R_1 = 100 \text{ k}\Omega = 0.1 \text{ M}\Omega$, $R_2 = 1 \text{ M}\Omega$, $C_1 = 15 \text{ pF}$; $C_2 = 3 \text{ pF}$, $t_p = 250 \mu\text{s}$, per cent duty cycle = 25%.

$$\text{Duty cycle} = \frac{t_p}{T} = 0.25 \quad T = \frac{250 \times 10^{-6}}{0.25} = 1000 \times 10^{-6} \text{ s}$$

The condition required for perfect compensation is $R_1 C_P = R_2 C_2$.

$$C_P = \frac{R_2 C_2}{R_1} = \frac{3 \times 10^{-12} \times 1 \times 10^6}{100 \times 10^3} = 30 \text{ pF}$$

$$C_1 = 15 \text{ pF}$$

As $C_1 < C_P$, the attenuator is said to be under compensated.

Initial response

$$v_o(o+) = \frac{C_1}{C_1 + C_2} v_i = \frac{15}{15 + 3} \times 10 = 8.33 \text{ V}$$

Final response

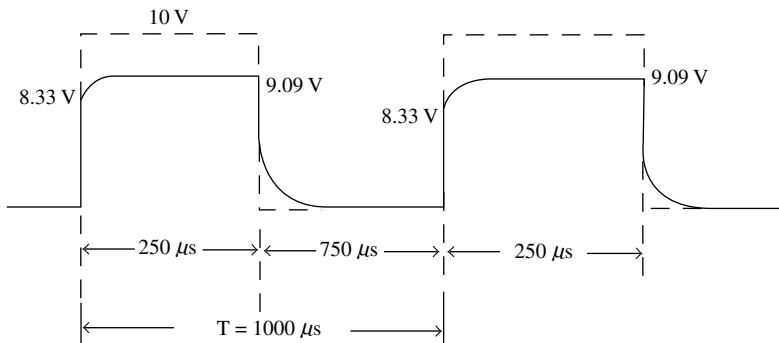


FIGURE 3.31(b) The output waveform

$$v_o(o+) = \left(\frac{R_2}{R_1 + R_2} \right) v_i = \frac{1}{0.1 + 1} \times 10 = 9.09 \text{ V}$$

$$t_r = 2.2 \left(\frac{R_1 R_2}{R_1 + R_2} \right) (C_1 + C_2) = 2.2 \left(\frac{0.1 \times 1}{0.1 + 1} \right) \times 10^6 (15 + 3) \times 10^{-12} = 3.6 \times 10^{-6} \text{ s}$$

Fall time = Rise time = 3.6×10^{-6} s

The output waveform is shown Fig. 3.31(b).

SUMMARY

- A low-pass circuit transmits low-frequency components and attenuates high frequencies.
- The cut-off frequency of a low-pass or high-pass circuit is the frequency at which the output is $1/\sqrt{2}$ (or 0.707) times the maximum output.
- The upper cut-off frequency of a low-pass circuit, f_2 is given by $1/2\pi RC$.
- f_2 is the bandwidth of the low-pass circuit.
- When a step is applied as input to a low-pass circuit, it takes a finite time for the output to reach the steady-state value. Rise time is defined as the time taken for the output to reach from 10 per cent of its final value to 90 per cent of its final value.
- The rise time t_r is given as 2.2τ ($= 0.35/f_2$).
- If n stages of low-pass circuits having rise times $t_{r1}, t_{r2}, \dots, t_{rn}$ are cascaded, then the rise time of the cascaded stages is given by $t_r = \sqrt{t_{r1}^2 + t_{r2}^2 + \dots + t_{rn}^2}$.
- A low-pass circuit behaves as an integrator if the time constant of the circuit is significantly greater than the time period of the input signal.
- Attenuators are essentially resistive networks employed to reduce the amplitude of the signal.
- An uncompensated attenuator is one in which the output depends on frequency.
- A compensated attenuator is one in which the output is independent of frequency.
- In an ideal attenuator, the output is independent of frequency.
- An attenuator is called a perfectly compensated attenuator if $v_o(0+) = v_o(\infty)$.
- An attenuator is treated as an over-compensated attenuator if $v_o(0+) > v_o(\infty)$.
- An attenuator in which $v_o(0+) < v_o(\infty)$ is called an under-compensated attenuator.
- At $t = 0+$, as capacitors behave as short circuit, $v_o(0+)$ is calculated by considering capacitors in an attenuator.
- At $t = \infty$, as the capacitors are fully charged, they behave as open circuit for dc. Hence, $v_o(\infty)$ is calculated considering only the resistances in an attenuator.
- A ringing circuit is an RLC circuit which produces (nearly) undamped oscillations.

MULTIPLE CHOICE QUESTIONS

- (1) If two stages of identical low-pass RC circuits are cascaded, the rise time of the cascaded stage is:
- $2t_r$
 - $\sqrt{2}t_r$
 - t_r^2
 - $0.2t_r$
- (2) A step input with certain pulse width is given to a low-pass RC circuit to transmit the same. To minimize the distortion:

- (a) Time constant must be equal to the pulse width
 (b) Time constant must be larger than the pulse width
 (c) Time constant must be smaller than the pulse width
 (d) Time constant and pulse width are independent of one another
- (3) The general solution for a single time constant circuit having initial and final values v_i and v_f respectively is given by:
- (a) $v_o = v_i + (v_f - v_i)e^{-t/\tau}$
 (b) $v_o = v_i + (v_i - v_f)e^{-t/\tau}$
 (c) $v_o = v_f + (v_i - v_f)e^{-t/\tau}$
 (d) $v_o = v_f + (v_f - v_i)e^{-t/\tau}$
- (4) The following type of attenuator will faithfully reproduce the signal which appears at its input terminals.
- (a) Under-compensated
 (b) Over-compensated
 (c) Perfectly compensated attenuator
 (d) Uncompensated attenuator
- (5) The transmission error, e_t when a ramp input with $RC \ll T$ is applied to a low-pass circuit is given by:
- (a) $\frac{T}{2RC}$
 (b) $\frac{T}{RC}$
 (c) $\frac{RC}{T}$
 (d) $\frac{RC}{2T}$
- (6) Integrators are invariably preferred over differentiators in analogue computer applications due to the following reason;
- (a) The gain of an integrator decreases with frequency
- (b) It is easier to stabilize
 (c) It is more convenient to introduce initial conditions
 (d) All of the above
- (7) The output of an integrator to a square wave input is:
- (a) Triangular wave
 (b) Square wave
 (c) Quadratic response
 (d) Spikes
- (8) The time required for the capacitor to get charged completely is nearly _____ the time constant.
- (a) five times
 (b) one time
 (c) equal to
 (d) two times
- (9) When $R_1C_1 = R_2C_2$, the attenuator is said to have achieved:
- (a) Perfect compensation
 (b) Over-compensation
 (c) Under-compensation
 (d) No compensation
- (10) When $R_1C_1 > R_2C_2$, the attenuator is said to have achieved:
- (a) Perfect compensation
 (b) Over-compensation
 (c) Under-compensation
 (d) No compensation
- (11) When $R_1C_1 < R_2C_2$, the attenuator is said to have achieved:
- (a) Perfect compensation
 (b) Over-compensation
 (c) Under-compensation
 (d) No compensation

SHORT ANSWER QUESTIONS

- (1) Obtain the expression for the bandwidth of a low-pass circuit.
- (2) The input to a low-pass RC circuit is a step of V . Obtain the expression for the output voltage.
- (3) What is meant by the rise time of a pulse? Obtain the expression for the rise time of a low-pass RC circuit.
- (4) The input to a low-pass circuit is a pulse of duration t_p and magnitude V . Plot its output when the time

- constant is very small and when the time constant is very large.
- (5) A symmetric square wave is applied as input to the low-pass circuit. Plot the output waveforms for different time constants.
 - (6) A ramp is applied as input to a low-pass circuit. Derive the expression for the transmission error, e_t .
 - (7) Show that a low-pass circuit can be used as an integrator if the time constant of the circuit is significantly larger than the time period of the input signal.
 - (8) What is an attenuator? Explain the drawbacks of an uncompensated attenuator.
 - (9) How can an uncompensated attenuator be modified as a compensated attenuator?
 - (10) Compare the responses of perfectly compensated, under-compensated and over-compensated attenuators.
 - (11) Illustrate, with a suitable diagram, how a compensated attenuator can be used as a CRO probe.
 - (12) Explain under which condition an RLC circuit behaves as a ringing circuit.

LONG ANSWER QUESTIONS

- (1) If a symmetric square wave referenced to 0 voltage is the input to a low-pass circuit, derive the expression for the steady-state voltage levels at the output. Plot the typical waveforms.
- (2) A ramp $v_i = \alpha t$ is applied as input to a low-pass RC circuit. Derive the expression for the output voltage. Plot the typical waveforms.
- (3) An exponential signal $v_i = V(1 - e^{-t/\tau_1})$ is the input to a low-pass RC circuit. Derive the

expressions for the output when (i) $\tau = \tau_1$ and (ii) $\tau \neq \tau_1$.

- (4) What is an uncompensated attenuator and its major limitations? Implement a compensated attenuator. Explain the conditions under which this is called a perfectly compensated, over-compensated and under-compensated attenuator.
- (5) Obtain the response of an RLC circuit under critically damped conditions.

UNSOLVED PROBLEMS

- (1) A pulse with zero rise time, an amplitude of 10 V and duration $10 \mu\text{s}$ is applied to an amplifier through a low-pass coupling network shown in Fig. 3p.1. Plot the output waveform to scale under the following conditions:
 - (i) $f_2 = 20 \text{ MHz}$,
 - (ii) $f_2 = 0.2 \text{ MHz}$.
- (2) A ramp shown in Fig. 3p.2 is applied to a low-pass RC circuit. Draw to scale the output waveform for the cases:
 - (i) $T = 0.2RC$,
 - (ii) $T = 10RC$.

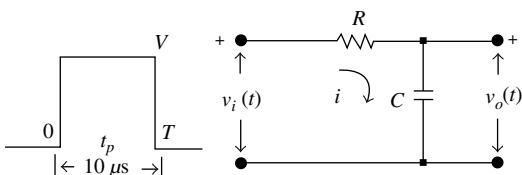


FIGURE 3p.1 The given coupling network with input

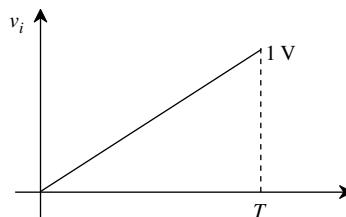


FIGURE 3p.2 The given input to the low-pass RC circuit

- (3) The input to a low-pass RC circuit is periodic and trapezoidal as shown in Fig. 3p.3. Find and sketch the steady-state output if $RC = 10 T_1 = 10 T_2$.

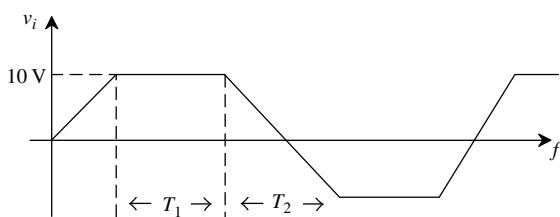


FIGURE 3p.3 The given input to the low-pass RC circuit

- (4) A 1 kHz symmetrical square wave of peak-to-peak voltage 20 V, as shown in Fig. 3p.4, is applied to a low-pass RC circuit with $R = 100 \Omega$, $C = 1 \mu F$. Sketch the output waveform to scale by determining the corner voltages.

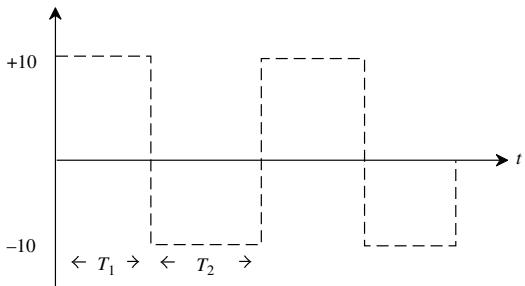


FIGURE 3p.4 The given input to the low-pass RC circuit

- (5) The input waveform shown in Fig. 3p.5 is applied to a low-pass RC network. Sketch the waveform of the voltage across the capacitor to scale for two cycles. The time constant of the RC circuit is 0.11 ms.

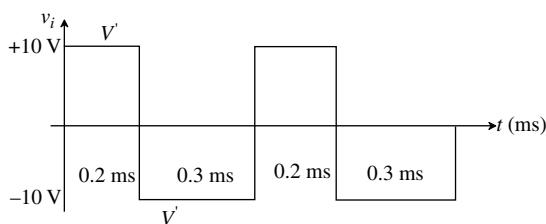


FIGURE 3p.5 The given input to a low-pass RC circuit

- (6) The periodic waveform shown in Fig. 3p.6 is applied to an RC integrating network whose time constant is $15 \mu s$. Sketch the output and calculate the maximum and minimum values of output voltage with respect to the ground.

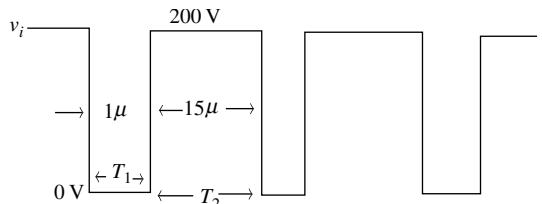


FIGURE 3p.6 The given input to a low-pass RC circuit

- (7) The waveform shown in Fig. 3p.7 is applied to a low-pass RC circuit. Sketch the output waveform to scale by determining the corner voltages for the following cases: (1) $RC = 20 T$, (2) $RC = T/20$.

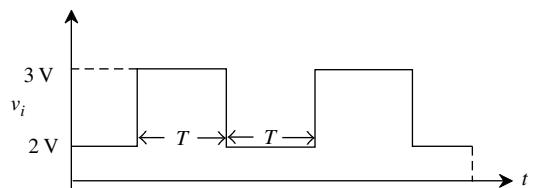


FIGURE 3p.7 The given input to the low-pass RC circuit

- (8) A square wave extends ± 0.5 V with respect to ground. The duration of the positive section is 0.1 s and the negative duration is 0.2 s, as shown in Fig. 3p.8. This waveform is applied as a input to a low-pass RC circuit whose time constant is 0.2 s, sketch the steady-state output waveform to scale, and find the maximum and minimum values of the output.

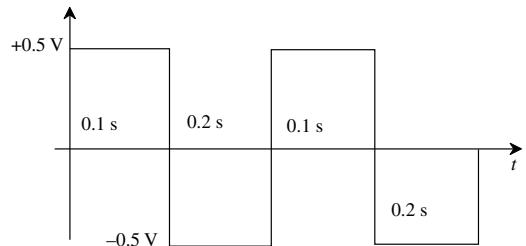


FIGURE 3p.8 The given input to the low-pass RC circuit

- (9) A pulse of amplitude 10 V and pulse width of $10 \mu s$, as shown in Fig. 3p.9, is applied to an RC circuit with $R = 100 \text{ k}\Omega$ and $C = 0.1 \mu F$. Sketch the capacitor voltage waveform to scale.

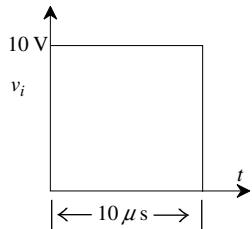


FIGURE 3p.9 The given input to the low-pass RC circuit

- (10) An oscilloscope has an input impedance of $10 \text{ M}\Omega$ in parallel with 25 pF . Design a $10:1$ voltage divider for the oscilloscope. Determine the values of the input resistance and the capacitance for the compensated divider.
- (11) The attenuator shown Fig. 3p.10 has $R_1 = R_2 = 1 \text{ M}\Omega$, $C_2 = 50 \text{ pF}$. Find the magnitudes of the initial and final responses and draw the output waveform to scale for $C_1 = 50 \text{ pF}$, 75 pF and 25 pF .

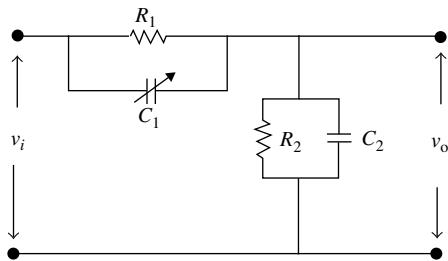


FIGURE 3p.10 The given attenuator circuit

- (12) The periodic ramp with $T_1 = T_2 = 2\tau$, shown in Fig. 3p.11, is applied to a low-pass RC circuit. Find the equations to determine the steady-state output waveform. The initial voltage on the condenser is V_1 . Find the maximum and minimum value of the voltage and plot the waveform.

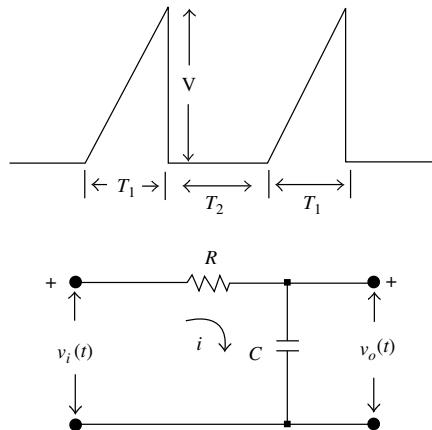


FIGURE 3p.11 The given periodic ramp input and the low-pass circuit

- (13) For a low-pass RC circuit, it is desired to pass a 3 ms sweep for a ramp input with less than 0.4 per cent transmission error. Calculate the upper 3-dB frequency.
- (14) A step input of 20 V is applied to an RC integrating circuit. Calculate the upper 3-dB frequency and the value of resistance, if the rise time and capacitor values are $100 \mu\text{s}$ and $0.28 \mu\text{F}$, respectively.

CHAPTER 4

Non-linear Waveshaping: Clipping Circuits and Comparators

LEARNING OBJECTIVES

After reading this chapter, you will be able to:

- Understand the use of diodes and transistors as switches
 - Describe various series- and shunt-clipping circuits and their combinations
 - Understand the principle of operation of two-level emitter-coupled transistor clippers and noise clippers
 - Describe simple diode comparators and double differentiators as amplitude comparators
 - Explain the applications of comparators
-

4.1 INTRODUCTION

Diodes, transistors and field-effect transistors (FETs) can be used as linear circuit elements if the operation is restricted to that limited region in the characteristic in which it can be approximated to a straight-line characteristic (small-signal conditions). However, when the input is increased further (under large-signal conditions), these devices no longer behave as linear circuit elements; and the operation can go into the non-linear region of the characteristic. When these non-linear circuit elements are used in waveshaping applications, the resultant process is termed *non-linear waveshaping*. In communication systems, sometimes it becomes necessary to eliminate a portion of the input signal, either at a single level or at two independent levels. The circuits that accomplish this task are called clipping circuits. These circuits can also be used to eliminate the noise associated with an input signal. Such clipping circuits are called noise clippers. The parameters of these devices can change with variations in temperature. Thus, in applications where precision is required, it becomes necessary to provide temperature compensation so that temperature variations do not influence the behaviour of the circuit.

Amplitude comparators (also called comparators) are circuits that compare an input with a reference signal and deliver a high output the moment the input reaches the reference level. A simple diode comparator circuit is discussed and possible techniques to improve the sharpness of the break region are presented in this chapter. A comparator circuit may be used to control other circuits with the help of its output; the instant the input reaches a predefined reference level.

4.2 DIODES AS SWITCHES

A physical switch either makes or breaks a contact between two nodes, meaning the resistance between the nodes is either 0 or ∞ . When electronic devices are used as switches, no physical contact is either made or broken; the resistance between the nodes is made either too small (ideally 0) or too large (ideally ∞). Diodes can be used as switches. We shall discuss the application of semiconductor and Zener diodes as switches in this section.

4.2.1 The Semiconductor Diode as a Switch

A semiconductor diode, used as a switch, is ON when forward-biased and OFF when reverse-biased. As such, this device may be used as a static switch. The voltage between the anode (A) and the cathode (K) is ideally zero; and hence, the resistance is zero when the switch is closed. In practice, however, there is a finite forward resistance (R_F), typically of a few ohms, as shown in Fig. 4.1(a). When the switch is open, ideally the current should be zero and the resistance infinity. However, in actuality, a diode will have a finite reverse resistance, R_r which is typically few mega ohms, as shown in Fig. 4.1(b).

Figure 4.2 shows the typical V–I characteristic of a semiconductor diode. Let the reverse saturation current be typically $50 \mu\text{A}$. When compared to this, the forward current is as large as 100 mA . Hence, the reverse current is negligible when compared to the forward current. This diode can, thus, be used as a one-way device, i.e., as a switch. Let the diode be an ideal diode. The V–I characteristic of an ideal diode is represented in Fig. 4.3.

However, a diode has a barrier potential, and the idealized characteristic of silicon and germanium diodes are represented in Figs. 4.4(a) and (b), respectively.

Consider the diode circuit in Fig. 4.5(a). Now let the input (v_i) to such a diode switch be as shown in Fig. 4.5(b). The currents in the switch are represented in Fig. 4.5(c).

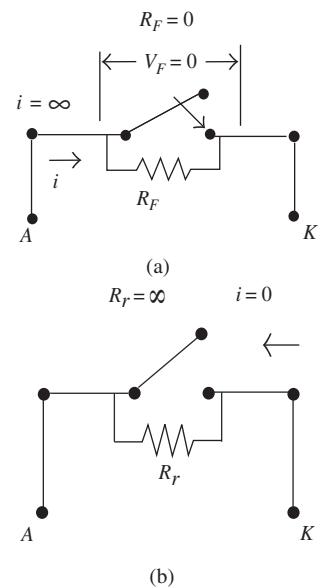


FIGURE 4.1 (a) Diode as a closed switch (b) Diode as an open switch

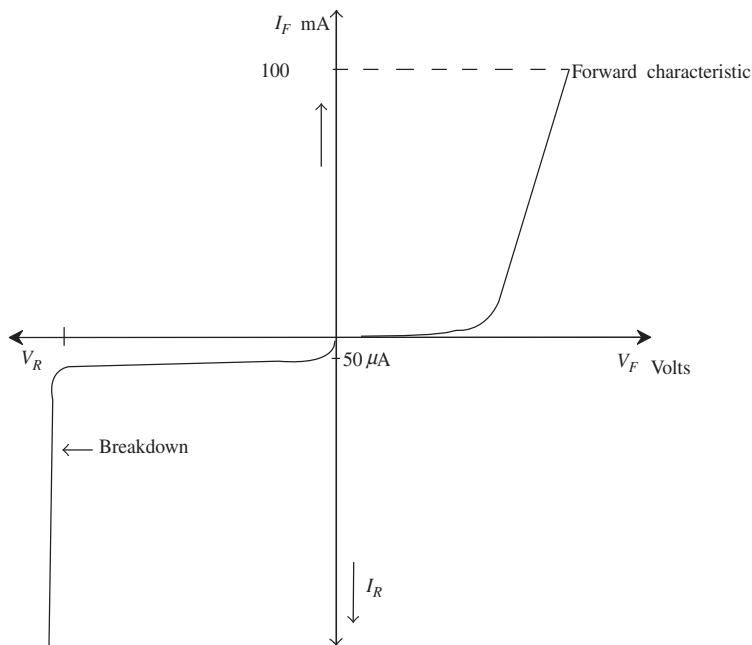


FIGURE 4.2 The V–I characteristic of a practical diode

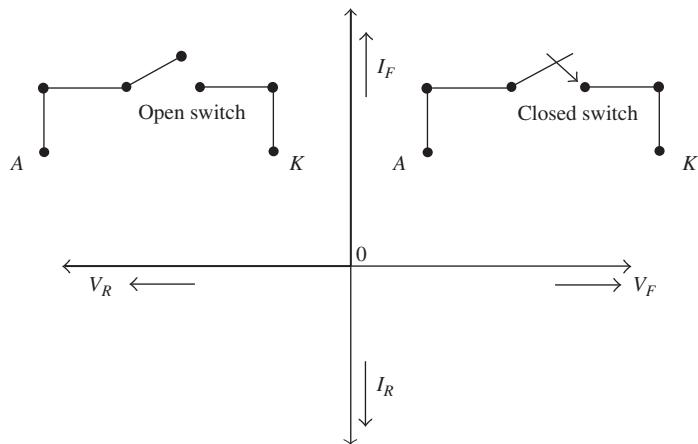


FIGURE 4.3 The V-I characteristic of an ideal diode

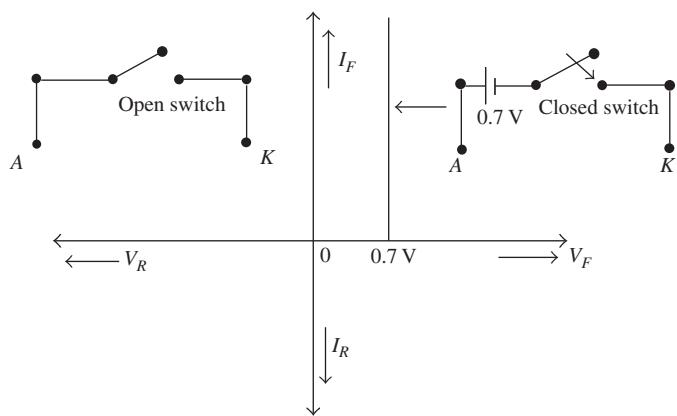


FIGURE 4.4(a) The idealized V-I characteristic of a silicon diode

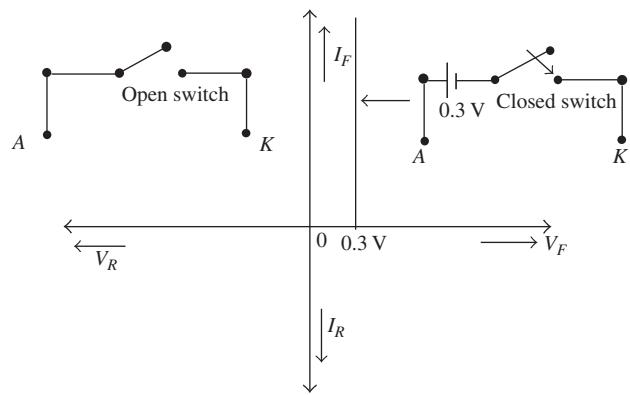


FIGURE 4.4(b) The idealized V-I characteristic of a germanium diode

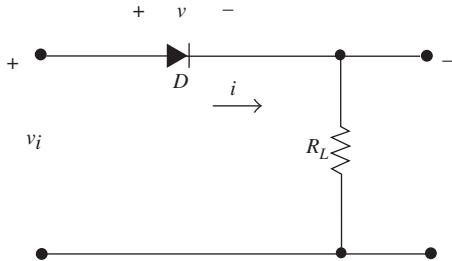


FIGURE 4.5(a) A simple diode circuit

During the period 0 to T_1 , the input forward-biases the diode. If the forward resistance of D is very small when compared to R_L , then $I_F = V_F/R_L$.

At T_1 , the polarity of the input reverses and the reverse voltage is V_R . Thus, $I_R (= -V_R/R_L)$ remains large for a time duration called the storage time t_s , though the diode is expected to go into the OFF state at T_1 . This is because of the presence of a large number of stored charges on either side of the junction in the forward-biased diode. After this time interval, charges get cleaned up, gradually reducing the current to a value I_s after a time interval t_t called the transition time. At this instant, the diode is said to be switched from the ON state into the OFF state. It can be seen from Fig. 4.5(c) that a finite time elapses before the current is the reverse saturation current. This indicates that a diode is switched from the ON state into OFF state not exactly at T_1 , when the input reverse-biases the diode but only after a time interval when the reverse current reaches I_s . The time interval ($t_s + t_t$) is called the reverse recovery time of the diode, t_{rr} .

This is the time interval for which the switch is still ON. The reverse recovery time, t_{rr} , may thus be defined as the time taken for the diode reverse current to fall to 10 per cent of its forward-current value when the diode is suddenly switched from the ON to the OFF state. If the forward current I_F , when the diode is ON, is 10 mA, then the time taken for this current to fall to 1 mA is the reverse recovery time. This can also be termed as the “turn-off” time of the diode. Similarly, when the device switches from the OFF state to the ON state, there is a small turn-on time, which is small when compared with the turn-off time. These time intervals tell us how fast we can switch the diode from one state to the other. Further, a reverse-biased diode has a transition capacitance C_T between the anode and the cathode. At low frequencies, this capacitance has no appreciable influence. However, at high frequencies, this offers low reactance, which will have to be taken into consideration when we consider diode series and shunt clippers.

4.2.2 The Zener Diode as a Switch

The V-I characteristic of a Zener diode is represented in Fig 4.6(a). If idealized, this characteristic may be represented as in Fig 4.6(b).

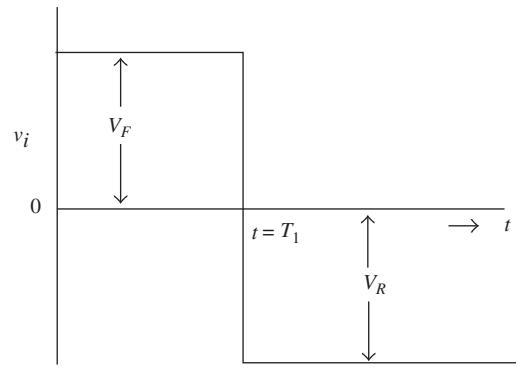


FIGURE 4.5(b) Suddenly changing input

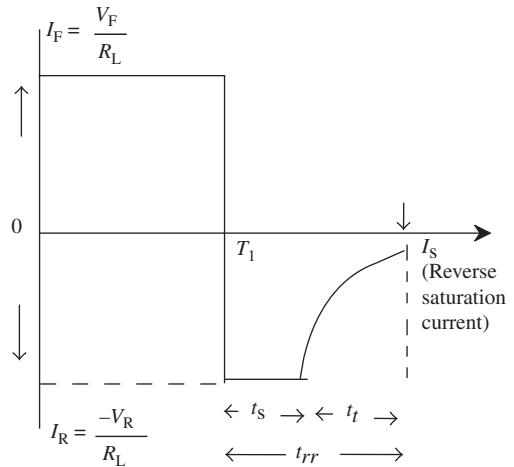


FIGURE 4.5(c) Diode currents

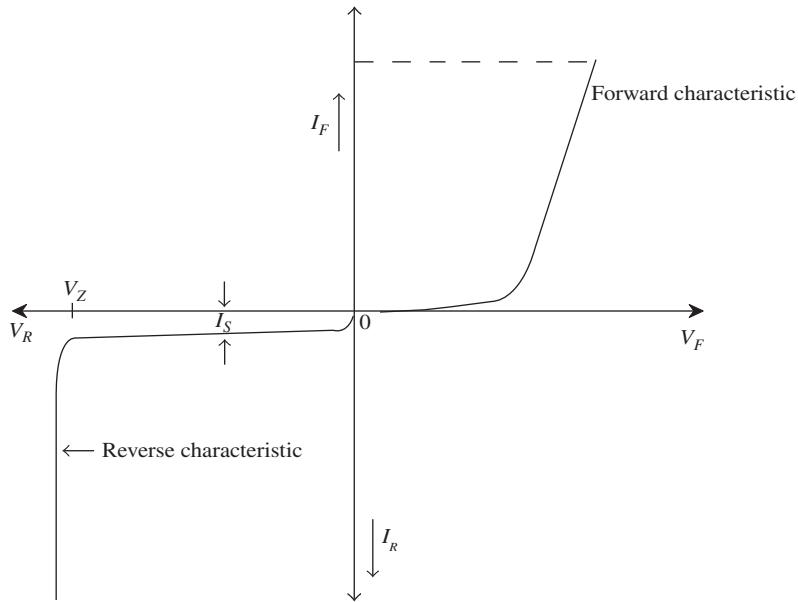


FIGURE 4.6(a) The V-I characteristic of a Zener diode

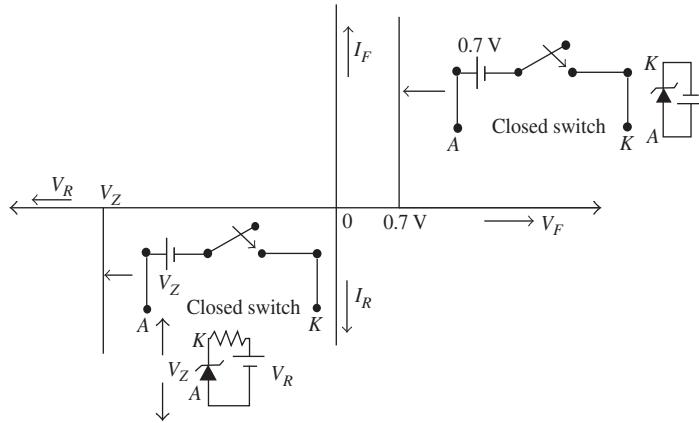


FIGURE 4.6(b) Idealized V-I characteristic of a Zener diode

An ideal Zener diode is ON for $V_F = 0$, whereas a practical Si-Zener conducts when $V_F = 0.7$ V. It is also switched ON when reverse-biased and when V_R is V_Z . Normally, a Zener diode is always operated in the reverse-biased condition. It can be considered as a switch that is open for $V_R < V_Z$ and closed for $V_R = V_Z$. These switches can be used to alter the shape of an input signal.

4.3 CLIPPING CIRCUITS

Clipping circuits select that part of the signal which lies above and below a reference level. Depending on whether the diode is connected in series with the load or in shunt with the load, these circuits are called either series-clipping circuits or shunt-clipping circuits.

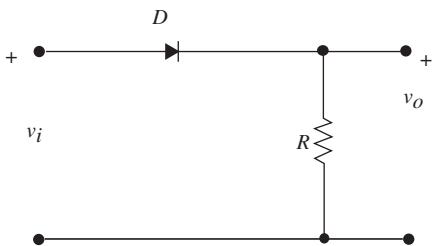


FIGURE 4.7(a) Series clipper that clips the negative half-cycles

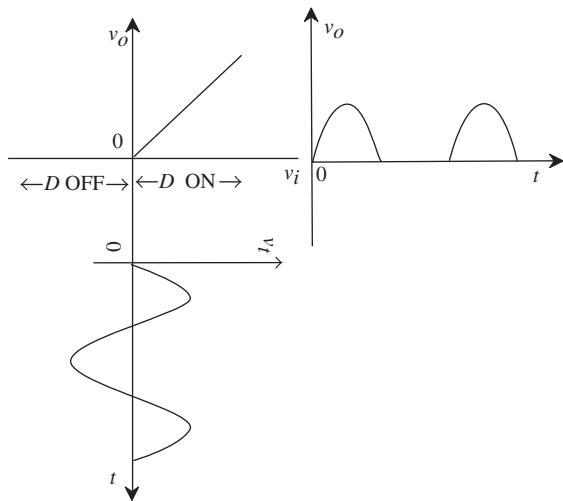


FIGURE 4.7(b) The transfer characteristic, input waveform and output waveform of a series clipper that clips negative half-cycles

4.3.1 Series Clippers

Consider the series-clipping circuit shown in Fig. 4.7(a) and its transfer characteristic (a plot that gives the relationship between the input and the output voltages) with input and output waveforms in Fig. 4.7(b). When v_i is positive, D conducts and the input signal is transmitted to the output, $v_o = v_i$. When v_i is negative, $v_o = 0$. There is no transmission of the signal as the diode is assumed to be ideal. The output is in the form of half-cycles, similar to the output of a half-wave rectifier; in fact, it is a half-wave rectifier.

Consider another clipping circuit shown in Fig. 4.8(a) and its transfer characteristic with input and output waveforms in Fig. 4.8(b). When v_i is negative, D conducts and the input v_i is transmitted to the output (i.e., $v_o = v_i$). When v_i is positive, D is OFF and $v_o = 0$. The signal is not transmitted to the output. The output once again is in the form of half-cycles.

In our discussion so far, we have assumed the diode to be ideal and have neglected the influence of the transition capacitance C_T that exists between the anode and the cathode of a reverse-biased diode. We now take into account this parameter to understand how this affects the output of a series clipper.

Consider the circuit shown in Fig. 4.8(a) when reverse-biased (during the positive half-cycle), to which, instead of a sinusoidal signal, a square-wave input is applied. So far we have assumed that during the period when the diode is OFF, there is no transmission. However, on account of the transition capacitance C_T being present, the circuit now behaves as a high-pass circuit [see Fig. 4.8(c)] and the input can now be transmitted to the output, though with distortion. Also, even if a sinusoidal signal is applied as input, at high frequencies, the capacitor offers a smaller reactance due to which the input can be transmitted to the output. This is the major limitation of a series clipper. Thus, a series clipper works best at low frequencies.

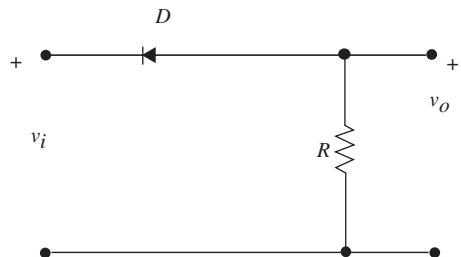


FIGURE 4.8(a) Series clipper that clips positive half-cycles

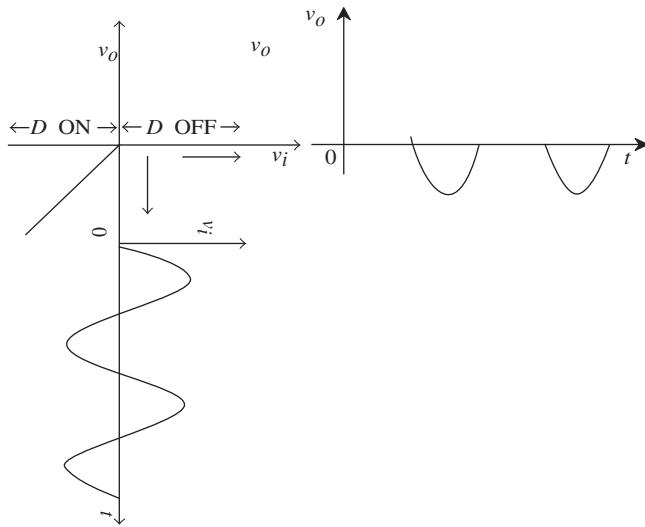


FIGURE 4.8(b) The transfer characteristic, input waveform and output waveform of a series clipper that clips positive half-cycles

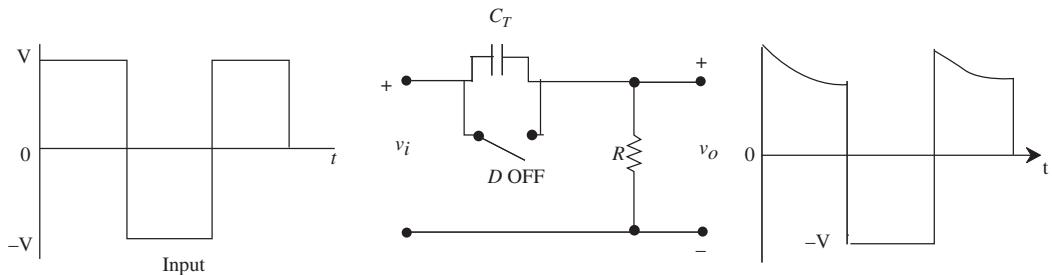


FIGURE 4.8(c) Series clipper that is expected to eliminate positive half-cycles

Base Clipper. If a battery (V_R) is included in the series-clipping circuit, such that the diode is connected in series with the load, as shown in Fig. 4.9(a), these circuits are called biased series clippers. The circuit in Fig. 4.9(a) clips the positive going input at its base, so it is also referred to as a base clipper.

Assume that the diode is ideal in the circuit shown in Fig. 4.9(a).

For $v_i < V_R$, D is OFF; hence, $v_o = V_R$. The resultant circuit is shown in Fig. 4.9(b).

For $v_i \geq V_R$, D is ON; hence, $v_o = v_i$. The resultant circuit is shown in Fig. 4.9(c).

The transfer characteristic is shown in Fig. 4.9 (d).

In the output of this circuit, the base portion of the input during the positive half-cycle is eliminated and only the positive peak is available when the input is either more than or equal to V_R . Hence, the name base clipper.

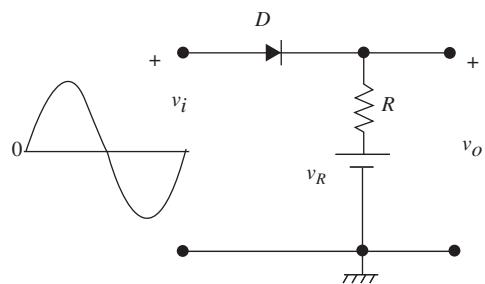


FIGURE 4.9(a) A base clipper

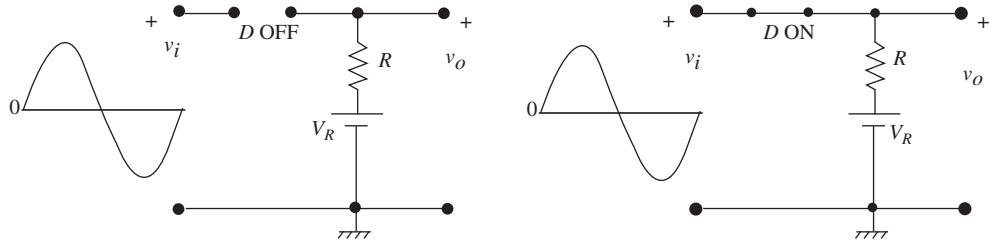


FIGURE 4.9(b) A base clipper with \$D\$ OFF; and (c) with \$D\$ ON

The battery V_R is assumed to have zero internal resistance. However, in practice, any voltage source will have some internal resistance R_S which appears in series with the battery. Now, as this R_S in the present case appears in series with R , where $R \gg R_S$, the performance of the circuit is not affected. This could be termed as an advantage of series clippers.

Positive-Peak Clipper. Consider the circuit shown in Fig. 4.10(a). As this circuit eliminates the positive peak of the input at the output, it is called a positive peak clipper.

For $v_i < V_R$, D is ON, and the resultant circuit is shown in Fig. 4.10(b). Hence, $v_o = v_i$. And for $v_i > V_R$, D is OFF, as shown in Fig. 4.10(c). Hence, $v_o = V_R$. Thus, the transfer characteristic, the input and output waveforms are as shown in Fig. 4.10(d). In the output of the circuit, the positive peak of the input above V_R is eliminated. Hence, this circuit is called a positive peak clipper.

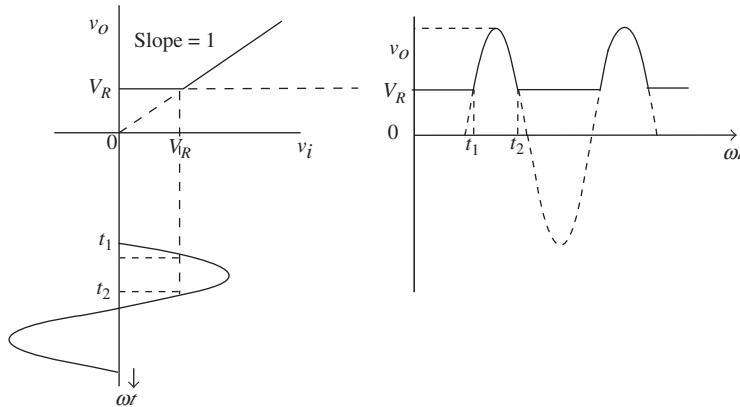


FIGURE 4.9(d) The transfer characteristic of a base clipper with input and output waveforms

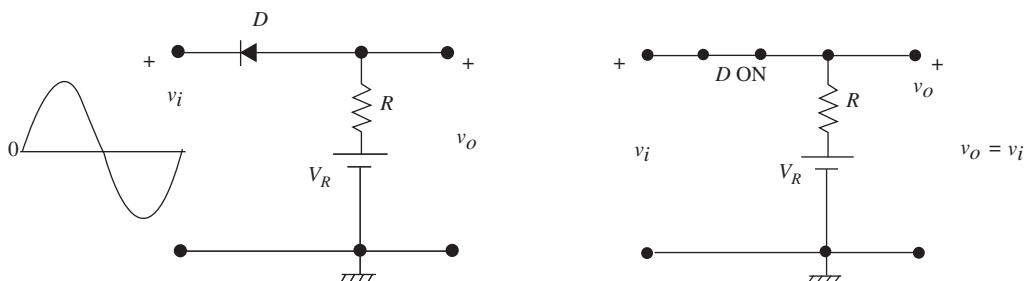


FIGURE 4.10(a) Positive-peak clipper

FIGURE 4.10(b) Circuit of Fig. 4.10(a) when D is ON

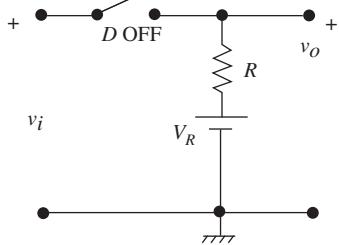


FIGURE 4.10(c) Circuit of Fig. 4.10(a) when D is OFF

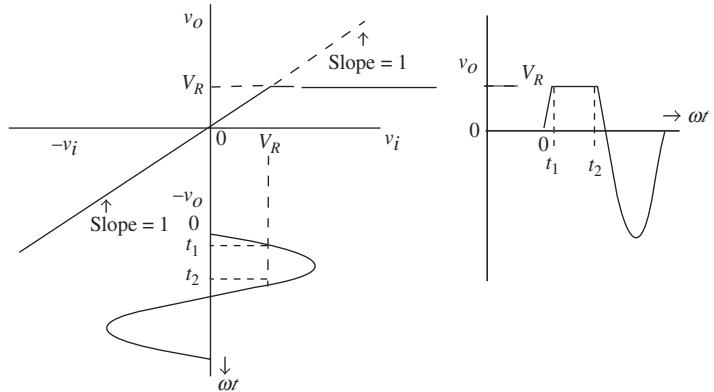


FIGURE 4.10(d) Transfer characteristic of a positive peak clipper in Fig. 4.10(a) with input and output waveforms

4.3.2 Shunt Clippers

A shunt clipper is one in which the diode is used as a shunt element. Consider a simple shunt clipper shown in Fig. 4.11(a). As long as the input is positive, D conducts and the output $v_o = 0$. When the input is negative, D is OFF and an open circuit. The input is transmitted to the output. The transfer characteristic, the input and output waveforms are shown in Fig. 4.11(b). This circuit clips the positive half-cycle. The same thing is done by the circuit shown in Fig. 4.8(a). The only difference is that the former is a series clipper and the latter a shunt clipper.

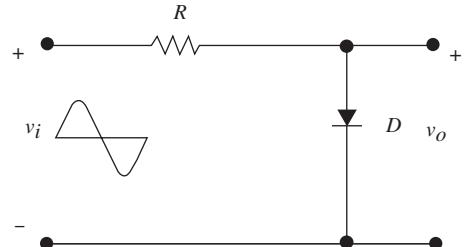


FIGURE 4.11(a) A shunt clipper that clips the positive half-cycle

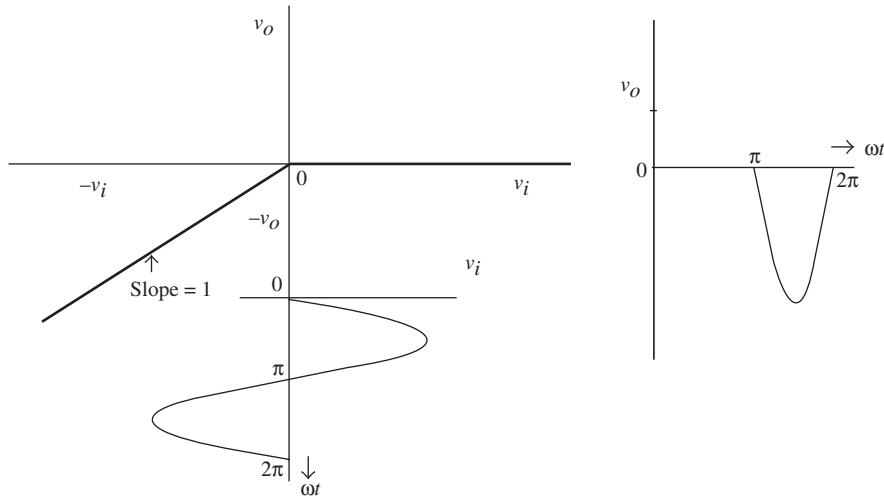


FIGURE 4.11(b) The transfer characteristic, the input and output waveforms

Till now we assumed that the diode to be ideal, that is, forward resistance of the diode was taken to be zero. A practical diode, however, has typically R_f in the range of 50Ω to 100Ω . Therefore, when D is ON, with R_f taken into account, the circuit is as shown in Fig. 4.11(c). In this circuit: $v_o = v_i R_f / (R_f + R)$.

This means that though the output is expected to be 0, there is a small sinusoidal swing at the output. This is one limitation of a shunt clipper. When D is OFF, it should ideally behave as an open circuit. But in a reverse-biased diode, we have transition capacitance. Taking C_T into account, Fig. 4.11(a) can be redrawn as shown in Fig. 4.11(d).

Now, when the diode is OFF, with a square wave as the input, we ideally expect the negative half-cycle of the input only at the output. However, when C_T is considered, the shunt clipper is a low-pass circuit. Hence, the output would rise with a time constant RC_T . This is another limitation of a shunt clipper. Consider an alternative form of the shunt clipper as shown in Fig. 4.12(a). The transfer characteristic along with the input and output waveforms is shown in Fig. 4.12(b). The negative half-cycle is completely eliminated as is done by the circuit in Fig. 4.7(a).

Now let us consider a slightly different shunt clipper called a biased shunt clipper that clips the positive half-cycle of the input waveform at a reference level V_R [see Fig. 4.13 (a)]. For the circuit in Fig. 4.13(a), the transfer characteristic is drawn in Fig. 4.13(b).

When $v_i < V_R$, D is OFF, hence, $v_o = v_i$.

When $v_i \geq V_R$, D is ON, hence, $v_o = V_R$.

To calculate and plot the output of the clipping circuit shown in Fig. 4.13(a), consider a sinusoidal input signal varying as $V_m \sin \omega t$.

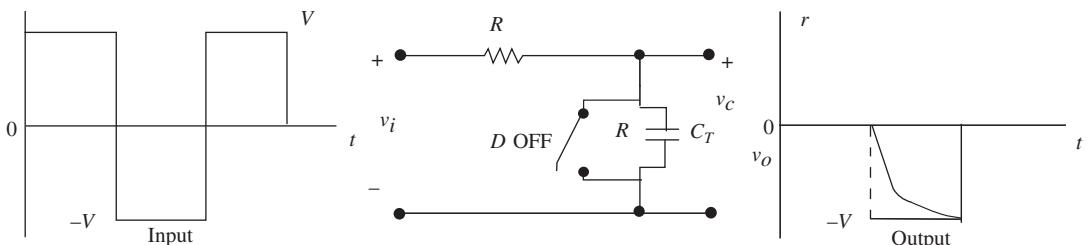


FIGURE 4.11(d) The shunt clipper considering C_T

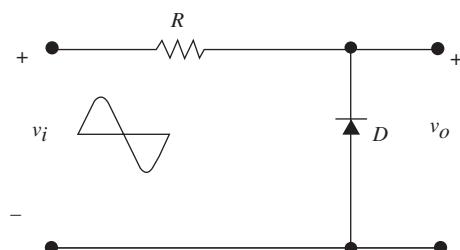


FIGURE 4.12(a) A shunt clipper that clips the negative half-cycle

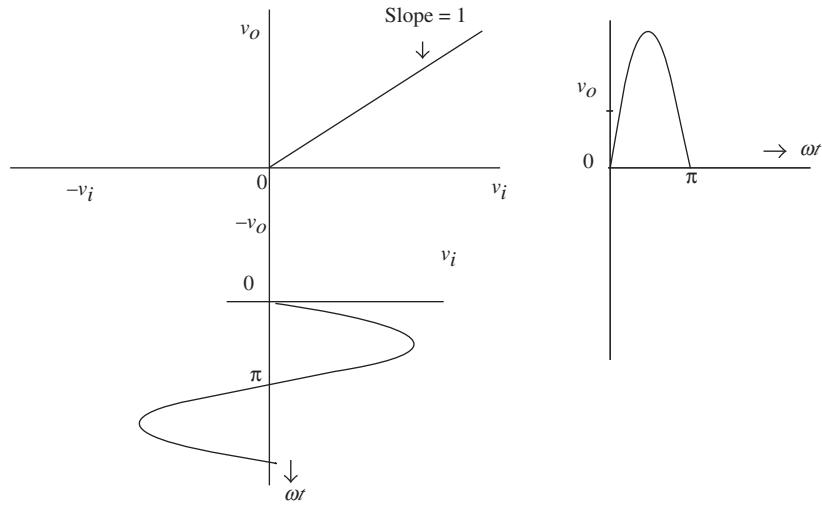


FIGURE 4.12(b) The transfer characteristic of the clipper in Fig. 4.12(a)

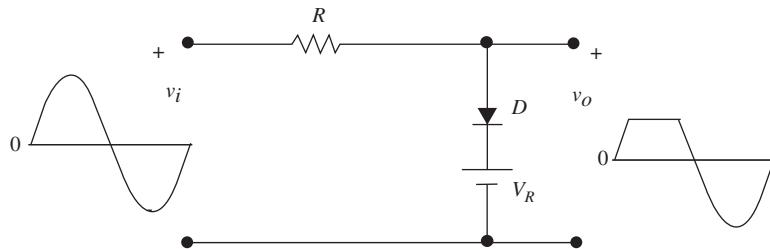


FIGURE 4.13(a) A positive peak clipper

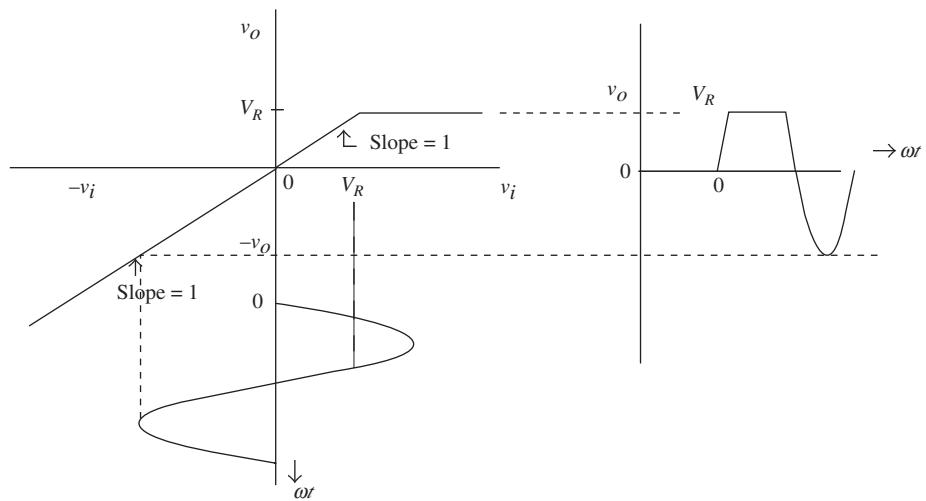


FIGURE 4.13(b) The transfer characteristic with input and output waveforms of the circuit in Fig. 4.13(a)

Case 1

When the diode is ideal, its R_f is 0 and R_r is ∞ .

$$v_i < V_R, \quad D \text{ is OFF}, \quad v_o = v_i$$

$$v_i \geq V_R, \quad D \text{ is ON}, \quad v_o = V_R$$

The output is as shown in Fig. 4.13(b).

Case 2 When the diode is not ideal and has finite forward and reverse resistances

- (a) When the diode is ON, it has a forward resistance R_f . For $v_i > V_R$ the resultant circuit is as shown in Fig. 4.13(c). Here:

$$v_o = (v_i - V_R) \times \frac{R_f}{R + R_f} + V_R$$

Thus, v_o is maximum when v_i is maximum that is when $v_i = V_m$.

If $V_m \approx 2V_R$

$$v_{o(\max)} = (2V_R - V_R) \times \frac{R_f}{R + R_f} + V_R = V_R \left(\frac{R_f}{R + R_f} + 1 \right) = V_R \left(\frac{R + 2R_f}{R + R_f} \right)$$

If the source V_R has an internal resistance R_s , $v_{o(\max)}$ computed using $R_{f1} = (R_f + R_s)$, instead of R_f . R_s will influence the slope of the transfer characteristic. This could be another drawback of a shunt clipper.

- (b) When $v_i < V_R$, the diode is OFF and the reverse resistance of the diode is R_r . The resultant circuit that enables us to calculate v_o is given in Fig. 4.13(d).

v_o is minimum when v_i is at its negative maximum, i.e., $v_i = -V_m \approx -2V_R$. Therefore,

$$\begin{aligned} v_{o(\min)} &= (v_i - V_R) \times \frac{R_r}{R + R_r} + V_R = (-2V_R - V_R) \times \frac{R_r}{R + R_r} + V_R \\ &= (-3V_R) \times \frac{R_r}{R + R_r} + V_R = V_R \left(1 - \frac{3R_r}{R + R_r} \right) = V_R \left(\frac{R + R_r - 3R_r}{R + R_r} \right) \\ &= V_R \left(\frac{R - 2R_r}{R + R_r} \right) \end{aligned}$$

In this case, R_s of the battery will not influence the output in any way because $R_r \gg R_s$. R is chosen based on the following considerations.

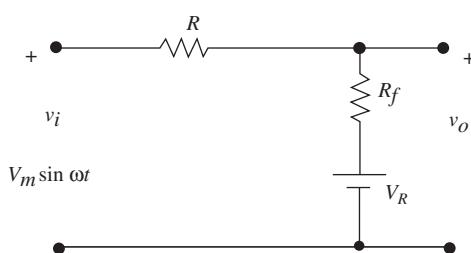


FIGURE 4.13(c) Circuit when D is ON and has a finite forward resistance R_f

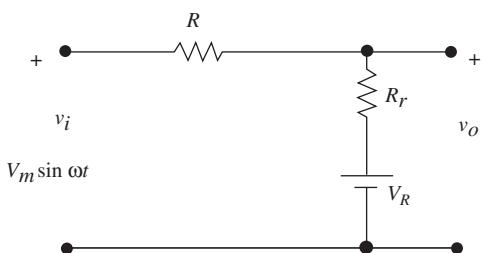


FIGURE 4.13(d) Circuit when D is OFF and has a finite reverse resistance R_r

Consider the circuit shown in Fig. 4.11(a). During the transmission period, the diode is OFF, offering a large reverse resistance R_r . For the input to be transmitted to the output terminals with negligible loss of signal, R_r should be much larger than R . This requirement says that:

$$R_r = aR \quad (4.1)$$

where a is a large number. Therefore,

$$R = \frac{R_r}{a} \quad (4.2)$$

When the diode is ON, the output signal is small and is said to be attenuated. This condition stipulates that R should be significantly larger than R_f , the forward resistance of the diode. This requirement means

$$R = aR_f \quad (4.3)$$

From Eqs. (4.2) and (4.3):

$$R^2 = R_r R_f \quad (4.4)$$

or

$$R = \sqrt{R_f R_r} \quad (4.5)$$

R is chosen as the geometric mean of R_f and R_r .

$$a = \sqrt{\frac{R_r}{R_f}} \quad (4.6)$$

To illustrate how to plot the output, consider Example 4.1.

E X A M P L E

Example 4.1: For the clipping circuit shown in Fig. 4.13(a), $V_R = 10$ V, $V_m = 20$ V, $R_f = 50 \Omega$, $R = 10 \text{ k}\Omega$ and $R_r = 100 \text{ k}\Omega$. Calculate and plot the output.

Solution:

$$v_{o(\max)} = V_R \left(\frac{R + 2R_f}{R + R_f} \right)$$

$$v_{o(\max)} = 10 \left(\frac{10 + 2 \times 0.05}{10 + 0.05} \right) = 10 \left(\frac{10.1}{10.05} \right) = 10.05 \text{ V}$$

$$v_{o(\min)} = V_R \left(\frac{R - 2R_f}{R + R_f} \right) = 10 \left(\frac{10 - 2 \times 100}{10 + 100} \right) = 10 \left(\frac{-190}{110} \right)$$

$$v_{o(\min)} = -17.27 \text{ V}$$

The waveforms of the clipping circuit shown in Fig. 4.13(a); (i) when the diode is ideal and (ii) when the diode has $R_f = 50 \Omega$ and $R_r = 100 \text{ k}\Omega$ are plotted in Fig. 4.13(e).

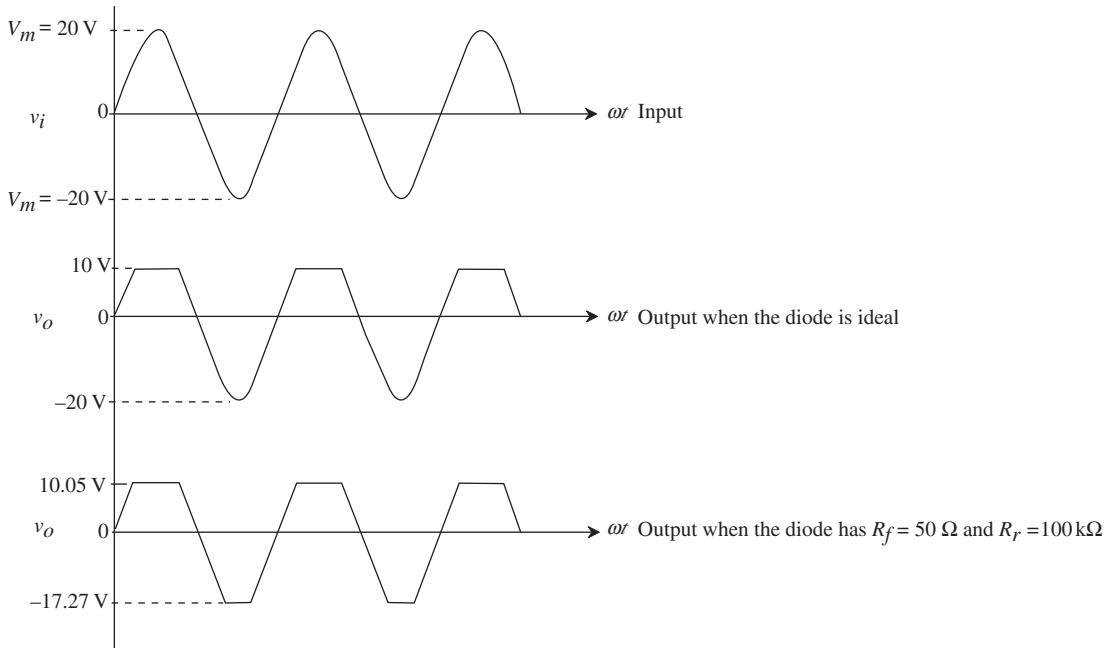


FIGURE 4.13(e) The input and output waveforms of the clipping circuit in Fig. 4.13(a)

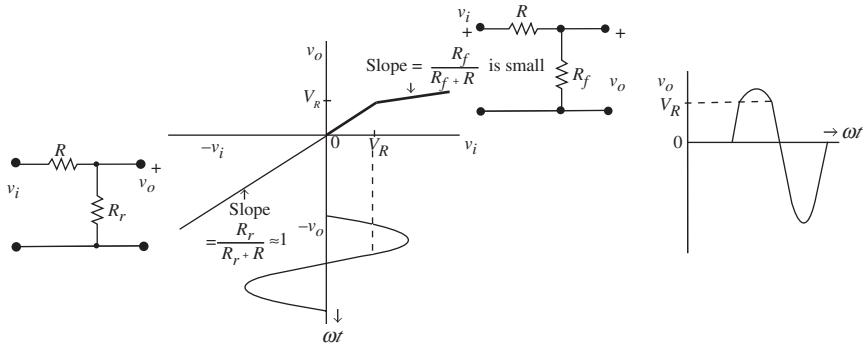
The transfer characteristic in Fig. 4.13(b) is drawn on the assumption that the diode forward resistance is ideally zero. However, in practice, there is a small forward resistance R_f , which, when accounted for, will not ensure flat clipping at V_R in the output, as shown in Fig. 4.13(f).

The circuit shown in Fig. 4.14(a) is a base clipper. This circuit is similar to the one shown in Fig. 4.13(a) except in the fact that the polarity of the diode is reversed here. When this is done, the positive peak clipper becomes a base clipper.

For the circuit in Fig. 4.14(a), the transfer characteristic is drawn in Fig. 4.14(b).

When $v_i < V_R$, D is ON and $v_o = V_R$.

When $v_i \geq V_R$, D is OFF and $v_o = v_i$.

FIGURE 4.13(f) The transfer characteristic and output, considering R_f

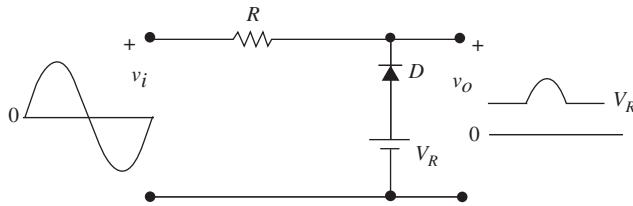


FIGURE 4.14(a) A base clipper

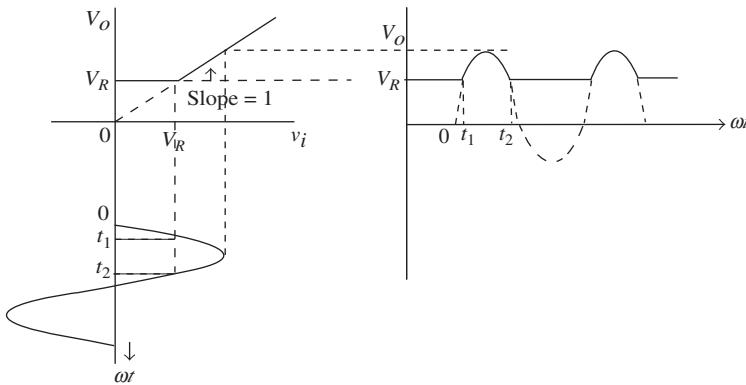


FIGURE 4.14(b) The transfer characteristic of the circuit in Fig. 4.14(a) with input and output

There can be many variations of one-level clippers. The relevant one level shunt- and series-clipping circuits along with transfer characteristics and output waveforms are summarized in Figs. 4.15(a) and Fig. 4.15(b) respectively, with a sinusoidal signal as input.

Clipping circuits are used to either select or eliminate a part of the waveform. As an example, consider the output of a low-pass circuit for a square-wave input as shown in Fig. 3.7(b). When τ is small, the output rises exponentially to reach V' or V'' , resulting in a distortion in the shape of the signal at the output. If a perfect square wave though with smaller amplitude is needed, we can eliminate the exponential part of the output by using peak clippers. Another example could be an astable multivibrator, where, as we shall see later, the square wave generated may not have sharp rising edges. If the astable multivibrator is required to derive a perfect square wave, we can use peak clippers. Similarly circuits shown in Figs. 2.21(a) and 2.21(b) are used to eliminate negative and positive spikes respectively. Depending on the requirement, we can use either a specific clipper or a combination.

4.3.3 Two-level Clippers

We have considered clippers which clip the input at one level. Let us now consider clippers which clip the signal at two independent levels. Two diode clippers may be used in a cascade to limit the output at two independent levels. If a positive-peak clipper and a negative-peak clipper are used in a pair, the resultant circuit is called a two-level clipper. If the positive and negative peaks are clipped at the same level, the two-level clipper is called a limiter. On the other hand, if a positive-peak clipper and a positive-base clipper are connected in tandem, the circuit is called a positive slicer.

Slicers. The input can be clipped at two independent levels, either during the positive going half-cycle or during the negative going half-period. If the input is clipped at two levels during the positive going half-cycle,

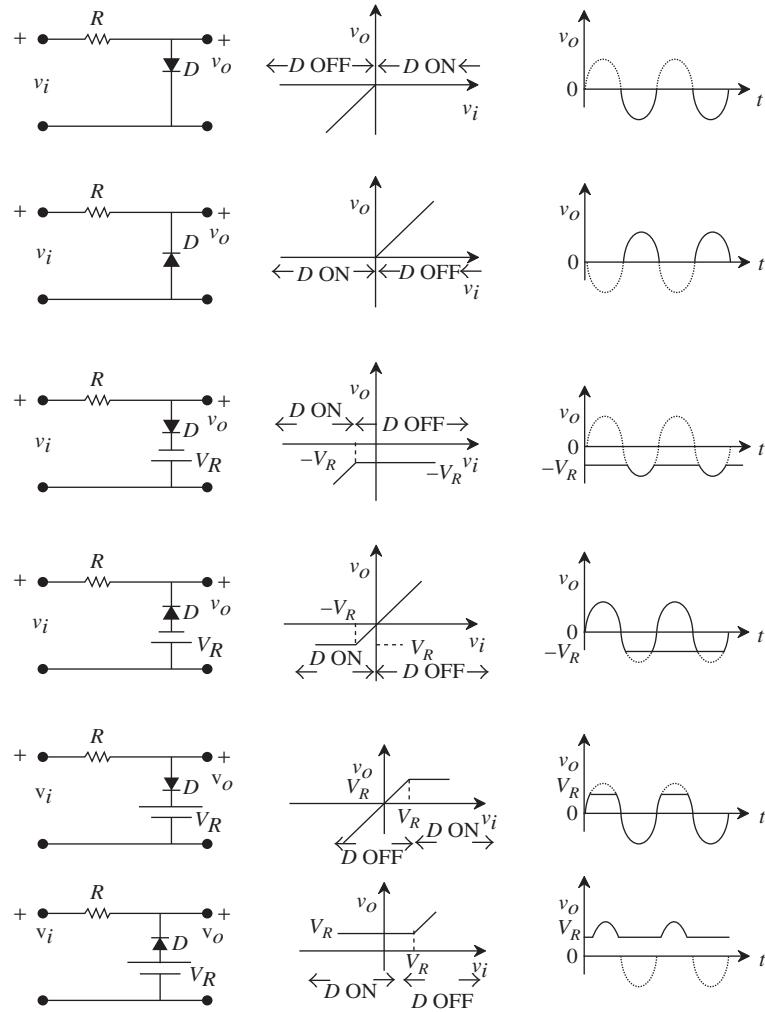


FIGURE 4.15(a) One-level shunt clippers

leaving only a slice of the input at the output, the circuit is called a positive slicer. If on the other hand, the signal is sliced during the negative half-cycle, the circuit is called a negative slicer.

Positive Slicers: The circuit shown in Fig. 4.16(a) is a positive slicer, as it slices the positive going signal at two independent levels.

Consider the following conditions:

- When $v_i < V_{R1}$, D_1 is ON, D_2 is OFF. The circuit in Fig. 4.16(a) reduces to that in Fig. 4.16(b). From Fig. 4.16(b), $v_o = V_{R1}$.
- When $V_{R1} < v_i < V_{R2}$, D_1 and D_2 are OFF. Hence, the resultant circuit is shown in Fig. 4.16(c). From Fig. 4.16(c), $v_o = v_i$.
- When $v_i > V_{R2}$, D_1 is OFF and D_2 is ON. Hence, the circuit reduces to that shown in Fig. 4.16(d). Hence, $v_o = V_{R2}$. Figure 4.16(e) represents the transfer characteristic, input and output of a positive slicer. We observe that in the output only a portion of the positive going signal is selected.

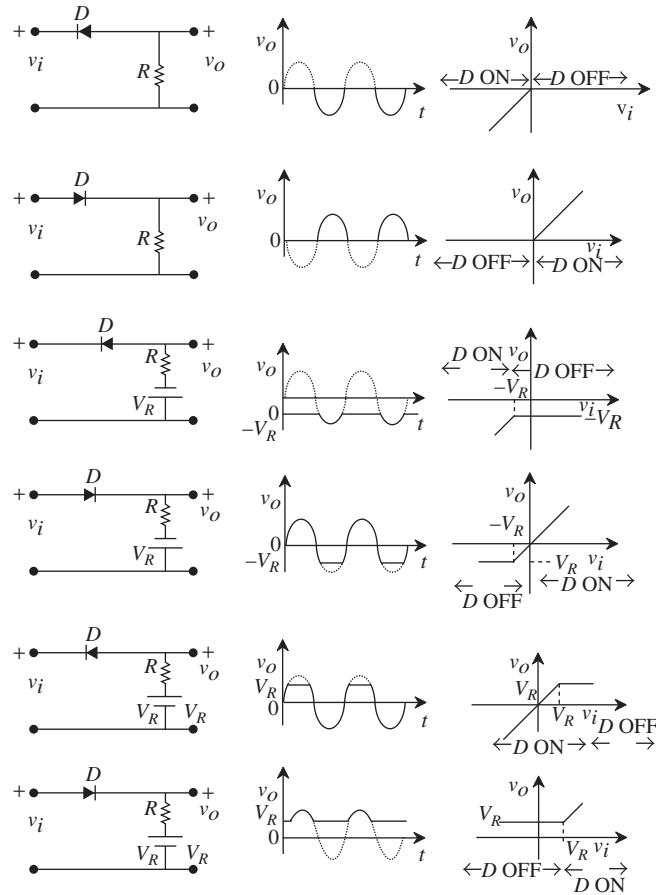


FIGURE 4.15(b) One-level series clippers

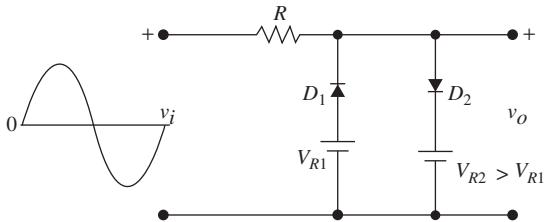
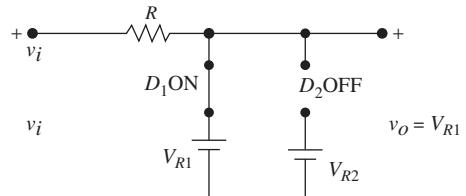


FIGURE 4.16(a) A positive slicer

FIGURE 4.16(b) The circuit of Fig. 4.16(a) when D_1 is ON and D_2 is OFF

Negative Slicers: To implement a negative slicer, consider the circuit shown in Fig. 4.17(a).

Consider the following conditions

- When $v_i \leq -V_{R1}$, D_1 is ON, D_2 is OFF. Hence, the circuit reduces to that shown in Fig. 4.17(b). Therefore, $v_o = -V_{R1}$.
- When $V_{R1} > v_i > -V_{R2}$, D_1 and D_2 are OFF. The resultant circuit is shown in Fig. 4.17(c). Hence, $v_o = v_i$

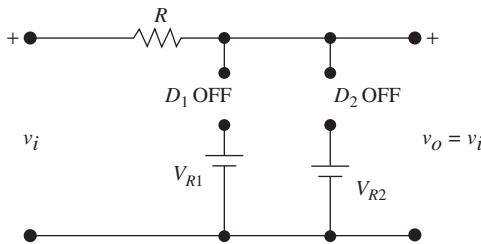
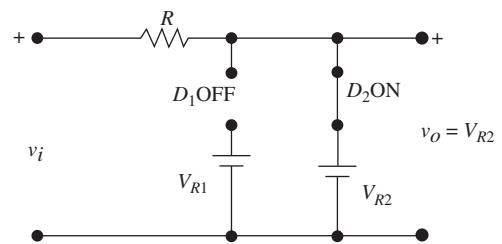
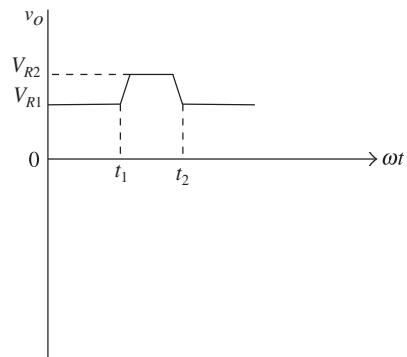
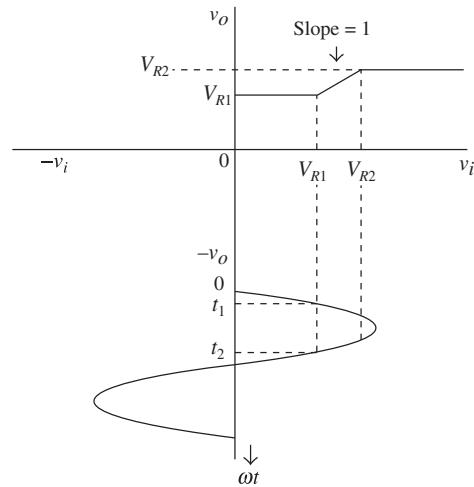
FIGURE 4.16(c) The circuit of Fig. 4.16(a) when D_1 and D_2 are OFFFIGURE 4.16(d) Circuit of Fig. 4.16(a) when D_1 is OFF and D_2 is ON

FIGURE 4.16(e) The transfer characteristic of a positive slicer with input and output waveforms

- (iii) When $v_i \leq -V_{R2}$, D_1 is OFF and D_2 is ON, the resultant circuit is shown in Fig. 4.17(d). Hence, $v_o = -V_{R2}$. The transfer characteristic is plotted in Fig. 4.17(e). We see that in the output only a portion of the negative going signal is selected.

Limiters. The combination of a positive-peak clipper and a negative-peak clipper, clipping the input symmetrically at the top and the bottom is called a limiter as shown in Fig. 4.18(a).

Consider the following conditions:

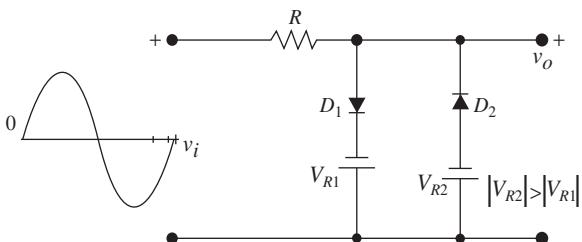
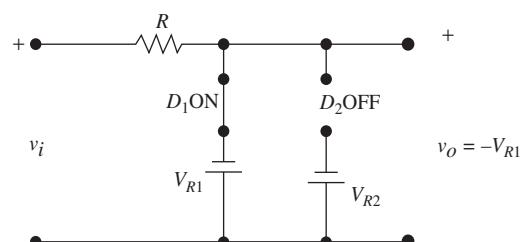


FIGURE 4.17(a) A negative slicer

FIGURE 4.17(b) The circuit of Fig. 4.17(a) when D_1 is ON D_2 is OFF

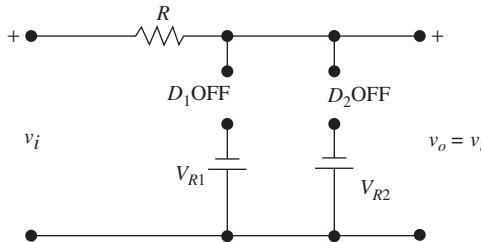


FIGURE 4.17(c) The circuit of Fig. 4.16(a) when D_1 and D_2 are OFF

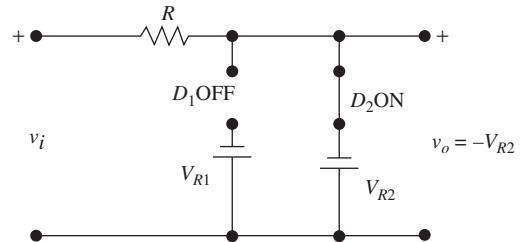


FIGURE 4.17(d) The circuit of Fig. 4.17(a) when D_1 is OFF and D_2 is ON

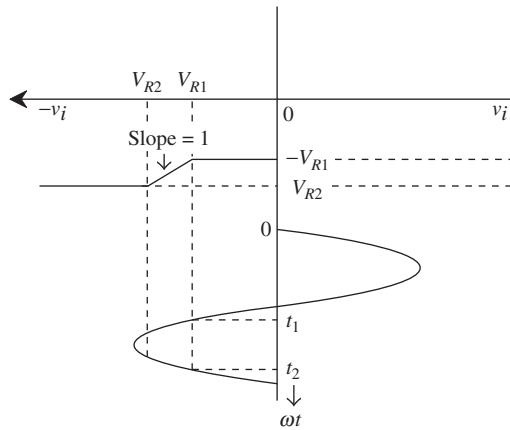


FIGURE 4.17(e) The transfer characteristic of the negative slicer with input and output waveforms

- When $-V_R < v_i < V_R$, D_1 and D_2 are OFF and the resultant circuit is shown in Fig. 4.18(b). Hence, $v_o = v_i$.
- When $v_i \geq V_R$, D_1 is ON and D_2 is OFF. Under this condition, the resultant circuit is shown in Fig. 4.18(c). Hence, $v_o = V_R$.
- When $v_i \leq -V_R$, D_1 is OFF, D_2 is ON. The circuit that is to be considered is shown in Fig. 4.18(d).

Hence, $v_o = -V_R$. The transfer characteristic of the limiter is as shown in Fig. 4.18(e).

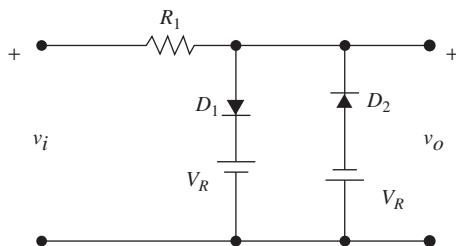


FIGURE 4.18(a) A limiter

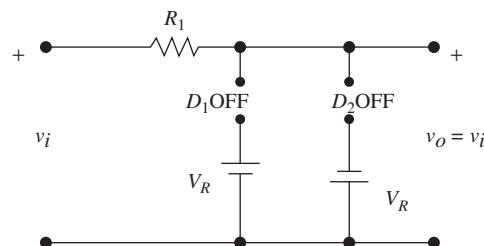


FIGURE 4.18(b) The circuit of Fig. 4.18(a) when both D_1 and D_2 are OFF

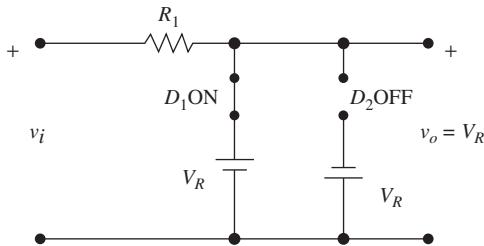


FIGURE 4.18(c) The circuit of Fig. 4.18(a) when, D_1 is ON and D_2 is OFF

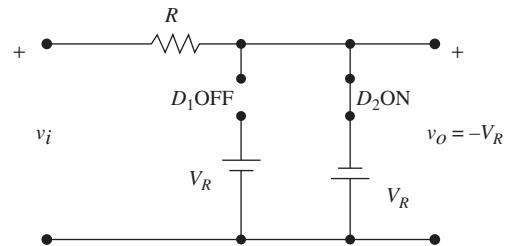


FIGURE 4.18(d) The circuit of Fig. 4.18(a) when D_1 is OFF, D_2 is ON

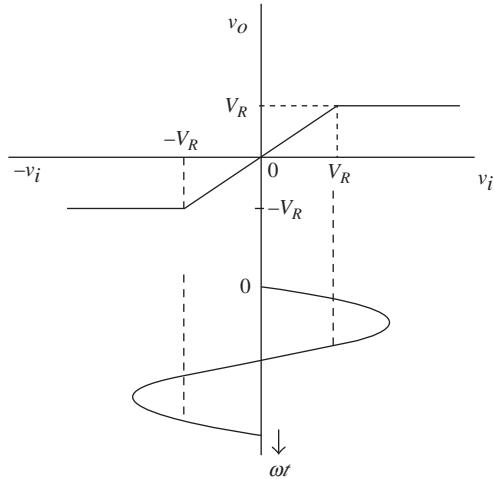


FIGURE 4.18(e) The transfer characteristic of a limiter with input and output waveforms

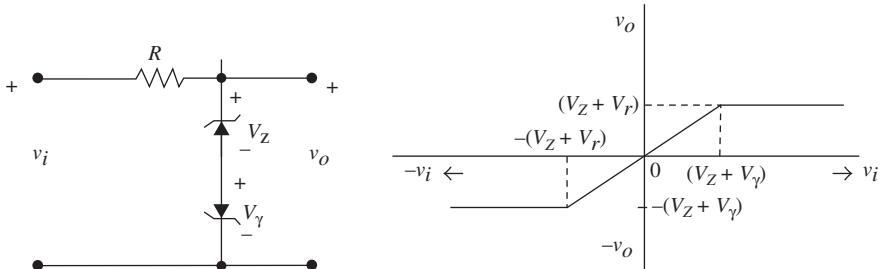


FIGURE 4.19(a) A limiter using Zener diodes and (b) the transfer characteristic

The limiter circuit can also be implemented using Zener diodes as shown in Fig. 4.19(a).

When $-(V_z + V_\gamma) < v_i < (V_z + V_\gamma)$, $v_o = v_i$

When $v_i \geq (V_z + V_\gamma)$, $v_o = (V_z + V_\gamma)$

When $v_i \leq -(V_z + V_\gamma)$, $v_o = -(V_z + V_\gamma)$

The transfer characteristic is drawn in Fig. 4.19(b). Limiters are used in frequency-modulated systems where only the frequency of the carrier is varied, but its amplitude remains constant.

Two-level Emitter-coupled Transistor Clipper.

The circuit shown in Fig. 4.20(a) is a two-level emitter-coupled transistor clipper. Let the input v_i to Q_1 be small enough ($< v_{i1}$) to keep Q_1 OFF. As a result, $I_{C1} \approx I_{E1} = 0$. If V_{BB} is adjusted such that Q_2 is in the active region, then the voltage $v_o = V_{CC} - I_{C2}R_C$. When v_i is increased further so that Q_1 conducts, there is I_{E1} through R_e , the drop across R_e increases which in turn reduces I_{B2} of Q_2 resulting in reduction of I_{C2} . Consequently, v_o increases. When v_i is increased further, v_o also rises. Thus, the output is proportional to the input in a limited region. A further increase in v_i to v_{i2} enables Q_1 to draw reasonably large I_{E1} and the drop across R_e can now reverse-bias the base-emitter diode of Q_2 , thereby driving Q_2 into the OFF state. As a result, v_o is limited to V_{CC} . The transfer characteristic with input and output waveforms is shown in Fig. 4.20(b). Thus, this circuit behaves as a two-level clipper (slicer). The region of linearity can be controlled by the choice of V_{BB} .

4.3.4 Noise Clippers

If an input signal has an associated noise component, it will cause the signal amplitude to fluctuate. This noise component may sometimes trigger sensitive circuits. Now, consider Figs. 4.21(a) and (b) which represent two input signals with associated noise components.

Series and Shunt Noise Clippers. An input signal with noise components seen in Fig. 4.21(a), can be eliminated by a series noise clipper shown in Fig. 4.21(c). As long as the noise magnitudes are small ($< |V_\gamma|$), the diodes are OFF. Hence, the output is zero during the period noise is present. The output is devoid of noise.

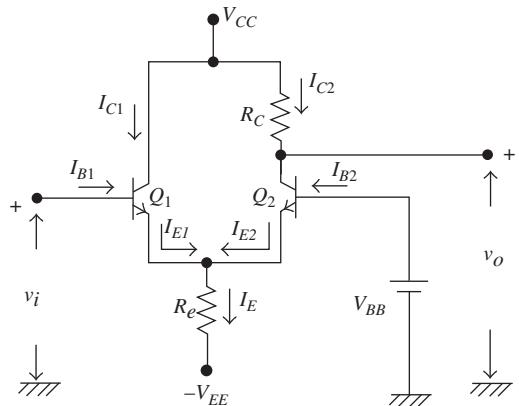


FIGURE 4.20(a) A two-level transistor clipper

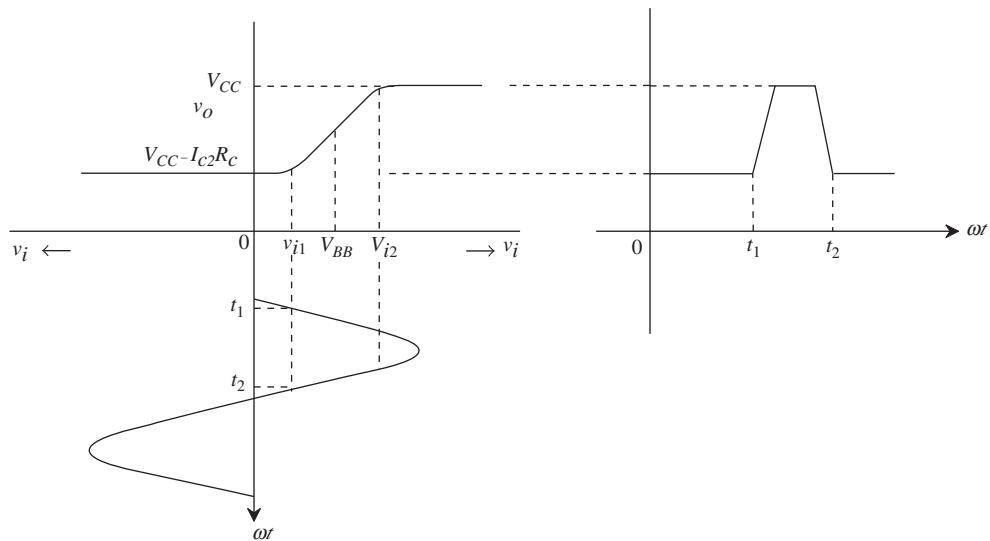


FIGURE 4.20(b) The transfer characteristic of a two-level transistor clipper with input and output waveforms

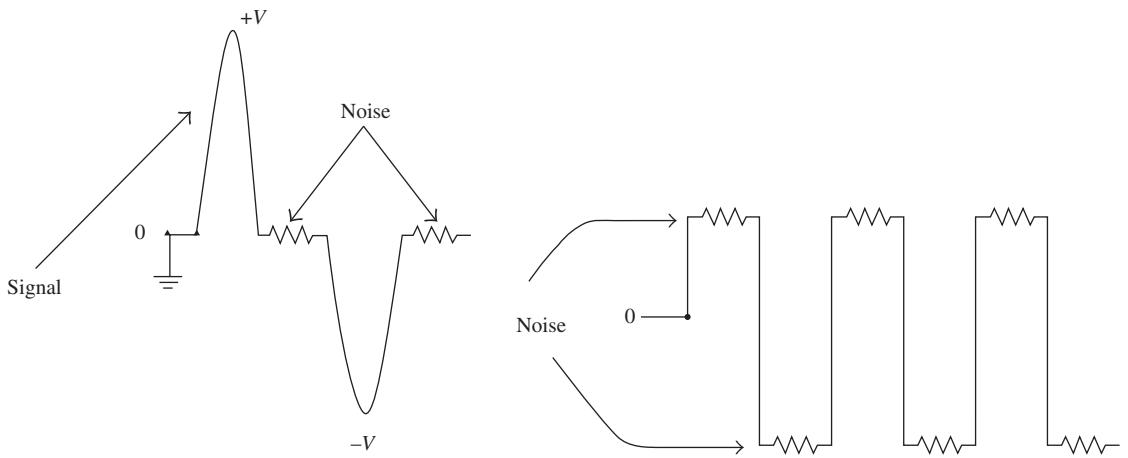


FIGURE 4.21(a) An input signal with an associated noise

FIGURE 4.21(b) An input signal with an associated noise

Now let the input signal have an associated noise as represented in Fig. 4.21(b). This noise can be eliminated by a shunt noise clipper, as shown in Fig. 4.22(a).

Here, the magnitude of the output is limited to V_F , the forward voltage of the diode and noise is eliminated in the output. If only the noise is to be eliminated, the diodes can be biased by an appropriate voltage, V [see Fig. 4.22 (b)].

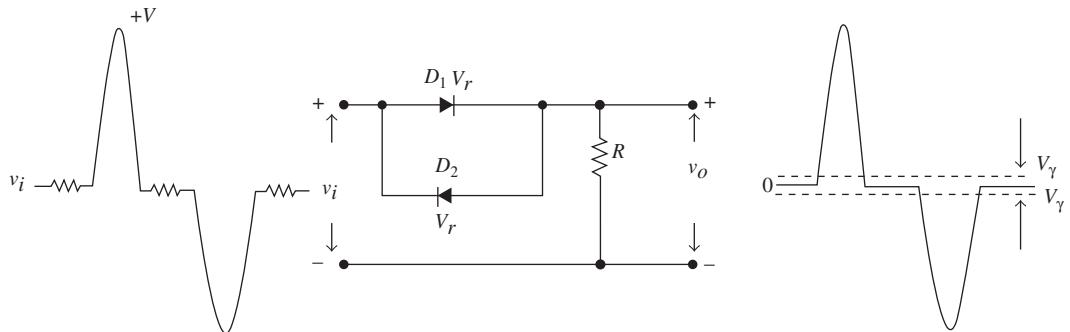


FIGURE 4.21(c) A series noise clipper

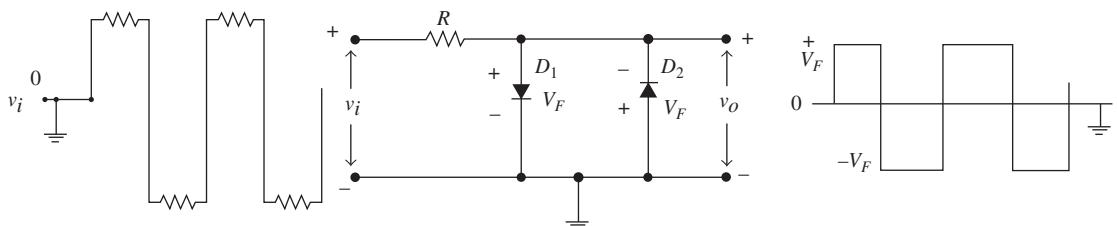


FIGURE 4.22(a) A shunt noise clipper

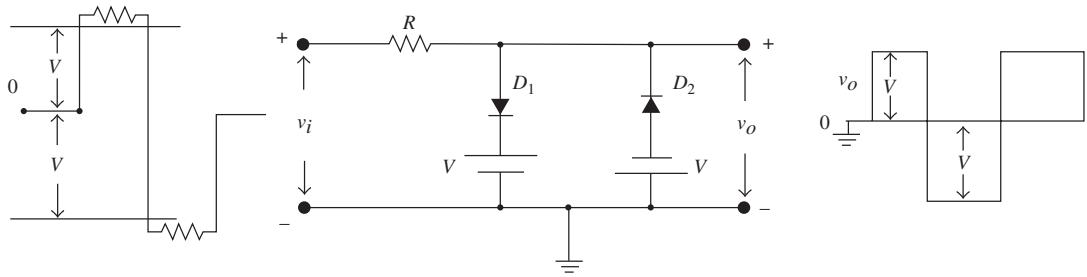


FIGURE 4.22(b) A biased noise clipper

Compensation for Changes with Temperature. We know that V_γ reduces by approximately $2.5 \text{ mV/}^\circ\text{C}$ rise in temperature. Consequently, the output of the clipping circuit can change. Compensation techniques may be employed in precision clipping circuits to take care of variation in V_γ by temperature changes. Let us consider the series clipping circuit in Fig. 4.23(a).

If the diode is ideal, this is simply a switch. But an idealized diode is represented by an ideal diode in series with V_γ ; hence the above circuit is redrawn as shown in Fig. 4.23(b). If V_γ now changes, the output will also change accordingly. To make sure that the output does not vary with temperature, the circuit shown in Fig. 4.23(c) may be employed.

The two diodes D_1 and D_2 are identical, which means that the variation of V_γ with temperature, is identical in both the diodes; hence, changes in temperature will not alter the output. However, D_2 should be always ON. For this, V_1 and R_1 are provided to forward-bias D_2 . The need for a separate source V_1 may be eliminated as shown in Fig. 4.23(d). Here D_2 is kept ON by V_R and R_1 . Figure 4.23(e) presents a modification of this circuit.

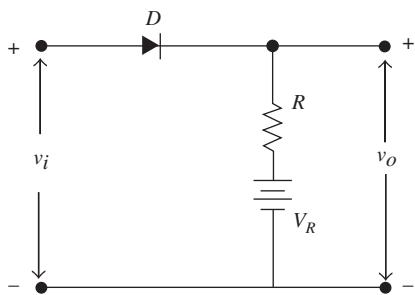


FIGURE 4.23(a) A base clipper

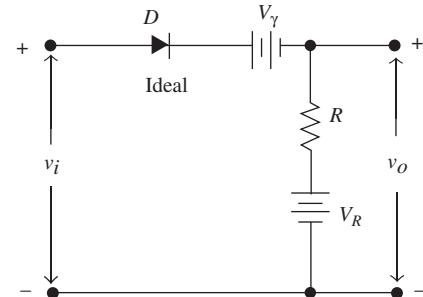


FIGURE 4.23(b) A base clipper with a practical diode

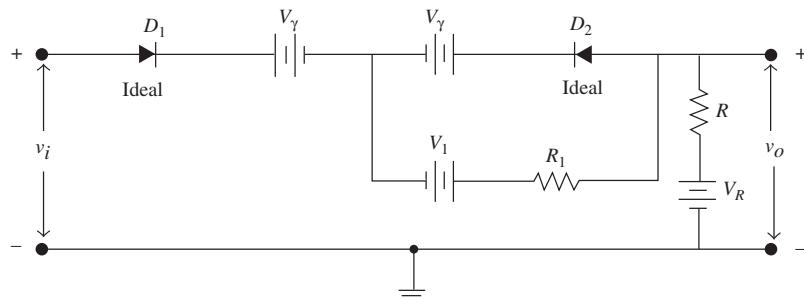


FIGURE 4.23(c) A base clipper with a temperature compensation

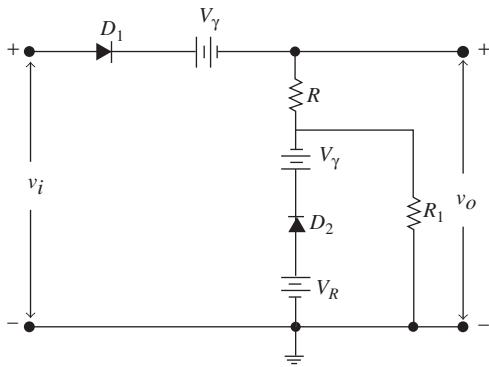


FIGURE 4.23(d) A base clipper with temperature compensation with no need for the source V_1

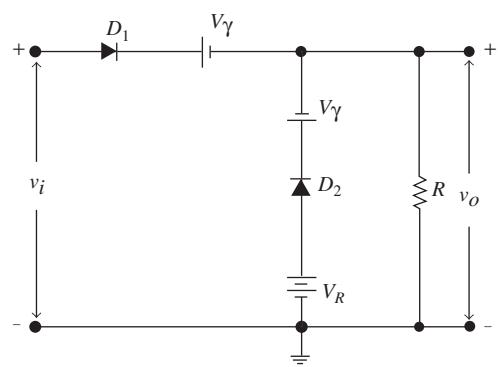


FIGURE 4.23(e) A modified base clipper

As long as $v_i < V_R$, D_1 is OFF, D_2 is ON, $v_o = V_R - V_\gamma$.

If $v_i > V_R$, D_1 is ON, D_2 is OFF, $v_o = v_i - V_\gamma$.

Thus, temperature compensation can be provided in other diode clipping circuits on similar lines.

4.4 COMPARATORS

An amplitude comparator is a circuit that tells the time instant at which the input amplitude has reached a reference level. A comparator is shown in Fig. 4.24.

Ideally, in this comparator:

$$v_o = 0 \quad \text{for } t < t_1$$

$$v_o = V \quad \text{for } t \geq t_1$$

The amplitude of the output abruptly rises from 0 to V at $t = t_1$, t_1 is the time instant at which v_i reaches V_R .

4.4.1 Diode Comparators

In this section, we discuss two types of diode comparators—pick-off and break-away diode comparators.

Pick-off Diode Comparators. A simple diode comparator circuit is shown in Fig. 4.25. A base clipper is used as a comparator. The input now is a ramp and V_R is the reference voltage. The circuit is required to tell the time instant at which the input reaches V_R .

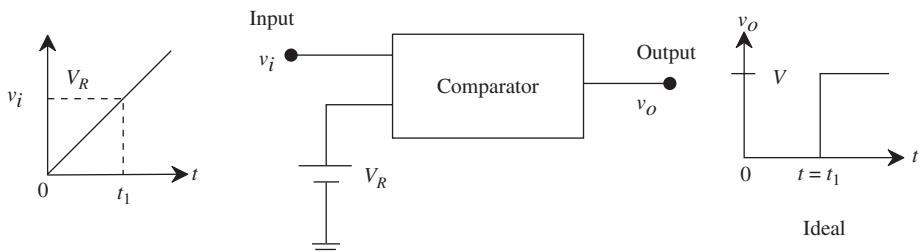


FIGURE 4.24 A comparator

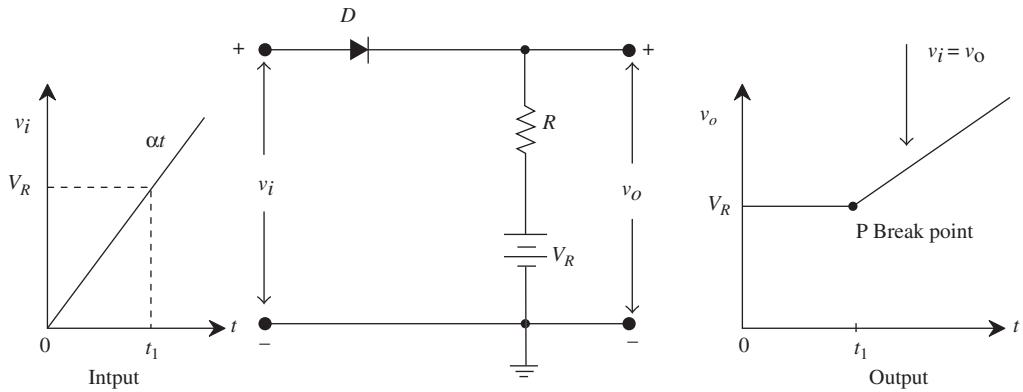


FIGURE 4.25 A pick-off diode comparator

Using an ideal diode, as long as, $v_i < V_R$, $v_o = V_R$. If $v_i \geq V_R$, $v_o = v_i$. Upto $t = t_1$, $v_o = V_R$ and the slope of the output is 0. At $t = t_1$, output suddenly rises as the input (the slope at the output has changed) and this is the time instant at which the input reaches the reference level V_R . The point P where the slope changes when the diode conducts is called the break point. The diode in this case is called a “pick-off” diode.

As is evident from the Fig. 4.25, there is a sudden change in the slope of the output at the instant the input reaches V_R . However, due to ageing and temperature variations, the diode may not switch from OFF to ON at exactly $t = t_1$ (break point, P). It may switch state at any instant after t_1 and before t_2 (see Fig. 4.26).

Hence, the break point (the point at which the device D changes state) may not exactly be at t_1 . Instead, there is a break region (t_1 to t_2), within which, at any instant the device may switch state. Therefore, there is a large region of uncertainty. After the break point, the output follows the input—it has the same slope as the input. If this region of uncertainty is to be reduced to know precisely at which time instant the input reaches the reference level, the break region should be sharp. To achieve this, an amplifier may be placed before or after the comparator.

Consider the response of the comparator circuit shown in Fig. 4.25. To the left of the break point, the diode is OFF. Hence, the reverse incremental resistance of the diode is significantly larger when compared to R . To the right of the break point, the forward incremental resistance of the diode is much smaller than R . If the break point is located at a point where the incremental resistance of the diode, (r) is equal to the resistance (R) then the incremental change in the output voltage (Δv_o) for a corresponding change at the input (Δv_i) is calculated using Fig. 4.27.

$$\Delta v_o = \Delta v_i \frac{R}{r + R}$$

If $r = R$:

$$\frac{\Delta v_o}{\Delta v_i} = \frac{R}{R + R} = \frac{1}{2}$$

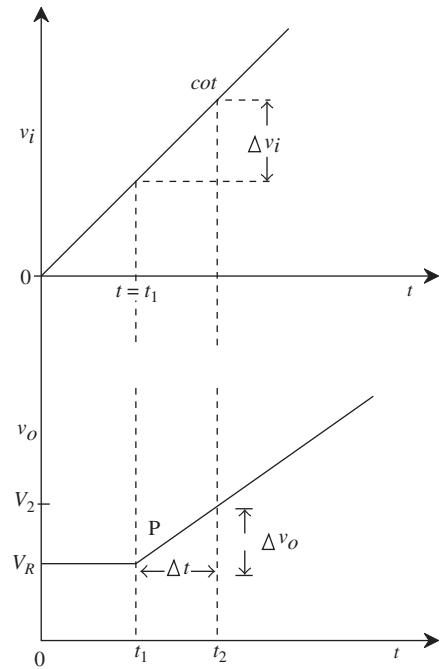


FIGURE 4.26 The input and output of the diode comparator

This relation tells that $\Delta v_i = 2 \Delta v_o$. That is, for a larger incremental change in the input, there is a smaller incremental change in the output. The region of uncertainty is larger.

A device is connected at the output of the comparator, and is required to be activated when the diode current is say, I and has a drop across R as IR . If, now an amplifier is connected at the output of the comparator to reduce the region of uncertainty, the output of this amplifier activates the device (see Fig. 4.28). Let the amplifier have a gain A . During $\Delta t = t_2 - t_1$, the output changes by $\Delta v_o = V_2 - V_R$, see Fig 4.26, the delay in the response is reduced to $\Delta t/A$ or $(t_2 - t_1)/A$.

Let the amplifier only amplify the change in the comparator input but not the reference voltage. The device to be activated is activated only when the drop across R is IR . However, now $I = I/A$. Hence, the device is activated when the drop across R is RI/A since the diode current is amplified by A and the dynamic diode resistance, $r = (\eta V_T/I)$, varies inversely with current. Therefore, it is evident that, the device to be activated by the comparator will respond at a current corresponding to $r = RA$.

$$\frac{\Delta v_o}{\Delta v_i} = A \frac{R}{r + R} = \frac{AR}{R + RA} = \frac{A}{1 + A}$$

$$\text{As } A \rightarrow \infty, \frac{\Delta v_o}{\Delta v_i} \rightarrow 1$$

Without an amplifier, $\Delta v_o/\Delta v_i$ (the transmission gain) was half and with an amplifier connected as in Fig. 4.29, $\Delta v_o/\Delta v_i$ is one; i.e., there is no marked improvement in the response of the comparator arrangement of Fig. 4.28.

Now, consider a comparator circuit where the amplifier precedes a comparator and the output of the comparator is directly connected to the device to be actuated. Let the amplifier have a gain A and Δv_i be the incremental change in the input needed to actuate the device when the output is directly connected to the device. With a pre-amplifier with gain A connected to the comparator, $\Delta v_i/A$ is now the incremental change in the input

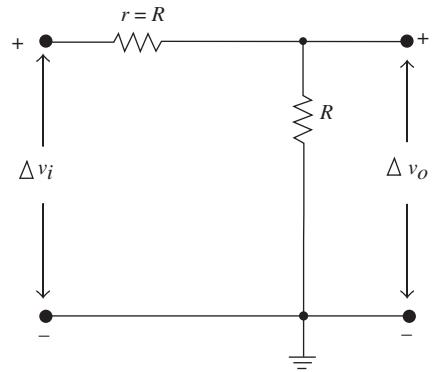


FIGURE 4.27 The circuit to calculate the incremental change in the output voltage

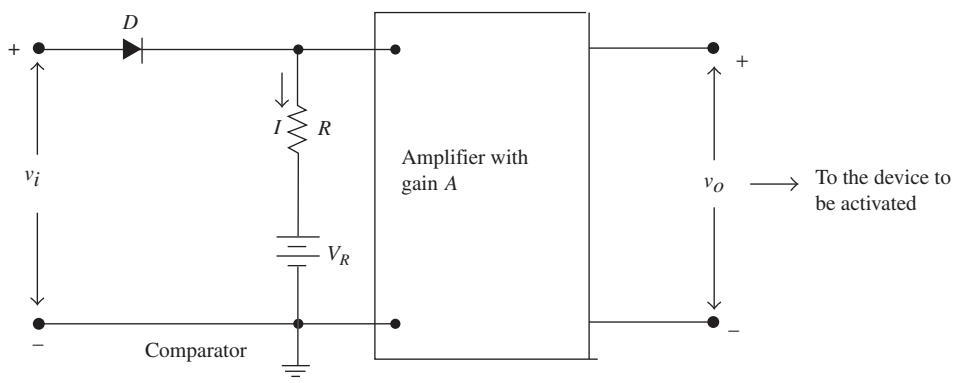


FIGURE 4.28 The output of the comparator connected to an amplifier

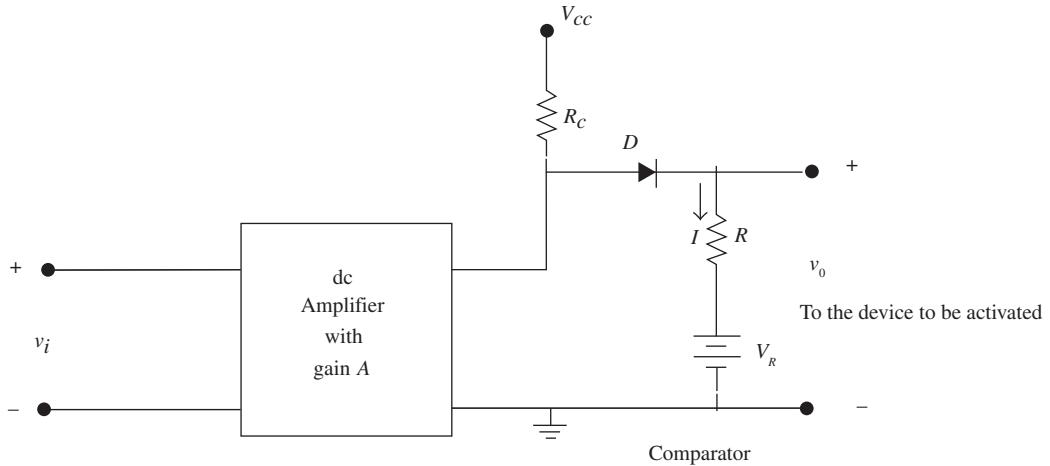


FIGURE 4.29 The output of the amplifier drives a comparator

needed to make the output change as in the previous case. As $\Delta v_i/A$ is small, the break region is reduced. Thus, this is a better comparator.

Break-away Diode Comparators. Consider the circuit in Fig. 4.30. If the input to the circuit is a negative ramp, then the output is as shown. The diode in this case is called a “break-away” diode. Here:

As long as $v_i > V_R$, D is ON and $v_o = V_R$. When $v_i \leq V_R$, D is OFF and $v_o = v_i$.

The Op-amp as a Comparator. Consider the op-amp comparator as shown in Fig. 4.31(a). The voltage at the inverting input is V_R .

$$V_R = V_{CC} \times \frac{R_2}{R_1 + R_2} = 15 \times \frac{10}{10 + 20} = 5 \text{ V}$$

When $v_i > V_R$, $v_o = +V_{sat}$ ($V_{CC} \approx 15 \text{ V}$, the positive supply voltage). Alternatively, when $v_i < V_R$, $v_o = -V_{sat}$ ($V_{EE} \approx -15 \text{ V}$, the negative supply voltage). The output thus jumps from $+V_{sat}$ to $-V_{sat}$ and vice versa when the input reaches V_R , as shown in Fig. 4.31(b). As we see in this comparator, the variation of the signal at the input has no relevance to the output, which is a pulse. This pulse can actuate a device.

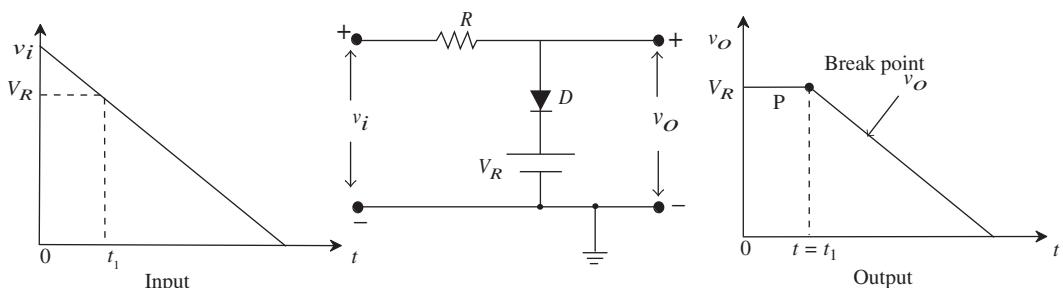


FIGURE 4.30 Break-away diode comparator

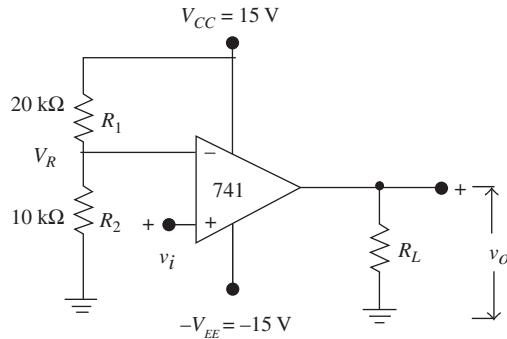


FIGURE 4.31(a) Op-amp as a comparator

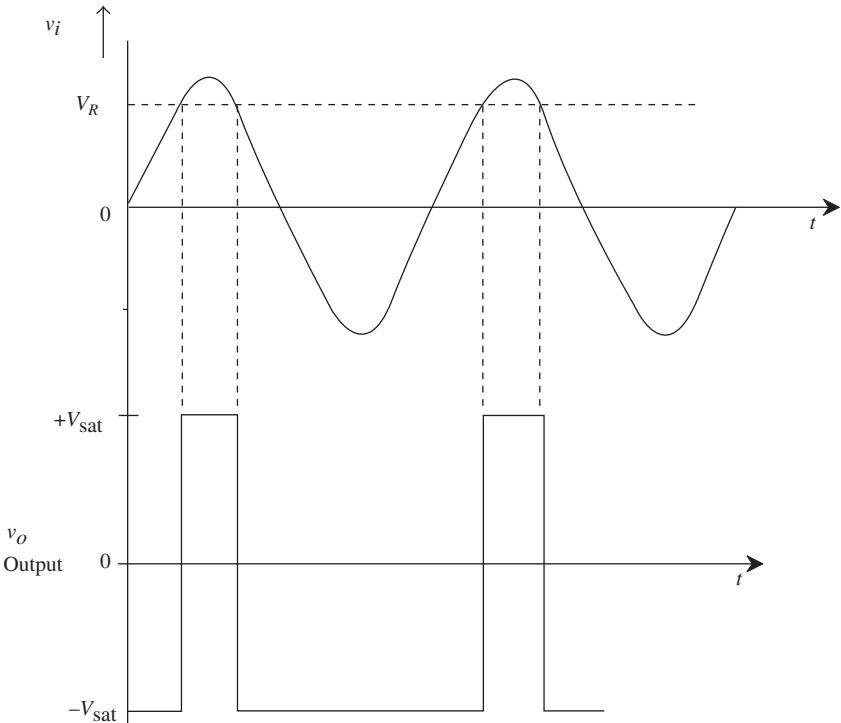


FIGURE 4.31(b) Input and output waveforms of the op-amp comparator

4.4.2 The Double Differentiator as a Comparator

In any comparator, if the output activates a device, the comparator output should reach the device to be activated just at the moment of comparison. Once the device has been activated by the output of the comparator, it is also desirable that the signal is not present. A double differentiator [see Figs. 4.32(a) and (b)] does these twin jobs.

Let the input to the comparator be a ramp. The output of the diode comparator is a step voltage V_R up to t' and is a ramp beyond this time instant. As long as the input to the first differentiator is a step, its output

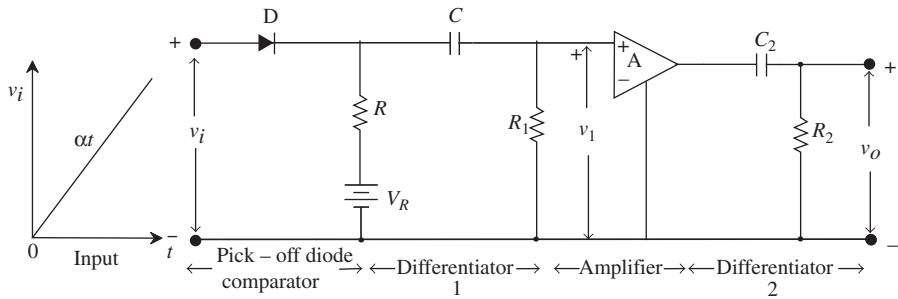


FIGURE 4.32(a) A double differentiator as a comparator

is zero in no time because C_1 blocks dc. At t' , the input to the high-pass circuit is ramp; hence, its output is an exponential. This signal is then connected to an amplifier with gain A and the resultant output, which is an exponential, is applied as an input to another high-pass circuit. The output of this is now a pulse whose amplitude and duration can be controlled.

In a double differentiator comparator, the device to be activated receives the signal only when the input reaches a reference level. Soon after, as the amplitude of the pulse dies down, no signal reaches the device to be activated. This could be called a practical comparator.

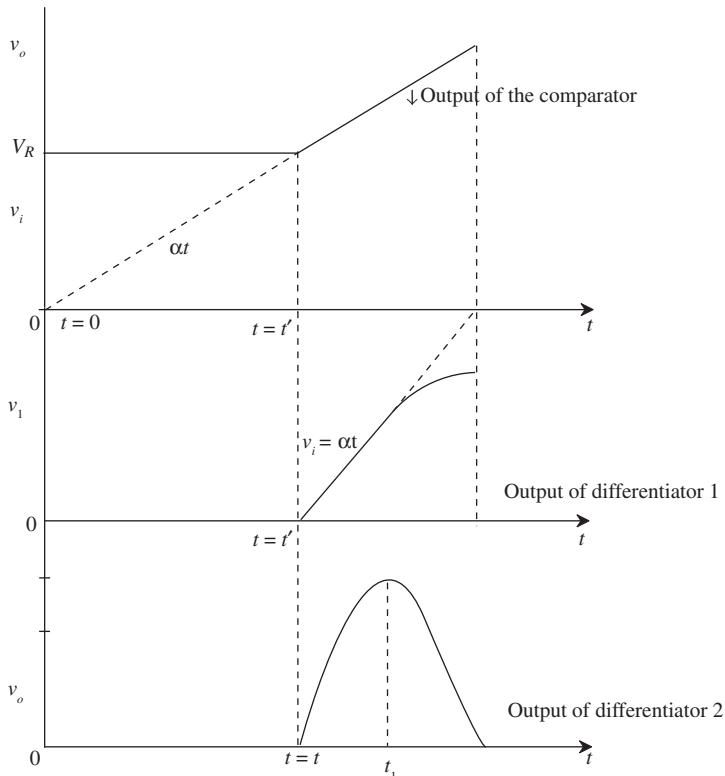


FIGURE 4.32(b) The waveforms of a double differentiator

4.5 APPLICATIONS OF COMPARATORS

Apart from being used as amplitude comparators, comparator circuits can be used for many applications. A few applications are presented in this section.

1. Measurement of time delays: In the comparator shown before, if V_{R1} is the reference level in the first comparator (double differentiator), then a pulse is generated with a peak at $t = t_1$. If V_{R2} is the reference level set in a second comparator then the pulse is generated with peak at $t = t_2$. Then the time difference between the two pulses is $(t_2 - t_1) = (V_{R2} - V_{R1})/\alpha$ where, α is the slope of the input ramp.

2. Timing markers generated from a sine wave: If a sine wave is applied as input, when the input reaches V_R , the output of the comparator is high till the input reaches V_R again. After differentiating and clipping negative spikes, we get positive spikes which can be implemented as timing markers, as shown in Fig. 4.33.

3. Phase meter: Let two sinusoidal inputs having a phase difference be applied to a comparator whose reference voltage is zero, as shown in Fig. 4.34. Here, the output pulses are differentiated and the time difference between the output spikes is proportional to the phase difference.

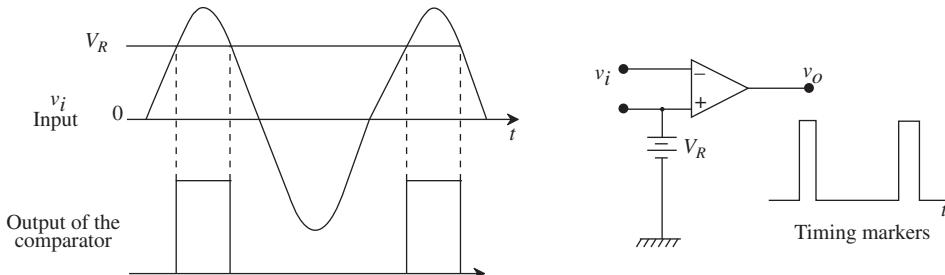


FIGURE 4.33 Comparator used to generate timing markers

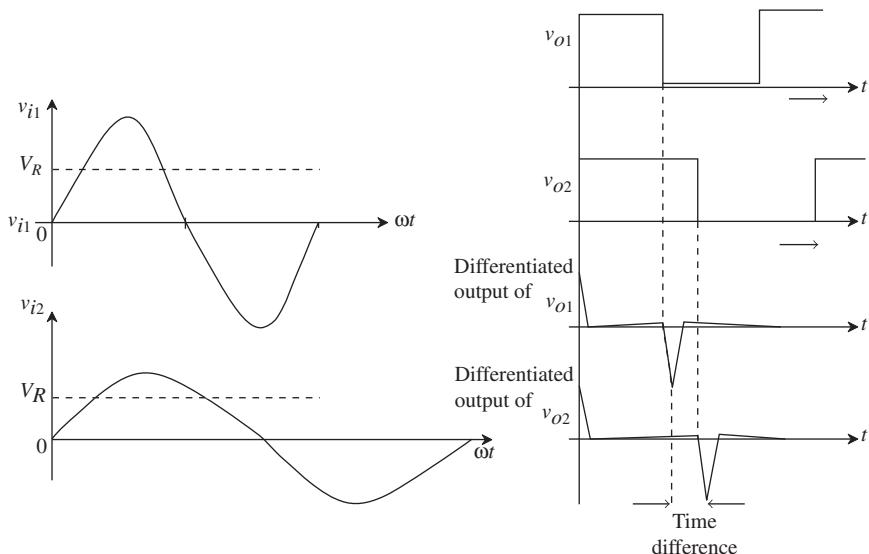


FIGURE 4.34 The Waveforms of a comparator used for the measurement of phase difference

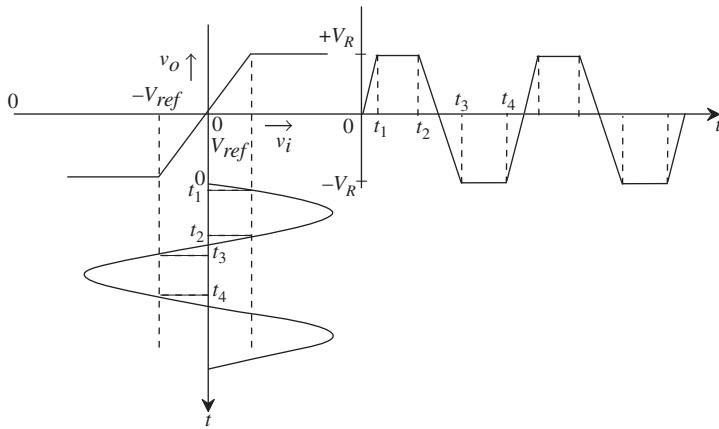


FIGURE 4.35 The comparator used to convert a sinusoidal input into a square-wave output

4. Square waves from sine waves: In a regenerative comparator (Schmitt trigger), as long as v_i is less than V_{ref} , v_o is the same as v_i , as shown in Fig. 4.35. If the input goes beyond $\pm V_{ref}$, the output of the comparator remains at either $+V$ or $-V$, thereby converting a sinusoidal input into a square-wave output, when the frequency is sufficiently large.

S O L V E D P R O B L E M S

Example 4.2: For the two-level clipper in Fig. 4.36(a), the input varies linearly from 0 to 150 V. Plot the transfer characteristic and obtain the output voltage. Assume ideal diodes.

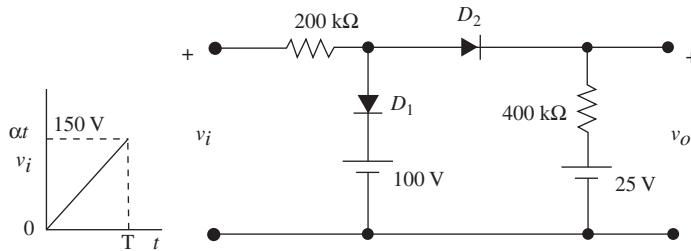


FIGURE 4.36(a) The given two-level clipper circuit

Solution: For ideal diodes $R_f = 0$, $R_r = \infty$, $V_Y = 0$

- (i) $0 \leq v_i < 25$ V then D_1 and D_2 are OFF.
The resultant circuit is as shown in Fig. 4.36(b).

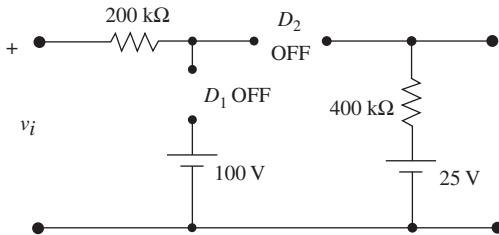
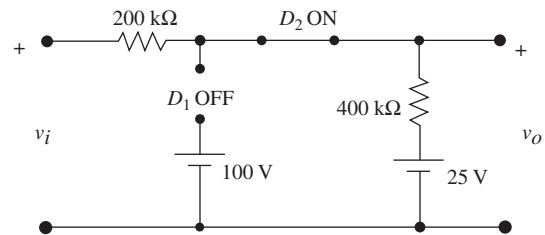
$$v_o = 25 \text{ V}, \text{ i.e., till } v_i \text{ rises to } 25 \text{ V}, v_o = 25 \text{ V.}$$

- (ii) $25 \leq v_i \leq 100$ V
 D_1 is OFF and D_2 is ON and the resultant circuit is shown in Fig. 4.36(c).

Using the superposition theorem:

$$v_o = v_i \times \frac{400}{200 + 400} + 25 \times \frac{200}{200 + 400}$$

$$v_o = \frac{2}{3}v_i + \frac{25}{3} \quad (1)$$

FIGURE 4.36(b) Circuit when D_1 is OFF and D_2 is OFFFIGURE 4.36(c) Circuit when D_1 is OFF and D_2 is ON

Since $v_i(\min) = 25$ V,

$$v_o = \frac{50}{3} + \frac{25}{3} = \frac{75}{3} = 25 \text{ V}$$

To find $v_i(\max)$ that satisfies above relation (1)

Put $v_o = 100$ V

$$v_o = \frac{2}{3}v_i + \frac{25}{3} \quad 100 \text{ V} = \frac{2}{3}v_i + \frac{25}{3} \quad \frac{2}{3}v_i = \left(100 - \frac{25}{3}\right) = \frac{275}{3}$$

$$v_i = \frac{275}{3} \times \frac{3}{2} = 137.5 \text{ V}$$

(iii) for $v_i > 137.5$ V both D_1 and D_2 conduct and $v_o = 100$ V

We thus have,

For $0 < v_i < 25$ V, $v_o = 25$ V

$$25 \text{ V} < v_i < 137.5 \text{ V}, v_o = \frac{2}{3}v_i + 8.333$$

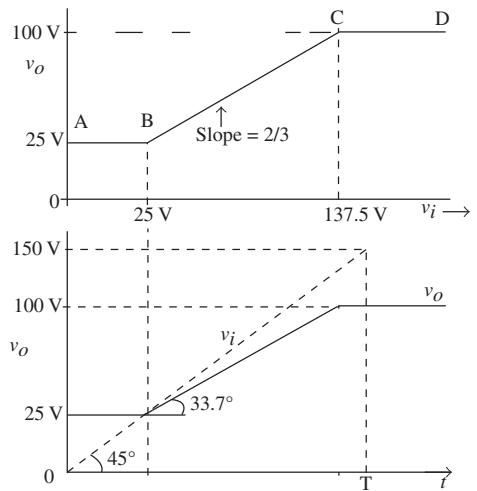


FIGURE 4.36(d) Transfer characteristic and output of the circuit in Fig. 4.36(a)

The transfer characteristic is presented in Fig. 4.36(d).

Example 4.3: For the circuit shown in Fig. 4.37(a), plot the transfer characteristic for v_i varying from 0 to 150 V linearly.

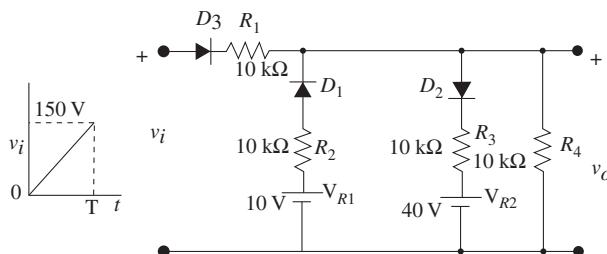


FIGURE 4.37(a) Clipping circuit with input

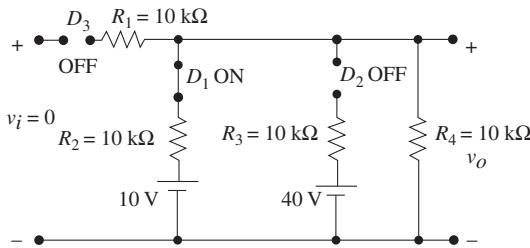


FIGURE 4.37(b) Equivalent circuit of Fig. 4.37(a) when D_1 is ON and D_2 and D_3 are OFF

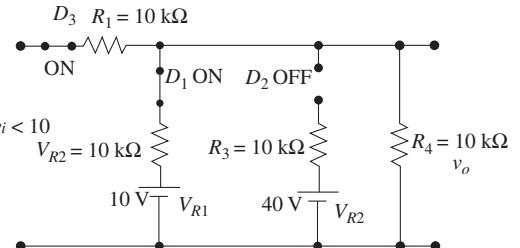


FIGURE 4.37(c) Circuit of Fig. 4.37(a) when D_1 , and D_3 are ON and D_2 is OFF

Solution:

- (i) When $v_i = 0$, D_1 is ON and D_2 and D_3 are OFF, the equivalent circuit to compute the output is as shown in Fig. 4.37(b).

$$v_o = \frac{10 \text{ V} \times 10 \text{ k}\Omega}{10 \text{ k}\Omega + 10 \text{ k}\Omega} = 5 \text{ V}$$

From this it is clear that for D_3 to conduct v_i should rise to 5 V.

Till $v_i = 5 \text{ V}$, $v_o = 5 \text{ V}$.

- (ii) For $5 < v_i < 10$

D_1 , and D_3 are ON and D_2 is OFF. The corresponding circuit is shown in Fig. 4.37(c).

Using the superposition theorem:

$$v_o = V_{R1} \times \frac{R_4 || R_1}{R_2 + (R_4 || R_1)} + v_i \times \frac{R_2 || R_4}{R_1 + (R_2 || R_4)}$$

$$v_o = 10 \times \frac{5}{10 + 5} + v_i \times \frac{5}{10 + 5} = \frac{10}{3} + \frac{v_i}{3}$$

For $v_o = 10 \text{ V}$

$$v_o = \frac{10}{3} + \frac{v_i}{3} \quad \frac{v_i}{3} = 10 - \frac{10}{3} = \frac{20}{3} \text{ V}$$

$v_i = 20 \text{ V}$

Therefore, for $5 \text{ V} < v_i < 20 \text{ V}$.

$$v_o = \frac{v_i}{3} + \frac{10}{3}$$

- (iii) For $v_i > 20 \text{ V}$ and $v_o < 40 \text{ V}$

D_3 conducts and D_1 and D_2 are OFF. The resultant circuit is shown in Fig. 4.37(d).

$$v_o = v_i \times \frac{10}{10 + 10} = \frac{v_i}{2}$$

For $v_o = 40 \text{ V}$, $v_i = 2 \times v_o = 2 \times 40 \text{ V} = 80 \text{ V}$

For $20 \text{ V} < v_i < 80 \text{ V}$, $v_o = \frac{v_i}{2}$

- (iv) For $v_i > 80$, D_3 and D_2 conduct and D_1 is OFF, the circuit is in Fig. 4.37(e).

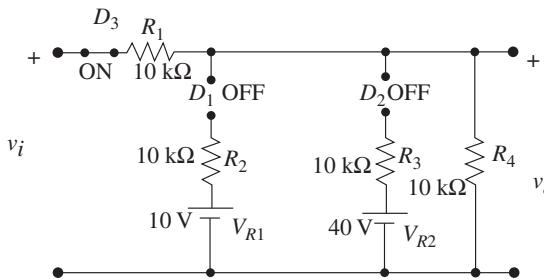


FIGURE 4.37(d) Equivalent circuit to compute the output when D_3 is ON and D_1 and D_2 are OFF

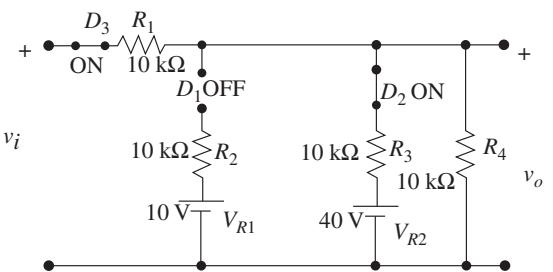


FIGURE 4.37(e) Equivalent circuit when D_3 and D_2 are ON and D_1 is OFF

$$\text{At } v_i = 150, v_o = \frac{150 + 40}{3} \approx 63.33 \text{ V}$$

$$0 < v_i < 5 \text{ V}, \quad v_o = 5 \text{ V} \quad 5 < v_i < 20 \text{ V}, \quad v_o = \frac{v_i}{3} + \frac{10}{3} \quad 20 \text{ V} < v_i < 80 \text{ V}, \quad v_o = \frac{v_i}{2}$$

$$v_i > 80 \text{ V}, \quad v_o = \frac{v_i}{3} + \frac{40}{3}$$

The transfer characteristic is presented in Fig. 4.37(f).

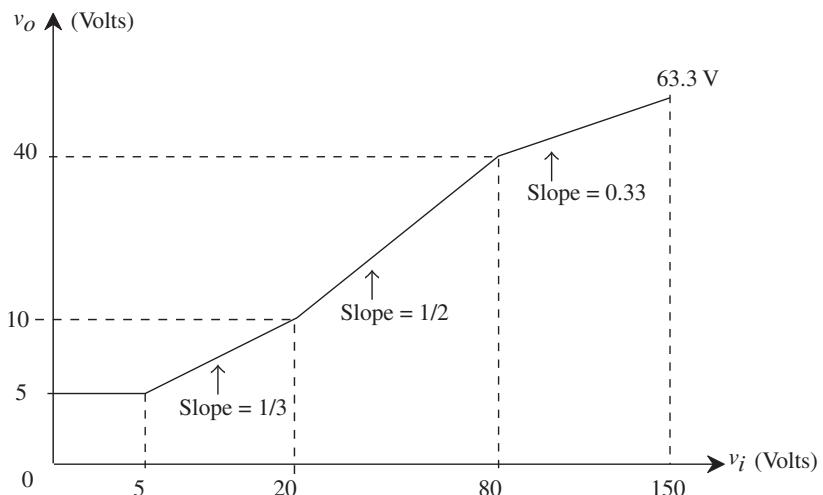


FIGURE 4.37(f) Transfer characteristic of Fig. 4.37 (a) for the given input

Example 4.4: For the clipper circuit in Fig. 4.38(a), sketch the output with and without C_1 and C_2 .

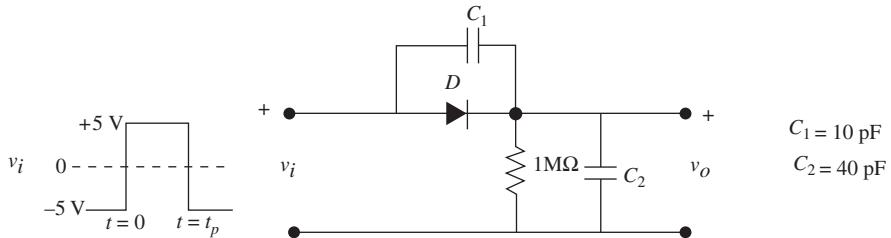


FIGURE 4.38(a) The given clipper circuit with input

Solution:

(i) Without C_1 and C_2 the circuit is as shown in Fig. 4.38(b).

When $v_i < 0$, D is OFF,

$$v_o = 0.$$

When $v_i > 0$, D is ON,

$$v_o = v_i.$$

The output is also shown in Fig. 4.38(b).

(ii) When C_1 and C_2 are included, when

$$v_i = -5, D \text{ is OFF, } v_o = 0$$

When $v_i = +5$ V (at $t = 0$, a change by 10 V), the output also rises from zero but not by the same amount.

$$v_o = \frac{C_1}{C_1 + C_2} v_i = \alpha v_i$$

$$\alpha = \frac{C_1}{C_1 + C_2} = \frac{10}{10 + 40} = 0.2$$

$$v_o = 0.2 \times 10 \text{ V} = 2 \text{ V}$$

Hence, the output v_o rises by 2 V. As the input remains at 5 V, the output rises exponentially to +5 V with a time constant of $(C_1 + C_2) R_f$. At $t = t_p$, as the input falls from +5 to -5 V (a change of 10 V) and the output drops by 2 V. Its value is $(5 - 2) = 3$ V. Since the input remains at -5 V, v_o decreases exponentially as shown in Fig. 4.38(c).

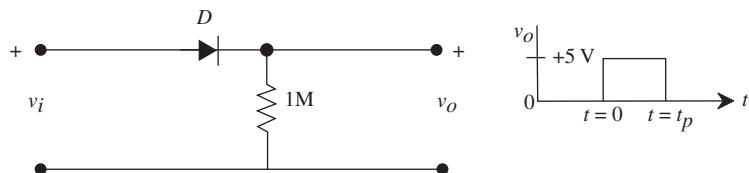


FIGURE 4.38(b) Clipping circuit without C_1 and C_2

(iii) When $C_1 \gg C_2$

$$\alpha = \frac{C_1}{C_1 + C_2} = \frac{C_1}{C_1} = 1$$

$$v_o = \alpha v_i = v_i$$

Hence, at $t = 0$, the input changes from -5 V to $+5$ V, as the diode conducts, the output also rises to 10 V from 0 V. When v_i is constant, the output decays exponentially and falls to 5 V; when v_i changes abruptly from $+5$ V to -5 V (a change of 10 V) the output also changes by the same amount i.e., to -5 V. As the input remains constant, the output decays to zero as shown in Fig. 4.38(d). Thus,

Discharging time constant $= (C_1 + C_2)R$

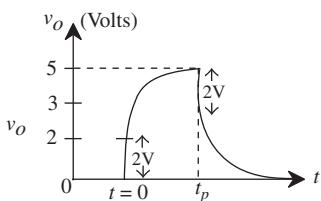


FIGURE 4.38(c) The output with C_1 and C_2 included

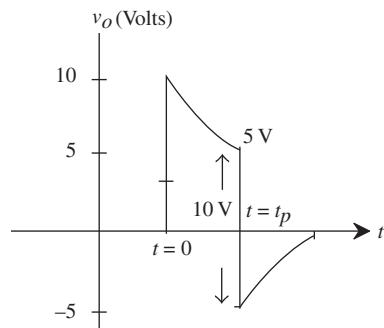


FIGURE 4.38(d) Output when $C_1 \gg C_2$

SUMMARY

- When non-linear circuit elements such as diodes, transistors and FETs are used in waveshaping applications, the resultant circuit is called a “non-linear waveshaping circuit”.
- A semiconductor diode is used as a switch; when forward-biased, it is an ON switch and when reverse-biased it is an OFF switch.
- Due to diffusion and transition capacitances, a diode does not respond instantaneously for a given excitation and there results some delay in switching the device from one state to the other state.
- The reverse recovery time of a diode is defined as the time taken for the diode reverse current to fall to 10 per cent of its forward current value when the diode is suddenly switched from the ON state into the OFF state.
- R in a clipping circuit is normally chosen as the geometric mean of the diode forward and reverse resistances, i.e., $R = \sqrt{R_f R_r}$.
- A high-frequency sine wave can be converted to a near square wave by using a limiter.
- A slicer is a clipping circuit that clips the input signal at two levels, either during the positive or the negative going period.
- A comparator tells us the time instant at which the input reaches a reference level.
- In a simple diode comparator, there is a sudden change in slope at the break point. However, the variation of the signal at the output is similar to the variation of the signal at the input after the break point.
- To improve the sharpness of a break region, an amplifier may be provided either before or after the comparator.
- In certain comparators—called regenerative comparators—like Schmitt trigger (which will be discussed later), the variation at the output does not follow the variation at the input; the output abruptly changes amplitude when the input reaches the reference level.

MULTIPLE CHOICE QUESTIONS

- (1) In a shunt diode clipper, the signal will be transmitted when the diode is:
- In the ON state
 - In the OFF state
 - In any one of the state
 - None of the above
- (2) Clipping circuits transmit _____ the input signal.
- a part of
 - whole of
 - negative portion of
 - no part of
- (3) The value of R in a clipper is chosen as:
- R_f/R_r
 - R_r/R_f
 - $R_f R_r$
 - $\sqrt{R_f R_r}$
- (4) The slope of the transfer characteristic in a series diode clipper is _____ when the diode is ON.
- 1
 - 1/2
 - 1/3
 - 2
- (5) In series diode clipper the signal is transmitted when the diode is:
- In the ON state
 - In the OFF state
 - In any one of the states
 - None of the above
- (6) Transfer characteristic of a clipping circuit is drawn between:
- Input voltage and output current
 - Output voltage and input current
 - Input voltage and output voltage
 - Output voltage and output current
- (7) Which of the following circuits is used to measure accurate time delays?
- Comparator
 - Clipping circuits
 - Slicer
 - Limiter
- (8) An example of a regenerative comparator is:
- Schmitt trigger
 - Limiter
 - Slicer
 - Simple diode comparator
- (9) The following circuit can also be used as an amplitude comparator:
- Clipping circuit
 - Slicer
 - Both slicer and clipper
 - None of the above
- (10) An emitter-coupled transistor clipper is a:
- Two-level clipper
 - One level clipper
 - One and two-level clipper
 - None of the above

SHORT ANSWER QUESTIONS

- What is a clipping circuit?
- Draw the circuit of a negative peak clipper.
- Compare series and shunt clippers.
- Explain the working of a limiter.
- Draw a slicer circuit that slices the given sinusoidal input signal during the negative going half-cycle.
- What is a comparator? Explain a simple diode comparator.
- Specify three applications of comparator.
- What is an emitter-coupled clipper?

LONG ANSWER QUESTIONS

- Explain the working of a diode shunt clipper as an amplitude comparator. What are the limitations? Suggest methods to improve the sharpness of the break region.
- With the help of waveforms, explain how a comparator is used for:
 - Measurement of time delays
 - Measurement of phase
 - Generating timing markers.
- Give the circuits of different types of shunt clippers and explain their operation with the help of their transfer characteristic.
- Draw the circuit diagram of an emitter-coupled clipping circuit and draw its transfer characteristic indicating all intercepts, slopes and voltage levels.
- Draw the circuit diagram of a limiter using Zener diodes and explain its operation with the help of its transfer characteristics.

UNSOLVED PROBLEMS

- (1) For the clipper circuit shown in Fig. 4p.1, the input $v_i = 100 \sin \omega t$. Plot the transfer characteristic and the input and output waveforms. Assume ideal diodes.

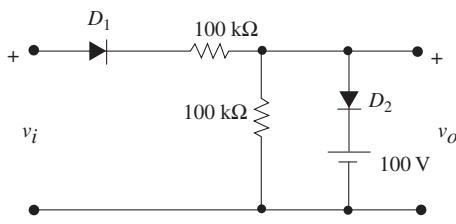


FIGURE 4p.1 The given clipping circuit for problem 1

- (2) For the clipper circuit shown in Fig. 4p.2, the input $v_i = 50 \sin \omega t$. Plot the transfer characteristic and the input and output waveforms. Assume ideal diodes.

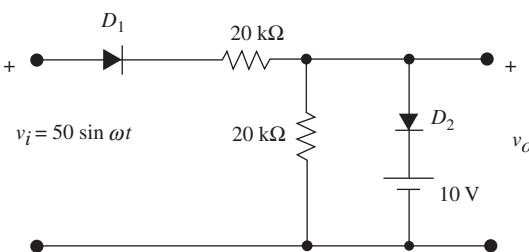


FIGURE 4p.2 Clipping circuit

- (3) The input to the two-level clipper shown in Fig. 4p.3 varies linearly from 0 to 100 V. Plot the transfer characteristic and obtain the output voltage. Assume ideal diodes.

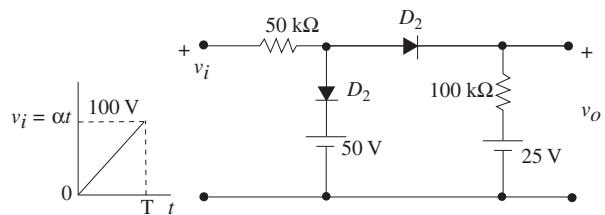


FIGURE 4p.3 The given Clipping circuit for problem 2

- (4) For the circuit shown in Fig. 4p.4, with v_i varying linearly up to 150 V, obtain the transfer characteristic and the output.

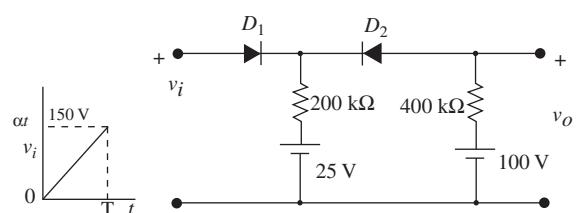


FIGURE 4p.4 Clipping circuit with input

- (5) For the circuit shown in Fig. 4p.5, v_i varies linearly up to 100 V. Obtain the transfer characteristic and the output.

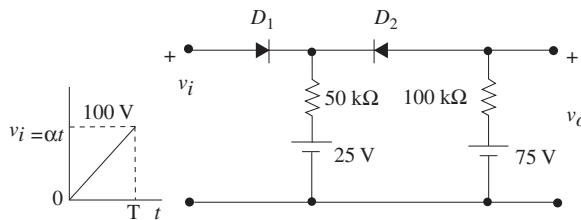


FIGURE 4p.5 The clipping circuit for problem 3

- (6) For the circuit shown in Fig. 4p.6, plot the transfer characteristic for v_i varying from 0 V to 75 V linearly.

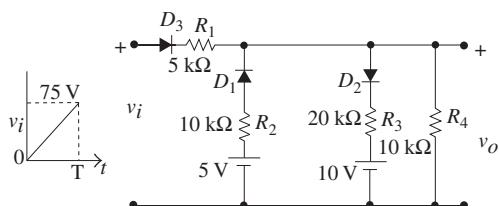


FIGURE 4p.6 The clipping circuit for problem 4

- (7) For the circuit shown in Fig. 4p.7, $R_f = 200 \Omega$, $R = 20 \text{ k}\Omega$, $V_Y = 0$ V. Sketch the output waveform for the given input.

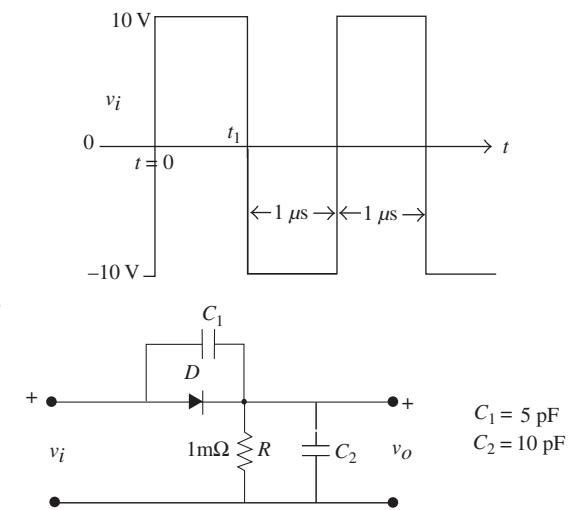


FIGURE 4p.7 Clipping circuit for problem 5

- (8) For the circuit shown in Fig. 4p.8, $R_f = 100 \Omega$, $R = 10 \text{ k}\Omega$, $V_Y = 0$ V. Sketch the output waveform for the specified input.

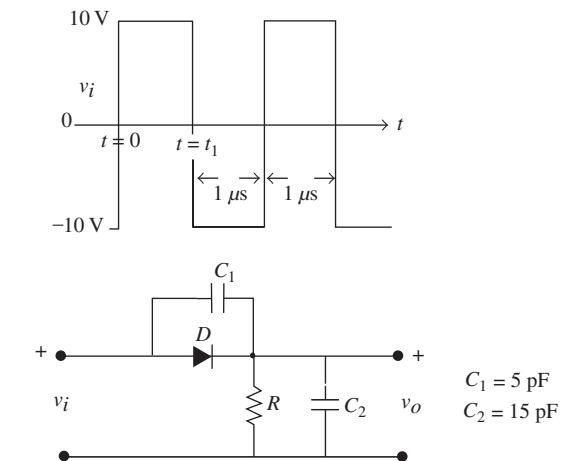


FIGURE 4p.8 The given clipping circuit with input.

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CHAPTER 5

Non-linear Waveshaping: Clamping Circuits

LEARNING OBJECTIVES

After reading this chapter, you will be able to:

- Describe various clamping circuits
 - Derive the necessary relations to plot steady-state output
 - Describe the effect of diode characteristics on the clamping voltage
 - Describe synchronized clamping
 - State and derive the clamping circuit theorem
-

5.1 INTRODUCTION

When a signal is transmitted through a capacitive coupled network, the dc component associated with the input is lost in the output since the capacitor blocks the dc. If the dc component needs to be restored, a clamping circuit is used. Thus, clamping circuits reintroduce the dc component lost during transmission through a capacitive coupled network and hence, are called either dc restorers or dc re-inserters. The output reaches the steady-state value in a few cycles after the application of the input to the clamping circuit (transient period). Circuits that clamp the positive peak of the signal to the zero level are called negative clamps and those that clamp the negative peak of the signal to the zero level are called positive clamps. In general, the output can be referenced to any arbitrarily chosen reference voltage. Circuits that clamp the output to zero or to any dc level are considered here. The necessary relations that enable us to plot the steady-state responses are then derived. The effect of the internal resistance of the source on the output and the influence of diode characteristics on the clamping voltage are also examined. In some applications, clamping is needed only for a finite duration and the time interval for which this is to be accomplished is determined by an external signal called the control signal. The circuit that performs this operation, called synchronized clamping circuit, is also discussed.

5.2 THE CLAMPING CIRCUIT

The clamping circuit essentially consists of an input source, a capacitor of a suitable value and a diode connected in shunt with the output terminals. This clamps the positive peak of the input signal (sinusoidal, in this case) to the zero level. The diode is assumed to be ideal and initially there is no charge on the condenser. v_A is the charge built up on the condenser, C . Figure 5.1 shows a basic clamping circuit.

As the input rises from 0 to V_m in the first quarter cycle, D conducts [see Figs 5.2(a) and 5.3(a)], C charges to V_m . During this period, $v_o = 0$ if the diode

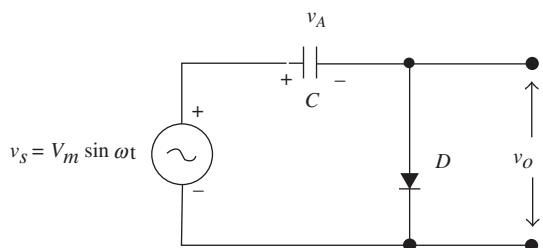


FIGURE 5.1 A negative clamping circuit

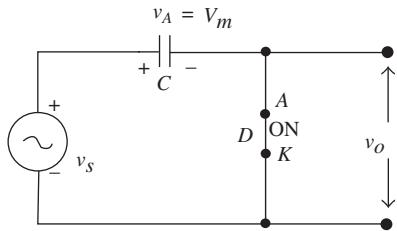


FIGURE 5.2(a) The clamping circuit when the diode is ON

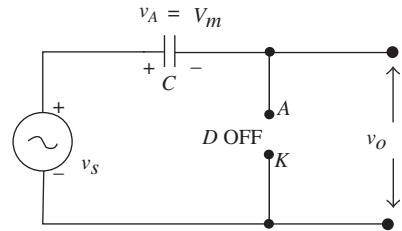


FIGURE 5.2(b) The clamping circuit when the diode is OFF

is ideal. The input falls after the first quarter cycle. $v_s < V_m$, where V_m is the charge on the condenser. As a result, the diode is reverse-biased by a voltage $(v_s - V_m)$. Hence, D is OFF, as shown in Fig. 5.2(b). Thus:

$$v_o = v_s - V_m \quad (5.1)$$

The voltage across C remains unchanged. From Eq. (5.1) at $v_s = 0$, $v_o = -V_m$. And if, $v_s = -V_m$, $v_o = -V_m - V_m = -2 V_m$ and at $v_s = V_m$, $v_o = v_m - V_m = 0$

During the next cycle, the positive peak of the output just reaches the zero level. Hence, in the output, the positive peak is clamped to the zero level. To clamp the positive peak to zero, a negative dc voltage is introduced in this circuit. Therefore, this circuit is called a negative clamp.

Alternatively, if a positive dc voltage is inserted by the clamping circuit so that the negative peak of the input signal is clamped to the zero level, the circuit is called a positive clamp [see Fig. 5.3(b)]. The input to this circuit in Fig. 5.3(b) is a sinusoidal waveform with zero reference level. The output is referenced to $+V_m$ and the negative peak is clamped to zero. The input and output waveforms of negative and positive clamp circuits are represented in Figs. 5.3(a) and 5.3(b), respectively.

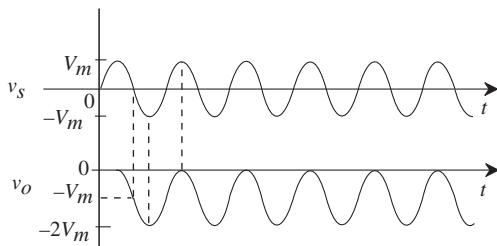
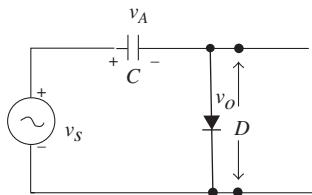


FIGURE 5.3(a) The circuit, input and output waveforms of a negative clamp

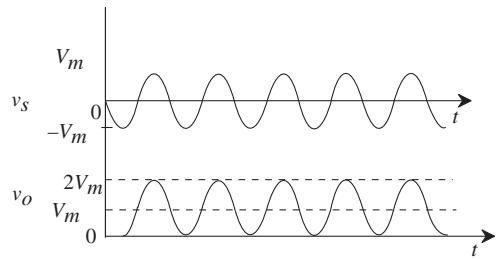
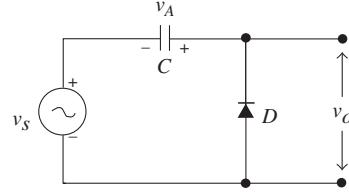


FIGURE 5.3(b) The circuit, input and output waveforms of a positive clamp

5.2.1 The Clamping Circuit for Varying Input Amplitude

In our description of the clamping circuit in the previous section, a steady input signal was assumed; which is always not the case. The amplitude of the input signal may either increase or decrease for various reasons. So, what is the effect of this variation on the output? To answer this question, let us analyse the behaviour of the circuit under the two possible conditions—increase in amplitude and decrease in amplitude.

If the amplitude of the input increases at $t = t_1$ [see Fig. 5.4(a)], once again the diode D conducts for a quarter cycle. The output is zero for this period. Subsequently, the positive peak of the output remains clamped to zero, as shown in Fig. 5.4(b). Obviously, this simple clamping circuit can clamp the output to zero, even if the input increases. However, the output is distorted for a quarter of a cycle.

However, this clamping circuit cannot handle an input signal with decreasing amplitude. When the amplitude of the input signal decreases, the voltage across the capacitor should change to the peak amplitude of the new input so as to clamp the positive peak to the zero level. In this circuit, there is no path for the charge on the capacitor to discharge. To facilitate the discharge of the condenser, a resistance R is introduced in shunt with the diode D , as shown in Fig. 5.5(a).

It is seen from Figs. 5.5(b)(i) and (b)(ii), at $t = t_1$, if the input amplitude is abruptly reduced, as the voltage across the capacitor cannot change instantaneously, the positive peaks will not reach the zero level. However, as the capacitor discharges, the voltage across the capacitor varies exponentially with a time constant, $\tau = RC$. The output reaches the zero level at $t = t_2$, and the positive peak is again clamped to zero after a few cycles [see Fig. 5.5(b)(iii)]. Let us examine the situation in detail, when the positive peak is clamped to zero as shown in Fig. 5.6.

In the proximity of a positive peak, D conducts and at $t = t_2'$, $v_o = 0$. In the absence of the diode, the output should have followed the dashed line with the peak at $t = t_2$. However, because of the diode, the output is zero from t_2' to t_2 ; and in the subsequent cycles the positive peaks of the sinusoidal waveform are clamped to zero. Although, for a small duration between t_2' and t_2 , the output is different from the variation of a sinusoidal signal, i.e., there is a distortion. If the distortion is to be minimized, the capacitor must not lose an appreciable charge in one cycle. For this, the time constant has to be very large as compared to the time period of the input signal.

5.2.2 The Practical Clamping Circuit

In our discussion so far, we have assumed an ideal voltage source with $R_S = 0$. However, a practical voltage source has a finite R_S and the influence of R_S on the output will have to be taken into account. In this section, we examine the influence of the internal resistance of the voltage source on the output of the clamping circuit.

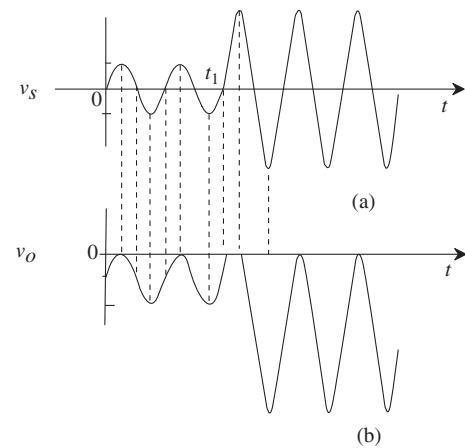


FIGURE 5.4(a) The amplitude of the input increases at t_1 ; (b) the output is once again clamped to zero in a quarter cycle

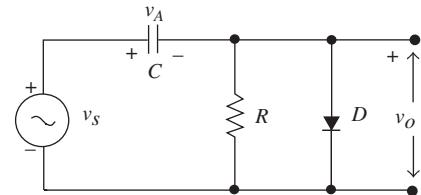


FIGURE 5.5(a) The clamping circuit with a resistance shunted across the diode

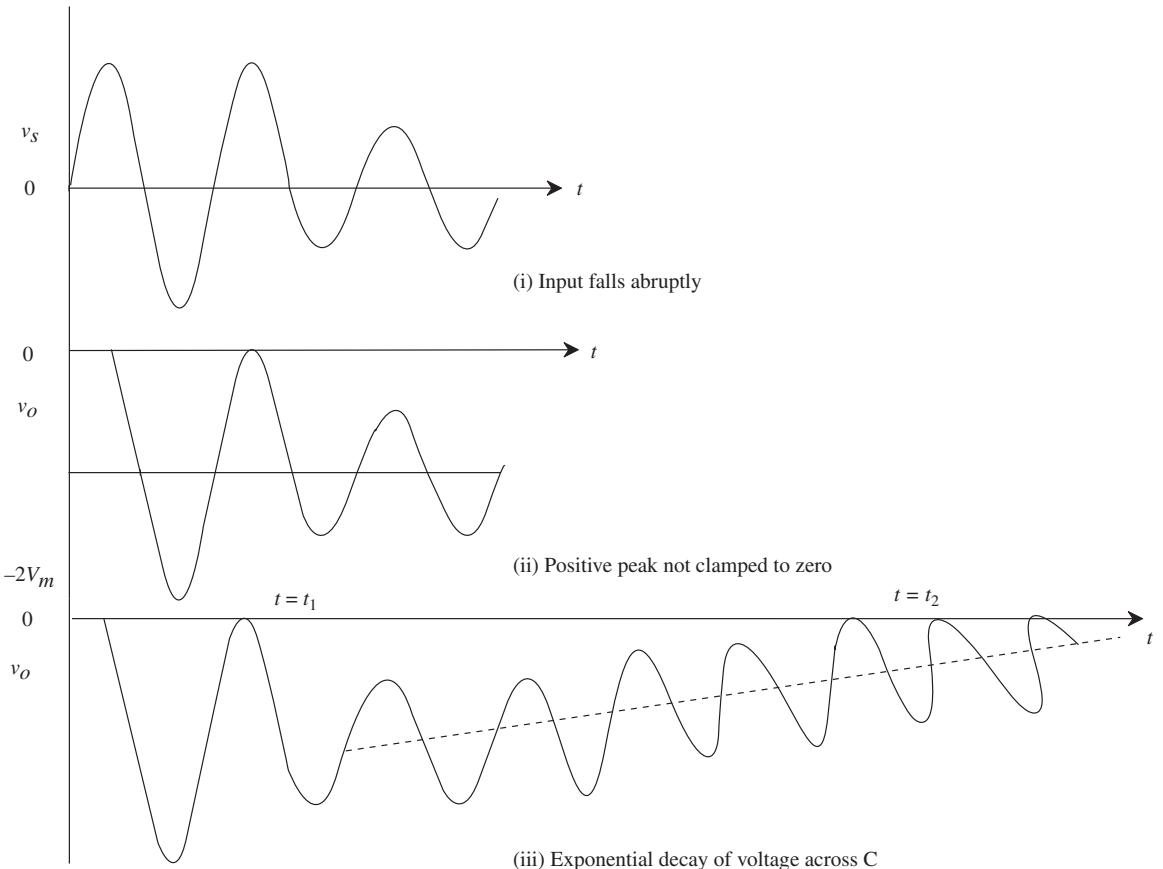


FIGURE 5.5(b) (i) The input when the amplitude decreases at $t = t_1$; (ii) the output when $R = \infty$; and (iii) the output with finite R

If the internal resistance of the source R_S is introduced into the clamping circuit, the modified circuit is as depicted in Fig. 5.7.

When the input is applied to this modified circuit, the output reaches the steady-state value after a few cycles and the positive peaks are clamped to zero. To understand how the output reaches the steady-state, let us examine the equivalent circuits for both the ON and the OFF states of the diode.

When the diode is ON, the circuit is as represented in Fig. 5.8(a). As $R_f \ll R$, this circuit reduces to that shown Fig. 5.8(b). For the purpose of computing the output, the circuit in Fig. 5.8(b) may be redrawn as shown in Fig. 5.8(c).

Figure 5.9 (a) depicts the circuit when the diode is OFF. As the reverse resistance $R_r \gg R$, the effective resistance is R and this circuit reduces as shown in Fig. 5.9(b). Again, for computing the output, the circuit in Fig. 5.9(b) is redrawn as in Fig. 5.9(c).

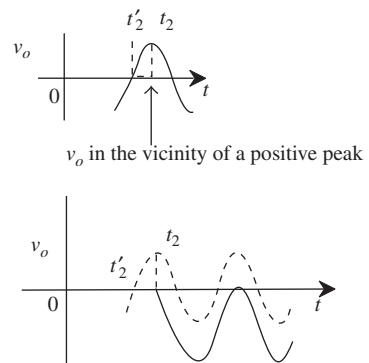


FIGURE 5.6 Output with expanded time scale in the vicinity of a positive peak

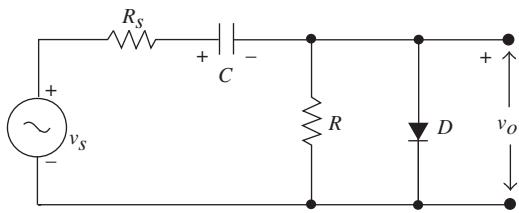


FIGURE 5.7 A clamping circuit where R_s has been taken into account

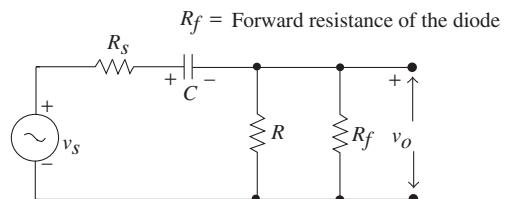


FIGURE 5.8(a) The circuit when the diode is ON

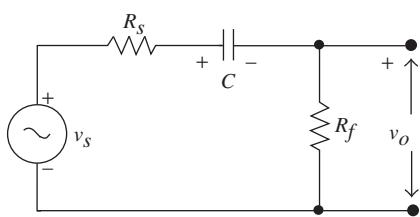


FIGURE 5.8(b) The circuit when D is ON and $R_f \ll R$

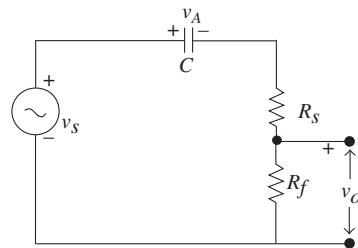


FIGURE 5.8(c) The circuit to calculate the output when the diode is ON

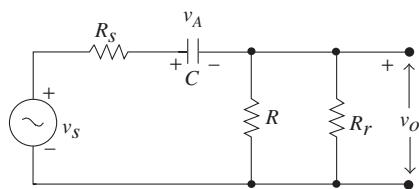


FIGURE 5.9(a) The circuit when D is OFF

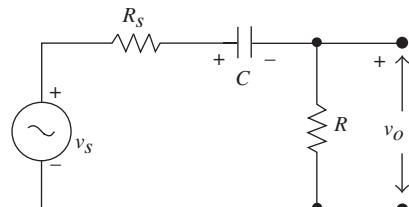


FIGURE 5.9(b) The circuit when $R_r \gg R$

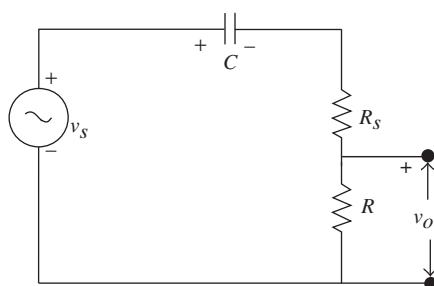


FIGURE 5.9(c) The circuit to calculate the output when the diode is OFF

Transient Response. Let us now consider the square wave v_s , shown in Fig. 5.10(a), applied as input to the clamping circuit in Fig. 5.7. It is expected that the positive peak of the signal will be clamped to the zero level at the output almost instantaneously, but this does not happen. It takes a few cycles for the positive peak to be clamped to the zero level at the output. When the input is applied, the amplitude of the signal above the zero level goes on decreasing with each successive cycle. The output reaches the steady-state only after a few cycles from the instant the input is applied. The variation of the output with time during this period is called the transient response. At the end of this period when the positive peak is clamped to the zero level, the output is said to have reached the steady state.

We now examine how the output reaches the steady-state value after a few cycles (transient response). The variation of the output for the first few cycles, during the periods when the diode is ON and OFF, is then calculated. The input to the clamping circuit is a square wave with a peak-to-peak amplitude V and a finite frequency $f (= 1/T)$ as shown in Fig. 5.10(a).

At $t = 0+$, the diode is ON. Using the equivalent circuit shown in Fig. 5.8(c):

$$v_o(0+) = V \times \frac{R_f}{R_S + R_f}$$

$$\text{If } R_S = R_f : \quad v_o(0+) = \frac{V}{2}$$

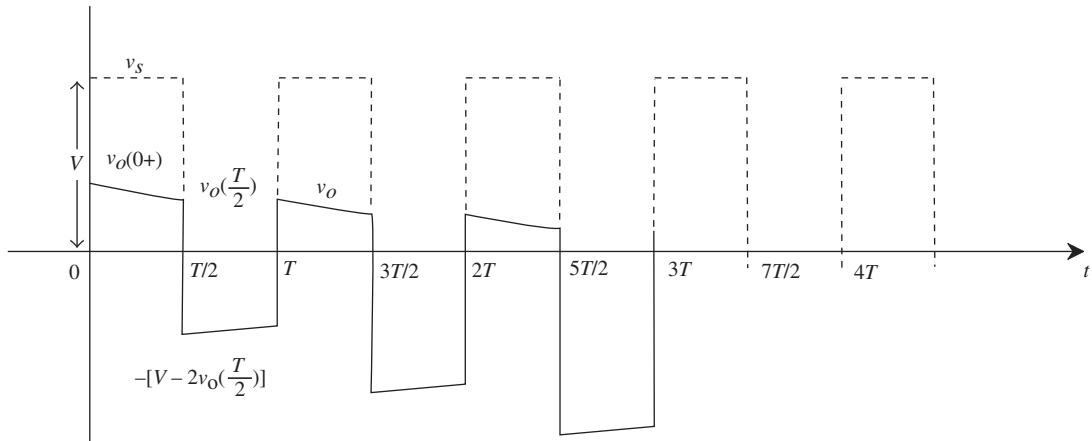


FIGURE 5.10(a) The input and output waveforms of the clamping circuit

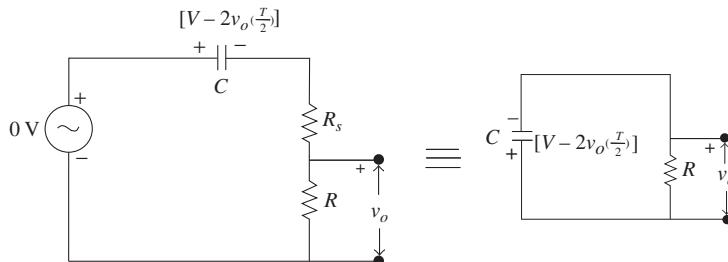


FIGURE 5.10(b) The equivalent circuit to compute the output when D is OFF

During the period 0 to $T/2$, as the input remains constant, the output decays exponentially with the time constant $\tau = C(R_S + R_f)$; and at $t = T/2$; the volatage across R_f is:

$$v_o \left(\frac{T}{2} \right) = v_o(0+) e^{-T/2\tau} = \frac{V}{2} e^{-T/2\tau}$$

Hence, the total voltage across $(R_s + R_f) = 2v_o (T/2)$. The voltage across C is $[V - 2v_o (T/2)]$.

Now at $t = T/2$, the input falls to 0 V, and the diode is OFF. The equivalent circuit shown in Fig. 5.10(b) is the same as the equivalent circuit shown in Fig. 5.9(c), except that the capacitor voltage is indicated here. Since $R_S \ll R$, the output voltage v_o is almost the same as $[V - 2v_o (T/2)]$ but with a negative sign. Hence the output at $(T/2)+$ abruptly falls to $[V - 2v_o (T/2)]$. During the period $T/2$ to T , the input remains constant, the output decays exponentially with the time constant $\tau = C(R + R_s)$.

$$v_o(T) = - \left[V - 2v_o \left(\frac{T}{2} \right) \right] e^{-T/2\tau}$$

The input once again changes by V . The process is repeated over a few cycles till a steady-state value is reached. Example 5.1 elucidates the process.

EXAMPLE

Example 5.1: The input in Fig. 5.11(a) is applied to the practical clamping circuit in Fig. 5.11(b). Compute the output till it reaches the steady-state. Given that $f = 5 \text{ kHz}$, $R_s = 0.1\text{k}\Omega$, $R_f = 0.1\text{k}\Omega$, $R_r = \infty$.

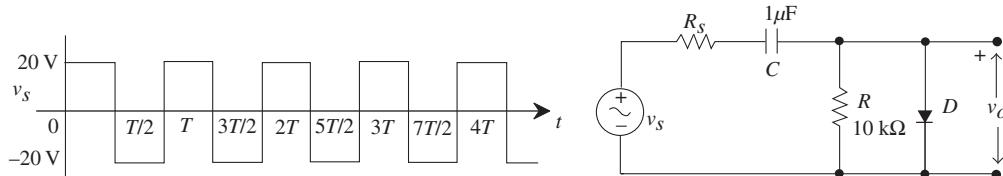


FIGURE 5.11(a) The Input, (b) the given practical clamping circuit

Solution: Assume that initially the capacitor is uncharged. The input to the circuit is a symmetric square wave whose amplitude varies from -20 V to 20 V . When the diode is conducting, using the circuit shown in Fig. 5.8(c), the output voltage can be calculated. Using Fig. 5.11(c):

$$v_o(0+) = 20 \text{ V} \times \frac{0.1\text{k}\Omega}{0.1\text{k}\Omega + 0.1\text{k}\Omega} = 10 \text{ V}$$

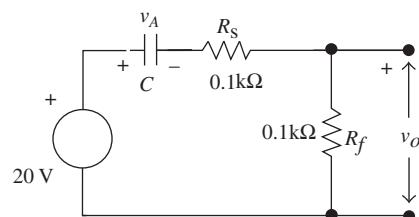


FIGURE 5.11(c) The circuit to calculate the output when D is ON

When the input abruptly changes by 20 V , the output also jumps by 10 V . As the input is constant during the period 0 to $T/2$, the output decays exponentially with time constant τ .

$$\tau = (R_f + R_s) C = 0.2 \times 10^3 \times 1 \times 10^{-6} = 0.2 \text{ ms}$$

As

$$f = 5 \text{ kHz}, \quad T = \frac{1}{f} = 0.2 \text{ ms} \quad T/2 = 0.1 \text{ ms}, \quad T = \tau$$

Hence,

$$v_o \left(\frac{T}{2} \right) = 10 e^{-T/2\tau} = 10 e^{-1/2} = 6 \text{ V}$$

Using Fig. 5.11(d), we can calculate the voltage v_A across C . The voltage across capacitor v_A is:

$$v_A = 20 \text{ V} - (6 \text{ V} + 6 \text{ V}) = 8 \text{ V}$$

At $t = T/2$, the input falls to -20 V , the diode is in the OFF state and the equivalent circuit of Fig. 5.11(e) is used. As $R \gg R_S$, the drop across R_S is negligible. This circuit is redrawn as shown in Fig. 5.11(f).

$$\therefore v_o = -20 \text{ V} - 8 \text{ V} = -28 \text{ V}$$

The output falls to -28 V suddenly. As the input remains constant from $T/2$ to T , the output decays with time constant $\tau' = 10.1 \text{ k}\Omega \times 1 \mu\text{F} = 10.1 \text{ ms}$. Thus, $T/2$ is 0.1 ms and $\tau' = 10.1 \text{ ms}$, which implies that $T/2 \ll \tau'$. Hence, there is no appreciable decay of the output when,

$$v_o(T) = -28 e^{-T/\tau'} \approx -28 \text{ V}$$

In other words, the output remains constant. In the interval $T/2$ to T , as the output remains constant, the voltage across the capacitor remains unchanged. At $t = T$, the input abruptly rises to 20 V . At that instant, D is ON, as the voltage across C is 8 V , $v_o = 6 \text{ V}$ and in the interval T to $3T/2$ the output voltage decays exponentially.

$$v_o \left(\frac{3T}{2} \right) = 6 e^{-1/2} = 3.6 \text{ V}$$

Voltage across $C = v_A = 20 - (3.6 + 3.6) = 12.8 \text{ V}$ and at $t = 3T/2$, $v_o = -20 \text{ V} - 12.8 \text{ V} = -32.8 \text{ V}$

As the voltage does not change much during the interval $3T/2$ to $2T$, at $t = 2T$, the output again returns to 3.6 V .

At $t = 5T/2$

$$v_o = 3.6 e^{-1/2} = 2.2 \text{ V}$$

$$\therefore v_A = 20 - (2.2 + 2.2) = 15.6 \text{ V}$$

$$v_o = -20 \text{ V} - 15.6 \text{ V} = -35.6 \text{ V}$$

The output remains at -35.6 V during the interval $5T/2$ to $3T$. This again returns to 2.2 V at $t = 3T$ and decays during the interval $3T$ to $7T/2$.

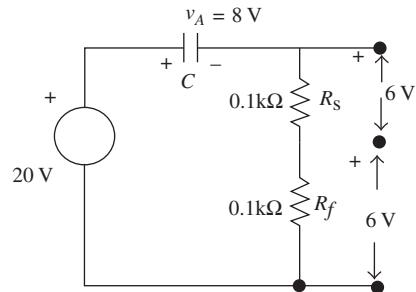


FIGURE 5.11(d) Circuit to calculate v_A

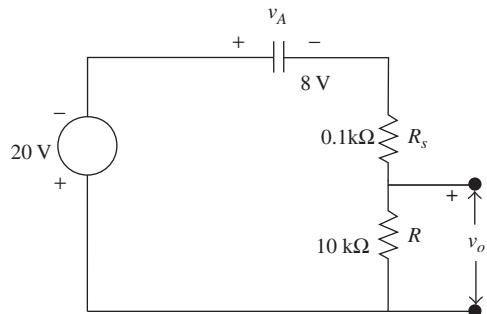


FIGURE 5.11(e) Circuit to calculate the output when D is OFF

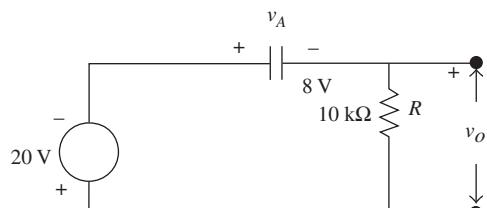


FIGURE 5.11(f) The simplified circuit to calculate the output voltage v_o

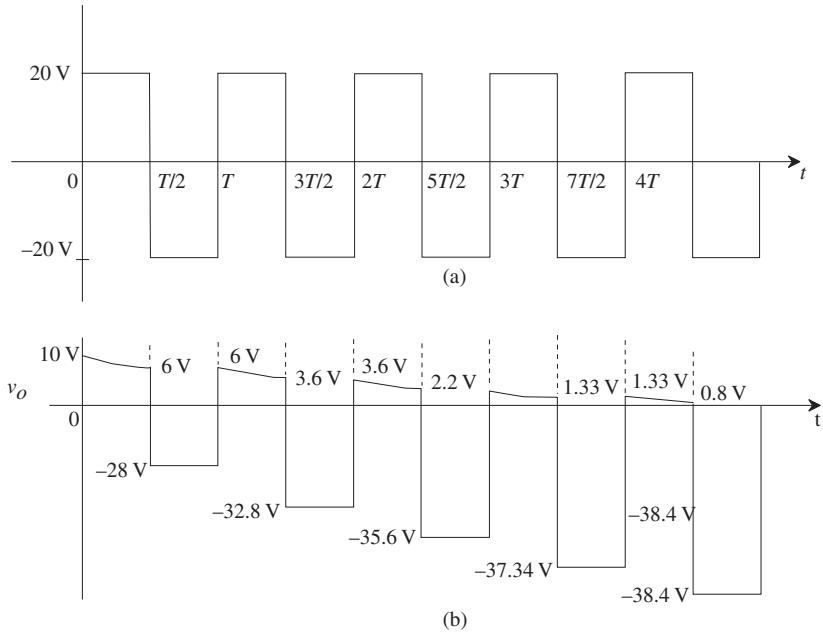


FIGURE 5.12(a) The given waveforms; (b) the output waveforms

$$v_o \left(\frac{7T}{2} \right) = 2.2 e^{-1/2} = 1.33 \text{ V} \quad v_A = 20 - (1.33 + 1.33) = 20 - 2.66 = 17.34 \text{ V}$$

$$v_o = -20 \text{ V} - 17.34 \text{ V} = -37.34 \text{ V}$$

This procedure is repeated. It is seen that the output reaches the steady state in a few cycles, wherein the positive peaks of the input are clamped to a zero level (strictly speaking, to V_Y) at the output (see Fig. 5.12).

Calculating the Steady-state Voltages. It is seen from Example 5.1 that if a square wave is applied as an input to a clamping circuit, the output reaches the steady-state value after a few cycles. Hence, for the input in Fig. 5.13(a), the output of the clamping circuit is given in 5.13(b).

The output at the steady-state is as shown in Fig. 5.13(b) with voltage levels V_1 , V'_1 , V_2 and V'_2 ; these can be plotted to scale after calculation. To calculate these four unknowns, four equations to be are obtained:

Consider the situation at $t = 0-$

At

$$t = 0-, \quad v_s = V'' \quad \text{and} \quad v_o = V'_2$$

The diode is reverse-biased and the corresponding equivalent circuit is as shown in Fig. 5.14(a).

The voltage across the capacitor terminals at $t = 0-$ is:

$$v_A(0-) = v_s - v_i \quad (5.2)$$

$$v_s = V'' \quad \text{and} \quad V'_2 = v_i \frac{R}{R_s + R}$$

$$\therefore v_i = V'_2 \frac{(R_s + R)}{R}$$

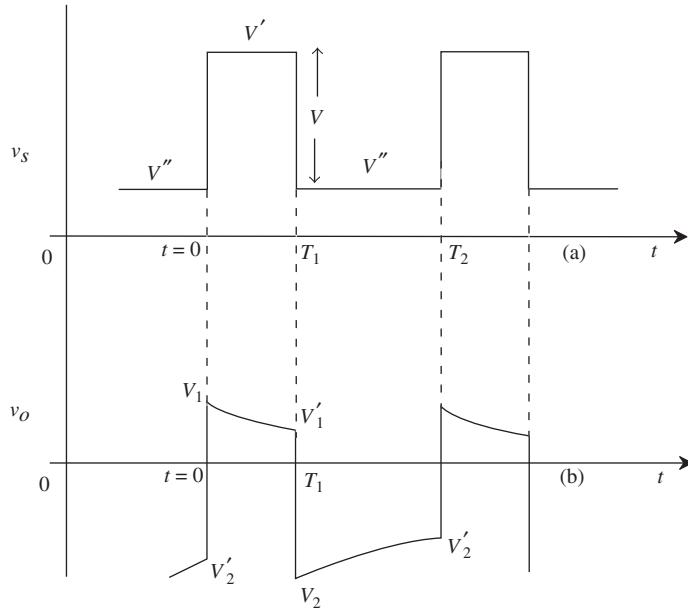


FIGURE 5.13(a) The input to the clamping circuit; and (b) the steady-state output

Substituting the values of v_s and v_i in Eq. (5.2):

$$v_A(0-) = V'' - V_2' \frac{(R_s + R)}{R} \quad (5.3)$$

Consider the situation at the instant $t = 0+$. At $t = 0+$, $v_s = V'$ and $v_o = V_1$. The diode is ON and the corresponding equivalent circuit is as shown in Fig. 5.14(b).

The voltage across the capacitor terminals at $t = 0+$ is:

$$v_A(0+) = v_s - v_i = V' - v_i \quad V_1 = v_i \frac{R_f}{R_s + R_f}$$

$$v_i = \frac{(R_s + R_f)}{R_f} V_1 \quad v_A(0+) = V' - \frac{(R_s + R_f)}{R_f} V_1 \quad (5.4)$$

Since the voltage across the capacitor cannot change instantaneously

$$v_A(0-) = v_A(0+).$$

Hence, from Eqs. (5.3) and (5.4):

$$V'' - \frac{R + R_s}{R} V_2' = V' - V_1 \frac{R_s + R_f}{R_f} \quad (5.5)$$

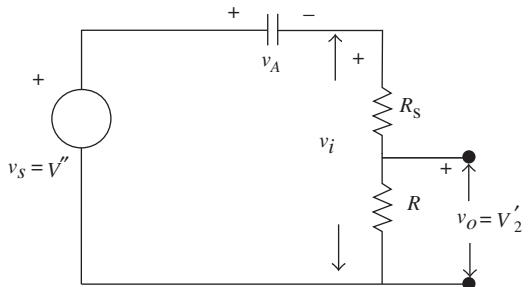


FIGURE 5.14(a) The equivalent circuit when the diode is reverse-biased

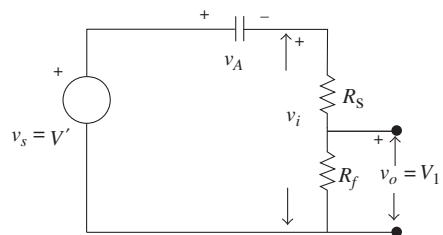


FIGURE 5.14(b) The equivalent circuit when the diode is forward-biased

The peak-to-peak amplitude of the input is V . Therefore,

$$V = V' - V''$$

From Eq. (5.5):

$$V = V' - V'' = V_1 \frac{R_s + R_f}{R_f} - \frac{R + R_s}{R} V_2' \quad (5.6)$$

Once again consider the situation at $t = T_1-$, when $v_s = V'$ and $v_o = V_1'$ and the diode is ON. The equivalent circuit is shown in Fig. 5.14(c).

$$v_A(T_1-) = v_s - v_i = V' - \frac{R_f + R_s}{R_f} V_1' \quad (5.7)$$

Similarly, at $t = T_1+$, since D is OFF, from the equivalent circuit shown in Fig. 5.14(d):

$$v_A(T_1+) = v_s - v_i = V'' - \frac{R + R_s}{R} V_2 \quad (5.8)$$

Again, as $v_A(T_1-) = v_A(T_1+)$, from Eqs. (5.7) and (5.8):

$$\begin{aligned} V' - \frac{R_f + R_s}{R_f} V_1' &= V'' - \frac{R + R_s}{R} V_2 \\ V = V' - V'' &= \frac{R_f + R_s}{R_f} V_1' - \frac{R + R_s}{R} V_2 \end{aligned} \quad (5.9)$$

Further at $t = 0+$, $v_o = V_1$ and in the interval 0 to T_1 , v_o decays with a time constant $(R_f + R_s) C$. Hence:

$$V_1' = V_1 e^{-T_1/(R_f + R_s)C} \quad (5.10)$$

Similarly, in the interval T_1 to T_2 , the diode is reverse-biased and the circuit time constant is $(R_s + R) C$. The voltage V_2 decays to V_2' .

$$V_2' = V_2 e^{-(T_2 - T_1)/(R_s + R)C} \quad (5.11)$$

Equations (5.6), (5.9), (5.10) and (5.11) will enable us to determine the voltages V_1 , V_1' , V_2 and V_2' . If in the circuit shown in Fig. 5.7 $R_s = 0$, equations (5.6) and (5.9) reduce to:

$$V = V_1 - V_2 = V_1' - V_2 \quad (5.12)$$

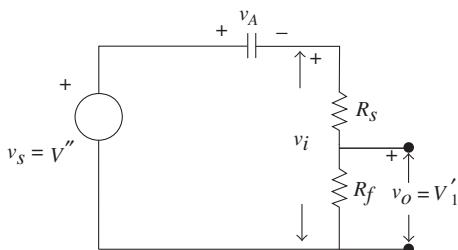


FIGURE 5.14(c) The circuit to calculate $v_A(T_1-)$

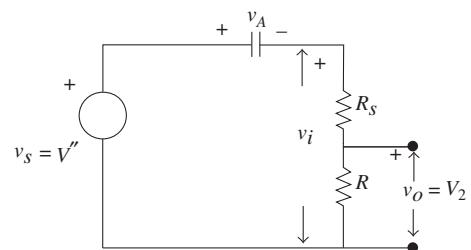


FIGURE 5.14(d) Circuit to calculate $v_A(T_1+)$

It is evident from the above discussion that the output is independent of the levels V' and V'' associated with the input and is only determined by the amplitude V .

Subtracting Eq. (5.9) from Eq. (5.6):

$$\frac{R_f + R_s}{R_f} (V_1 - V'_1) - \frac{R + R_s}{R} (V'_2 - V_2) = 0 \quad (5.13)$$

If $V_1 - V'_1 = \Delta_f$ and $V'_2 - V_2 = \Delta_r$, from Eq. (5.13):

$$\frac{R_f + R_s}{R_f} \Delta_f = \frac{R + R_s}{R} \Delta_r$$

$$\Delta_f = \left(\frac{R_f}{R_s + R_f} \right) \left(\frac{R + R_s}{R} \right) \Delta_r \quad (5.14)$$

If $R_s \ll R$

$$\Delta_f = \frac{R_f}{R_s + R_f} \Delta_r \quad (5.15)$$

where, Δ_f is the tilt in the forward direction and Δ_r is the tilt in the reverse direction.

If $R_s \ll R_f$:

$$\Delta_f \approx \Delta_r \quad (5.16)$$

5.2.3 Clamping the Output to a Reference Voltage (V_R)

In the clamping circuit seen in Fig. 5.7, the positive peak of the input signal is clamped to the zero level at the output. However, if the positive peak is to be clamped to a chosen reference voltage V_R for the circuit in Fig. 5.7, a dc voltage V_R is to be included in the output. The circuit in Fig. 5.15 shows a clamping circuit similar to that seen in Fig. 5.7 except for the fact that a reference voltage V_R is included and R_s is zero.

To obtain the steady-state response of the circuit, we assume that V_R is zero. This circuit, then, is the clamping circuit that clamps the positive peak of the input signal to V_Y as shown in Fig. 5.7.

The steady-state responses for symmetric and unsymmetric square-wave inputs are plotted in Fig. 5.16(a) and Fig. 5.16(b), respectively.

Solving the four equations [Eqs. (5.6), (5.9), (5.10) and (5.11)], the values of V_1 , V'_1 , V_2 and V'_2 can be evaluated. To find these steady state output voltages with V_R included, add the value of V_R to each of these values. If, on the other hand, the polarity of V_R is reversed, add $-V_R$ to each of the values computed. The result is that the positive peak in the output is clamped to $-V_R$, as shown in Fig. 5.17.

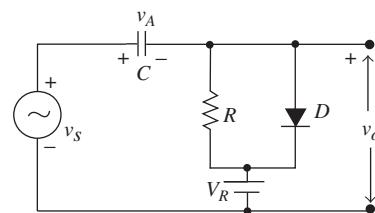


FIGURE 5.15 The circuit that clamps the positive peak of the input to V_R

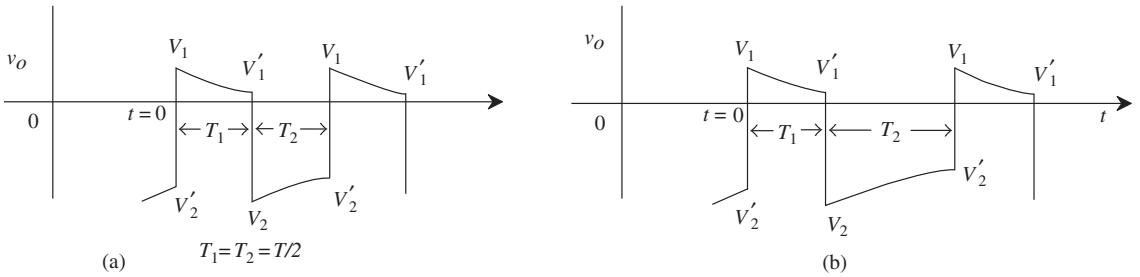
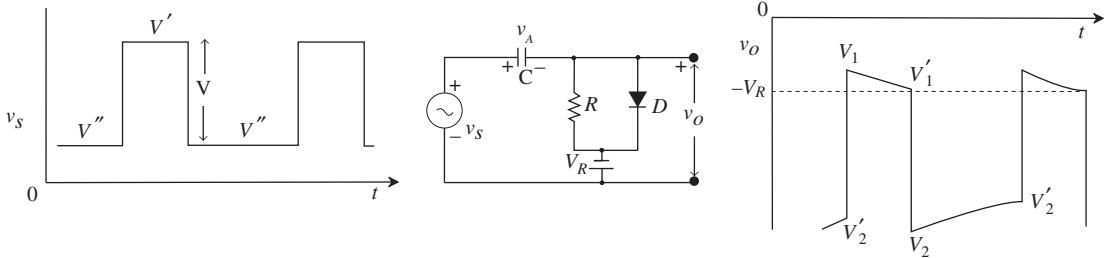
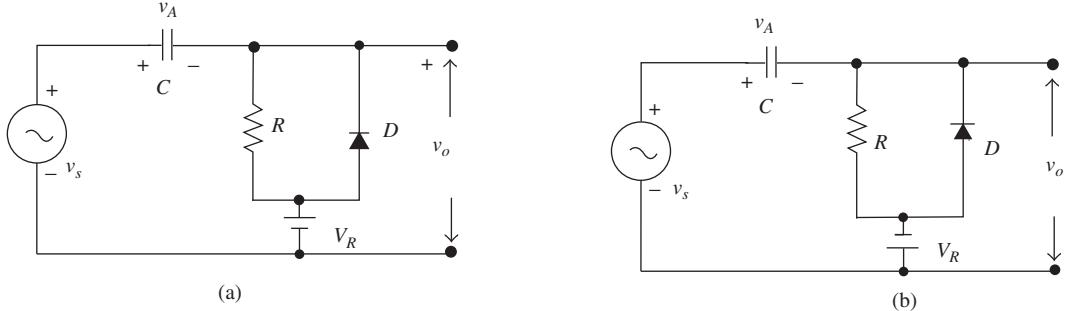


FIGURE 5.16 The steady-state response for (a) symmetric square-wave input; and (b) unsymmetric square-wave input

FIGURE 5.17 The positive peak of the input clamped to $-V_R$ FIGURE 5.18 (a) The negative peak of the input clamped to $+V_R$; and (b) the negative peak of the input clamped to $-V_R$

Similarly, look at the circuits in Fig. 5.18(a) and (b). The circuits here clamp the negative peak of the input to $+V_R$ and $-V_R$ respectively. To simplify the analysis of the clamping circuits let us assume:

- The forward resistance of the diode D when ON is negligible. We assume that there is no distortion in the output when D is ON.
- The time constant $\tau (= RC)$ is so large when compared to the time period of the signal under consideration that practically there is no change in the voltage on the condenser C , when D is OFF.
- The internal resistance of the source v_s , $R_s = 0$.

Based on these assumptions, a simple and straight forward method to analyse clamping circuits is as follows:

- Step 1:** Start the analysis from the time duration during which D is ON. If the starting time duration keeps D OFF, skip that time interval.
- Step 2:** Consider the relevant circuit, taking care of the polarities of the voltages. Calculate v_o .
- Step 3:** Find v_A , the voltage on C .

Step 4: Consider the next time interval. Draw the circuit, taking care of the polarities of the input and v_A . Calculate v_o .

If the input is periodic you can plot the steady-state output. To understand the procedure let us consider an example.

E X A M P L E

Example 5.2: For the clamping circuit shown in Fig. 5.19(a) from the given input, calculate and plot the steady-state output. Given $C = 0.1 \mu\text{F}$, $R = 100 \text{k}\Omega$, $V_R = 5 \text{ V}$, $f = 5000 \text{ Hz}$.

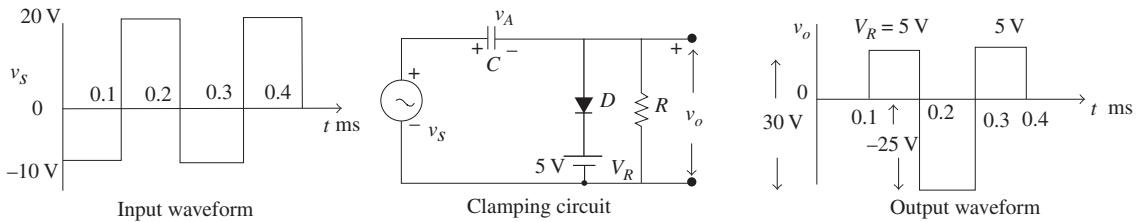


FIGURE 5.19(a) The given biased clamping circuit with input and output waveforms

Solution: Given $f = 5000 \text{ Hz}$. Therefore, $T = \frac{1}{5000} = 0.2 \text{ ms}$.

$$\frac{T}{2} = 0.1 \text{ ms}, \tau = RC = 100 \times 10^3 \times 0.1 \times 10^{-6} = 10 \text{ ms}.$$

$\tau \gg T/2$, hence the voltage on C remains unchanged during the period D is OFF.

Step 1: During the interval 0 to 0.1 ms, as v_s is -10 V D is OFF and $v_o = 0$.

Step 2: During the interval 0.1 to 0.2 ms, v_s is 20 V, hence D is ON. The circuit of Fig. 5.19(a) is drawn as shown in Fig. 5.19(b), $v_o = 5 \text{ V}$

Step 3: Now applying the KVL equation around the input loop, we have: $v_A = v_s - V_R = 20 - 5 = 15 \text{ V}$. The assumption is that v_A remains unchanged.

Step 4: During 0.2 to 0.3 ms, D is OFF. $v_A = 15 \text{ V}$, $v_s = -10 \text{ V}$. The circuit is as shown in Fig. 5.19(c).

Thus: $v_o = -v_s - v_A = -10 - 15 = -25 \text{ V}$.

The output waveform is plotted in Fig. 5.19(a). The positive peak of the input is clamped to +5 V. The peak-to-peak swing at the input is 30 V. It remains the same in the output.

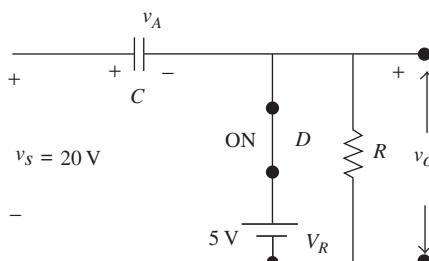


FIGURE 5.19(b) The circuit when D is ON during 0.1 to 0.2 ms

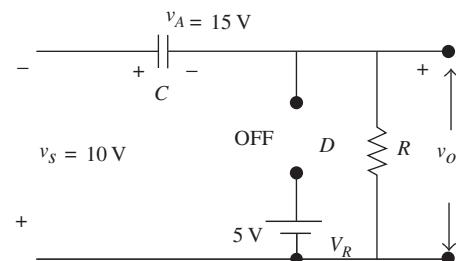


FIGURE 5.19(c) The circuit during 0.2 and 0.3 ms when D is OFF

EXAMPLE

Example 5.3: Working with the same circuit and inputs, repeat Example 5.2, using a Si diode with $V_{AK} = 0.7$ V, when D is ON.

Solution:

Step 1: During the interval 0 to 0.1 ms, as v_s is -10 V, D is OFF and $v_o = 0$.

Step 2: During the interval 0.1 to 0.2 ms, v_s is 20 V, hence D is ON. The circuit of Fig. 5.19(a) is drawn as shown in Fig. 5.19(d). $v_o = 5.7$ V

Step 3: Now applying the KVL equation around the input loop, we have:

$$v_A = v_s - V_R - V_{AK} = 20 - 5 - 0.7 = 14.3 \text{ V}$$

Step 4: During 0.2 to 0.3 ms, D is OFF, $v_A = 14.3$ V, $v_s = -10$ V. The circuit is shown in Fig. 5.19(e). Thus:

$$v_o = -v_s - v_A = -10 - 14.3 = -24.3 \text{ V.}$$

The output waveform is plotted in Fig. 5.19(f). The positive peak of the input is clamped to $+5.7$ V. The peak-to-peak swing at the input is 30 V. It remains the same in the output also.

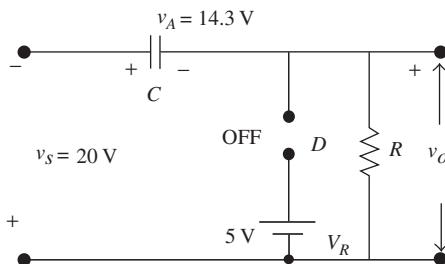


FIGURE 5.19(e) The circuit during 0.2 and 0.3 ms when D is OFF

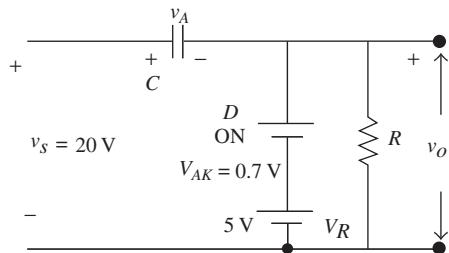


FIGURE 5.19(d) Circuit when D is ON during 0.1 to 0.2 ms

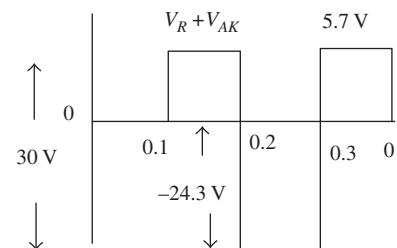


FIGURE 5.19(f) The output waveform

EXAMPLE

Example 5.4: Draw the steady-state output waveform for the given biased clamping circuit shown in Fig. 5.20, when the input is a square-wave signal of amplitude ± 10 V. Assume that C is large.

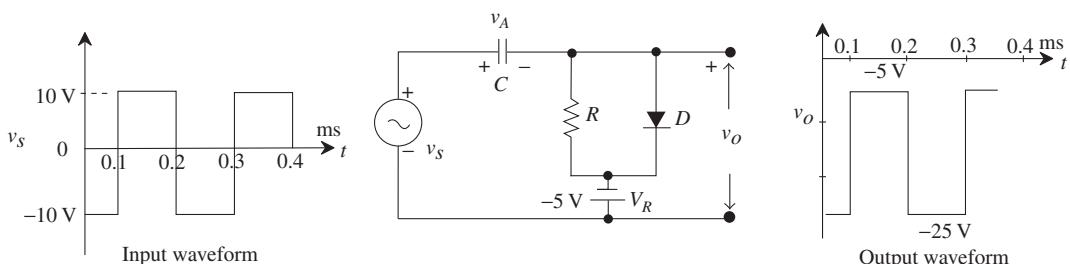


FIGURE 5.20 The given biased negative clamper with $V_R = -5$ V

Solution: The diode D conducts, when the input changes to $+10$ V, $V_o = -5$ V Then the capacitor charges to $(v_s - v_o) = 15$ V.

Under steady-state conditions $v_o = v_s - v_A = v_s - 15$ V

When $v_s = 10$ V, $v_o = 10 - 15 = -5$ V

When $v_s = -10$ V, $v_o = -10 - 15 = -25$ V

The positive peak is clamped to $V_R = -5$ V, in the output, as shown in Fig.5.20.

EXAMP LE

Example 5.5: Draw the steady-state output waveform for the given biased clamping circuit shown in Fig. 5.21, when the input is ± 10 V square wave. Assume that C is large.

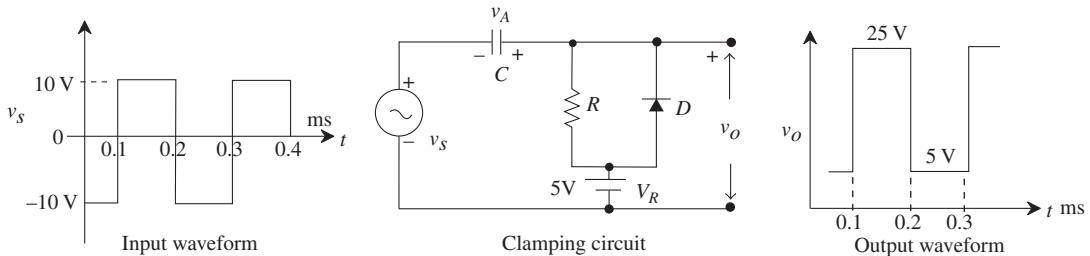


FIGURE 5.21 The given biased positive clamper with $V_R = 5$ V

Solution: The diode D conducts, when v_s changes to -10 V, then the capacitor charges to $v_A = -15$ V.

Under steady-state conditions $v_o = v_s - (-v_A) = v_s + v_A = v_s + 15$ V

When $v_s = 10$ V, $v_o = 10 + 15 = 25$ V

When $v_s = -10$ V, $v_o = -10 + 15 = 5$ V

The negative peak is clamped to $V_R = 5$ V in the output, Fig.5.21.

EXAMP LE

Example 5.6: Draw the steady state output waveform for the given biased clamping circuit shown in Fig. 5.22, when the input is ± 10 V square wave. Assume that C is large.

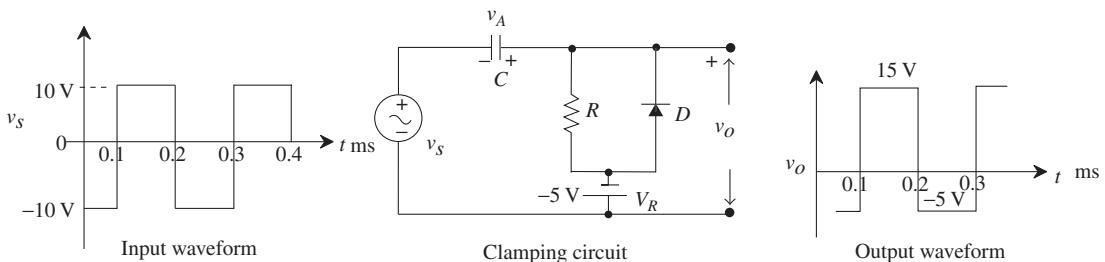


FIGURE 5.22 The given biased positive clamper with $V_R = -5$ V

Solution: The diode D conducts, when v_s changes to -10 V. Then the capacitor charges to $v_A = v_s - V_R = -10 - (-5) = -5$ V.

Under steady-state conditions, $v_o = v_s - (-v_A) = v_s + v_A = v_s - 5$ V.

When $v_s = 10$ V, $v_o = 10 + 5 = 15$ V.

When $v_s = -10$ V, $v_o = -10 + 5 = -5$ V.

The negative peak is clamped to $V_R = -5$ V in the output, as shown in Fig.5.22.

5.2.4 The Design of a Clamping Circuit

Let us now try to design a clamping circuit to clamp the positive peak of an input signal (say, a sinusoidal signal) to zero level as shown in Fig. 5.5(a). As discussed in Section 5.2.1 earlier, when the diode is OFF, ideally its reverse resistance is either infinity or, in practice, very large (of the order of tens of mega ohms). If the input abruptly falls in amplitude, as shown in Fig. 5.5(b), the time constant associated with the discharge of $C (= R, C)$ is large. Then the positive peak of the signal in the output may not be clamped to zero, even after many cycles, in the absence of R . In numerous applications, the requirement is that the signal should once again be clamped to zero level in at least a few cycles. Hence, R is shunted across the diode D to reduce the time constant. On this account, R is so chosen that it is significantly smaller than R_r . Hence,

$$R = \frac{R_r}{a} \quad (5.17a)$$

where a is a large number. During the period the diode is OFF, some charge is lost by the condenser C . This lost charge is replenished when the diode is ON; during this period the resistance offered by the diode is R_f , which is very small (of the order of few tens of ohms). To ensure that the charge is acquired by the capacitor in a relatively small amount of time, R should be significantly larger than R_f . Hence,

$$R = aR_f \quad (5.17b)$$

From Eqs. (5.17a) and (5.17b),

$$R = \sqrt{R_f R_r} \quad (5.17c)$$

If the relation between $f (= 1/T)$, the frequency of the applied input and RC is specified as a desired value k :

$$\frac{RC}{T} = k \quad (5.18)$$

Then C is chosen as:

$$C = \frac{kT}{R} \quad (5.19)$$

If the negative peak of the input is to be clamped to V_{R1} as in Fig.5.23, the reference voltage to be assigned is

$$V_R = V_{R1} + V_D, \quad (5.20)$$

where V_D is the diode voltage when ON. Let us consider a specific example to illustrate this.

E X A M P L E

Example 5.7: Design a clamping circuit to clamp the negative peaks to 5 V given that $R_f = 0.1 \text{ k}\Omega$, $R_r = 1000 \text{ k}\Omega$, $V_{R1} = 5$ V, $f = 2 \text{ kHz}$ and $k = 10$, $V_D = 0.7$ V.

Solution: Using Eq. (5.17a):

$$R = \sqrt{R_f R_r} = \sqrt{0.1 \times 1000} = 10 \text{ k}\Omega$$

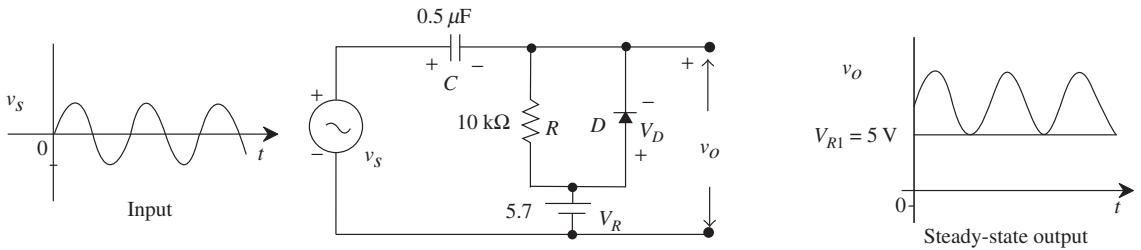


FIGURE 5.23 The given biased positive clamping circuit and the steady-state output

Using Eq. (5.19):

$$C = \frac{10T}{R} = \frac{10 \times 0.5 \times 10^{-3}}{10 \times 10^3} = 0.5 \mu\text{F}$$

As the negative peak is required to be clamped to +5 V, the reference voltage source is chosen using Eq. (5.20) as:

$$V_R = V_{R1} + V_D = 5 + 0.7 = 5.7 \text{ V}$$

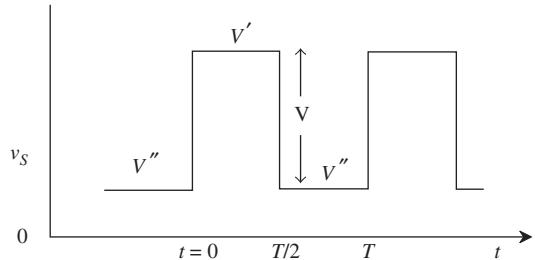
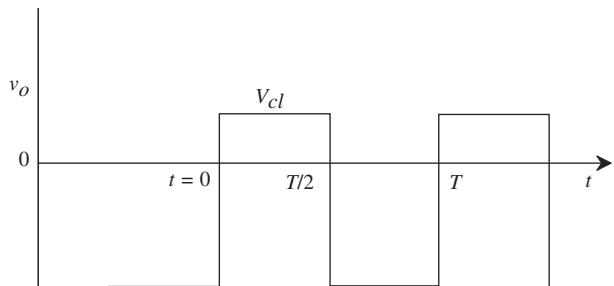
The circuit with input and output waveforms is shown in Fig. 5.23.

5.3 THE EFFECT OF DIODE CHARACTERISTICS ON THE CLAMPING VOLTAGE

For the clamping circuit shown in Fig. 5.7, to obtain the steady-state response, the diode is replaced by R_f when ON and $R_f = \infty$ when OFF. Though the positive peak of the signal in the output is ideally required to be clamped to the zero level, in practice it is clamped to a voltage $V_{cl} = V_y$, where V_y is the cut-in voltage of the diode. In a practical diode, the current variation is non-linear in nature. Hence, we consider the influence of the diode characteristics on the clamping voltage, V_{cl} and show that the clamping voltage (V_{cl}) changes with a change in the amplitude of the input signal. Let us consider the clamping circuit described in Fig. 5.7 and let its input be a symmetric square wave as shown in Fig. 5.24(a).

If C is large, irrespective of whether the diode is ON or OFF, the time constants are large so that the output is also a square wave. The steady-state output has a general form as shown in Fig. 5.24(b).

In obtaining the steady-state response, we assumed that the diode is ideal with a small R_f . In practice, however, an idealized diode, when ON, is represented as a switch in series with a battery voltage of V_y , a resistance R_f [see Figure 5.24(c)]; and biased by V' as shown in Fig. 5.24(a).

FIGURE 5.24(a) A symmetric square-wave input with peak-to-peak amplitude V FIGURE 5.24(b) The steady-state output with a large C

We now consider the V-I characteristic of the practical diode to understand the influence of the diode characteristics on the clamping voltage. The diode current is given by the relation:

$$I = I_0 e^{V/\eta V_T} \quad (5.21)$$

When the diode is ON, the positive peak of the signal is clamped to V_{cl} and the current in the diode is I_{cl} . V_{cl} is the voltage to which the positive peak is clamped.

$$I_{cl} = I_0 e^{V_{cl}/\eta V_T} \quad (5.22)$$

The equivalent circuit when the diode is ON, when $v_s = V'$ with $R_S = 0$ is shown in Fig. 5.24(d). From Fig. 5.24(d):

$$v_A = V' - V_{cl} \quad (5.23)$$

During the negative half-cycle of the square-wave input, $v_s = V''$ and the diode is OFF. The equivalent circuit is given in Fig. 5.24(e).

From Fig. 5.24(e):

$$v_A = V'' + v_o \quad (5.24)$$

And

$$v_o \simeq V - V_{cl} \quad (5.25)$$

Using Eqs. (5.24) and (5.25):

$$v_A - V'' = V - V_{cl} \quad (5.26)$$

In practice, $V_{cl} \approx V_\gamma$ and V can be typically of the order of a few tens of volts. Thus, $V \gg V_{cl}$. From Eq. (5.26):

$$v_A - V'' = V \quad (5.27)$$

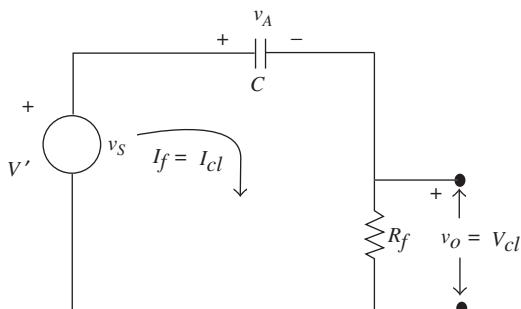


FIGURE 5.24(d) The equivalent circuit when the diode is ON

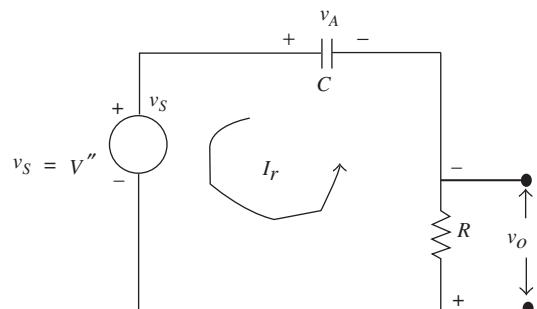


FIGURE 5.24(e) The equivalent circuit when the diode is OFF

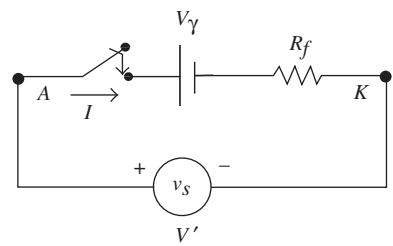


FIGURE 5.24(c) The equivalent circuit of the forward-biased diode

As the net voltage across R is V , I_r the discharging current of C is given by the relation:

$$I_r = \frac{V}{R} \quad (5.28)$$

As the input is a symmetric square wave, under steady-state, the charge gained by C when the diode is ON should be equal to the charge lost by C when the diode is OFF.

Therefore,

$$I_{cl} = I_r \quad (5.29)$$

From Eqs. (5.22) and (5.28):

$$\frac{V}{R} = I_o e^{V_{cl}/\eta V_T} \quad (5.30)$$

$$e^{V_{cl}/\eta V_T} = \frac{V}{I_o R}$$

Taking logarithms to the natural base:

$$\frac{V_{cl}}{\eta V_T} = \ln \frac{V}{I_o R}$$

$$V_{cl} = \eta V_T \ln \frac{V}{I_o R} \quad (5.31)$$

$$\frac{dV_{cl}}{dV} = \eta V_T \times \frac{I_o R}{V} \times \frac{1}{I_o R} = \frac{\eta V_T}{V}$$

$$dV_{cl} = \eta V_T \times \frac{dV}{V} \quad (5.32)$$

Equation (5.31) gives the steady-state clamping voltage and Eq. (5.32) describes the variation in the clamping voltage with a change in the amplitude of the input signal. For a silicon diode used in a clamping circuit for which $V_{cl} = V_\gamma = 0.5$ V, $\eta = 2$, $V = 10$ V and $dV = 1$ V:

$$dV_{cl} = 2 \times 26 \text{ mV} \times \frac{1}{10} = 5.2 \text{ mV}$$

Equation (5.32) suggests that as V increases, the change in the clamping voltage, dV_{cl} , becomes smaller. Also, when the diode is ON, V is the forward-bias. Hence, to ensure that the clamping voltage remains unaltered, the diode must be forward-biased by a larger voltage. The circuit for this is represented in Fig. 5.25(a).

Let us now try to calculate dV_{cl} for this circuit to verify whether this arrangement really ensures negligible change in V_{cl} or not. Redrawing the circuit in Fig. 5.25(a) gives Fig. 5.25(b). The equivalent circuit when the diode is ON, i.e., when $v_s = V$, is shown in Fig. 5.25(c).

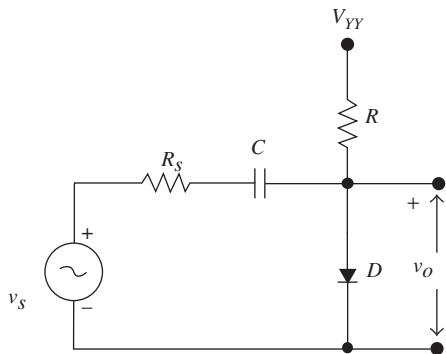


FIGURE 5.25(a) A clamping circuit in which the diode is forward-biased by a large voltage V_{YY}

From Eq. (5.22):

$$I_{cl} = I_0 e^{V_{cl}/\eta V_T}$$

From Fig. 5.25(c):

$$I_R = \frac{V_{YY} - V_{cl}}{R} \approx \frac{V_{YY}}{R} \quad (5.33)$$

as $V_{cl} \ll V_{YY}$.

Writing the KCL equation at node A:

$$I_f + I_R - I_{cl} = 0 \quad (5.34)$$

$$I_f = I_{cl} - I_R = I_{cl} - \frac{V_{YY}}{R} \quad (5.35)$$

Also,

$$v_A = V' - V_{cl} - I_f R_s = V' - V_{cl} - \left(I_{cl} - \frac{V_{YY}}{R} \right) R_s \quad (5.36)$$

When the input goes to V'' , the diode is OFF and the equivalent circuit is as shown in Fig. 5.25(d).

The discharging current I_r is:

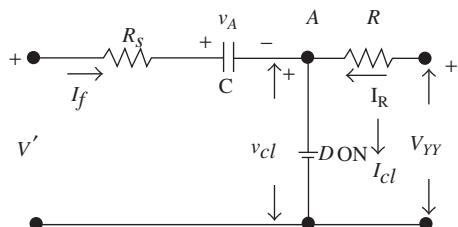


FIGURE 5.25(c) The equivalent circuit of Fig. 5.25(b) when the diode is forward-biased

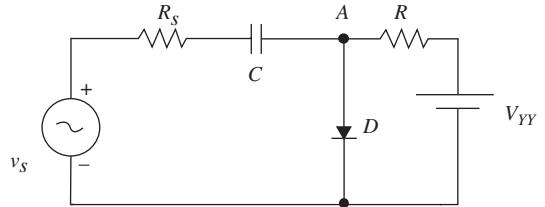


FIGURE 5.25(b) The modified circuit of Fig. 5.25(a)

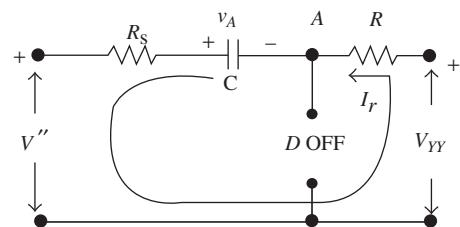


FIGURE 5.25(d) The equivalent circuit of Fig. 5.25(b) when the diode is OFF

$$I_r = \frac{V_{YY} - V'' + v_A}{R + R_S} = \frac{V_{YY} - V'' + v_A}{R} \quad (5.37)$$

since $R \gg R_S$. Put Eq. (5.36) in (5.37):

$$I_r = \frac{1}{R} \left[V_{YY} - V'' + V' - V_{cl} - \left(I_{cl} - \frac{V_{YY}}{R} \right) R_S \right] = \frac{1}{R} \left[V_{YY} \left(1 + \frac{R_S}{R} \right) - V'' + V' - V_{cl} - I_{cl} R_S \right]$$

But $V' - V'' = V$. Therefore:

$$I_r = \frac{1}{R} \left[V_{YY} \left(1 + \frac{R_S}{R} \right) + V - V_{cl} - I_{cl} R_S \right]$$

We know that $V \gg V_{cl}$ and $R_S \ll R$. Therefore:

$$I_r = \frac{1}{R} [V_{YY} + V - I_{cl} R_S] \quad (5.38)$$

As the input is a symmetric square wave, $I_f = I_r$. Therefore, from Eqs. (5.35) and (5.38):

$$I_{cl} - \frac{V_{YY}}{R} = \frac{1}{R} [V_{YY} + V - I_{cl} R_S]$$

$$I_{cl} \left(1 + \frac{R_S}{R} \right) = \frac{1}{R} [V_{YY} + V_{YY} + V] = \frac{2V_{YY} + V}{R}$$

As $R_S \ll R$:

$$I_{cl} = \frac{2V_{YY} + V}{R} \quad (5.39)$$

From Eq. (5.22):

$$I_{cl} = I_0 e^{V_{cl}/\eta V_T} \quad \frac{2V_{YY} + V}{R} = I_0 e^{V_{cl}/\eta V_T}$$

Taking logarithms to the natural base:

$$V_{cl} = \eta V_T \ln \left(\frac{2V_{YY} + V}{I_0 R} \right) \quad (5.40)$$

$$\frac{d}{dV} V_{cl} = \eta V_T \frac{I_0 R}{2V_{YY} + V} \times \frac{1}{I_0 R} = \frac{\eta V_T}{2V_{YY} + V}$$

$$dV_{cl} = \eta V_T \frac{dV}{2V_{YY} + V} \quad (5.41)$$

If a Si diode used in the clamping circuit, for which $\eta = 2$, $V_T = 26$ mV, $dV = 1$ V, $V = 10$ V and $V_{YY} = 50$ V:

$$dV_{cl} = 2 \times 26 \text{ mV} \times \frac{1}{2 \times 50 + 10} = 0.472 \text{ mV}$$

On the contrary, dV_{cl} (when $V_{YY} = 0$) = 5.2 mV (calculated earlier).

We see from the above calculations that dV_{cl} with large V_{YY} ($= 50$ V) is approximately one-tenth of dV_{cl} with $V_{YY} = 0$. Thus, the use of a biased diode improves the stability of the clamping level. However, one major constraint in the circuit of Fig. 5.25(a) is that the diode will remain ON continuously if the input signal (V) is small. The minimum peak-to-peak value of the signal V can be determined as follows:

When the input magnitude is V' , D is ON, the voltage across the diode is V_γ so that the current in R is [from Eq. (5.33)]:

$$I_R = \frac{V_{YY} - V_\gamma}{R}$$

When the input drops by V , the current I_S through R_S is, $I_S = -V/R_S$. If $I_R \gg I_S$, then the diode is continuously ON. Therefore, to make sure that diode switches OFF when the input falls to V'' , $I_R \leq I_S$.

$$\frac{V_{YY} - V_\gamma}{R} \leq \frac{-V}{R_S}$$

$$V \geq (V_{YY} - V_\gamma) \frac{R_S}{R} \quad (5.42)$$

Hence, for the proper circuit operation, Eq. (5.42) has to be satisfied in the clamping circuit of Fig. 5.25(a).

5.4 SYNCHRONIZED CLAMPING

In the clamping circuits examined in this chapter, the duration for which clamping is effective is controlled by the signal alone—the signal remains clamped as long as its amplitude remains unaltered. However, in some applications it may become necessary that the time of clamping be determined by the control or gating signal that occurs synchronously with the signal. Two or more signals are said to be synchronized if they arrive at a particular reference point in their cycles at the same time. The simultaneous presence of the gating signal during the period of constant amplitude input enables the two waveforms to be synchronized and the output to be referenced to V_R . One typical application could be in a CRO, where, for the spot to move vertically, the signal applied to the X-deflecting plates of the CRT varies in both directions but returns to a reference level V_R , as shown in Fig. 5.26(a).

Let the signal then be transmitted through a capacitive coupled network like a high-pass network shown in Fig. 5.26(b).

For the duration 0 to T_1 , when the input is a ramp, the output varies exponentially from point A with a time constant τ . At $t = T_1$, both the input and the output fall by V , giving rise to an undershoot. During the interval T_1 to T_2 , as the input remains constant, the output decays exponentially to zero (point B). A similar variation takes place during the period the signal is negative. The resultant output waveform v_o is shown in Fig. 5.26(c).

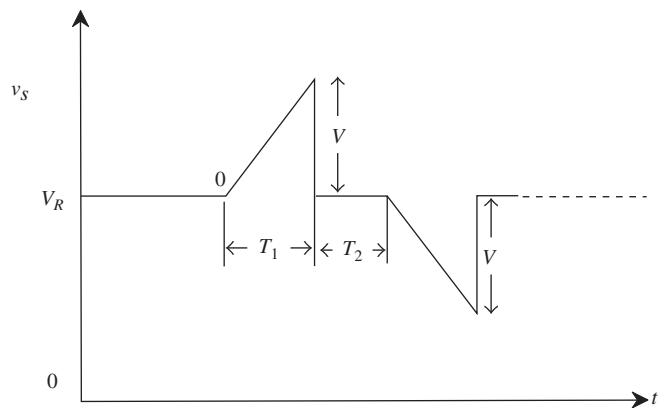


FIGURE 5.26(a) The signal that varies in both directions but is referenced to V_R

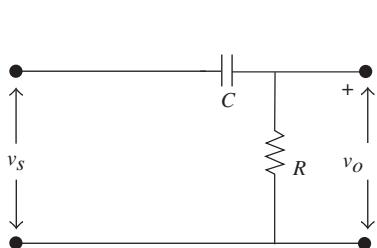
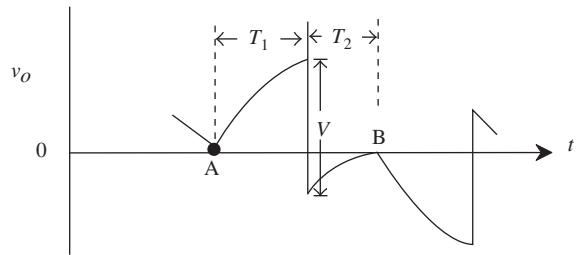

 FIGURE 5.26(b) A high-pass RC circuit


FIGURE 5.26(c) The output of a capacitive coupling network (high-pass circuit)

This output is devoid of a dc component. To reintroduce the dc component, we apply a signal referenced to the zero level [see Fig. 5.27(a)] as input to the circuit, as shown in Fig. 5.27(b). The output waveform of this circuit is shown in Fig. 5.28.

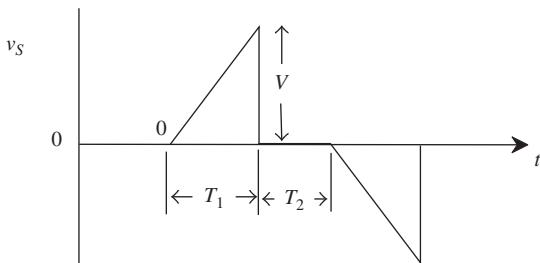


FIGURE 5.27(a) The input signal;

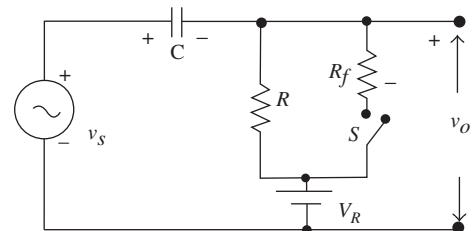
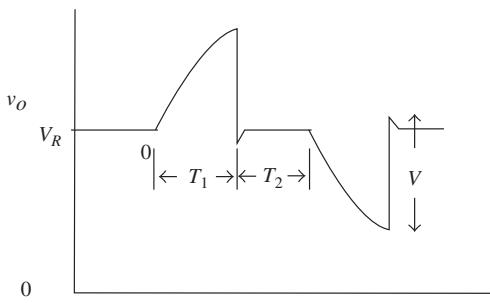

 (b) The switch S operates in sync with the signal to clamp the output to V_R


FIGURE 5.28 The output of the circuit in Fig. 5.27(b)

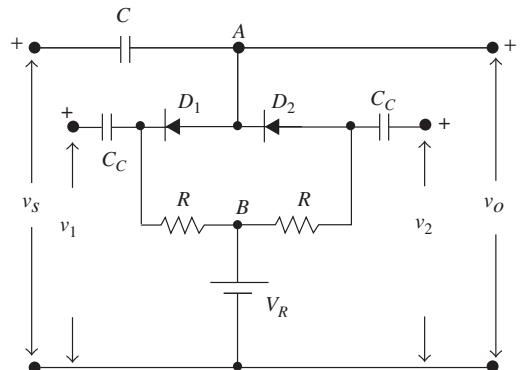


FIGURE 5.29(a) A synchronized clamping circuit

When the switch S closes, during the interval T_2 , $v_o = V_R$. When the switch S opens during the interval T_1 , C charges resulting in the waveform shown in Fig. 5.28. The small spikes can be reduced to negligible values if the switch has a zero resistance in the ON position.

The circuit in Fig. 5.27(b) can be implemented practically using diodes D_1 and D_2 , and two control signals v_1 and v_2 , with a 180° phase shift, as shown in Figs. 5.29(a), 5.30(a) and 5.30(b). If the signal in Fig. 5.30(c) is referenced to the zero level; the output in Fig. 5.30(d) is referenced to V_R .

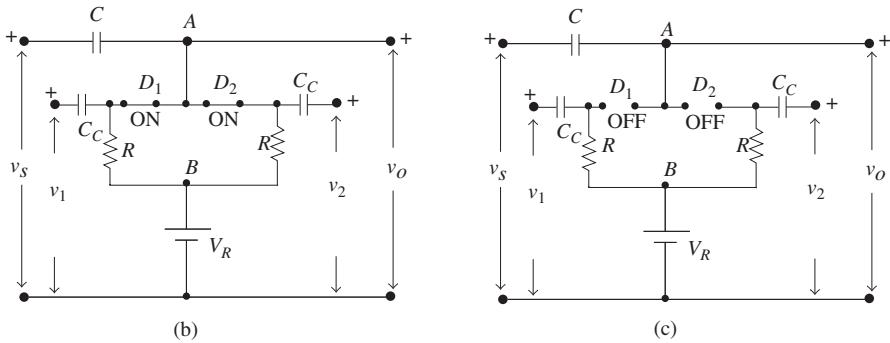


FIGURE 5.29(b) The circuit when D_1 and D_2 are ON; and (c) the circuit when D_1 and D_2 are OFF

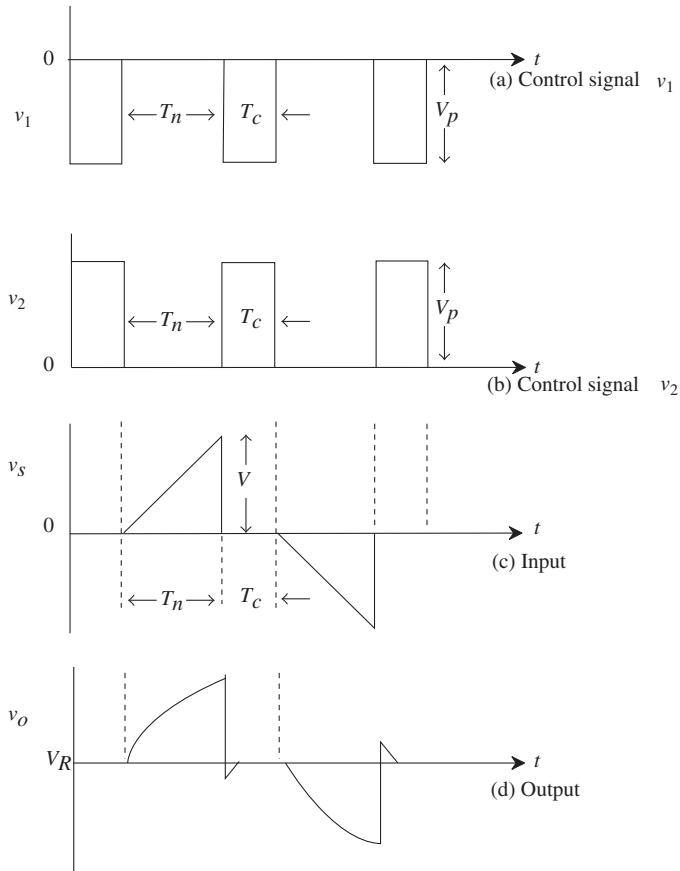


FIGURE 5.30 The waveforms of a synchronized clamping circuit

T_c is the time duration of the control signals and T_n is the time period during which the control signals are zero. The input to the clamping circuit is synchronized with the control signals v_1 and v_2 . Since the input v_s is referenced to the zero level, the purpose of this circuit is to introduce a dc voltage (V_R) so that the output v_o is now referenced to V_R instead of the zero level. From the circuit in Fig. 5.29(a), it is evident, for the given

polarities of the control signals that the diodes D_1 and D_2 conduct during the period T_c , resulting in the circuit of Fig. 5.29(b). As v_1 and v_2 are of equal magnitudes but of the opposite polarity, their net effect is zero at the output. The result is the output V_R .

However, when the control signals are zero, diodes D_1 and D_2 are OFF, resulting in the circuit of Fig. 5.29(c). The input is transmitted to the output terminals with a slight distortion in amplitude, as the capacitor charges exponentially. The output of this circuit is now referenced to V_R , meaning that a dc voltage V_R is introduced by the clamping circuit.

5.5 THE CLAMPING CIRCUIT THEOREM

This theorem enables us to calculate the voltage level to which the output is clamped by considering the areas above and below the reference level, when the values of R_f and R are known.

The clamping circuit theorem states that under steady-state conditions, for any input waveform, the ratio of the area under the output voltage curve in the forward direction to that in the reverse direction is equal to the ratio R_f/R . To prove the clamping circuit theorem, consider a typical steady-state output for the clamping circuit, represented in Fig. 5.31.

In the time interval t_1 to t_2 , D is ON. Hence, during this period, the charge builds up on the capacitor C . If i_f is the diode current, the charge gained by the capacitor during the interval t_1 to t_2 is:

$$q_1 = \int_{t_1}^{t_2} i_f dt \quad (5.43)$$

However, $i_f = V_f/R_f$, where V_f is the diode forward voltage:

$$q_1 = \frac{1}{R_f} \int_{t_1}^{t_2} V_f dt \quad (5.44)$$

During the interval t_2 to t_3 , D is OFF. Hence, the capacitor discharges and the charge lost by C is:

$$q_2 = \int_{t_2}^{t_3} i_r dt \quad (5.45)$$

Put $i_r = V_r/R$, where V_r is the diode reverse voltage:

$$q_2 = \frac{1}{R} \int_{t_2}^{t_3} V_r dt \quad (5.46)$$

At steady state, the charge gained is equal to the charge lost. In other words, $q_1 = q_2$.

Therefore,

$$\frac{1}{R_f} \int_{t_1}^{t_2} V_f dt = \frac{1}{R} \int_{t_2}^{t_3} V_r dt \quad (5.47)$$

However,

$$A_f = \int_{t_1}^{t_2} V_f dt \quad \text{and} \quad A_r = \int_{t_2}^{t_3} V_r dt \quad (5.48)$$

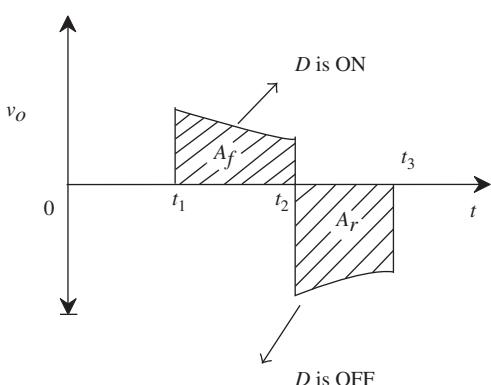
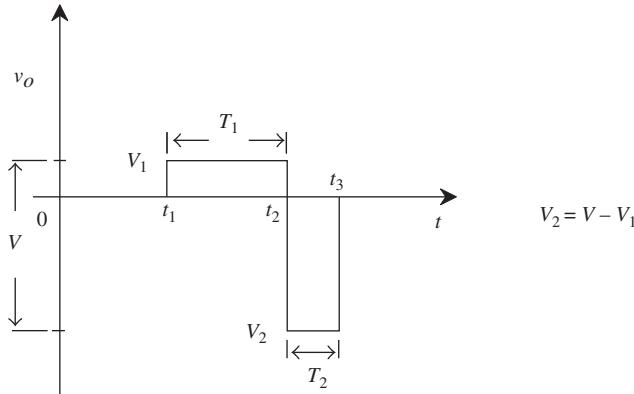


FIGURE 5.31 Typical steady-state output of the clamping circuit

FIGURE 5.32 The output of the clamping circuit when C is large

Here, A_f is the area with D in the ON state and A_r is the area under the output curve with D in the OFF state. From Eqs. (5.47) and (5.48):

$$\frac{A_f}{R_f} = \frac{A_r}{R} \quad \text{or} \quad \frac{A_f}{A_r} = \frac{R_f}{R} \quad (5.49)$$

This relation is known as the clamping circuit theorem.

Consider Fig. 5.32 in which the output of the clamping circuit is assumed to remain almost constant during the periods T_1 and T_2 when the diode D is ON and OFF by choosing large values of C .

If V_1 and T_1 are the voltage and time duration above the reference level and V_2 and T_2 are the voltage and time duration below the reference level under steady-state, then as per this theorem:

$$\frac{A_f}{A_r} = \frac{V_1 T_1}{V_2 T_2} = \frac{V_1 T_1}{(V - V_1) T_2} = \frac{R_f}{R}$$

Assuming that T_1 , T_2 , R_f , R and the amplitude of the signal V are known, it is possible to compute the voltage level V_1 to which the signal is clamped at the output.

S O L V E D P R O B L E M S

Example 5.8: The input shown in Fig. 5.33(a) is applied to the clamping circuit [see Fig. 5.33(b)]. Plot the output waveform. Given that $R_s = R_f = 50 \Omega$, $R = 10 \text{ k}\Omega$, $R_r = \infty$, $C = 1 \mu\text{F}$

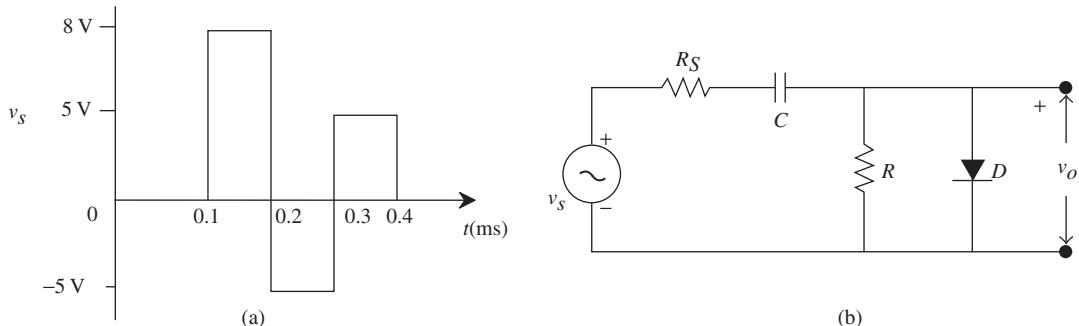


FIGURE 5.33(a) The given Input; and (b) the given clamping circuit

Solution: The equivalent circuit, when the diode conducts, is shown in Fig. 5.34(a). When the diode does not conduct, the equivalent circuit is as shown in Fig. 5.34(b).

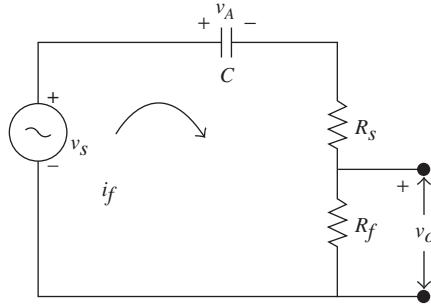


FIGURE 5.34(a) The equivalent circuit when D is ON

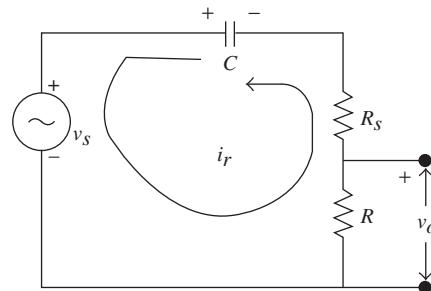


FIGURE 5.34(b) The equivalent circuit when D is OFF

- (i) At $t = 0.1$ ms, v_s abruptly rises to 8 V. As the capacitor cannot allow sudden changes in the voltage it behaves as a short circuit.

$$v_o = \frac{8 \times 50}{100} = 4 \text{ V}$$

- (ii) The input remains constant at 8 V from 0.1 to 0.2 ms. So v_o decays exponentially with time constant $(R_s + R_f) C$.
At $t = 0.2$ ms

$$v_o = 4 e^{-0.1 \times 10^{-3} / (50+50)(1 \times 10^{-6})} = 4 e^{-1} = 1.47152 \text{ V}$$

$$\text{Voltage across the capacitor} = v_A = 8 - 2 \times 1.47152 = 5.05696 \text{ V}$$

- (iii) At $t = 0.2$ ms, v_s abruptly falls to -5 V. The resultant circuit is as shown in Fig. 5.34(c).

$$v_o = -5 - 5.05696 = -10.05696 \text{ V}$$

- (iv) From $t = 0.2$ ms to 0.3 ms, v_s remains at -5 V. Hence, the output voltage should decay exponentially with a time constant $(R + R_s) C$.

At 0.3 ms,

$$v_o = -10.05696 e^{-0.1 \times 10^{-3} / (10000+50)(1 \times 10^{-6})} = -9.958 \text{ V}$$

$$\text{Voltage across } C = v_A = -5 + 9.958 = 4.958 \text{ V}$$

- (v) At $t = 0.3$ ms and $v_s = 5$ V. The equivalent circuit to be considered is shown in Fig. 5.34(d).

$$v_o = \frac{5 - 4.958}{2} = 0.0213 \text{ V}$$

As v_s remains constant, v_o decays exponentially from $t = 0.3$ ms to 0.4 ms.

At $t = 0.4$ ms $v_o = 0.0213 e^{-1} \approx 0$ V. The output voltage now varies as shown in Fig. 5.34(e).

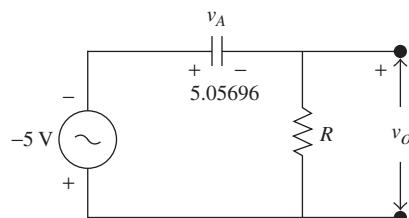


FIGURE 5.34(c) The circuit to calculate the output

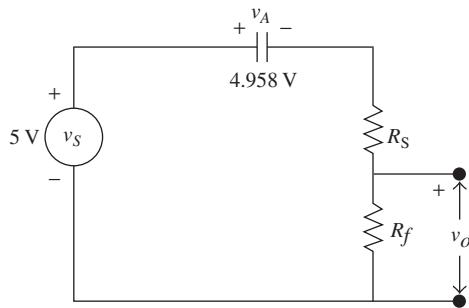


FIGURE 5.34(d) The circuit to calculate the output

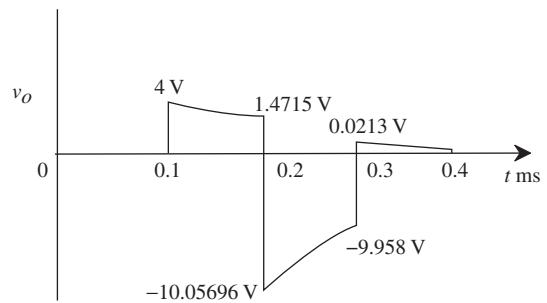


FIGURE 5.34(e) The steady-state output waveform

Example 5.9: A clamping circuit and the input applied to it are shown in Fig. 5.35(a) and (b). Calculate and plot to scale the steady-state output. Given that: $R_s = R_f = 100 \Omega$, $T_1 = T_2 = 500 \mu\text{s}$.

Solution: To calculate the steady-state voltages, first calculate V_1 , V'_1 , V_2 and V'_2 by making $V_R = 0$. During the interval 0 to T_1 , the charging time constant of the capacitor C is:

$$\tau_f = (R_s + R_f) C = (100 + 100)0.5 \times 10^{-6} = 100 \mu\text{s}$$

The capacitor discharges during the interval T_1 to T_2 and the time constant, τ_r , is:

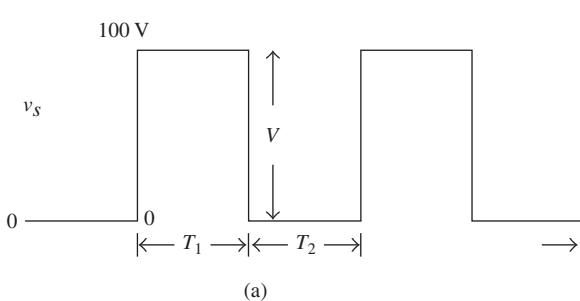
$$\tau_r = (R_s + R)C = (100 + 200000)0.5 \times 10^{-6} = 100050 \mu\text{s} = 100.050 \text{ ms}$$

$$V'_1 = V_1 e^{-T_1/\tau_f} = V_1 e^{-500/100} = 0.00674 V_1$$

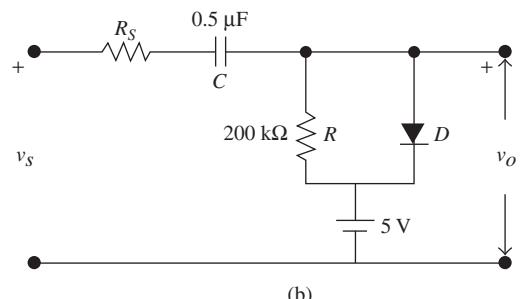
$$V'_1 = 0.00674 V_1 \quad (1)$$

$$V'_2 = V_2 e^{-T_2/\tau_r} = V_2 e^{-500/100050} = 0.995 V_2$$

$$V'_2 = 0.995 V_2 \quad (2)$$



(a)



(b)

FIGURE 5.35(a) The given input; and (b) clamping circuit

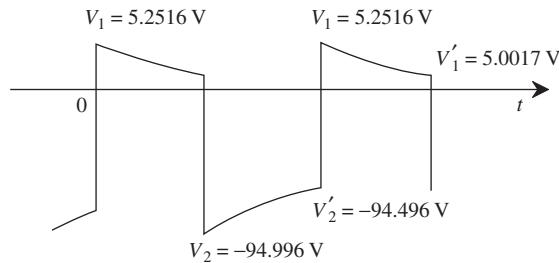


FIGURE 5.35(c) The steady-state output

$$V = \frac{R_f + R_s}{R_f} V_1 - \frac{R + R_s}{R} V_2' = \frac{100 + 100}{100} \times V_1 - \frac{200 \text{ k}\Omega + 100}{200 \text{ k}\Omega} \times V_2'$$

$$100 = 2V_1 - V_2' \quad (3)$$

Also,

$$V = \frac{R_f + R_s}{R_f} V_1' - \frac{R + R_s}{R} V_2$$

$$100 = 2V_1' - V_2 \quad (4)$$

Solving Eqs. (1), (2), (3) and (4):

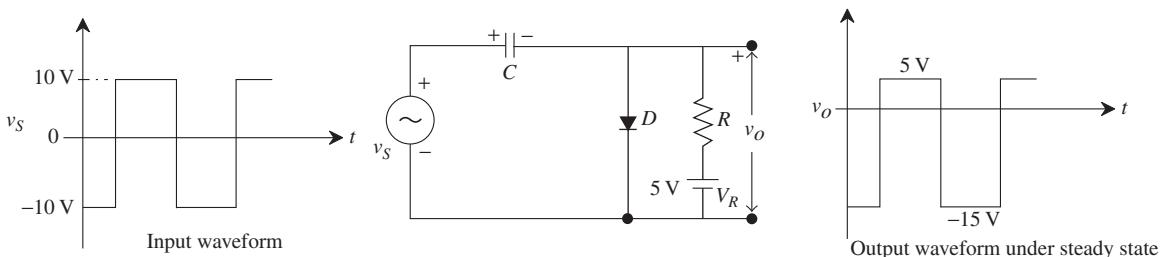
$$V_1 = 0.2516 \text{ V}, \quad V_1' = 0.0017 \text{ V} \quad V_2 = -99.996 \text{ V} \quad V_2' = -99.496 \text{ V}$$

To get the steady-state output, we add V_R to the values of V_1 , V_1' , V_2 and V_2' for the given circuit in Fig. 5.35(a). Therefore,

$$V_1 = 5.2516 \text{ V} \quad V_1' = 5.0017 \text{ V} \quad V_2 = -94.996 \text{ V} \quad V_2' = -94.496 \text{ V}.$$

The steady-state output is as shown in Fig. 5.35(c).

Example 5.10: Draw the output waveform under the steady state for the given biased clamping circuit shown in Fig. 5.36, when the input is 10 V square wave. Assume that C is very large so that the change in the output voltages during the periods when D is ON and OFF is negligible.

FIGURE 5.36 The given biased negative clamper with $V_R = 5 \text{ V}$ and the corresponding input and output waveforms

Solution: The diode D conducts when the input changes to +10 V. Then capacitor charges to +5 V after few cycles.

Under steady-state conditions $v_o = v_s - v_A = v_s - 5$

When $v_s = 10$ V, $v_o = 10 - 5 = 5$ V

When $v_s = -10$ V, $v_o = -10 - 5 = -15$ V

The positive peak is clamped to $V_R (= 5$ V), in the output.

SUMMARY

- The dc component, that is blocked when a signal passes through a capacitive coupling network can again be restored using a clamping circuit.
- A clamping circuit, generally, is called a dc restorer and dc re-inserter, meaning that it reintroduces exactly the same amount of dc voltage lost. However, it is a dc inserter, which means that it introduces any desired dc voltage.
- A simple clamping circuit consists of a signal source, a capacitor of appropriate value and a diode connected across the output terminals.
- The positive or negative extremity of an input signal can be clamped to a zero level or to an arbitrarily chosen reference level by using a clamping circuit.
- The dc level associated with the input signal has absolutely no say in determining the steady-state response of the clamping circuit.
- The clamping circuit theorem states that for any input waveform under steady-state conditions $A_f/A_r = R_f/R$.
- A synchronized clamping circuit is one in which the time of clamping is not determined by the signal but by a control signal which is in synchronization with the signal.

MULTIPLE CHOICE QUESTIONS

(1) Strictly speaking, a clamping circuit should be called:

- dc restorer
- dc re-inserter
- dc eliminator
- dc inserter

(2) A positive clamping circuit is one that clamps:

- The positive extremity of the signal to the zero level
- The positive extremity of the signal to a positive dc voltage
- The negative extremity of the signal to the zero level
- None of the above

(3) A negative clamping circuit is one that clamps:

- The positive extremity of the signal to the zero level
- The positive extremity of the signal to a positive dc voltage
- The negative extremity of the signal to the zero level
- None of the above

(4) The clamping theorem states that:

- $\frac{A_f}{A_r} = \frac{R_f}{R}$
- $\frac{A_f}{A_r} = \frac{R}{R_f}$
- $\frac{A_f}{A_r} = \frac{R_r}{R_f}$
- $\frac{A_f}{A_r} = \frac{R_r}{R}$

(5) In a clamping circuit, the tilts in the forward and reverse directions are related by:

- $\Delta f = \frac{R_f}{R_f + R_S} \times \frac{R + R_S}{R} \times \Delta r$
- $\Delta f = \frac{R_r}{R + R_S} \times \frac{R_f + R_S}{R} \times \Delta r$
- $\Delta f = \frac{R_f}{R} \times \Delta r$
- None of the above

SHORT ANSWER QUESTIONS

- (1) What is a clamping circuit?
- (2) Why do we call a clamping circuit a dc inserter?
- (3) What do you understand by positive clamping and negative clamping?
- (4) State the clamping circuit theorem.

- (5) What is synchronized clamping?

(6) If $\Delta f = \frac{R_f}{R_f + R_S} \times \frac{R + R_S}{R} \times \Delta r$, show that
 $\Delta f = \Delta r$ when R_S is small

- (7) What do you understand by biased clamping?

LONG ANSWER QUESTIONS

- (1) A sinusoidal signal is applied as an input to a negative clamping circuit and suddenly the amplitude of the input signal falls. Explain how clamping is restored in the circuit?
- (2) State and prove the clamping circuit theorem.
- (3) Consider the steady-state output waveform of a clamping circuit for a square-wave input and

derive the relation between the tilt in the forward direction to that in the reverse direction.

- (4) Explain the principle of synchronized clamping.
- (5) Discuss the influence of the diode characteristics on the clamping voltage.

UNSOLVED PROBLEMS

- (1) Design a diode clamer shown in Fig. 5p.1 to restore the positive peaks of the input signal to a voltage level to 5 V. Assume the diode cut-in voltage is 0.5 V, $f = 1$ kHz, $R_f = 1$ k Ω , $R_r = 200$ k Ω and $RC = 20$ T.

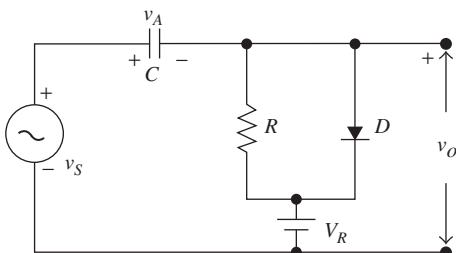


FIGURE 5p.1 The given clamping circuit with reference voltage V_R

- (2) For the excitation as shown in Fig. 5p.2(a) and the clamping circuit [see Fig. 5p.2(b)], calculate and plot to scale, the steady-state output.

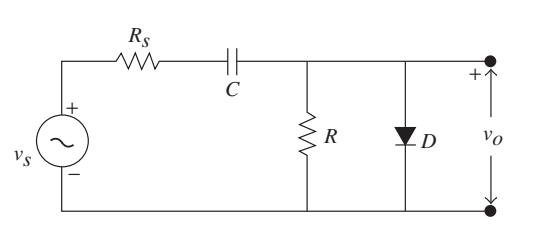
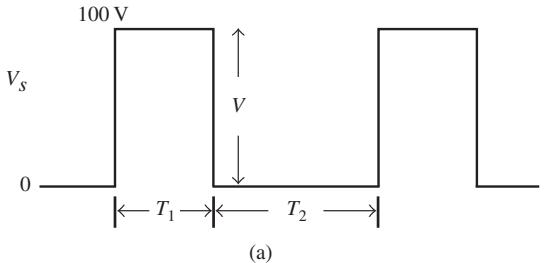


FIGURE 5p.2 The given Input, and (b) the clamping circuit

- (3) Sketch the steady-state output voltage for the clamer circuit shown in Fig. 5p.3 and locate the output dc level and the zero level. The diode used

has $R_f = 100 \Omega$, $R_r = 500 \text{ k}\Omega$, $V_\gamma = 0$. C is arbitrarily large and $R = 20 \text{ k}\Omega$. The input is a $\pm 20\text{V}$ square wave with 50 per cent duty cycle.

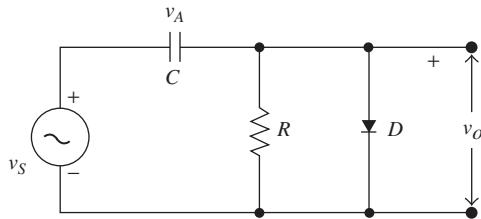


FIGURE 5p.3 The given clamping circuit for problem 2

- (4) For the circuit shown in Fig. 5p.4(a), $R_s = R_f = 50 \Omega$, $R = 10 \text{ k}\Omega$, $R_r = \infty$, $C = 2.0 \mu\text{F}$, the input varies as shown in Fig. 5p.4(b). Plot the output waveform.

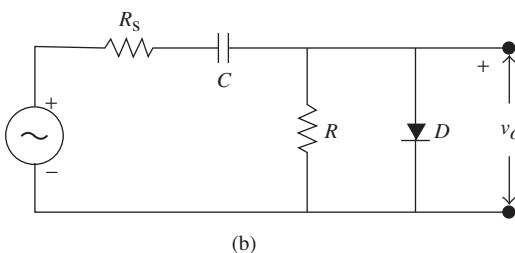
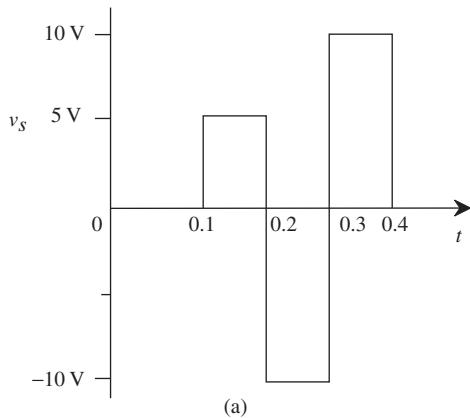


FIGURE 5p.4 The given input; and (b) the given clamping circuit

- (5) The input as shown in Fig. 5p.5(a) is applied to the clamping circuit shown in Fig. 5p.5(b) with $R_s = R_f = 100 \Omega$, $R = 10 \text{ k}\Omega$, $R_r = \infty$, $C = 1.0 \mu\text{F}$; $V_\gamma = 0$. Draw the output waveform and label all the voltages

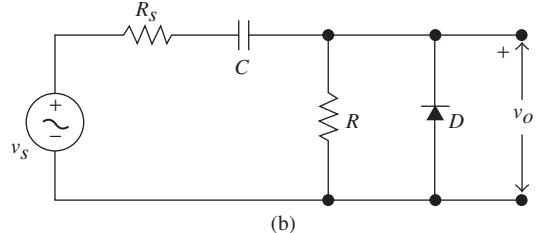
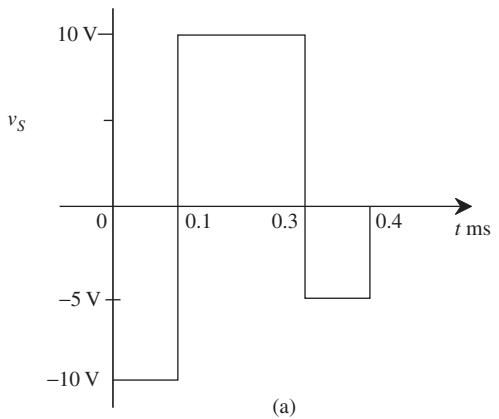


FIGURE 5p.5 The given input; and (b) the given clamping circuit

- (6) A clamping circuit and input applied to it are shown in Fig. 5p.6. Assume that C is quite large. Find at which voltage level the positive peak is clamped in the output if $T_1 = 1 \text{ ms}$, $T_2 = 1 \mu\text{s}$, $R_f = 100 \Omega$ and $R = 100 \text{ k}\Omega$.

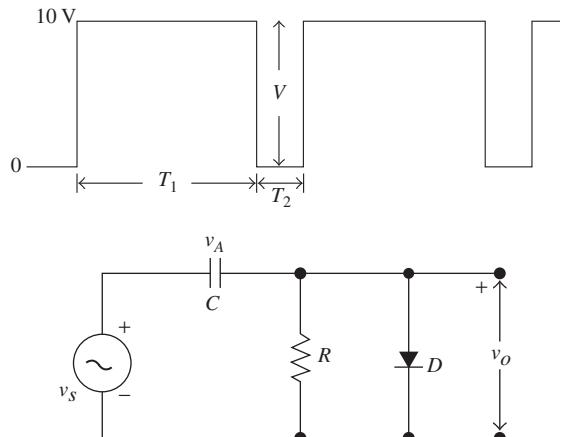


FIGURE 5p.6 The given input and clamping circuit for problem 3

(Hint: Use the clamping Theorem.)

- (7) Calculate and draw the steady-state output waveform of the circuit in Fig. 5p.7. Assume $R_f = 50 \Omega$, $R_r = 500 \text{ k}\Omega$ and $T_1 = T_2 = 1 \text{ ms}$.

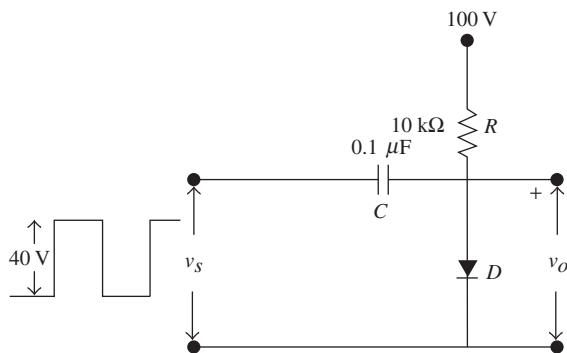


FIGURE 5p.7 The given clamping circuit with large V_{YY}

- (8) Design a biased clamping circuit to derive the output voltage as shown in Fig. 5p.8(b), given the input as

shown in Fig. 5p.8: (a) $f = 1000 \text{ Hz}$, $R_f = 100 \Omega$, $R_r = 1 \text{ M}\Omega$ and $RC/T = 10$. Assume that D is ideal.

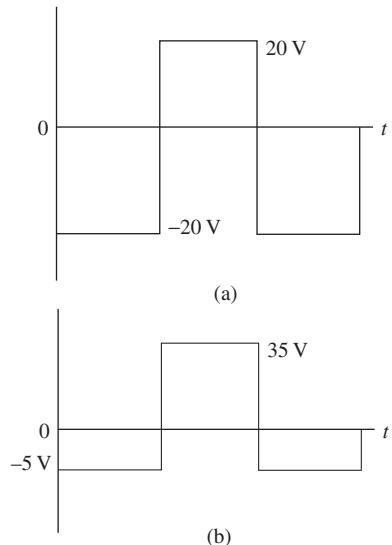


FIGURE 5p.8 (a) The given input to the clamping circuit; and (b) the required output

CHAPTER 6

Switching Characteristics of Devices

LEARNING OBJECTIVES

After studying this chapter, you will be able to:

- Use diodes and transistors as switches
 - Describe the effect of inter-electrode capacitances on switching times
 - Describe the switching times of devices and derive the necessary relations
 - Describe the temperature dependence of the transistor on various parameters
 - Understand the use of transistor switch as a latch
 - Realize the use of transistor switches with inductive and capacitive loads
-

6.1 INTRODUCTION

Active devices such as semiconductor and Zener diodes, transistors and FETs can be used as static switches. To use these switches for high-speed applications, it is necessary to know the influence of inter-electrode capacitors on the switching speed of these devices. For transistors, the switching speed can be improved with the use of speed-up capacitors and expressions for the switching times of a transistor are derived to calculate the turn-on and turn-off times of a transistor. Further, the choice of the supply voltage depends on the breakdown voltages of the transistor and the saturation parameters of the transistor are temperature dependent. The influence of temperature on these parameters is discussed in this chapter. Finally, a transistor switch with inductive or capacitive loads is considered and also the application of a transistor switch as a latch. In most applications, the ON transistor is driven into saturation. This in turn increases the storage time that results in a longer turn-off time, thereby reducing the switching speed. To overcome this problem, a non-saturating switch is discussed.

6.2 THE DIODE AS A SWITCH

Semiconductor and Zener diodes can be used in switching applications. To understand the working of a two-terminal device as a switch, we need to consider its V–I characteristic and switching times.

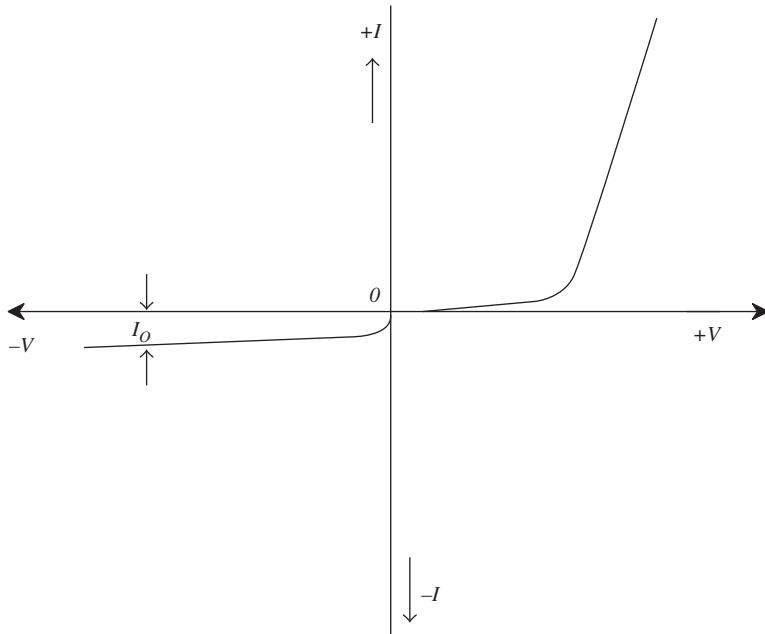
6.2.1 Diode Characteristics

A *p*–*n* junction diode can be used as a switch. When the diode is forward-biased, the switch is said to be in the ON state and when it is reverse-biased, the switch is in the OFF state. Figure 6.1 shows the V–I characteristic of a *p*–*n* junction diode.

The diode current is given by the relation:

$$I = I_0 (e^{V/\eta V_T} - 1) \quad (6.1)$$

where, V is the bias voltage, $\eta = 1$ or 2 depending on whether it is a Ge or Si diode and V_T is the Volt-equivalent for temperature.

FIGURE 6.1 The V-I characteristic of a $p-n$ junction diode

$$V_T = \frac{T}{11600} = 26 \text{ mV}$$

where, T is the room temperature. If $e^{V/\eta V_T} \gg 1$, Eq. (6.1) reduces to:

$$I = I_o e^{V/\eta V_T} \quad (6.2)$$

When the diode is forward-biased, V is positive and I is a positive current that varies exponentially with the variation of V . When the diode is reverse-biased, V is a negative voltage and the current I now flows in the opposite direction ($I = -I_o$), I_o almost remains constant and it is called the reverse saturation current. The reverse saturation current gets doubled for every 10°C rise in temperature. The leakage currents in Ge are significantly larger when compared to that in Si devices. Ge diodes develop large reverse currents at elevated temperatures whereas the increase in the reverse current in Si diodes is negligible.

When used as a switch, a diode can be either ON or OFF, depending on the polarity of the signal applied to change the state. Though the diode is expected to switch between these two states almost instantaneously, in case of a high-frequency switching signal, it may not be possible to drive the switch from one state to the other abruptly because of junction capacitances and there arises a finite time delay before the device switches its state.

6.2.2 Transition Capacitance

When a $p-n$ junction diode is reverse-biased, electrons from the p -side will move to the n -side, aided by the external field and the holes move away from the junction. As a result, negative charge is developed on the p -side and positive charge on the n -side. The width of the space-charge region increases with reverse-bias. This can be considered as the parallel plate condenser whose value changes with the width of the depletion

region. This capacitance is called as transition capacitance or depletion-region capacitance and its value is given by:

$$C_T = \frac{\varepsilon A}{W} \quad (6.3)$$

where, W = Spacing between the plates of the capacitor (in m),

A = Area (in m^2), and

ε = permittivity of the material.

For some simplified geometries:

$$C_T = \frac{\lambda}{V^n} \quad (6.4)$$

where, λ is a constant,

V is the external voltage applied,

$n = 1/2$ for an abrupt junction, and

$n = 1/3$ for a gradual junction.

6.2.3 Diffusion Capacitance

In a forward-biased junction diode there is a junction capacitance—called the diffusion capacitance—due to the injected charges being proportional to the applied external voltage V . This is given by the relation:

$$C_D = \frac{I\tau}{\eta V_T} \quad (6.5)$$

where, $\eta = 1$ for Ge and $\eta = 2$ for Si,

τ = mean life time for holes,

V_T = Volt-equivalent for temperature, and

I = hole current.

The diffusion capacitance C_D is usually significantly larger than the transition capacitance C_T . These junction capacitances influence the switching times of a diode. When the diode switches state, the response is accompanied by a transient.

6.2.4 Junction Diode Switching Times

Forward Recovery Time. The forward recovery time, t_{fr} of a diode is defined as the time difference between the 10 per cent value of the diode voltage and the time when this voltage reaches and remains within 10 per cent of its final value, i.e., 110 per cent or 90 per cent of the steady-state value. The forward recovery time is typically of the order of a few tens of nanoseconds.

Let the diode be in the OFF state for some time. When it is switched into the ON state, there occurs a transient response before the diode recovers to the steady state. If a large current step, equal to or greater than the rated forward current of the diode, is applied, then the diode voltage will have an overshoot and the response will reach the steady-state value after a finite time interval. At large currents, the diode is represented as a combination of a resistor and an inductor. For a current step of smaller value, the diode is represented as a combination of a resistance and a capacitance. The resultant responses when the current is either large or small are shown in Fig. 6.2. Note that here we have assumed the rise time of the current pulse to be negligible.

Reverse Recovery Time. Initially, if the diode is in the OFF state due to reverse-bias voltage, then the resultant current is a reverse saturation current. When the diode is ON with a forward voltage for some time and turned OFF by reverse-biassing, then the current cannot reach the initial reverse saturation current instantaneously. The reverse recovery time of the diode is defined as the time taken for the diode current to reach its initial reverse saturation current, when the diode is turned OFF from the ON state. If the diode is ON for some time, then there is a large current due to injected hole or electron density, as shown in Fig. 6.3(a).

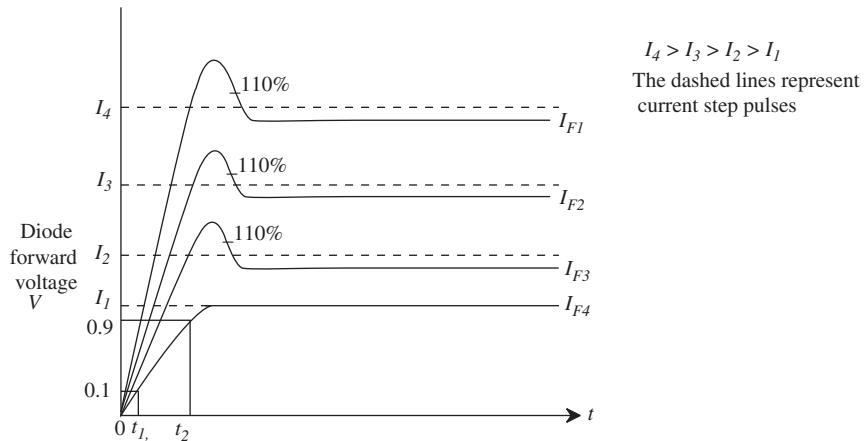
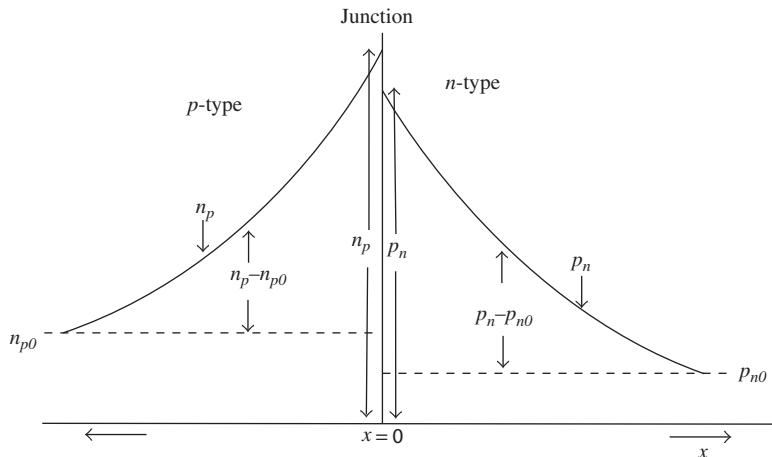


FIGURE 6.2 Diode response for currents of different amplitudes



p_{no} = density of holes on the n -side at equilibrium

n_{p0} = density of electrons on the P -side at equilibrium

n_p = density of electrons on the P -side when forward-biased

p_n = density of holes on the n -side when forward-biased

$p_n - p_{n0}$ = injected or excess hole density on the n -side

$n_p - n_{p0}$ = injected or excess electron density on the P -side

FIGURE 6.3(a) The minority carrier density distribution as a function of x , the distance from the junction when the diode is ON

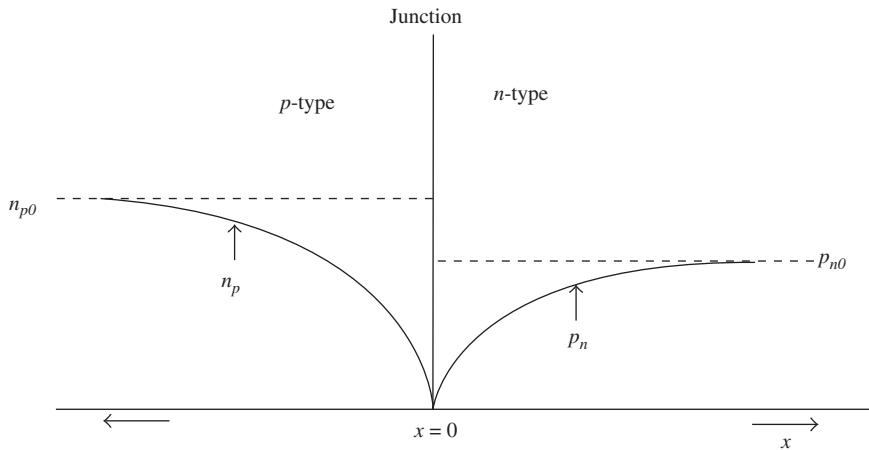


FIGURE 6.3(b) Minority carrier density distribution as a function of x , the distance from the junction when the diode is OFF

When the diode is ON, the number of minority carriers is large [see Fig. 6.3(a)]. When the polarity of the external voltage is suddenly reversed, the diode forward current is expected to reduce to a negligible reverse current. However, this does not happen as it takes a finite time delay for the minority carrier density distribution to take the form shown in Fig. 6.3(b). During this period, the injected minority carrier density will drop to zero and the minority carrier density reaches the equilibrium value.

Let us try to understand the situation when a diode, which is ON for sometime, is abruptly reverse-biased, as shown in Fig. 6.4. The voltage shown in Fig. 6.5(b) is applied to the diode circuit shown in Fig. 6.4.

- (i) As long as the voltage $v_i = V_F$ (till t_1), the diode is ON. The forward resistance of the diode is negligible when compared to R_L . Thus,

$$I_F = \frac{V_F}{R_L}$$

- (ii) At $t = t_1$, the polarity of v_i is abruptly reversed:

$$v_i = -V_R \quad \text{and} \quad -I_R = \frac{-V_R}{R_L}, \text{ until } t = t_2$$

This is the time at which the minority carrier density p_n at $x = 0$ has reached the equilibrium value p_{n0} .

If the diode resistance now is R_d , the diode voltage falls slightly by an amount $(I_F + I_R) R_d$ but, the voltage still remains positive. At $t = t_2$ the charge carriers have been cleaned up, the polarity of the diode voltage reverses, and the diode current starts to decrease.

The time duration t_1 to t_2 , during which period the stored minority charge becomes zero, is called the storage time t_s . The time interval from t_2 to the instant the diode has recovered ($V = -V_R$) is called the transition time, t_t . The sum of the storage time, t_s and the transition time, t_t is called the reverse recovery time of the diode, t_{rr} .

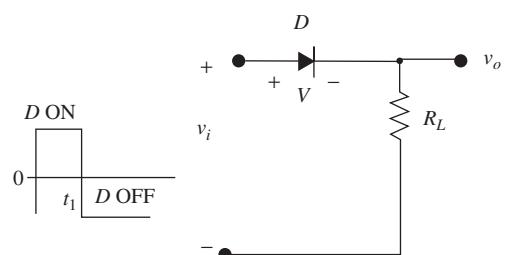


FIGURE 6.4 Driving an ON diode into the OFF state

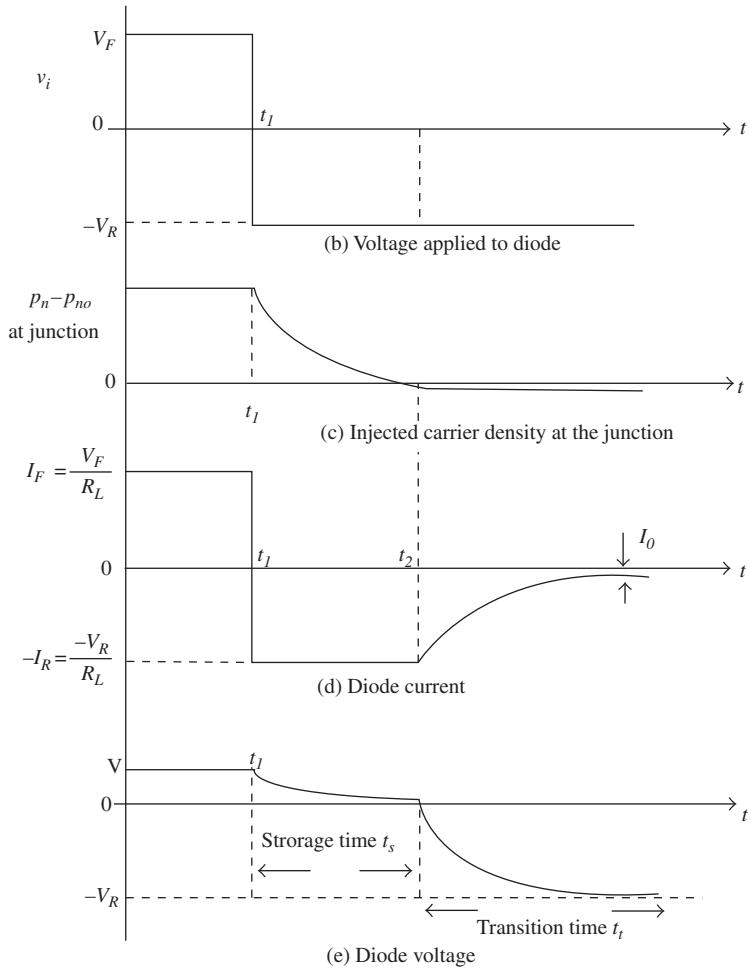


FIGURE 6.5 The switching times of a diode

$$t_{rr} = t_s + t_t \quad (6.6)$$

t_s is given by the relation:

$$t_s = \tau \ln \left(1 + \frac{I_F}{I_R} \right) \quad \text{and} \quad t_t = 3R_L C_T \quad (6.7)$$

6.2.5 Piecewise Linear Diode Model

The diode characteristics in Fig. 6.1 is a non-linear characteristic. In the simplified analysis of a diode circuit, it is advisable that the diode be represented by its electrical equivalent. Hence, the non-linear characteristic of a diode is piecewise linearized so that the diode can be represented by an electrical equivalent. The practical V-I characteristic and the piecewise linear V-I characteristic of a $p-n$ diode are shown in Figs. 6.6(a) and (b), respectively.

Figure 6.6(b) gives the piecewise linear V-I characteristic of the diode. When $V \geq V_\gamma$, the diode is ON and when $V < V_\gamma$, the diode is OFF. Figures 6.6(c) and (d) show the forward-biased and reverse-biased diode equivalent circuits respectively for large signal conditions.

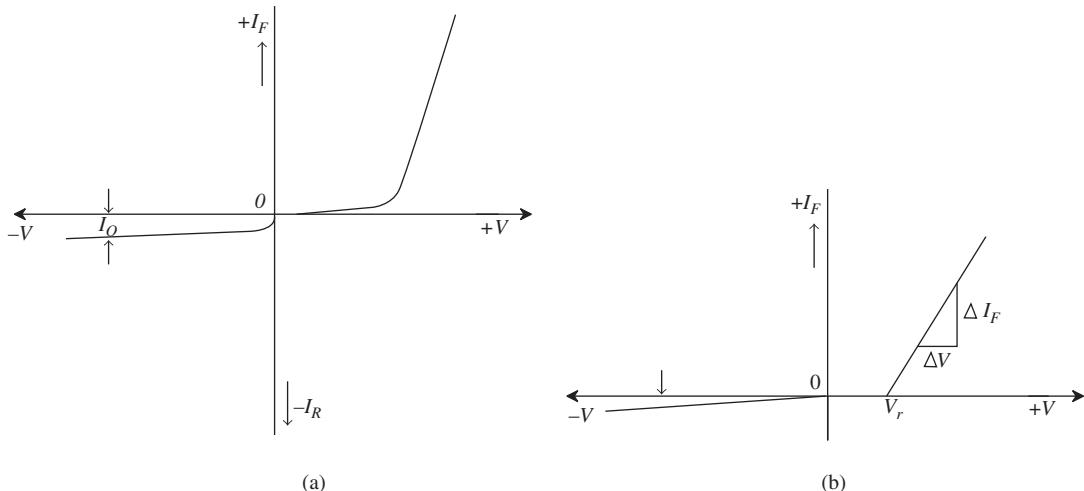


FIGURE 6.6 Diode characteristics (a) V-I characteristic of a practical diode; and (b) piecewise linear characteristic of a diode

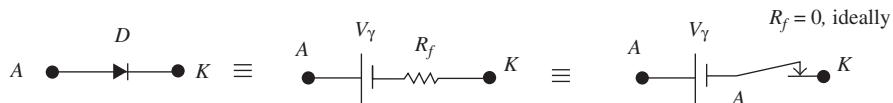


FIGURE 6.6(c) The diode when forward-biased

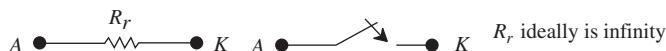


FIGURE 6.6(d) The diode when reverse-biased

6.2.6 Breakdown Diodes

Avalanche or Zener diodes are normally operated when reverse-biased. At a voltage called the breakdown voltage, the current abruptly rises to a large value but the voltage across the two terminals of the device remains almost constant. So, these devices are used as voltage reference or constant voltage devices. These breakdown diodes are used as voltage regulators. The V-I characteristic of a typical avalanche or Zener diode is shown in Fig. 6.7.

The maximum power dissipation in the Zener, $P_{D(\max)} = V_z I_{z(\max)}$.

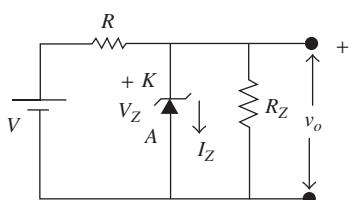


FIGURE 6.7(a) A reverse-biased Zener diode

Avalanche multiplication takes place when a sufficient reverse-bias voltage is applied to a diode and the charge carrier acquires sufficient kinetic energy due to the applied potential. This carrier, in turn, may collide with a crystal ion and, in the process, may transfer sufficient energy to break the covalent bond. Now a new electron-hole pair is generated which in turn may acquire sufficient energy, collide with another crystal ion and create a new electron-hole pair. This cumulative process of multiplication of electron-hole pairs is called avalanche multiplication, resulting in a large current in a reverse-biased diode.

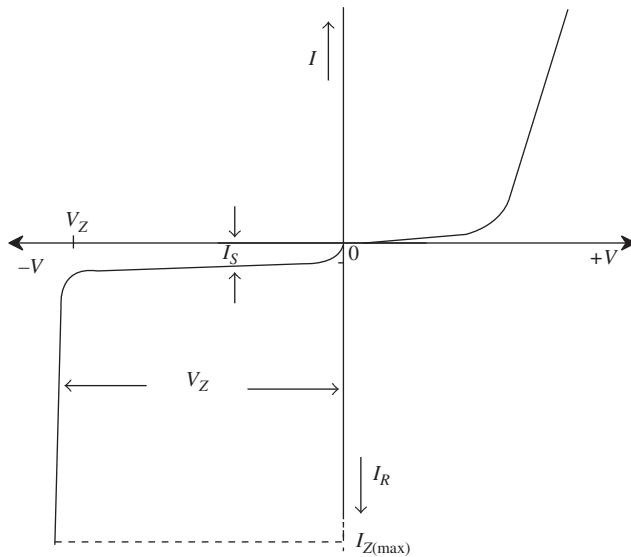


FIGURE 6.7(b) The V-I characteristic of a Zener diode

On the other hand, Zener breakdown occurs due to the physical rupturing of covalent bonds due to a strong electric field and a large current flows in a reverse-biased Zener diode. The breakdown voltage can be controlled by adjusting the doping levels. Zener breakdown voltages are usually less than 6 V; and if the breakdown voltage is more than 6 V, the mechanism involved is an avalanche breakdown.

The breakdown voltage may also vary with the temperature. Normally, data sheets specify the temperature co-efficient as ± 0.1 per cent/ $^{\circ}\text{C}$. The temperature co-efficient is taken as positive for avalanche breakdown and negative for Zener breakdown.

As temperature has a profound effect on V_Z , the change in breakdown voltage due to an increase in temperature can be calculated if the temperature co-efficient is known, as:

$$\Delta V_Z = V_Z \alpha_Z (T_2 - 25^{\circ}\text{C}) \quad (6.8)$$

where, α_Z is the temperature coefficient, which is negative for Zener diode and is positive for an avalanche diode. V_Z at T_2 is given by:

For a Zener diode:

$$V_{Z(T_2)} = V_Z - \Delta V_Z \quad (6.9)$$

For an avalanche diode:

$$V_{Z(T_2)} = V_Z + \Delta V_Z \quad (6.10)$$

Let us consider Example 6.1.

EXAMPLE

Example 6.1: A Zener has a breakdown potential $V_Z = 3.8$ V. If $\alpha_Z = -0.1$ per cent/ $^{\circ}\text{C}$ and the temperature changes from 25°C to 100°C , calculate the Zener voltage at 100°C .

Solution:

Using Eq. (6.8):

$$\Delta V_Z = 3.8 \times \frac{-0.1}{100} \times (100 - 25) = -3.8 \times 0.1 \times 0.75 = -0.285 \text{ V}$$

Using Eq. (6.9):

$$V_{Z(100^\circ\text{C})} = V_Z - 0.285$$

$$V_{Z(100^\circ\text{C})} = 3.8 - 0.285 = 3.515 \text{ V}$$

EXAMPLE

Example 6.2: An avalanche diode has a breakdown potential $V_Z = 12 \text{ V}$. If $\alpha_Z = 0.1 \text{ per cent}/^\circ\text{C}$ and the temperature changes from 25°C to 100°C , calculate the breakdown voltage at 100°C .

Solution:

Given, $V_Z = 12 \text{ V}$, $\alpha_Z = 0.1 \text{ per cent}/^\circ\text{C}$ and the temperature changes from 25°C to 100°C .

Using Eq. (6.8):

$$\Delta V_Z = 12 \times \frac{0.1}{100} \times (100 - 25) = 0.9 \text{ V}$$

Using Eq. (6.10):

$$V_{Z(100^\circ\text{C})} = 12 + 0.9 = 12.9 \text{ V}$$

6.3 THE TRANSISTOR AS A SWITCH

In many applications, the transistor is used as a switch. Consider the output characteristics of a transistor in the CE configuration as shown in Fig. 6.8. Condition *A* corresponds to the switch in the ON state and in saturation. Condition *B* corresponds to the switch in the OFF state.

6.3.1 The Transistor as an Open Switch

Consider the transistor switch as shown in Fig. 6.9.

As long as the driving signal amplitude is zero, the base current is zero; and hence, the collector current is ideally zero. Therefore, the drop across R_C is also zero and the voltage at the collector, $V_{CE} = V_{CC}$. The resistance between the collector and the emitter terminals is the OFF resistance of this static switch. Ideally:

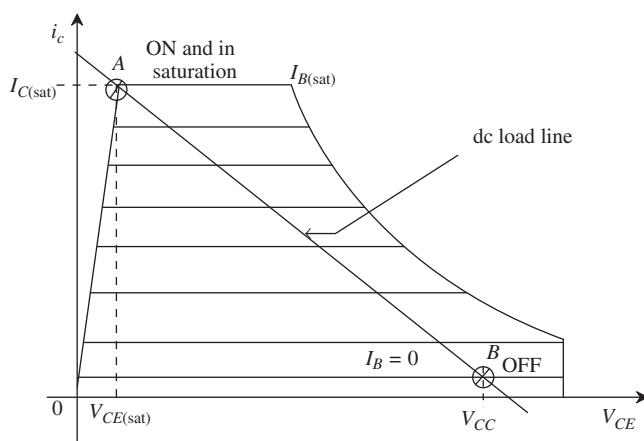
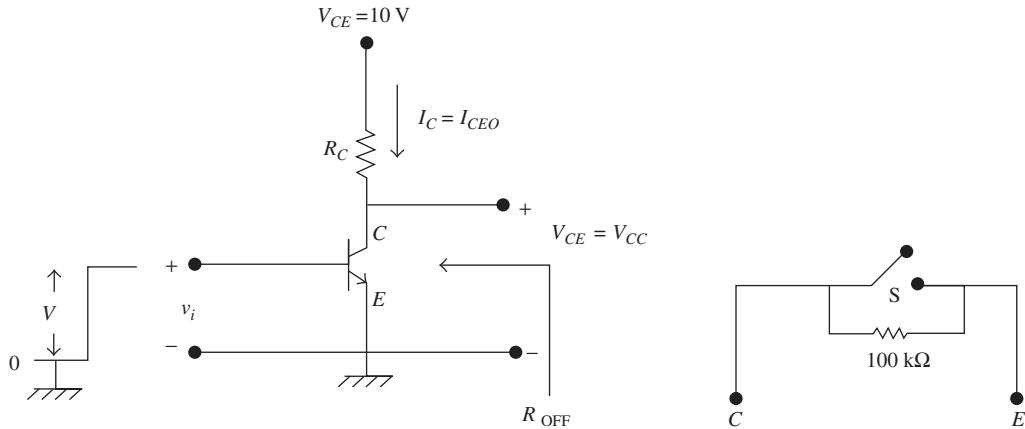


FIGURE 6.8 The output characteristics in CE configuration: the transistor is driven between extreme limits of saturation and cut off

FIGURE 6.9 A transistor as an open switch when $v_i = 0$ FIGURE 6.10 The resistance between the two terminals of the OFF switch is $100 \text{ k}\Omega$

$$R_{OFF} = \frac{V_{CC}}{I_C} = \frac{V_{CC}}{0} = \infty$$

However, the collector current is not zero as assumed. There is a leakage current I_{CEO} . If $I_{CEO} = 0.1 \text{ mA}$ then,

$$R_{OFF} = \frac{V_{CC}}{I_{CEO}} = \frac{10 \text{ V}}{0.1 \text{ mA}} = 100 \text{ k}\Omega$$

This means, when the switch is OFF, it has a resistance of $100 \text{ k}\Omega$ between the terminals as shown in Fig. 6.10. It may not be an acceptable condition. To reduce the leakage current, the base-emitter diode is reverse-biased. Then the leakage current reduces to $I_{CBO} = I_{CO}$, (see Fig. 6.11). Let $I_{CBO} = 1 \mu\text{A}$.

$$\text{If, } v_i = 0, R_{OFF} = \frac{V_{CC}}{I_{CBO}} = \frac{10 \text{ V}}{1 \mu\text{A}} = 10 \text{ M}\Omega$$

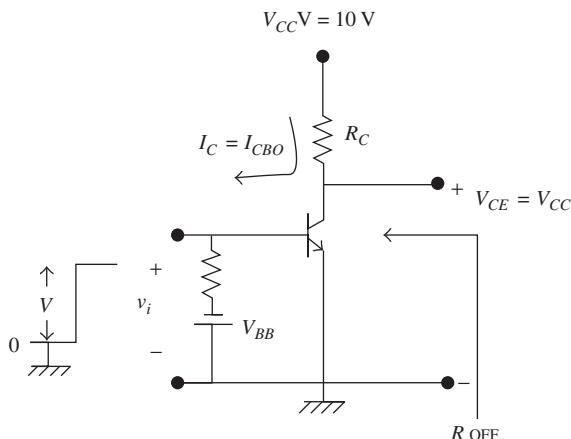


FIGURE 6.11 The transistor switch with emitter diode reverse-biased

Now the resistance between the two terminals of the OFF switch is $10 \text{ M}\Omega$. In some cases, even this may not be acceptable. We know that silicon devices are preferred over germanium devices mainly because of the fact that the leakage currents are much smaller. Thus, if for a silicon transistor $I_{CBO} = 1 \text{nA}$, then:

$$R_{OFF} = \frac{V_{CC}}{I_{CBO}} = \frac{10 \text{ V}}{1 \text{nA}} = 10,000 \text{ M}\Omega$$

This could be an acceptable OFF resistance of the switch.

6.3.2 The Transistor as a Closed Switch

Let the amplitude of the input V be sufficiently large so as to drive the transistor into saturation, as shown in Fig. 6.12.

If $I_{C(\text{sat})} = 10 \text{ mA}$,

$$R_{ON} = \frac{V_{CE(\text{sat})}}{I_{C(\text{sat})}} = \frac{0.2 \text{ V}}{10 \text{ mA}} = 20 \Omega$$

This is a small resistance. Hence the switch may be called a closed switch.

6.3.3 Over-driven Transistor Switches

In the circuit shown in Fig. 6.13, the emitter and the collector diodes are forward-biased and the transistor is driven into saturation. This transistor switch is called an over-driven switch.

When the transistor is in saturation, $V_{CE} = V_{CE(\text{sat})}$:

$$I_C = \frac{V_{CC} - V_{CE(\text{sat})}}{R_C} \quad (6.11)$$

Then,

$$I_{B(\text{min})} = \frac{I_C}{h_{FE}} \quad (6.12)$$

If $I_B > I_{B(\text{min})}$, the transistor is said to be over-driven.

The advantage of an over-driven transistor switch is that the delay time and the rise time can be reduced, because with large I_B , the junction capacitances are charged faster. The disadvantage, however, is that the storage time becomes longer. Hence, in an over-driven transistor switch, the turn-on time can be reduced with

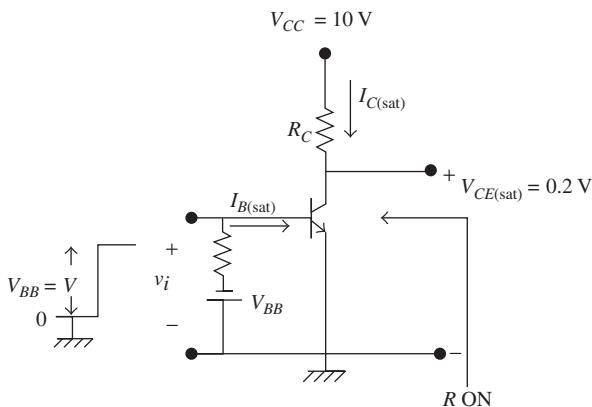


FIGURE 6.12 A transistor as a closed switch

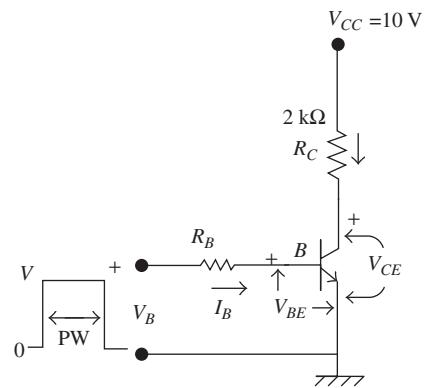


FIGURE 6.13 An over-driven transistor switch

a consequently longer turn-off time. To reduce the turn-off time, it is required to provide a negative input voltage at switch-off. This gives rise to a reverse base current which ensures that the junction capacitance discharges rapidly. This may again lengthen the turn-on time.

It is evident that, for fast switching, V_{BE} should be zero and I_B should be large at switch-on to reduce the turn-on time and this value should quickly settle down to $I_{B(\min)}$ required for saturation.

On the other hand, to reduce the turn-off time, switch-off has to be accomplished by a large reverse-bias voltage which quickly returns to zero. Both these requirements are satisfied when a capacitor is connected in shunt with R_B ; and this capacitor is called the speed-up or commutating capacitor. The effect of a commutating condenser at switch-on is shown in Fig. 6.14.

The moment v_i abruptly rises from 0 to V at $t = 0$, the capacitor behaves as a short-circuit, the charging current becomes large, $I_{B(\max)}$ and decays to $I_{B(\min)}$ as shown in Fig. 6.15. However, when v_i of opposite polarity is applied at switch-off, the capacitor discharge current assists in faster turn-off of the switch as shown in Fig. 6.16.

Here again, when the input suddenly reverses polarity and abruptly falls, C_1 behaves as a short circuit. There is a large negative current which eventually decays to zero, as shown in Fig. 6.17.

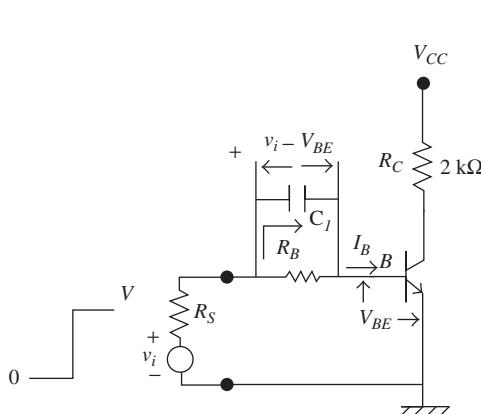


FIGURE 6.14 The effect of commutating condenser at switch-on

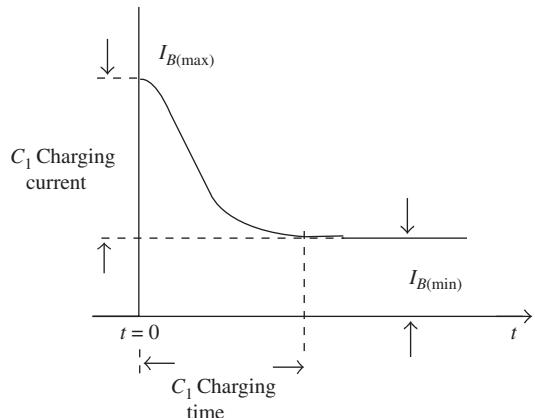


FIGURE 6.15 The charging current of C_1 at switch-on

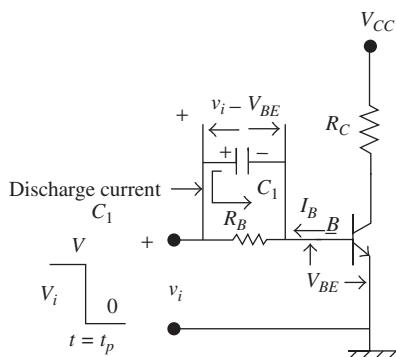


FIGURE 6.16 The effect of a commutating condenser at switch-off

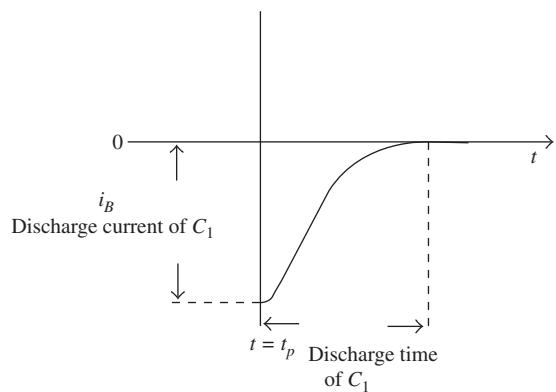


FIGURE 6.17 The discharge current of C_1 at switch-off

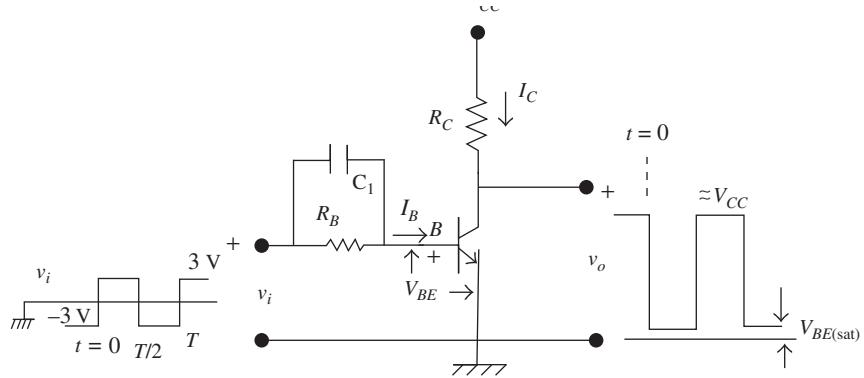


FIGURE 6.18 The transistor inverter with an unbiased emitter diode

C_1 is chosen such that its charging current, which is also the base current I_B , (see Fig. 6.14), should be at its maximum value during the turn-on time. It is allowed to drop by only 10 per cent of its maximum value during this period. This implies that C_1 can only charge by 10 per cent during the turn-on time. Consequently C_1 is chosen as:

$$t_{\text{turn-on}} = 0.1 R_s C_1 \quad (6.13)$$

where, R_s is the internal resistance of the source. However, after switch-off and next switch-on, the charge on C_1 should discharge by 90 per cent. This time interval is called the settling time, t_{settling} , (see Fig. 6.16). We have this value as:

$$t_{\text{settling}} = 2.3 R_B C_1 \quad (6.14)$$

From Eq. (6.14) we have the maximum value of C_1 as:

$$C_1(\text{max}) = \frac{t_{\text{settling}}}{2.3 R_B} \quad (6.15)$$

In the absence of specification of the turn-on time, a rule of thumb to calculate C_1 is:

$$R_B C_1 = 1 \mu\text{s} \quad (6.16)$$

6.3.4 The Design of a Transistor Inverter

In the transistor switch, also seen as the inverter, the emitter diode may be unbiased or reverse-biased to ensure that leakage currents are negligibly small and that the switch is not triggered by stray signals. In this section, both these possibilities are considered in the design of a transistor switch.

The Design of a Transistor Switch with Unbiased Emitter Diode. For the silicon transistor shown in Fig. 6.18. let input be a symmetric square wave. Here, the emitter diode is biased only by the external signal.

Let V_{CC} , I_C and $h_{FE(\text{min})}$ be specified. If the transistor is driven into saturation, when ON, R_C is chosen as:

$$R_C = \frac{V_{CC} - V_{CE(\text{sat})}}{I_C} \quad (6.17)$$

From Eq. (6.12) we have:

$$I_{B(\text{min})} = \frac{I_C}{h_{FE(\text{min})}}$$

Choose R_B such that $I_B = 1.5 \times I_{B(\text{min})}$

$$R_B = \frac{V_i - V_{BE}}{I_B} \quad (6.18)$$

C_1 is calculated using Eq. (6.13) or Eq. (6.16). Let us consider an example.

E X A M P L E

Example 6.3: Design the transistor inverter shown in Fig. 6.18. Let V_{CC} be 10 V and I_C be 1 mA and $h_{FE} = 50$.

$$R_C = \frac{V_{CC} - V_{CE(\text{sat})}}{I_C} = \frac{10 - 0.2}{1\text{mA}} = 9.8\text{ k}\Omega$$

Solution:

Choose $R_C = 10\text{ k}\Omega$

If $h_{FE} = 50$

$$I_{B(\text{min})} = \frac{I_C}{h_{FE}} = \frac{1\text{ mA}}{50} = 0.02\text{ mA}$$

$$I_B = 1.5 I_{B(\text{min})} = 1.5 \times 0.02 = 0.03\text{ mA}$$

$$R_B = \frac{V_i - V_{BE}}{I_B} = \frac{3 - 0.6}{0.03\text{ mA}} = 80\text{ k}\Omega$$

C_1 is calculated from Eq. (6.16)

$$C_1 = \frac{1\mu\text{s}}{80\text{ k}\Omega} = 12.5\text{ pF}$$

The Design of a Transistor Switch when Emitter Diode is Reverse-biased. Let us now try to design the transistor switch given in Fig. 6.19(a), in which the emitter diode is reverse-biased. The transistor switch is essentially an inverter, as shown in Fig. 6.19(a).

Case I (Q is ON and in saturation): When $v_i = V(\approx V_{CC})$, Q goes into saturation.

The circuit to be considered is shown in Fig. 6.19(b).

When Q is in saturation:

$$I_{C(\text{sat})} = \frac{V_{CC} - V_{CE(\text{sat})}}{R_C} \quad (6.19)$$

or

$$R_C = \frac{V_{CC} - V_{CE(\text{sat})}}{I_{C(\text{sat})}} \quad (6.20)$$

$$I_{B(\text{min})} = \frac{I_{C(\text{sat})}}{h_{FE}} \quad (6.21)$$

To make sure that Q is in saturation, choose:

$$I_{B(\text{sat})} = 1.5 \times I_{B(\text{min})} \quad (6.22)$$

Choose,

$$I_2 = \frac{1}{10} I_{C(\text{sat})} \quad (6.23)$$

Then,

$$R_2 = \frac{V_{BE(\text{sat})} + V_{BB}}{I_2} \quad (6.24)$$

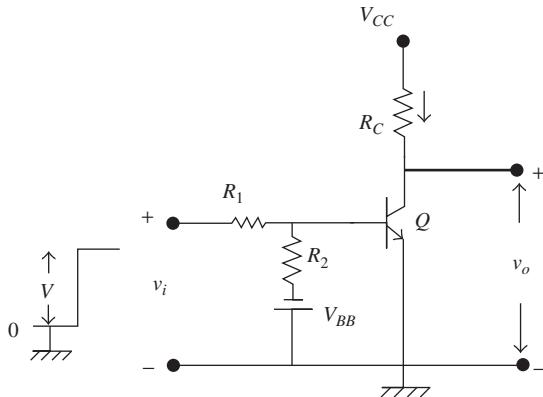
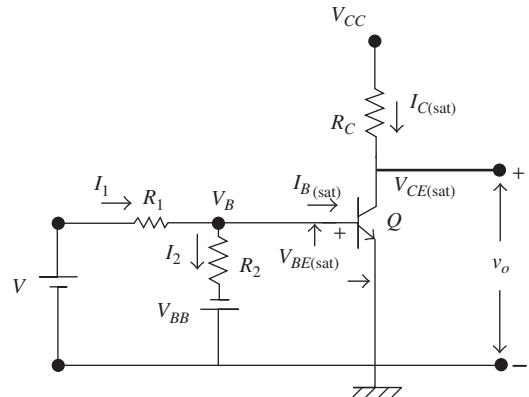


FIGURE 6.19(a) A transistor switch

FIGURE 6.19(b) The circuit of Fig. 6.19 (a) when $v_i = V$

We can calculate I_1 as:

$$I_1 = I_2 + I_{B(\text{sat})} \quad (6.25)$$

Therefore,

$$R_1 = \frac{V - V_{BE(\text{sat})}}{I_1} \quad (6.26)$$

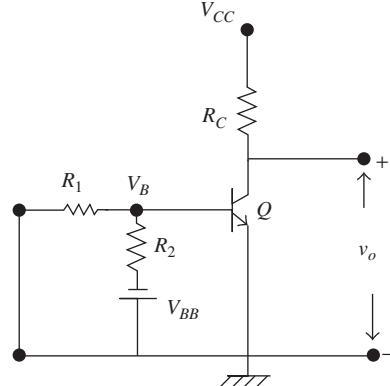
Case II (Q is OFF): As long as $v_i = 0$, Q is OFF and the output is V_{CC} . The circuit, when $v_i = 0$, is shown in Fig. 6.19(c).

Calculate V_B and verify whether Q is OFF or not.

$$V_B = -V_{BB} \frac{R_1}{R_1 + R_2} \quad (6.27)$$

$V_B = 0$ for silicon transistor to be OFF and $V_B = -0.1$ V for Ge transistor to be OFF. Further, we need to verify whether V_B reverse-biases the base-emitter diode or not.

If this diode is reverse-biased, Q is OFF and the output $v_o = V_{CC}$. Let us consider some examples.

FIGURE 6.19(c) Circuit of Fig. 6.19(a) when $v_i = 0$

EXAMP

Example 6.4: For the transistor switch in Fig. 6.19(a), if $V_{CC} = 10$ V and $V_{BB} = -5$ V, $I_{C(\text{sat})} = 5$ mA and $h_{FE} = 50$, the input signal changes from 0 to 10 V. Design the transistor switch.

Solution:

$$R_C = \frac{10 - 0.2}{5 \text{ mA}} = 1.96 \text{ k}\Omega \approx 2 \text{ k}\Omega$$

With this R_C , $I_{C(\text{sat})} = \frac{10 - 0.2}{2 \text{ k}\Omega} = 4.9 \text{ mA}$

I_B (min) for Q to be in saturation is:

$$I_{B(\text{min})} = \frac{4.9 \text{ mA}}{50} = 0.098 \text{ mA}$$

To make sure that Q is in saturation, choose $I_{B(\text{sat})} \approx 1.5I_{B(\text{min})}$.

$$I_{B(\text{sat})} = 1.5 \times 0.098 \text{ mA} = 0.147 \text{ mA}$$

Let

$$I_2 = \frac{1}{10} I_{C(\text{sat})} = \frac{4.9}{10} = 0.49 \text{ mA}$$

$$R_2 = \frac{V_{BE(\text{sat})} + V_{BB}}{I_2} = \frac{0.7 + 5}{0.49 \text{ mA}} = 11.6 \text{ k}\Omega$$

Choose $R_2 = 12 \text{ k}\Omega$

With $R_2 = 12 \text{ k}\Omega$

$$I_2 = \frac{V_{BE(\text{sat})} + V_{BB}}{12 \text{ k}\Omega} = \frac{0.7 + 5}{12 \text{ k}\Omega} = \frac{5.7}{12 \text{ k}\Omega} = 0.475 \text{ mA}$$

$$I_1 = I_2 + I_{B(\text{sat})} = 0.475 + 0.147 = 0.622 \text{ mA}$$

$$R_1 = \frac{V - V_{BE(\text{sat})}}{I_1} = \frac{10 - 0.7}{0.622 \text{ mA}} = \frac{9.3}{0.622 \text{ mA}} = 14.95 \text{ k}\Omega$$

Choose $R_1 = 15 \text{ k}\Omega$

Now calculate V_B when $v_i = 0$ to verify whether Q is OFF or not.

$$V_B = -5 \times \frac{15}{15 + 12} = \frac{-75}{27} = -2.78 \text{ V}$$

This negative voltage at the base keeps Q OFF.

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Example 6.5: A silicon transistor switch shown in Fig. 6.20(a) has $h_{FE(\text{min})} = 50$ and the input varies from 0 to 10 V with negligible rise time. Find the output levels, neglecting the junction voltages.

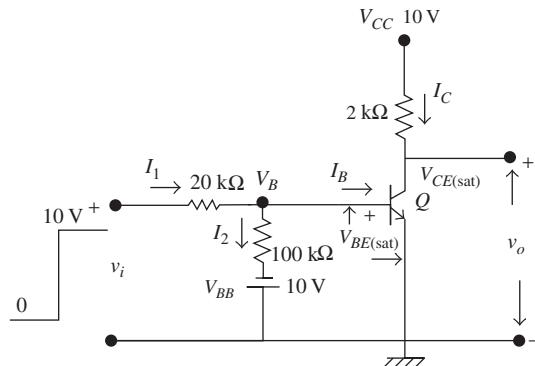


FIGURE 6.20(a) The given transistor switch

Solution:

(i) When $v_i = 0$, [see Fig. 6.20(b)], the voltage at the base V_B is:

$$V_B = -10 \times \frac{20}{20 + 100} = -1.67 \text{ V}$$

Hence, Q is OFF when $v_i = 0$.

(ii) When $v_i = 10$ V, [see Fig. 6.20(c)], the assumption is that Q goes into saturation. The calculations are based on this assumption and we also justify the assumptions.

From Fig. 6.20(c):

$$V_{BE(\text{sat})} = V_{CE(\text{sat})} = 0V \quad I_B = I_1 - I_2$$

$$I_1 = \frac{10 - V_{BE(\text{sat})}}{20 \text{ k}\Omega} = \frac{10 - 0}{20 \text{ k}\Omega} = \frac{10}{20 \text{ k}\Omega} = 0.5 \text{ mA} \quad I_2 = \frac{V_{BE(\text{sat})} + V_{BB}}{100 \text{ k}\Omega} = \frac{0 + 10}{100 \text{ k}\Omega} = \frac{10}{100 \text{ k}\Omega} = 0.1 \text{ mA}$$

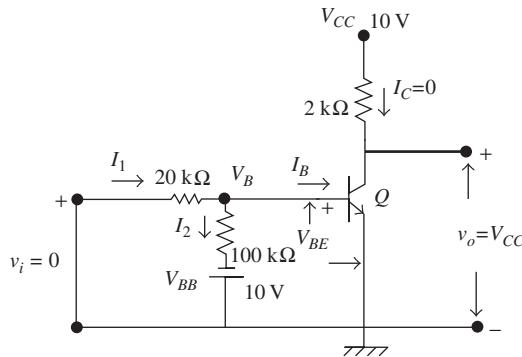


FIGURE 6.20(b) The transistor switch when $v_i = 0$

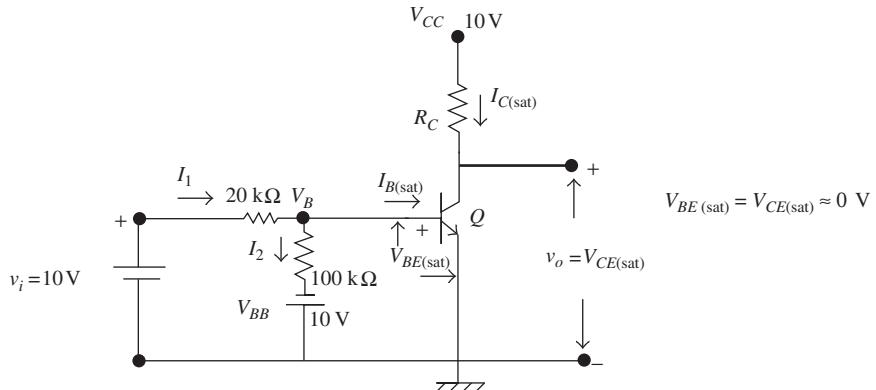


FIGURE 6.20(c) Transistor switch when $v_i = 10$ V

$$I_B = I_1 - I_2 = 0.5 - 0.1 = 0.4 \text{ mA} \quad I_C = \frac{V_{CC} - V_{CE(\text{sat})}}{R_C} = \frac{10 - 0}{2 \text{ k}\Omega} = 5 \text{ mA}$$

$$I_{B(\text{min})} = \frac{I_C}{h_{FE(\text{min})}} = \frac{5 \text{ mA}}{50} = 0.1 \text{ mA} \quad I_B \gg I_{B(\text{min})}$$

Hence, Q is in saturation.

$\therefore v_o = V_{CE(\text{sat})} \approx 0V$ as assumed

Thus, when $v_i = 0$ V, $v_o = 10$ V and when $v_i = 10$ V, $v_o = 0$ V.

EXAMPLE

Example 6.6: Calculate the output levels of the circuit in Fig. 6.21(a) for inputs of 0 V and 10 V. Verify that the circuit is an inverter. What is the minimum value of h_{FE} required? Neglect junction saturation voltages and assume an ideal diode.

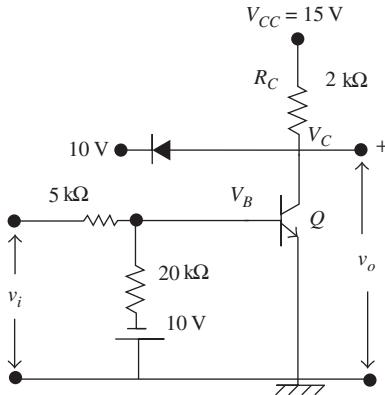


FIGURE 6.21(a) The given transistor inverter

Solution:

When $v_i = 0$,

$$V_B = -10 \times \frac{5}{20+5} = -2 \text{ V}$$

Then Q is OFF, $\therefore V_C = 15 \text{ V}$

D now conducts $\therefore v_o = 10 \text{ V}$.

(ii) Let $v_i = 10 \text{ V}$, [see Fig. 6.21(b)]

$$I_1 = I_2 + I_B \quad I_B = I_1 - I_2$$

$$I_B = \frac{10}{5 \text{ k}\Omega} - \frac{10}{20 \text{ k}\Omega} = 2 \text{ mA} - 0.5 \text{ mA} = 1.5 \text{ mA}$$

since Q is ON and $V_{CE(\text{sat})} = 0$:

$$I_C \approx \frac{15}{2 \text{ k}\Omega} = 7.5 \text{ mA.}$$

$$v_o = 15 - 7.5 \times 10^{-3} \times 2 \times 10^3 = 0 \text{ V}$$

$\therefore h_{FE}$ required is,

$$h_{FE} = \frac{I_C}{I_B} = \frac{7.5 \text{ mA}}{1.5 \text{ mA}} = 5 \quad \therefore h_{FE(\text{min})} = 5$$

The circuit acts like an inverter for inputs 0 V and 10 V.

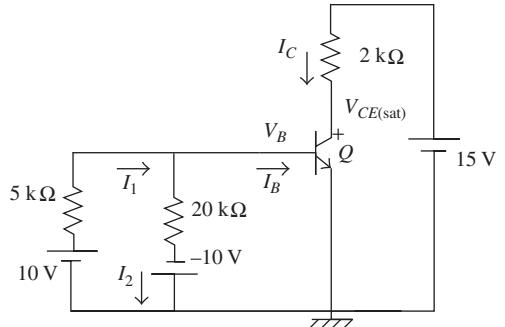


FIGURE 6.21(b) Circuit when $v_i = 10 \text{ V}$

Non-Saturating Transistor Switches. When a transistor is driven hard into saturation, the turn-off time becomes longer because of a larger storage time. To overcome this handicap, the transistor may be held in the active region. Such a transistor switch is called a non-saturating switch. To ensure this, a small reverse-bias voltage is provided for the collector diode using a diode and an external source V_R , shown in Fig. 6.22.

When Q is ON and if V is large enough to drive it into saturation, the voltage at the collector tends to reach a value $V_{CE(sat)}$. However, the moment the voltage at the collector is less than V_R by V_γ , diode D conducts, clamping the collector to V_R . V_R is chosen typically as 1 to 2 V so that no appreciable reverse-bias voltage is provided to the collector diode.

JFET Switches. An FET is a high-input-resistance device which can also be used as a switch. An n -channel JFET used as a switch is shown in Fig. 6.23(a).

For the FET, let $I_{D(OFF)}$, R_D , V_{DD} and $R_{D(ON)}$ be given:

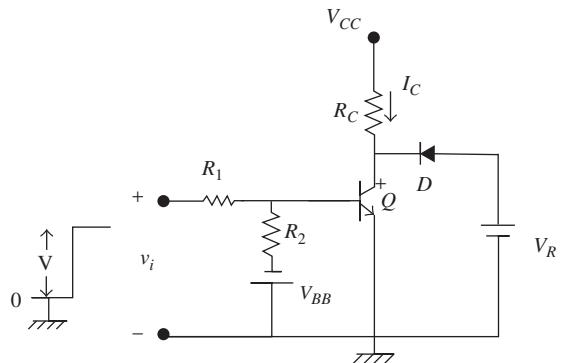


FIGURE 6.22 A non-saturating transistor switch

$$V_{DS(OFF)} = V_{DD} - I_{D(OFF)}R_D \quad (6.28)$$

$I_{D(ON)}$ is given as:

$$I_{D(ON)} \approx \frac{V_{DD}}{R_D} \quad (6.29)$$

$$V_{DS(ON)} = I_D \times R_{D(ON)} \quad (6.30)$$

where, $R_{D(ON)}$ is the resistance between the drain and source terminals when the FET is ON, which typically is a few ohms. Let us consider an example to calculate the output when the switch is ON and when it is OFF.

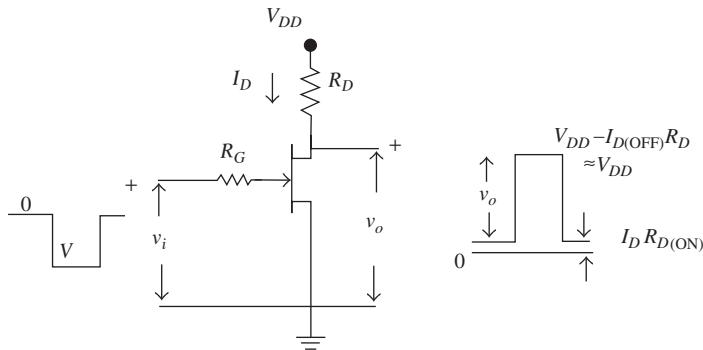


FIGURE 6.23(a) A JFET switch

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Example 6.7: For the FET switch given in Fig. 6.23(b), calculate the output when the switch is ON and when it is OFF, given that, $I_{D(OFF)} = 0.2 \text{ nA}$, $R_D = 5 \text{ k}\Omega$, $V_{DD} = 12 \text{ V}$ and $R_{D(ON)} = 100 \Omega$.

Solution:

$$\therefore v_o = V_{DS(OFF)} = V_{DD} - I_{D(OFF)}R_D = 12 - 0.2 \times 10^{-9} \times 5 \times 10^3 \approx 12 \text{ V}$$

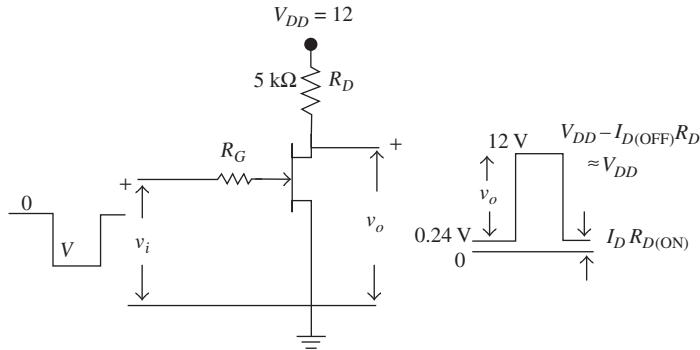


FIGURE 6.23(b) A JFET switch

$$\therefore I_D = \frac{V_{DD}}{R_D} = \frac{12}{5 \text{ k}\Omega} = 2.4 \text{ mA} \quad \therefore v_o = V_{DS(\text{ON})} = I_D R_{D(\text{ON})} = 2.4 \times 10^{-3} \times 0.1 \times 10^3 = 0.24 \text{ V.}$$

6.4 SWITCHING TIMES OF A TRANSISTOR

Instead of a step, if a pulse is applied to the transistor switch, how does the device respond? To understand this, we consider the switching times of a transistor (see Fig. 6.24).

Let the input to the transistor switch be a pulse of duration T . When a pulse is applied, because of stray capacitances, collector current will not reach the steady-state value instantaneously. To know exactly when the device switches into the ON state and also into the OFF state, we define the following switching times of the transistor.

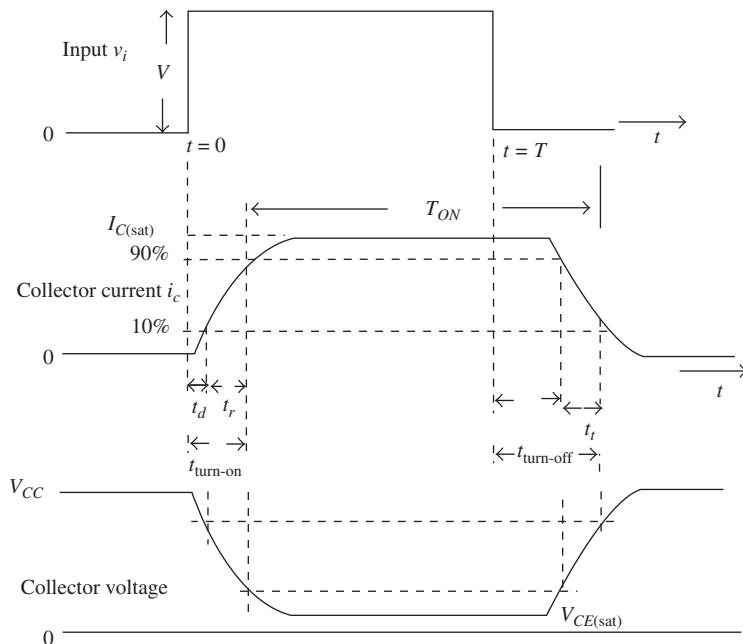


FIGURE 6.24 Switching times of the transistor

6.4.1 The Turn-on Time of a Transistor

Turn-on time of the transistor is the time taken by the transistor from the instant the pulse is applied to the instant the transistor switches into the ON state and is the sum of the delay time and rise time. To find out the turn-on time of the transistor, the delay time and rise time have to be calculated.

Delay Time (t_d). It is the time taken for the collector current to reach from its initial value to 10 per cent of its final value.

If the rise of the collector current is linear, the time required to rise to 10 per cent $I_{C(sat)}$ is 1/8 the time required for the current to rise from 10 per cent to 90 per cent $I_{C(sat)}$.

It is given as:

$$t_d = \frac{1}{8} t_r \quad (6.31)$$

where, t_r is the rise time.

Rise Time. Rise time, t_r is the time taken for the collector current to reach from 10 per cent of its final value to 90 per cent of its final value. From Fig. 6.24 it is seen that the moment input pulse is zero, the collector current is expected to fall to zero. However, because of the stored charges, the current remains unaltered for sometime interval t_{s1} and then begin to fall. The time taken for this current to fall from its initial value at t_{s1} to 90 per cent of its initial value is t_{s2} . The sum of these t_{s1} and t_{s2} is approximately $t_{s1} = t_s$ and is called the storage time. To calculate the rise time, consider the transistor switch as shown in Fig. 6.25.

Let I_B be the base current pulse that drives the transistor into saturation at I_{B1} and into OFF state at I_{B2} . If R_S is large when compared to h_{ie} ,

$$I_{B1} \approx \frac{v_i}{R_S} = \frac{V}{R_S} \quad (6.32)$$

The response of the transistor to the current step I_{B1} is given by:

$$i_C = \frac{h_{FE} R_S I_{B1}}{R_S + h_{ie}} (1 - e^{-2\pi f_2 t}) \quad (6.33)$$

If R_S is large,

$$i_C = h_{FE} I_{B1} (1 - e^{-2\pi f_2 t}) \quad (6.34)$$

where f_2 = Upper 3-dB frequency of the low-pass RC circuit.

$$f_2 = \frac{1}{2\pi\tau} \quad (6.35)$$

where, τ is the time constant.

Substituting Eq. (6.35) in Eq. (6.34),

$$i_C = h_{FE} I_{B1} (1 - e^{-t/\tau}) \quad (6.36)$$

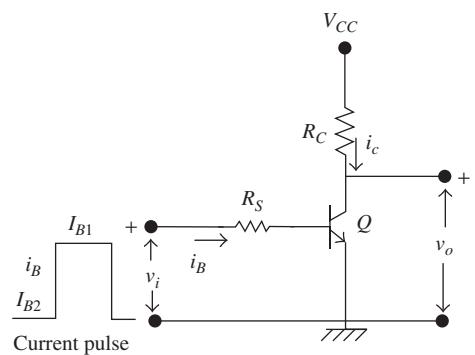


FIGURE 6.25 A transistor switch

If the device does not go into saturation, i_C would have increased as shown by the dashed line in Fig. 6.26 and would have reached a value $h_{FE}I_{B1}$ as $t \rightarrow \infty$. The gain bandwidth product of a transistor amplifier in which the transistor is replaced by an ideal current source $h_{FE}I_B$ (since $(1/h_{oe}) \approx \infty$) is given as:

$$h_{FE}f_2 = \frac{f_T}{1 + 2\pi f_T C_{TC} R_C} \quad (6.37)$$

where, f_T is the frequency at which the short circuit common emitter current gain has a value 1 and C_{TC} is the collector diode transition capacitance.

From Eq. (6.37):

$$2\pi h_{FE}f_2 = \frac{2\pi f_T}{1 + 2\pi f_T C_{TC} R_C} = \frac{\omega_T}{1 + \omega_T C_{TC} R_C}$$

$$\frac{1}{2\pi f_2} = \frac{h_{FE}}{\omega_T} (1 + \omega_T C_{TC} R_C)$$

Therefore:

$$\tau = \frac{h_{FE}}{\omega_T} (1 + \omega_T C_{TC} R_C) \quad (6.38)$$

The variation of the collector current i_C is plotted in Fig. 6.26 using Eq. (6.36).

When in saturation Eq. (6.36) is written as:

$$\frac{I_{C(\text{sat})}}{h_{FE}I_{B1}} = (1 - e^{-t/\tau})$$

Let $\frac{h_{FE}I_{B1}}{I_{C(\text{sat})}} = N_1$

$$As \quad \frac{I_{C(\text{sat})}}{h_{FE}} = I_{B1(\text{min})} \quad N_1 = \frac{I_{B1}}{I_{B1(\text{min})}}$$

$$\text{If } N_1 > 1, \text{ the transistor is in saturation (over-driven transistor). Hence, } \frac{1}{N_1} = (1 - e^{-t/\tau}).$$
(6.39)

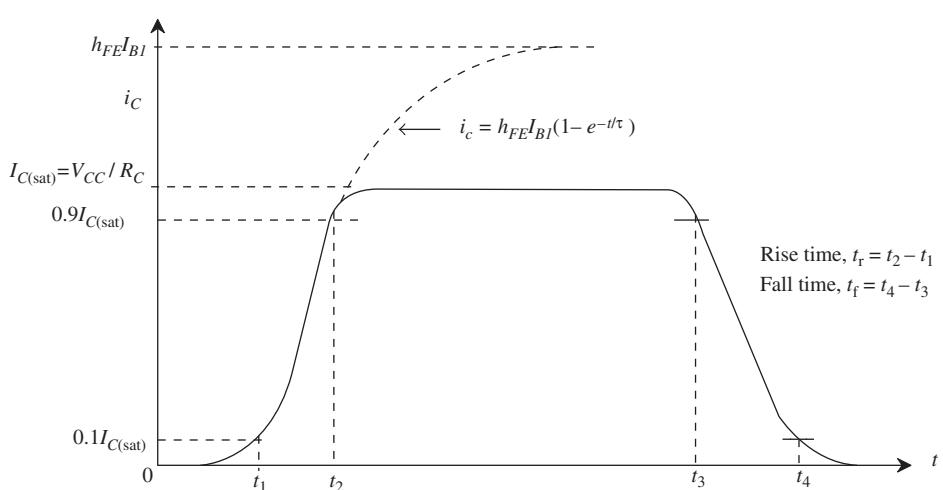


FIGURE 6.26 Variation of i_C (i) when the device is in saturation (ii) when the device is not in saturation and (iii) when the device switches into OFF state

At $t = t_1$, $1/N_1$ is $0.1/N_1$

$$\frac{0.1}{N_1} = 1 - e^{-t_1/\tau}$$

$$e^{-t_1/\tau} = 1 - \frac{0.1}{N_1}$$

$$e^{t_1/\tau} \frac{1}{1 - \frac{0.1}{N_1}} \quad t_1 = \tau \ln \frac{1}{1 - \frac{0.1}{N_1}}$$

$$\text{Similarly } t_2 = \tau \ln \frac{1}{1 - \frac{0.9}{N_1}}$$

$$\therefore t_r = t_2 - t_1 = \tau \ln \frac{1 - \frac{0.1}{N_1}}{1 - \frac{0.9}{N_1}}$$

We know that $\ln(1 + x) = x - \frac{x^2}{2} + \frac{x^3}{3} - \dots$

$$\begin{aligned} t_r &= \tau \left[\ln \left(1 - \frac{0.1}{N_1} \right) - \ln \left(1 - \frac{0.9}{N_1} \right) \right] \\ &= \tau \left[\left(-\frac{0.1}{N_1} - \frac{0.01}{2N_1^2} - \frac{0.001}{3N_1^3} \right) - \left(-\frac{0.9}{N_1} - \frac{0.81}{2N_1^2} - \frac{0.729}{3N_1^3} \right) \right] \\ t_r &= \tau \left(\frac{0.8}{N_1} + \frac{0.8}{2N_1^2} + \frac{0.728}{3N_1^3} \right) = \frac{0.8\tau}{N_1} \left(1 + \frac{0.5}{N_1} + \frac{0.30}{N_1^2} + \dots \right) \end{aligned}$$

For $N_1 \gg 1$, considering only the 1st term

$$t_r = \frac{0.8\tau}{N_1} \quad (6.40)$$

From Eq. (6.39),

$$N_1 = \frac{h_{FE} I_{B1}}{I_{C(\text{sat})}}$$

$$\therefore t_r = 0.8\tau \frac{I_{C(\text{sat})}}{h_{FE}} \times \frac{1}{I_{B1}} \quad (6.41)$$

The rise time t_r , is inversely proportional to I_{B1} . Therefore, if the turn-on time is to be small it is desirable to have a larger base current drive (over-driven transistor).

EXAMP E

Example 6.8: Consider the switch in Fig. 6.27, C_{TC} = collector transition, capacitance = 7 pF, $h_{FE} = 100$ and $f_T = 10$ MHz. Calculate the turn-on time of the transistor.

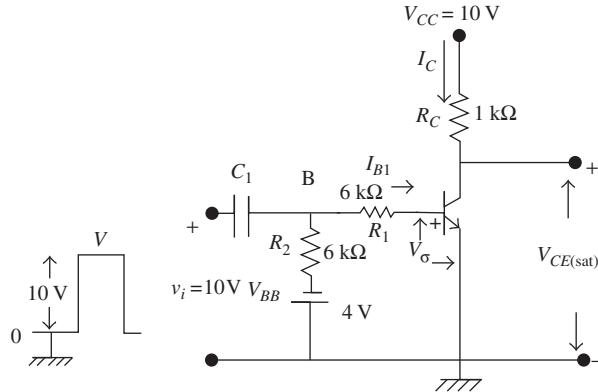


FIGURE 6.27 The given transistor switch

Solution:

To calculate the turn-on time, we have to calculate t_r and t_d .

From Fig. 6.27, we have,

$$I_{C(\text{sat})} = \frac{V_{CC} - V_{CE(\text{sat})}}{R_C} \approx \frac{V_{CC}}{R_C} = \frac{10 \text{ V}}{1 \text{ k}\Omega} = 10 \text{ mA}$$

$$I_{B1(\text{min})} = \frac{I_{C(\text{sat})}}{h_{FE}} \approx \frac{10 \text{ mA}}{100} = 0.1 \text{ mA}$$

In the quiescent state the voltage at B is -4 V. However, when a pulse of 10 V appears at the input this voltage at B is 6 V.

$$I_{B1} = \frac{(10 - V_\sigma)}{R_1} \approx \frac{10}{6 \text{ k}\Omega} = 1.0 \text{ mA}$$

We have from Eq. (6.39), $N_1 = \frac{I_{B1}}{I_{B1(\text{min})}}$

$$N_1 = \frac{1.0 \text{ mA}}{0.1 \text{ mA}} = 10$$

Hence, $N_1 \geq 1$. Equation (6.41) is valid when the overdrive factor $N_1 \geq 1$. ω_T is the radial frequency at which the current gain is unity. The rise time t_r is calculated using Eq. (6.41) as,

$$t_r = 0.8 \frac{\tau}{h_{FE}} \times \frac{I_{C(\text{sat})}}{I_{B1}}$$

and from Eq.(6.38),

$$\frac{\tau}{h_{FE}} = \left(\frac{1}{\omega_T} + C_{TC} R_C \right) \quad (6.42)$$

where τ is the time constant.

Using Eq. (6.42)

$$\frac{\tau}{h_{FE}} = \left(\frac{1}{2 \times \pi \times 10 \times 10^6} + 7 \times 10^{-12} \times 10^3 \right) = 23 \text{ ns}$$

From Eq. (6.41)

$$t_r = 0.8 \times 23 \text{ ns} \times \frac{10}{1.0} = 184 \text{ ns} \quad \text{and} \quad t_d = \frac{1}{8} \times t_r = \frac{184}{8} = 23 \text{ ns}$$

$$t_{\text{turn-on}} = t_r + t_d = 184 + 23 = 207 \text{ ns.}$$

E X A M P L E

Example 6.9: A transistor has $f_T = 50$ MHz, $h_{FE} = 50$, $C_{TC} = 5$ pF, (C_{TC} = collector transition capacitance) and the supply voltage $V_{CC} = 10$ V, $R_C = 0.5$ k Ω . Initially the transistor is operating in the neighbourhood of the cut-in point. What base current must be applied to drive the transistor into saturation in $1\mu\text{s}$?

Solution:

We have

$$t_r = 0.8 \frac{\tau}{h_{FE}} \times \frac{I_{C(\text{sat})}}{I_{B1}} \quad \therefore I_{B1} = 0.8 \frac{\tau}{h_{FE}} \times \frac{I_{C(\text{sat})}}{t_r}$$

Also

$$\frac{\tau}{h_{FE}} = \left(\frac{1}{\omega_T} + C_{TC} R_C \right)$$

$$\therefore I_{B1} = 0.8 \left(\frac{1}{\omega_T} + C_{TC} R_C \right) \times \frac{I_{C(\text{sat})}}{t_r}$$

$$\omega_T = 2\pi f_T = 2 \times \pi \times 50 \times 10^6 = 314 \times 10^6 \text{ radians}$$

$$C_{TC} R_C = 5 \times 10^{-12} \times 0.5 \times 10^3 = 2.5 \times 10^{-9} \text{ s}$$

$$I_{C(\text{sat})} = \frac{V_{CC}}{R_C} = \frac{10\text{V}}{0.5\text{k}\Omega} = 20 \text{ mA}$$

$$t_r = 1 \times 10^{-6}$$

$$I_{B1} = 0.8 \left(\frac{1}{314 \times 10^6} + 2.5 \times 10^{-9} \right) \times \left(\frac{20 \times 10^{-3}}{1 \times 10^{-6}} \right)$$

$$= 0.8 \times 10^{-9} \left(\frac{1}{0.314} + 2.5 \right) \times 20 \times 10^3 = 16 \left(\frac{1}{0.314} + 2.5 \right) 10^{-6}$$

$$= 16(3.18 + 2.5) \mu\text{A} = 90.88 \mu\text{A}$$

A transistor is said to be switched from the OFF state into the ON state only when the collector current is 90 per cent of its final value. Thus we see that even though the transistor is expected to switch from OFF to ON at $t = 0$ when $v_t = V$, the device switches actually into the ON state only when a finite time elapses and we call this time interval as the turn-on time of the transistor. From Example 6.8:

$$t_{\text{turn-on}} = t_d + t_r = 23 + 184 = 207 \text{ ns}$$

6.4.2 The Turn-off Time of a Transistor

Again at $t = T$ (at the end of the pulse), the transistor is required to switch into the OFF state instantaneously. But this is not going to happen. Once the device is driven hard into saturation, because of large number of stored charges on either side of the junction, the collector current is not going to fall to a smaller value instantaneously. To calculate the turn-off time we have to calculate the storage time and the fall time.

Storage Time (t_s). Storage time, t_s , is the time taken for the collector current to fall from its initial value to 90 per cent of its initial value.

$$\text{Storage time } t_s \cong \tau_s \ln \frac{I_{B1} - I_{B2}}{I_{B1(\text{min})} - I_{B2}} \quad (6.43)$$

I_{B1} is the base current, when the pulse amplitude is $V = 10$ V and I_{B2} is the base current, when the pulse amplitude is zero, (see Fig. 6.27).

Here

$$\tau_s = \frac{\omega_N + \omega_I}{\omega_N \omega_I (1 - \alpha_{N0} \alpha_{I0})} \quad (6.44)$$

$$\alpha_N = \frac{\alpha_{N0}}{1 + j \frac{\omega}{\omega_N}} \quad \text{and} \quad \alpha_I = \frac{\alpha_{I0}}{1 + j \frac{\omega}{\omega_I}} \quad (6.45)$$

where, α_I and α_N are the inverted mode and normal mode current gains in terms of Ebers–Moll parameters. α_{N0} is the normal direction current gain and its 3-dB frequency is ω_N . α_{I0} is the inverted mode current gain and the 3-dB frequency is ω_I .

E X A M P L E

Example 6.10: From Fig. 6.27, calculate the storage time if $h_{FE} = 100$, $\alpha_{N0} = 0.99$, $\alpha_{I0} = 0.5$, $f_N = 1.2 f_T$, $f_T = 1.2 \times 1 \times 10^6 = 1.2$ MHz, $f_I = 1$ MHz

Solution:

From Eq. (6.44):

$$\tau_s = \frac{2\pi(1.2 + 1) \times 10^6}{(2\pi)^2(1.2 \times 10^6)(1 \times 10^6) \times [1 - (0.99)(0.5)]} = 0.577 \mu\text{s}$$

If $V = 10$ V

$$I_{B1} = \frac{6\text{V}}{6\text{k}\Omega} = 1\text{mA}$$

$$I_{B1(\min)} = \frac{I_{C(\text{sat})}}{h_{FE}} = \frac{10\text{mA}}{100} = 0.1\text{mA}$$

$$I_{B2} = \frac{-4\text{V}}{6\text{k}\Omega} = -0.67\text{mA}$$

Using Eq. (6.43):

$$t_s = 0.577 \ln \frac{1 + 0.67}{0.1 + 0.67} = 0.577 \times 0.775 = 447\text{ns}$$

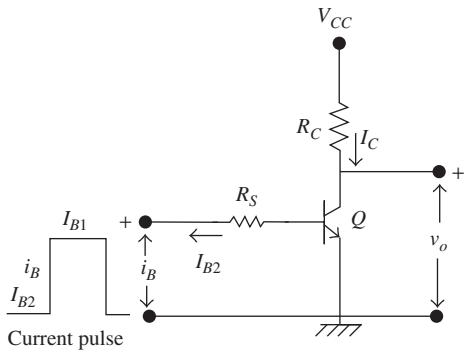
Further, the transistor is said to be switched from the ON state to OFF state only when the collector current falls to 10 per cent of its initial value. This is the fall time.

Fall Time. Fall time, t_f , is the time taken for the collector current to fall from 90 per cent of its initial value to 10 per cent of its initial value. To calculate the fall time, consider Fig. 6.28 when the base current is I_{B2} .

The fall time calculation is similar to the rise time calculation. Here, I_{B2} flows in the opposite direction. The device returns from saturation to active region where the collector current is $h_{FE}I_{B2}$.

$$\text{Now let } N_2 = \frac{-h_{FE}I_{B2}}{I_{C(\text{sat})}} \quad (6.46)$$

As I_{B2} flows in the opposite direction N_2 is positive. We have,

FIGURE 6.28 Base current is I_{B2}

$$\frac{I_{C(\text{sat})}}{h_{FE}I_{B2}} = (1 - e^{-t/\tau}) \quad \frac{-1}{N_2} = (1 - e^{-t/\tau})$$

From Fig. 6.26 at $t = t_3$, $1/N_2$ is $0.9/N_2$

$$\frac{-0.9}{N_2} = (1 - e^{-t_3/\tau}) \quad e^{-t_3/\tau} = 1 + \frac{0.9}{N_2}$$

$$e^{t_3/\tau} = \frac{1}{1 + \frac{0.9}{N_2}}$$

$$\text{Similarly, } t_4 = \tau \ln \frac{1}{1 + \frac{0.1}{N_2}}$$

$$t_3 = \tau \ln \left(\frac{1}{1 + \frac{0.9}{N_2}} \right)$$

$$t_f = t_4 - t_3 = \tau \ln \frac{1 + \frac{0.9}{N_2}}{1 + \frac{0.1}{N_2}}$$

$$t_f = \frac{0.8\tau}{N_2} \left[\left(1 - \frac{0.5}{N_2} + \frac{0.30}{N_2^2} - \dots \right) \right] = \frac{0.8\tau}{N_2} = -0.8\tau \frac{I_{C(\text{sat})}}{h_{FE}} \times \frac{1}{I_{B2}}$$

Fall time, t_f again is inversely proportional to I_{B2} . If the turn-off time is to be small, I_{B2} should be relatively large.

It is given as:

$$t_f = 0.8 \frac{\tau}{h_{FE}} \times \frac{I_{C(\text{sat})}}{I_{B2}} \quad (6.47)$$

Equation (6.47) is valid when $N_2 > 1$.

EXAMPLE

Example 6.11: For the circuit in Fig. 6.27, calculate the fall time.

Solution:

$$N_2 = \frac{h_{FE}I_{B2}}{I_{C(\text{sat})}} = \frac{100 \times 0.67}{10} = 6.7 \quad \therefore N_2 \geq 1$$

From Eq. (6.47), we have,

$$t_f = 0.8 \frac{\tau}{h_{FE}} \times \frac{I_{C(\text{sat})}}{I_{B2}}$$

$$t_f = 0.8 \times 23 \text{ ns} \times \frac{10}{0.67} = 274.6 \text{ ns}$$

Therefore, from the calculations made in Examples 6.10 and 6.11, we have the turn-off time of the transistor as,

$$t_{\text{turn-off}} = t_s + t_f = 447 + 274 = 721\text{ns}.$$

The major concern now in switching applications is – how quickly can we drive a transistor from one state to the other. This switching speed obviously depends on the switching times of the transistor.

6.5 BREAKDOWN VOLTAGES

We have seen that by the application of a signal of proper polarity and magnitude, a transistor switch can be driven into saturation. As a result, the voltage at the collector of the device is $V_{CE(\text{sat})}$ (typically 0.1 V for Ge and 0.2 V for Si). Now, when a signal of opposite polarity is applied as input to the switch, ideally the voltage at the collector rises to V_{CC} . Thus, we see that the change in voltage at the collector is $V_{CC} - V_{CE(\text{sat})} \approx V_{CC}$. This output is connected to operate some other circuits. For proper operation, it is desirable that V_{CC} be made reasonably large. However, by increasing the value of V_{CC} , the reverse-bias voltage on the collector base diode could become so large that an avalanche breakdown may occur in the collector diode. The leakage current I_{CO} will then become $M_n I_{CO}$ where, M_n is the avalanche multiplication factor. M_n depends on V_{CB} . An empirical relation for M_n , applicable for many transistor types is given as:

$$M_n = \frac{1}{1 - \left(\frac{V_{CB}}{V_{CBO(\text{max})}} \right)^n} \quad (6.48)$$

Here, $V_{CBO(\text{max})}$ is a maximum reverse-bias voltage that can be applied between the collector and base terminals of the transistor when the emitter lead is open-circuited and n is typically in the range of 2 to 10 which controls the sharpness of onset of a breakdown. Calculation of M_n is illustrated in the Example 6.12.

EXAMPLE

Example 6.12: If $V_{CBO(\text{max})} = 50$, $V_{CB} = 45$ V and then, calculate the avalanche multiplication factor for (a) $n = 10$ and (b) $n = 2$.

Solution:

(a) Consider a case when n is large, $n = 10$, using Eq. (6.48),

$$M_{10} = \frac{1}{1 - \left(\frac{V_{CB}}{V_{CBO(\text{max})}} \right)^{10}} = \frac{1}{1 - \left(\frac{45}{50} \right)^{10}} = 1.52$$

(b) When $n = 2$

$$M_2 = \frac{1}{1 - \left(\frac{45}{50} \right)^2} = 5.26$$

When n is large, M remains almost approximately at unity till such time V_{CB} reaches $V_{CBO(\text{max})}$ at which time it becomes infinity abruptly. On the other hand, if n is small, the onset of breakdown occurs more gradually.

Let us consider the CB characteristics when extended into the breakdown region. Fig. 6.29.

It is seen from the characteristics, that I_C almost remains constant upto V_{CB1} . Beyond V_{CB1} , I_C varies slowly and I_C rises sharply as V_{CB} reaches $V_{CBO(\text{max})}$. The current gain in the CB configuration being h_{FB} , the collector current $I_C = h_{FB} I_E$. Taking the avalanche multiplication into consideration, then,

$$I_C = M_n h_{FB} I_E \quad (6.49)$$

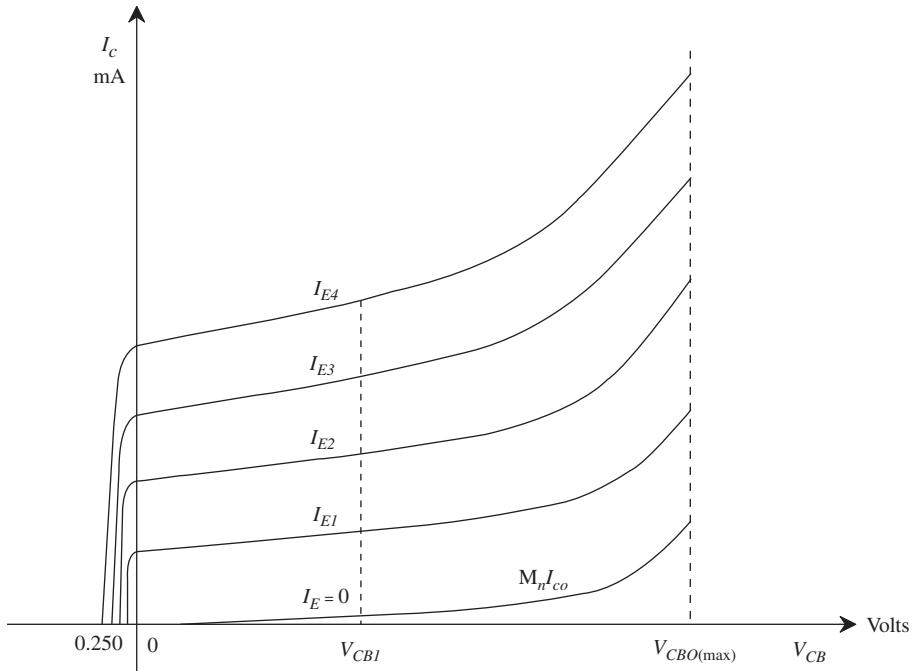


FIGURE 6.29 CB characteristics extended into breakdown region

This means that if avalanche multiplication takes place, h_{FB} is seen to have increased by a factor M_n so that h_{FB}^* in the presence of avalanche multiplication is,

$$h_{FB}^* = M_n h_{FB} \quad (6.50)$$

6.5.1 The CE Configuration

We know that the current gain in CE configuration is h_{FE} and that

$$h_{FE} = \frac{h_{FB}}{1 - h_{FB}} \quad (6.51)$$

Therefore, h_{FE} in the presence of avalanche multiplication is h_{FE}^* and is given by:

$$h_{FE}^* = \frac{h_{FB}^*}{1 - h_{FB}^*} = \frac{M_n h_{FB}}{1 - M_n h_{FB}} \quad (6.52)$$

$$\text{If } M_n h_{FB} = 1 \quad (6.53)$$

h_{FE} becomes infinity. This means an abruptly large collector current flows when $M_n h_{FB} = 1$ which suggests that breakdown has occurred in the device.

From Eq. (6.53),

$$M_n = \frac{1}{h_{FB}} \quad (6.54)$$

Substituting Eq. (6.54) in Eq. (6.48):

$$\frac{1}{1 - \left(\frac{V_{CB}}{V_{CBO(\max)}} \right)^n} = \frac{1}{h_{FB}} \quad \left(\frac{V_{CB}}{V_{CBO(\max)}} \right)^n = 1 - h_{FB}$$

And

$$V_{CB} = V_{CBO(\max)} \sqrt[n]{1 - h_{FB}} \quad (6.55)$$

Also

$$V_{CE} = V_{CB} + V_{BE} \quad (6.56)$$

V_{CB} at breakdown is very much larger than V_{BE} . From Eq. (6.56),

$$\therefore V_{CE} \approx V_{CB}$$

Equation (6.55) is written as:

$$V_{CE} = V_{CBO(\max)} \sqrt[n]{1 - h_{FB}} \quad (6.57)$$

As

$$\frac{h_{FB}}{1 - h_{FB}} = h_{FE} \quad \text{and} \quad h_{FB} \approx 1$$

$$1 - h_{FB} = \frac{h_{FB}}{h_{FE}} \approx \frac{1}{h_{FE}} \quad (6.58)$$

Using Eqs. (6.57) and (6.58):

$$V_{CEO(\max)} = V_{CBO(\max)} \sqrt[n]{\frac{1}{h_{FE}}} \quad (6.59)$$

Equation (6.59) enables us to calculate $V_{CEO(\max)}$, if $V_{CBO(\max)}$, n and h_{FE} are known. Let us consider an example.

E X A M P L E

Example 6.13: Calculate $V_{CEO(\max)}$, if for a transistor, $n = 6$, $h_{FE} = 100$ and $V_{CBO(\max)} = 50$ V.

Solution:

We have from Eq. (6.59),

$$V_{CEO(\max)} = V_{CBO(\max)} \sqrt[n]{\frac{1}{h_{FE}}} = V_{CBO(\max)} \sqrt[6]{\frac{1}{100}}$$

$$V_{CEO(\max)} = 0.464 \times V_{CBO(\max)}$$

$$V_{CEO(\max)} = 0.464 \times 50 = 23.2 \text{ V}$$

$V_{CEO(\max)}$ is approximately half of $V_{CBO(\max)}$.

The CE characteristics extended up to $V_{CEO(\max)}$ are plotted in Fig. 6.30. From these characteristics it is seen that as long as $V_{CE} \leq V_{CE1}$, the collector current I_C almost remains constant. When V_{CE} is further increased, I_C increases with increasing voltage and finally at $V_{CE} = V_{CEO(\max)}$, I_C abruptly rises to a very large value indicating that breakdown has occurred.

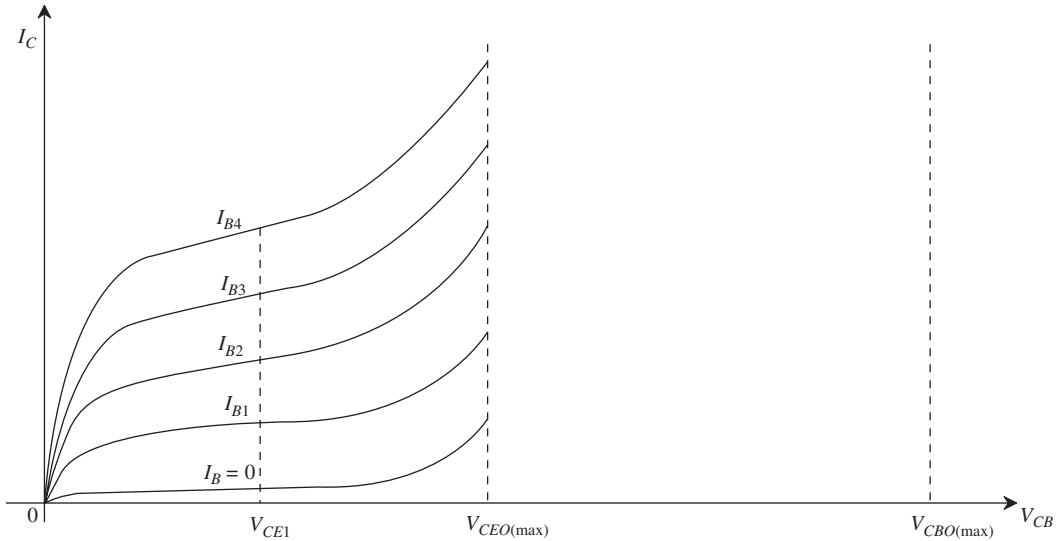
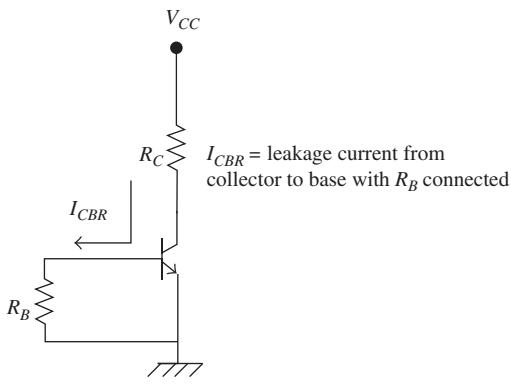


FIGURE 6.30 CE characteristics extended up to the breakdown region

6.5.2 The Breakdown Voltage with Base Not Open Circuited

Consider the figure shown in Fig. 6.31. $V_{CEO(\max)}$ is the breakdown voltage between the collector and emitter terminals with the base lead open. Now, if the base lead is not open circuited, but a resistance R_B is connected between the base and emitter terminals, the new breakdown voltage may be termed as $V_{CER(\max)}$. The expectation is that $V_{CER(\max)}$ lies somewhere between $V_{CEO(\max)}$ and $V_{CBO(\max)}$. Let us try to calculate the value of $V_{CER(\max)}$.

FIGURE 6.31 R_B is connected between base and emitter terminals

From Eq. (6.60):

$$\frac{1}{M_n} = \frac{I_{C0}R_B}{V_\gamma} \quad (6.62)$$

$$\text{i.e., } h_{FB} = \frac{I_{C0}R_B}{V_\gamma} \quad (6.63)$$

It is known that unless a voltage of V_γ exists between base and emitter terminals, the diode forward current is small and the collector to base leakage current will now flow through R_B . Once the forward-bias voltage of the base emitter diode is more than V_γ , a large current flows through the collector and the corresponding breakdown voltage is $V_{CEO(\max)}$. Breakdown occurs when V_{CE} is greater than $V_{CEO(\max)}$. When the threshold voltage V_γ is reached, at that instant the collector current is $M_n I_{CO}$. Thus, at breakdown the current through R_B is $M_n I_{CO}$.

$$M_n I_{CO} R_B = V_\gamma \quad (6.60)$$

We have from Eq. (6.54):

$$h_{FB} = \frac{1}{M_n} \quad (6.61)$$

Using Eqs. (6.55) and (6.57) we can write $V_{CER(\max)}$ as:

$$V_{CER(\max)} = V_{CBO(\max)} \sqrt[n]{1 - h_{FB}} \quad (6.64)$$

Using Eq. (6.63):

$$V_{CER(\max)} = V_{CBO(\max)} \sqrt[n]{1 - \frac{I_{C0}R_B}{V_\gamma}} \quad (6.65)$$

Equation (6.65) is valid only when R_B is not too large. If $R_B = 0$, $V_{CER(\max)}$ is designated as $V_{CES(\max)}$. From Eq. (6.65),

$$V_{CES(\max)} = V_{CBO(\max)} \quad (6.66)$$

Now let us consider that V_{BB} is added in series with R_B as shown in Fig. 6.32. The breakdown voltage may be increased by reverse-biasing the base emitter diode by V_{BB} . When breakdown occurs, let us also consider the base spreading resistance $r_{bb'}$.

The cross sectional area in the base is very narrow and its ohmic resistance is large. The dc ohmic base resistance, called $r_{bb'}$, is the base spreading resistance and is the resistance offered to the recombination current. It is typically a few hundred ohms and is practically less than $1 \text{ k}\Omega$.

Using the circuit shown in Fig. 6.33,

$$M_h I_{C0}(R_B + r_{bb'}) = V_\gamma + V_{BB} \quad (6.67)$$

Writing for the breakdown voltage, in general for a given reverse-bias voltage V_{BB} , using the Eq. (6.65) we have,

$$V_{CEX(\max)} = V_{CBO(\max)} \sqrt[n]{1 - \frac{I_{C0}(r_{bb'} + R_B)}{V_\gamma + V_{BB}}} \quad (6.68)$$

Now let us obtain the relationship between I_C and V_{CE} , extending into breakdown region for the various conditions discussed (see Fig. 6.34) viz:

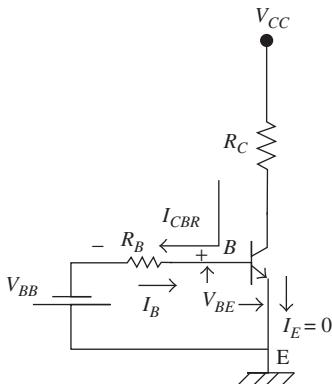


FIGURE 6.32 Reverse-biasing the emitter diode by V_{BB} to increase the breakdown voltage

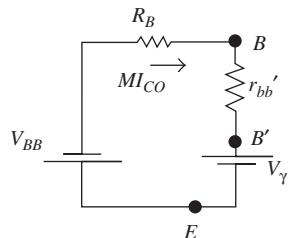


FIGURE 6.33 Considering $r_{bb'}$ when breakdown occurs

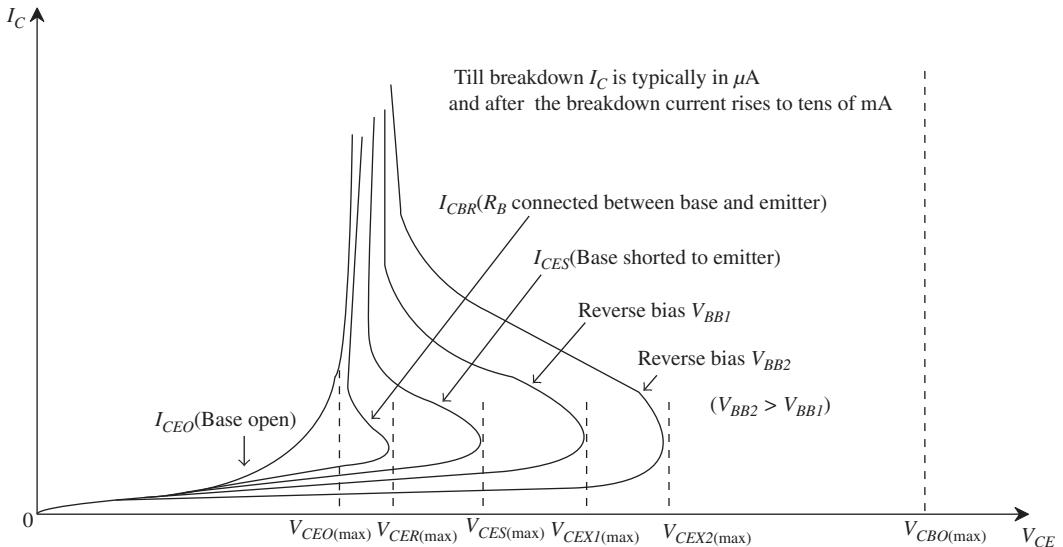


FIGURE 6.34 I_C vs. V_{CE} extended into breakdown region for different conditions

- When the base is open circuited ($I_C = I_{CEO}$)
- When R_B is connected between the base and emitter
- When R_B is connected with a reverse-bias voltage V_{BB} .

From Fig. 6.34, it is apparent that breakdown occurs at $V_{CEO(\max)}$ with base lead open at the point, the current rises abruptly. $V_{CEO(\max)}$ is called the sustaining voltage. When R_B is connected between the base and emitter, the breakdown occurs at a larger voltage $V_{CER(\max)}$. After breakdown the voltage returns to the sustaining voltage. If $R_B = 0$, breakdown occurs at a slightly larger voltage. Further, we also see from the characteristics that if the emitter diode is reverse-biased, the breakdown occurs at a still larger voltage. The larger is the reverse-bias voltage, the larger is the breakdown voltage. These characteristics explain the possible breakdown voltages for different conditions on the emitter diode, so that at these prohibited voltages the transistor is not operated. The currents for all the possible connections (except for I_{CEO}) give two values for the same voltage. Also, once the breakdown occurs current in the transistor increases with decreasing voltage, which means that the transistor exhibits negative resistance characteristic. The transistor when used in the breakdown region is called an avalanche transistor.

From Eq. (6.59) we see that $V_{CEO(\max)}$ is dependent on h_{FE} which in turn depends on the collector current I_C . DC current gain is the ratio of I_C/I_B at an operating point and is designated as h_{FE} or β_{dc} . The parameter h_{FE} is useful in determining whether a transistor is in saturation or not and it varies with collector current I_C (see Fig. 6.30). Typically h_{FE} varies as shown in Fig. 6.35 which is called current gain characteristic.

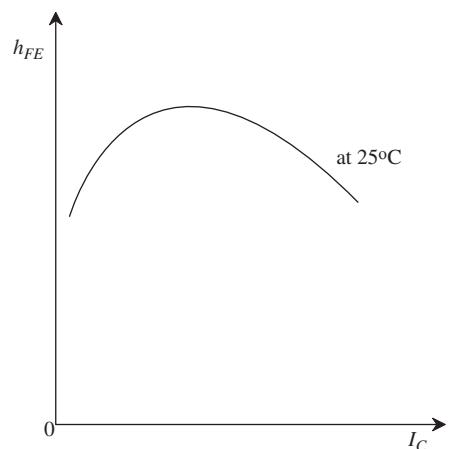


FIGURE 6.35 Current gain curve

6.6 THE SATURATION PARAMETERS OF A TRANSISTOR AND THEIR VARIATION WITH TEMPERATURE

The output characteristics of *n*-*p*-*n* transistor having $P_T = 250$ mW at room temperature in the CE configuration are given in Fig. 6.36. The dc load line for $R_L = 400 \Omega$ is superimposed on the characteristics. However, from the characteristics in Fig. 6.36 the saturation voltage $V_{CE(sat)}$ can not be found as its value is typically a fraction of a volt (0.1 V for Ge and 0.2 V for Si). A transistor is said to be in saturation when the emitter and collector diodes are forward-biased.

$$R_L = 400 \Omega, V_{CC} = 10 \text{ V}$$

To draw the dc load line:

$$I_{C(sat)} = \frac{10\text{V}}{400 \Omega} = 25 \text{ mA}$$

$$V_{CE(\text{cut-off})} = V_{CC} = 10 \text{ V}$$

To be able to read $V_{CE(sat)}$, the characteristics in the voltage range 0 to 0.5 V are expanded and the dc load line for $R_L = 400 \Omega$ is again superimposed, as shown in Fig. 6.37(a). The region [see Fig. 6.37(b)] around $I_B = 0.175$ mA is expanded to see the variation in I_C for larger values of I_B as shown as the dotted region in Fig. 6.37(a). It is seen for $I_B > 0.175$ mA, that there is no appreciable change in the collector current for a change in the base current as shown in Fig. 6.37(b), which indicates that the transistor is driven into saturation. Again from these characteristics we see that for $I_B = 0.175$ mA, $V_{CE(sat)} = 250$ mV and for $I_B = 0.35$ mA, $V_{CE(sat)} = 125$ mV. This variation explains that, the larger is the value of I_B , the smaller is the value of $V_{CE(sat)}$. At a given operating point, the ratio of $V_{CE(sat)}/I_C$ is called the saturation resistance R_{CS} . R_{CS} at the point Q is

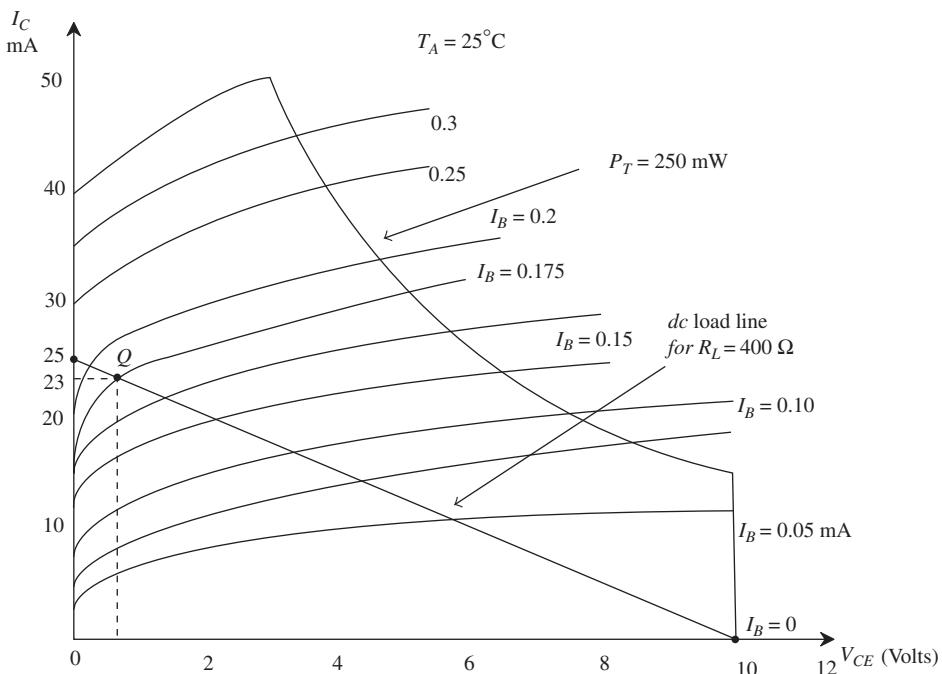


FIGURE 6.36 Typical output characteristics of an *n*-*p*-*n* transistor in the CE mode

$$R_{CS} = \frac{V_{CE(\text{sat})}}{I_C} = \frac{250 \text{ mV}}{23 \text{ mA}} = 10.87 \Omega.$$

From the plots shown in Fig. 6.37(a) and (b) we infer that I_C varies by larger amounts for smaller values of I_B and by smaller amounts for larger values of I_B , indicating that saturation has been reached and there will be no further increase in the collector current when the base current is increased. Also, we see that for smaller values of I_B , $V_{CE(\text{sat})}$ is larger and is smaller for larger values of I_B .

The above discussion essentially focuses on the dependence of $V_{CE(\text{sat})}$ and I_C on I_B . We conclude from the above discussion that variation in $V_{CE(\text{sat})}$ is dependent on I_B . If I_B is large, $V_{CE(\text{sat})}$ is small and vice-versa. Similarly, as I_B tends to become larger the variation in I_C becomes smaller. For smaller values of I_B , the variation in I_C is relatively large.

Figure 6.38, gives the variation of $V_{BE(\text{sat})}$ as a function of I_C/I_B , keeping I_C constant and varying I_B . These plots, which are normally given in the data sheets, tell us that $V_{BE(\text{sat})}$ is larger for smaller I_C/I_B ratio, for a given I_C and decreases with increasing ratio of I_C/I_B .

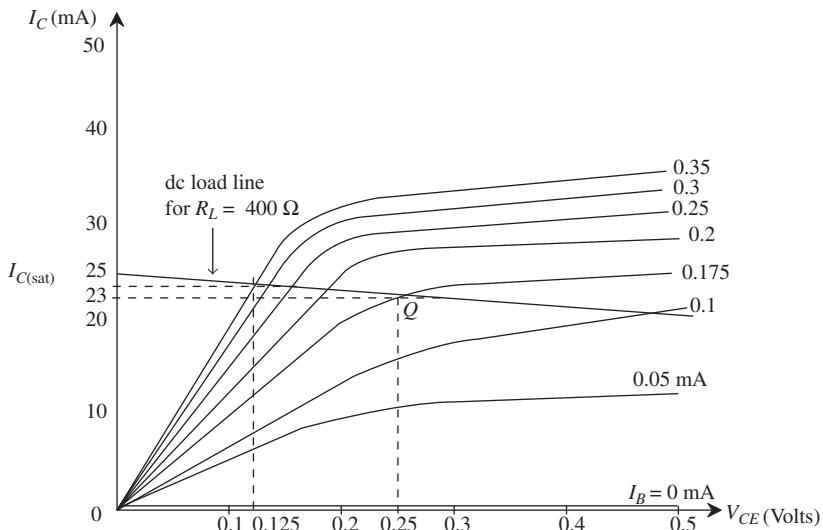


FIGURE 6.37(a) Expanded characteristics from 0 to 0.5 V

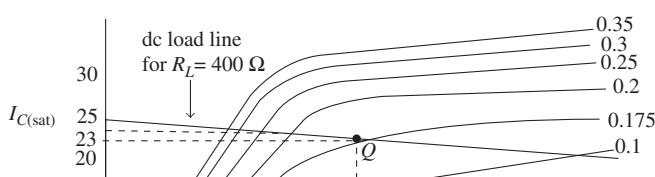
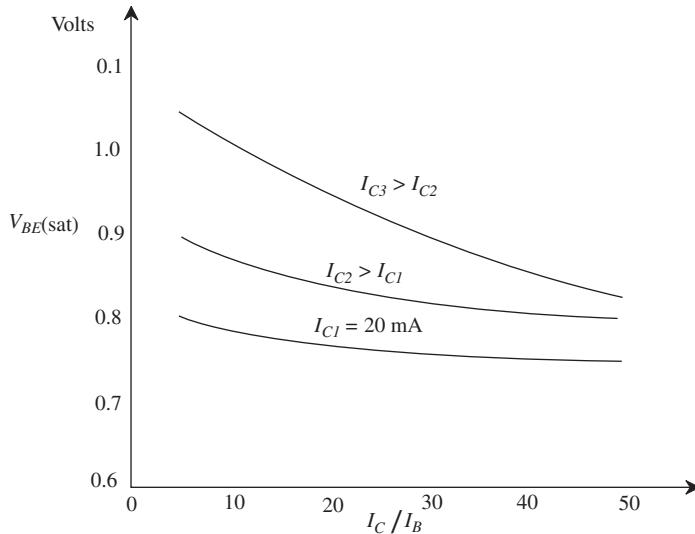
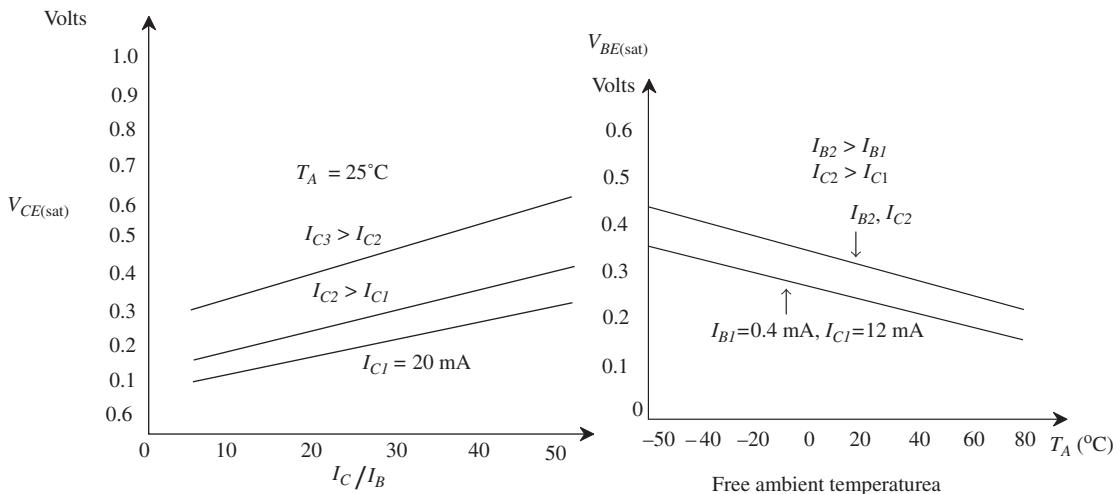


FIGURE 6.37(b) Expanded characteristic in the dotted region in Fig. 6.37(a)

FIGURE 6.38 The variation of $V_{BE(sat)}$ as a function of I_C/I_B with I_C as a parameter

Some data sheets specify R_{CS} for a few values of I_B . Sometimes data sheets specify the value of R_{CS} by the plot that gives the variation of $V_{CE(sat)}$ as a function of I_C/I_B for various values of I_C . A typical plot is shown in Fig. 6.39.

$V_{BE(sat)}$ varies with temperature and has a typical temperature sensitivity in the range of -1.5 to -200 $mV/^\circ C$. Variation of $V_{BE(sat)}$ with temperature is presented in Fig. 6.40. The variation of $V_{CE(sat)}$ as a function of temperature with I_B and I_C as parameters is shown in Fig. 6.41.

FIGURE 6.39 The variation of $V_{CE(sat)}$ with of I_C/I_B for I_C as a parameterFIGURE 6.40 The variation of $V_{BE(sat)}$ as a function of temperature with I_B and I_C as parameters

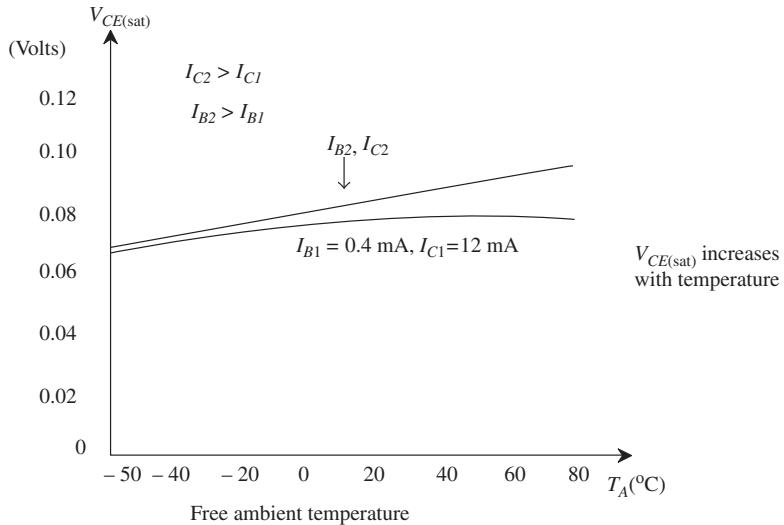


FIGURE 6.41 The variation of $V_{CE(sat)}$ as a function of temperature with I_B and I_C as parameters

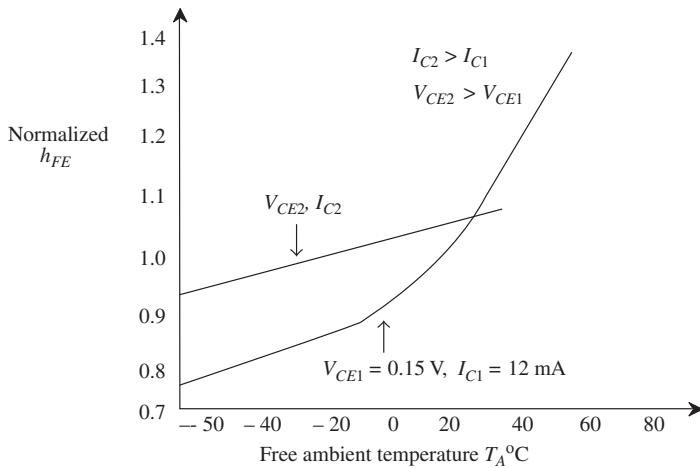


FIGURE 6.42 Variation of normalized h_{FE} as a function of temperature with I_C as parameter

Variation of normalized h_{FE} (h_{FE} at a given temperature divided by h_{FE} at 25°C) as a function of temperature with I_C as a parameter is shown in Fig. 6.42. This indicates that h_{FE} varies by larger amounts with temperature at smaller values of I_C . For larger values of I_C , h_{FE} is insensitive to temperature variations.

6.7 LATCHING IN A TRANSISTOR SWITCH

The transistor switch is driven into saturation, when ON and into cut-off when OFF, so that the operating point shifts from one extremity to the other as shown in Fig. 6.43.

Through the application of proper signal, the transistor switch is driven into saturation (point S), the intersection of the dc load line and the output characteristic for $I_B = I_{B(\text{sat})}$. Now by the application of a signal of opposite polarity, the switch can be driven into the OFF state (point O) and the intersection of the dc load

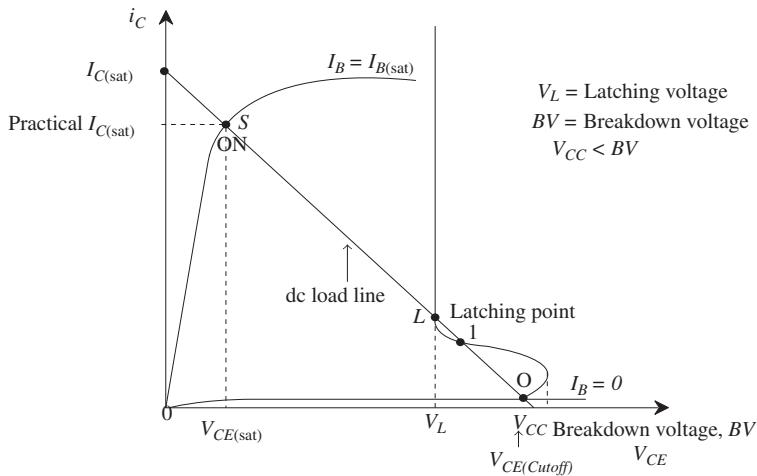


FIGURE 6.43 Latching in a transistor switch

line and the output characteristic for $I_B = 0$. However, when breakdown occurs, the sustaining voltage is the latching voltage V_L . When the device switches from ON to OFF, the operating point is expected to move along the load line from S to O. But the dc load line cuts the characteristic at three points, O, S and L. This prevents the operation from shifting to O (corresponding to V_{CC}) and the operating point will terminate at L which is the point of intersection of the breakdown characteristic with the load line and is called latching point. It is the point at which the voltage is called the latching voltage V_L . If initially the switch is in the OFF state (point O) and is driven into the ON state the operation shifts from O to S. However, when switched from ON to OFF, the operation will not terminate at O but will terminate at L. This is similar to a latch on a door. The shift in the operating point is restricted in one direction but not in the other direction.

6.8 TRANSISTOR SWITCHES WITH COMPLEX LOADS

Transistor switch may not necessarily have a resistive load always. Depending on the requirement, the load can either be inductive or capacitive. A transistor switch with inductive and capacitive loads is studied in the sections below.

6.8.1 Switches with Inductive Loads

Consider a transistor switch, shown in Fig. 6.44 for which the load is an inductor, L in parallel with R . As the dc resistance offered by L is negligible, to ensure that the current in the transistor does not abruptly rise to a very large value when the transistor is driven into saturation, a resistance R_C is added in series with the combination to limit the saturation current.

The gating signal v_i is a pulse train and the resultant output of the switch is shown in Fig. 6.45. When the gating signal is at V' , Q is OFF. The voltage at the collector is V_{CC} at $t = 0$. However, prior to this, the switch was ON and there was an inductor current I_L . Suddenly, when the switch is driven into the OFF state, the inductor current does not become zero but flows through R and decays exponentially with a time constant L/R . Consequently, a spike of magnitude $I_L R$ appears across the inductor. Thus, momentarily

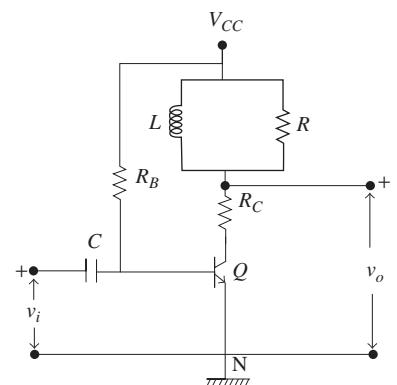


FIGURE 6.44 Switch with inductive load

there is a large reverse-bias voltage at the collector ($= V_{CC} + I_L R$)

with respect to the base. It must be ensured that this voltage is not more than the breakdown potential of the collector diode. For this, R must be small. If R is small, the spike takes a longer time to decay. Alternately, if R is large, time constant becomes small, which allows the spike to decay faster. However, at the same time the magnitude of the spike $= I_L R$ becomes larger. Therefore, one has to strike a compromise in choosing R . The equivalent circuits that will enable us determine the output, when Q is OFF and when Q is ON are shown in Figs.6.46 and 6.47.

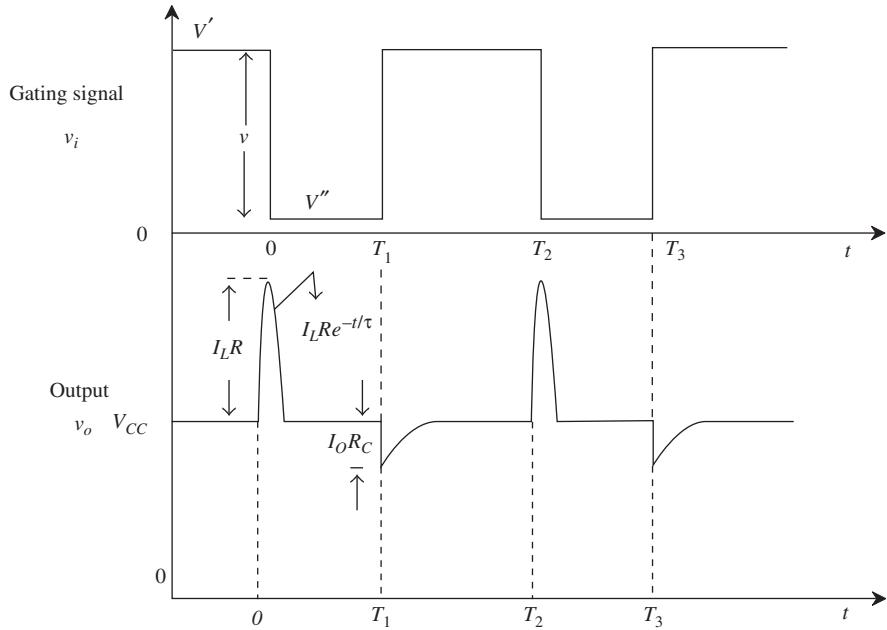


FIGURE 6.45 The input and output waveforms of a transistor switch with inductive load

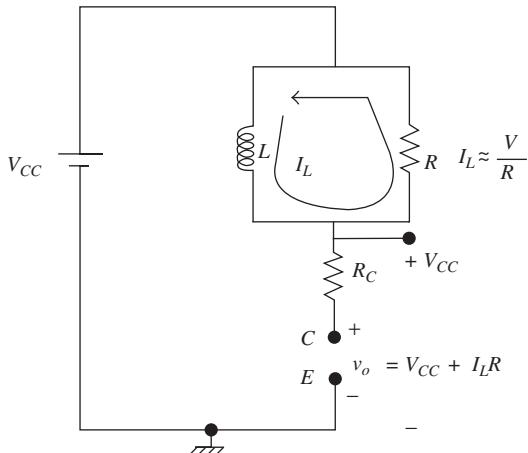


FIGURE 6.46 The equivalent circuit when Q is OFF

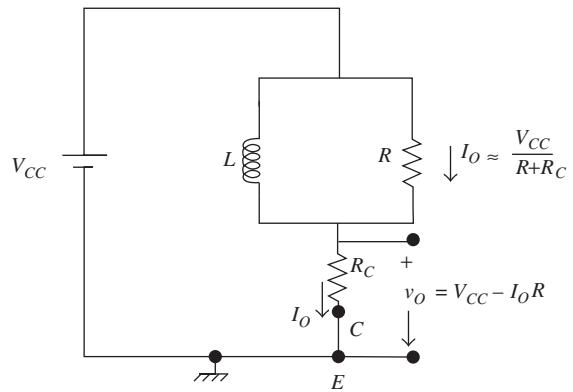


FIGURE 6.47 Equivalent circuit when Q is ON

Again, at $t = t_1$, Q goes ON and as the inductor will not allow any sudden change in the current, it behaves as an open circuit. If $I_O [= V_{CC}/(R_C + R)]$ is now the current through R_C , a negative spike of $I_O R_C$ is developed and it decays exponentially with a time constant L/R' where R' is the parallel combination of R and R_C . Now if a damper diode, D (in place of R) is connected across L , only positive spikes over and above V_{CC} are available at the output, as shown in Fig. 6.48. If the polarity of the diode is reversed, only negative spikes are available at the output (see Fig. 6.49).

6.8.2 Switches with Capacitive Loads

A transistor switch with capacitive load is shown in Fig. 6.50. Once again the gating signal is a pulse train and the waveforms are shown in Fig. 6.51.

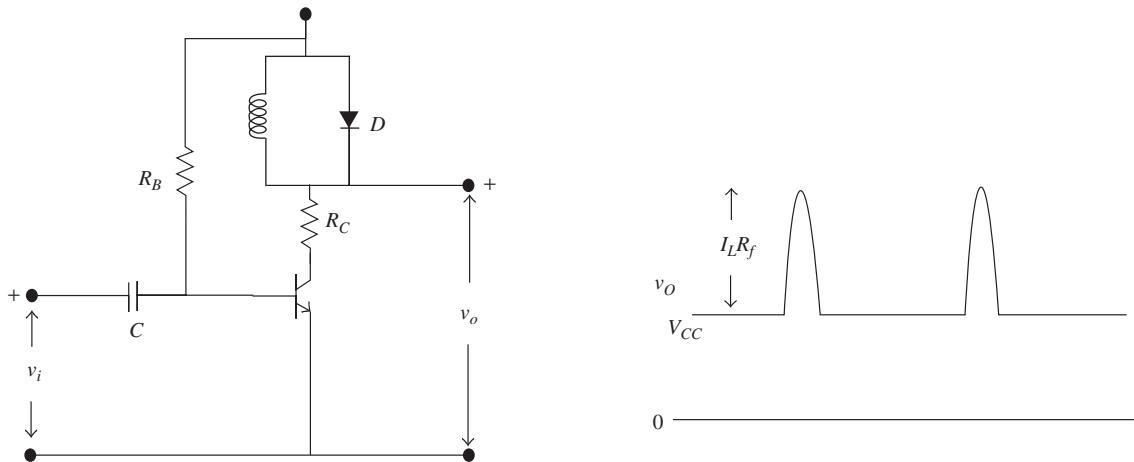


FIGURE 6.48 A switch with damping diode to derive positive spikes at the output

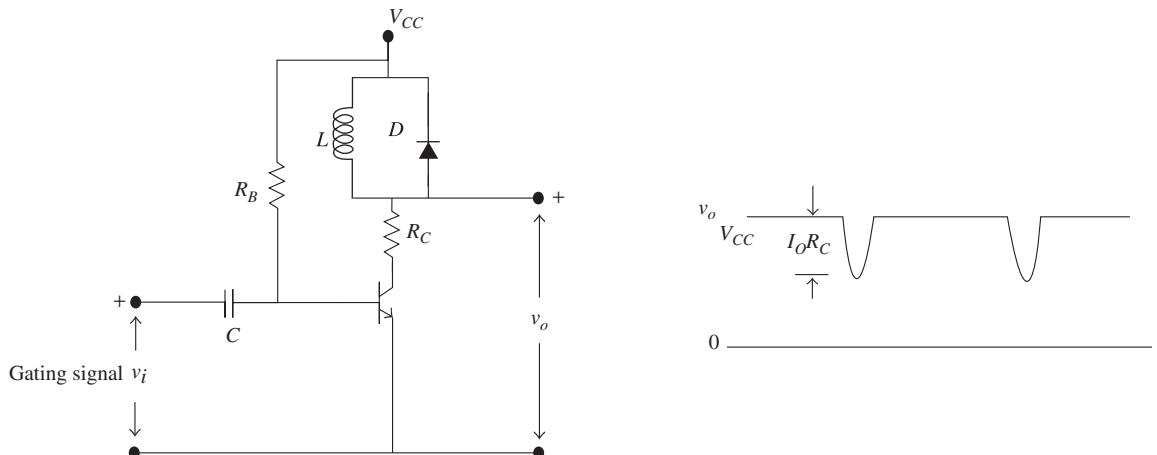


FIGURE 6.49 A switch with damping diode to derive negative spikes

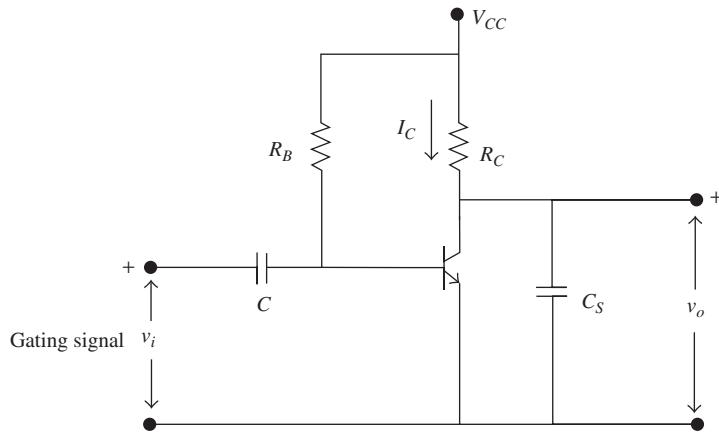


FIGURE 6.50 A transistor switch with capacitive load

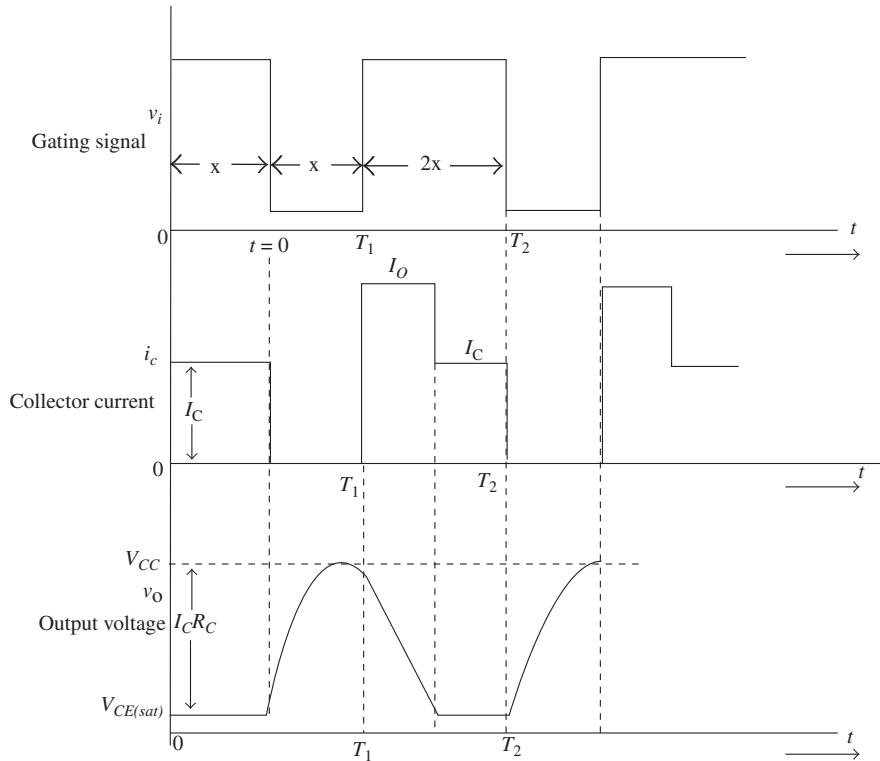


FIGURE 6.51 The waveforms of a transistor switch with capacitive load

The working of the circuit is explained as follows: Prior to $t = 0$. (i.e., at $t = 0-$), the input gating signal drives the transistor into saturation. As a result, the collector current is I_C . The voltage at the output $v_o = V_{CE(\text{sat})}$.

$$I_C = \frac{V_{CC} - V_{CE(\text{sat})}}{R_C}$$

However at $t = 0+$, the input drives the switch into the OFF state, the resultant equivalent circuit is as shown in Fig. 6.52.

When Q is turned OFF, the capacitor begins to charge to V_{CC} . The voltage v_o at $t = 0^+$ was $V_{CE(sat)}$ and now as the capacitor charges, the output rises exponentially and ultimately reaches V_{CC} . During this period $I_C = 0$ as Q is OFF. At $t = T_1$ the input forward-biases the emitter diode and Q is driven into active region resulting in a collector current $I_C = h_{FE}I_B = I_o$. Since Q is ON, the charge on C_S discharges exponentially as shown in Fig. 6.53.

The moment the voltage at the collector forward-biases the collector diode, Q goes into saturation, I_o falls to I_C and v_o returns to $V_{CE(sat)}$, as shown in Fig. 6.51. The output can be a near square wave by using collector catching diodes D_1 and D_2 , as shown in Fig. 6.54.

The output voltage of the transistor switch with capacitive load (with and without collector catching diodes) is as shown in Fig. 6.55. Diode D_1 conducts when the voltage at the collector is more than V_1 by V_γ . As a result, the output is V_1 . Similarly, diode D_2 conducts when the collector voltage is less than V_2 by V_γ . As a result, the output is V_2 . The output is a near square wave.

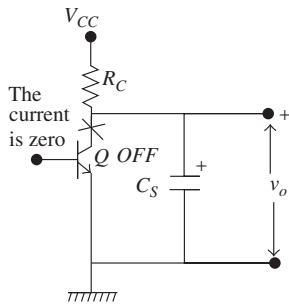


FIGURE 6.52 The output circuit when Q is OFF

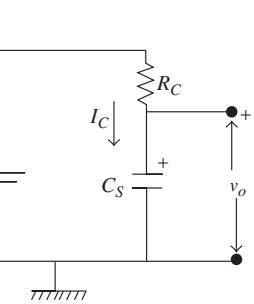


FIGURE 6.53 The equivalent circuit when Q is ON and is in active region

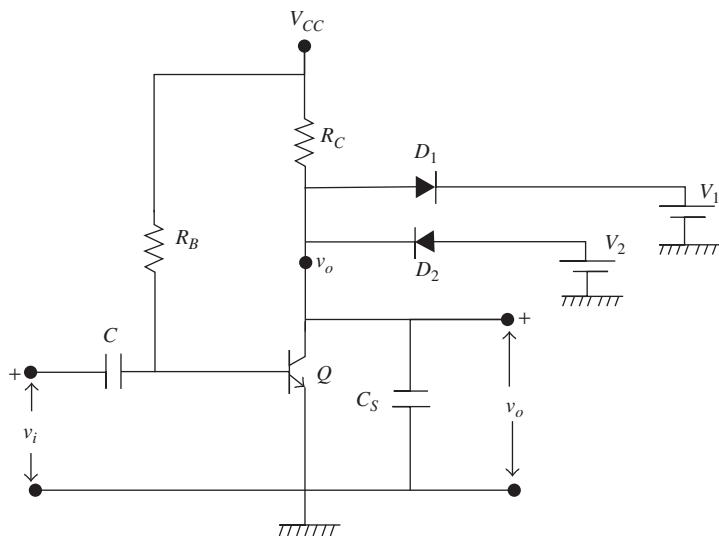
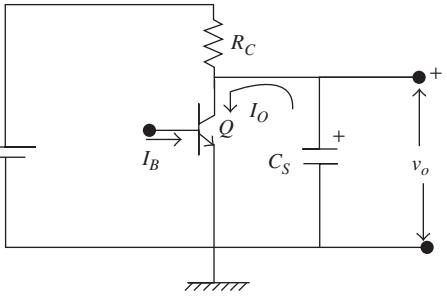


FIGURE 6.54 A transistor switch with capacitive load using collector catching diodes

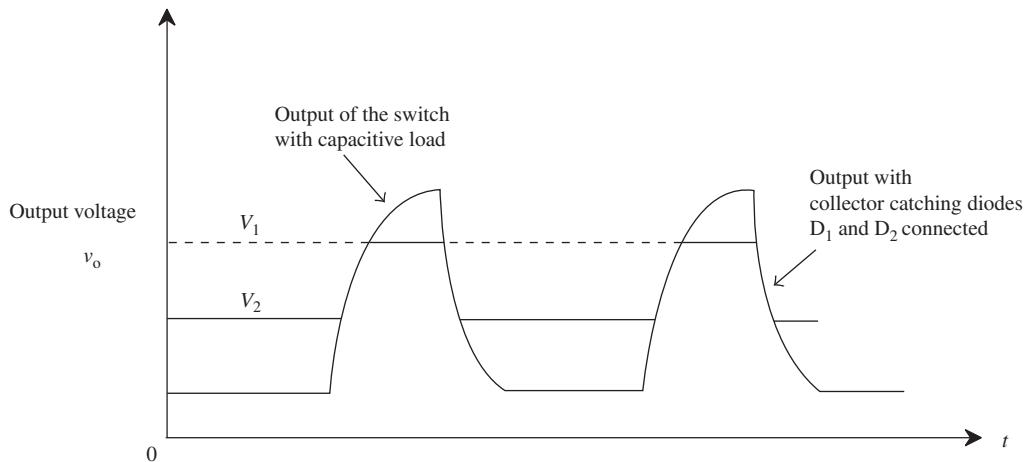


FIGURE 6.55 The output of the switch with collector catching diodes

S O L V E D P R O B L E M S

Example 6.14: For the given common-emitter circuit shown in Fig. 6.56, calculate the minimum base current to achieve saturation for (i) $R_C = 33\text{k}\Omega$ and (ii) $3.3\text{ k}\Omega$. Given $V_{CE(\text{sat})} = 0.3\text{ V}$ and $h_{FE} = 60$.

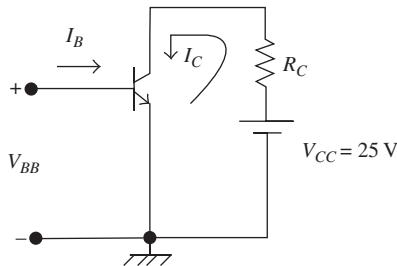


FIGURE 6.56 The given CE circuit

Solution:

$$V_{CC} = I_C R_C + V_{CE(\text{sat})} \quad I_C = \frac{V_{CC} - V_{CE(\text{sat})}}{R_C}$$

(i) $R_C = 33\text{k}\Omega$

$$I_C = \frac{25 - 0.3}{33K} = 0.748\text{ mA}$$

Given $h_{FE(\text{min})} = 60$

$$I_{B(\text{min})} = \frac{I_C}{h_{FE(\text{min})}} = \frac{0.748\text{ mA}}{60} = 0.012\text{ mA}$$

(ii) $R_C = 3.3\text{k}\Omega$

$$I_C = \frac{25 - 0.3}{3.3\text{ k}\Omega} = 7.48\text{ mA} \quad I_{B(\text{min})} = \frac{7.48\text{ mA}}{60} = 0.12\text{ mA}$$

Example 6.15: For the CE circuit shown in Fig. 6.57 with $V_{CC} = 15$ V and $R_C = 1.5 \text{ k}\Omega$, $V_{CE(\text{sat})} = 0.3$ V. Calculate (a) the transistor power dissipation in cut-off and saturation; and (b) Power dissipation in the load.

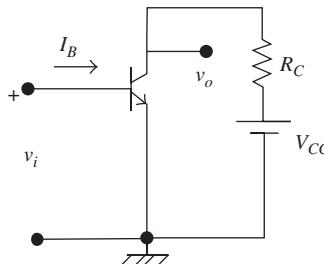


FIGURE 6.57 The given CE circuit

Solution:

When the transistor is in cut-off, the power dissipation is zero. When the transistor is in saturation, apply KVL to the output circuit:

$$V_{CC} = I_C R_C + V_{CE(\text{sat})} \quad 15 = I_C (1.5 \text{ k}\Omega) + 0.3 \text{ V} \quad I_C = \frac{15 - 0.3}{1.5 \text{ k}\Omega} = 9.8 \text{ mA}$$

$$\text{Power dissipation in the transistor} = V_{CE(\text{sat})} I_C = 0.3 \times 9.8 \times 10^{-3} = 2.94 \text{ mW.}$$

$$\text{Power dissipation in the load} = I_C^2 R_C = (9.8 \times 10^{-3})^2 \times 1.5 \times 10^3 = 144 \text{ mW}$$

SUMMARY

- Semiconductors and Zener diodes, transistors and FETs can be used as switches.
- A semiconductor diode switch is ON when forward-biased and OFF when reverse-biased.
- Avalanche and Zener diodes are operated as switches when reverse-biased. As long as the reverse-bias voltage is less than V_Z , the breakdown potential, the switch is OFF; and when the reverse-bias voltage is V_Z , it is a closed switch.
- Zener breakdown occurs due to the physical rupturing of covalent bonds on account of a strong electric field and avalanche breakdown is due to the avalanche multiplication of electron-hole pairs, aided by the external field.
- The reverse recovery time of a semiconductor diode is the time taken for the reverse current to fall to 10 per cent of its forward current value when the device is suddenly switched from the ON state into the OFF state.
- The breakdown voltages of avalanche and Zener diodes are temperature dependent. For a Zener diode, the breakdown voltage decreases with increase in temperature (negative temperature co-efficient) whereas for an avalanche diode, the breakdown voltage increases with temperature (positive temperature co-efficient).
- For a current step of a small value, the diode is represented as a combination of resistance and capacitance.
- For a current step of a larger magnitude, the diode is represented as a combination of resistance and inductance.
- A transistor switch is said to be ON (saturation) when both the collector and emitter diodes are forward-biased.
- A transistor switch is said to be OFF (cut-off) when both the collector and emitter diodes are reverse-biased.

- Rise time is the time taken for the collector current to rise from 10 per cent of its final value to 90 per cent of its final value.
- Fall time is the time taken for the collector current to fall from 90 per cent of its initial value to 10 per cent of its initial value.
- The sum of delay time and rise time is called the turn-on time of the transistor.
- The sum of storage time and fall-time is called the turn-off time of the transistor.
- A commutating condenser can be used to reduce turn-on and turn-off times of a transistor.
- h_{FE} of a transistor is a function of temperature and collector current.
- The transistor can be used as a latch.
- To reduce the turn-off time of a transistor, it is preferable to reverse-bias the collector diode by a small voltage.

MULTIPLE CHOICE QUESTIONS

- (1) A diode when forward-biased behaves as an:
 - Open switch
 - Closed switch
 - Toggle switch
 - None of the above
- (2) A diode when reverse-biased behaves as an:
 - Open switch
 - Closed switch
 - Toggle switch
 - None of the above
- (3) A transistor switch is said to be in the OFF state when the:
 - Collector and emitter diodes are reverse-biased
 - Collector diode is reverse-biased and the emitter diode is forward-biased
 - Collector and emitter diodes are forward-biased
 - Collector diode is forward-biased and the emitter diode is reverse-biased
- (4) A transistor switch acts as a perfectly closed switch when operated in the:
 - Cut-off region
 - Saturation region
 - Active region
 - None of above
- (5) The turn-on time of a transistor is given as:
 - $t_d + t_r$
 - $t_r + t_f$
 - $t_s + t_f$
 - $t_r + t_s$
- (6) The turn-off time of a transistor is given as:
 - $t_d + t_r$
 - $t_r + t_f$
 - $t_s + t_f$
 - $t_r + t_s$

SHORT ANSWER QUESTIONS

- (1) Briefly explain how a diode can be used as a switch.
- (2) What is meant by the reverse recovery time of a diode?
- (3) Distinguish between avalanche and Zener breakdowns.
- (4) Define the switching times of a diode.
- (5) A transistor is required to be operated in the active region. How do you bias the device?
- (6) A transistor is required to be operated in the cut-off region. How do you bias the device?
- (7) A transistor is required to be operated in the saturation region. How do you bias the device?
- (8) Define the switching times of a transistor.
- (9) A Zener diode has a breakdown potential $V_Z = 6.8$ V at 25°C . Calculate V_Z at 75°C if $\alpha_Z = -0.1$ per cent/ $^\circ\text{C}$.
- (10) How does a commutating condenser improve the switching speed of a transistor switch?
- (11) Briefly discuss the influence of breakdown voltages on the choice of supply voltage in a transistor switch.
- (12) What do you understand by latching in a transistor switch?
- (13) What is a non-saturating transistor switch?

LONG ANSWER QUESTIONS

- (1) Explain with the help of suitable waveforms the switching times of a diode switch. Derive the expression for reverse recovery time.
- (2) Explain with the help of neat circuit diagrams and waveforms, the method of improving the switching speed of a transistor switch by using a commutating condenser.
- (3) Derive the expression for the rise time of a transistor switch.
- (4) Derive the expression for the fall time of a transistor switch.
- (5) Discuss the effect of temperature on the saturation parameters of the transistor.
- (6) Explain what you understand by latching in a transistor switch.
- (7) Write short notes on:
 - i. A transistor switch with inductive load,
 - ii. A transistor switch with capacitive load, and
 - iii. A non-saturating transistor switch.

UNSOLVED PROBLEMS

- (1) Calculate the output levels for the inputs 0 and -5 V to the circuit shown in Fig. 6p.1 and verify that the circuit is an inverter. Find the minimum value of h_{FE} required. Neglect the junction saturation voltages. Assume ideal diode.
- (2) For a common-emitter circuit $V_{CC} = 15\text{ V}$, $R_C = 1.5\text{k}\Omega$ and $I_B = 0.3\text{ mA}$.
 - i. Determine the value of h_{FE} for saturation to occur.
 - ii. Will the transistor saturate if $R_C = 250\text{ }\Omega$?
- (3) For a transistor, $V_{CB} = 50\text{ V}$, $M_h = 10$, $n = 8$, $h_{FE} = 100$. Calculate (a) $V_{CBO}(\text{max})$ and (b) $V_{CEO}(\text{max})$.

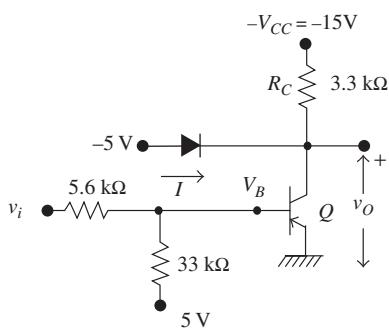


FIGURE 6p.1 The given transistor switch

- (4) Design the CE transistor switch shown in Fig. 6p.4, operating with $V_{CC} = 20\text{ V}$ and $-V_{BB} = -20\text{ V}$. The transistor is expected to operate at $I_{C(\text{sat})} = 5\text{ mA}$, $h_{FE} = 25$, $V_{CE}(\text{sat}) = 0$, $V_{BE}(\text{sat}) = 0$ and $R_2 = 4R_1$. Determine the values of resistors R_C , R_1 and R_2 .

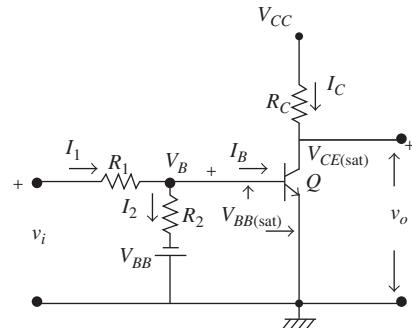


FIGURE 6p.4 The given CE transistor switch

- (5) Design a CE transistor switch shown in Fig. 6p.5, operating with $V_{CC} = 25\text{ V}$ and $-V_{BB} = -25\text{ V}$. The transistor is expected to operate at $I_{C(\text{sat})} = 4\text{ mA}$, $I_{B(\text{sat})} = 0.3\text{ mA}$, $h_{FE} = 25$, $V_{CE}(\text{sat}) = 0$, $V_{BE}(\text{sat}) = 0$ and $R_2 = 2R_1$. Determine the values of resistors R_C , R_1 and R_2 . v_i varies from 0 to V_{CC} .

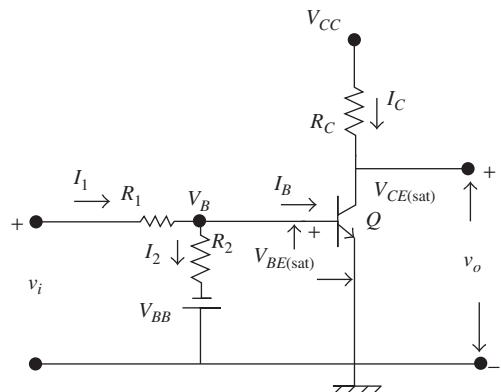


FIGURE 6p.5 The given CE transistor switch

- (6) For the circuit in Fig. 6p.6, the input is a pulse of 16 V and duration $T = 5 \mu s$, f_T is 10 MHz and $f_I = 1$ MHz, $\alpha_{NO} = 0.99$ and $\alpha_{NI} = 0.5$, $C_{TC} = 5 \text{ pF}$ and $h_{FE} = 100$, $V_{BE(\text{sat})} = V_{CE(\text{sat})} = 0$. Calculate (a) the turn-on time (b) turn-off time and (c) the time for which the switch is ON.

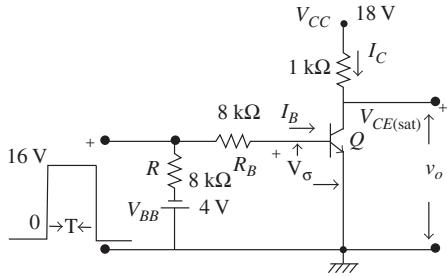


FIGURE 6p.6 The given transistor switch

- (7) For the circuit shown in Fig. 6p.7, the input is a pulse of 15 V and duration $T = 1 \mu s$, f_T is 5 MHz and $f_I = 1$

MHz, $\alpha_{NO} = 0.99$ and $\alpha_{NI} = 0.5$, $C_{TC} = 5 \text{ pF}$ and $h_{FE} = 100$. Calculate (a) the turn-on time (b) turn-off time and (c) the time for which the switch is ON.

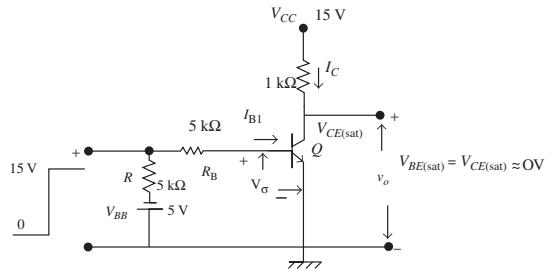


FIGURE 6p.7 The given transistor switch

- (8) For a transistor, $V_{CB} = 40 \text{ V}$, $M_n = 5$, $n = 4$, $h_{FE} = 100$. Calculate (a) $V_{CBO(\text{max})}$ and (b) $V_{CEO(\text{max})}$.

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CHAPTER 7

Astable Multivibrators

LEARNING OBJECTIVES

After reading this chapter, you will be able to:

- Describe the working of collector-coupled and emitter-coupled astable multivibrators
 - Derive the expressions for the frequency of oscillations of astable multivibrators
 - Plot the waveforms at various points in the circuit
 - Design an astable multivibrator
 - Use an astable multivibrator for applications such as voltage to frequency converter and frequency modulator
-

7.1 INTRODUCTION

Multivibrators are switching circuits that employ positive feedback by cross-coupling the output of one stage to the input of the other stage, such that if one device is ON, the other is OFF. The interchange of states is possible either by the use of external pulses or by internal capacitive coupling. These circuits are used either to generate waveforms of a desired nature or to store binary information. Multivibrators are of three types—astable, monostable and bistable. An astable multivibrator is basically a square-wave generator. A monostable multivibrator generates a gated output (pulse) of a desired duration. A bistable multivibrator stores binary bits. In this chapter, we focus on astable multivibrators.

A transistor Q_1 or Q_2 is said to be in the stable state, if it is either ON or OFF permanently. If the state of the device, say Q_1 , changes from ON to OFF, and automatically returns to the ON state after a time duration, the device is said to be in the quasi-stable state for this specified time interval. The devices in this multivibrator will not remain in any one state (ON or OFF) forever. The change of state in the device occurs automatically after a finite time interval, depending on the circuit components employed. Hence, this circuit has two quasi-stable states.

In an astable multivibrator, if Q_1 is ON, then Q_2 is OFF; and they will remain in this state for a limited time duration, after which Q_1 automatically switches into the OFF state and Q_2 into the ON state and so on. The output of the circuit is a square wave with two time periods, T_1 and T_2 . If $T_1 = T_2 = T/2$ the circuit is a symmetric astable multivibrator. If $T_1 \neq T_2$, it is called an un-symmetric astable multivibrator. The main application of an astable multivibrator is as a clock in digital circuits.

The astable multivibrator is essentially a square-wave generator (oscillator). We consider two circuits: the collector-coupled astable multivibrator and the emitter-coupled astable multivibrator in the following sections.

7.2 COLLECTOR-COUPLED ASTABLE MULTIVIBRATORS

A collector-coupled astable multivibrator is shown in Fig. 7.1. Here, there is a cross-coupling from the second collector to the first base and also a cross-coupling from the first collector to the second base. This means that the output of one device is the input for the other. While analysing the functioning of this circuit, it is assumed that the circuit is an oscillator; and working backwards, we can justify that it does indeed oscillate.

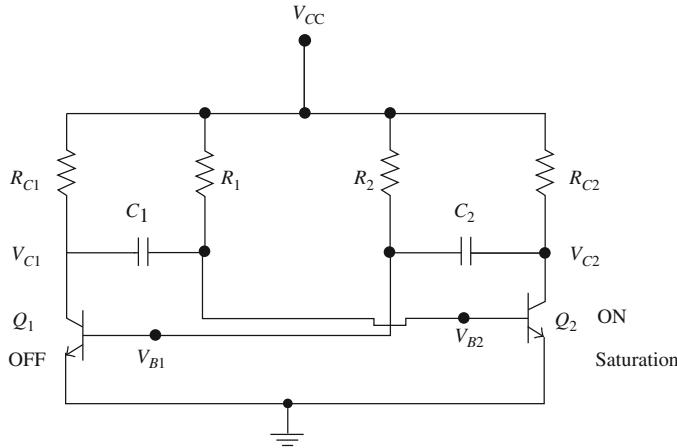
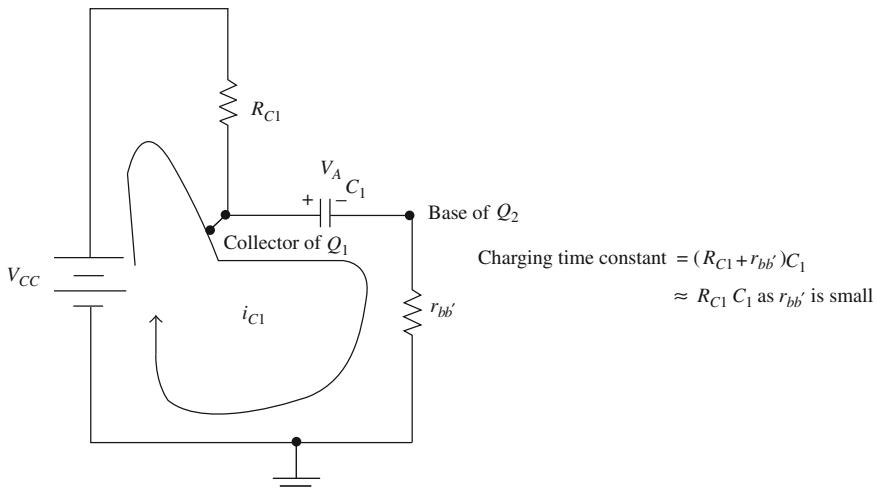


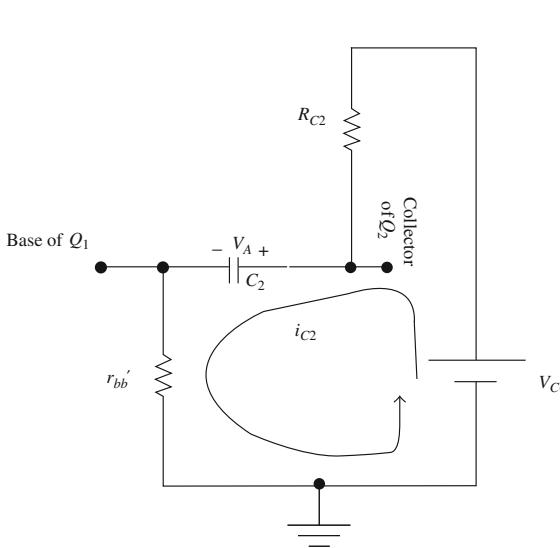
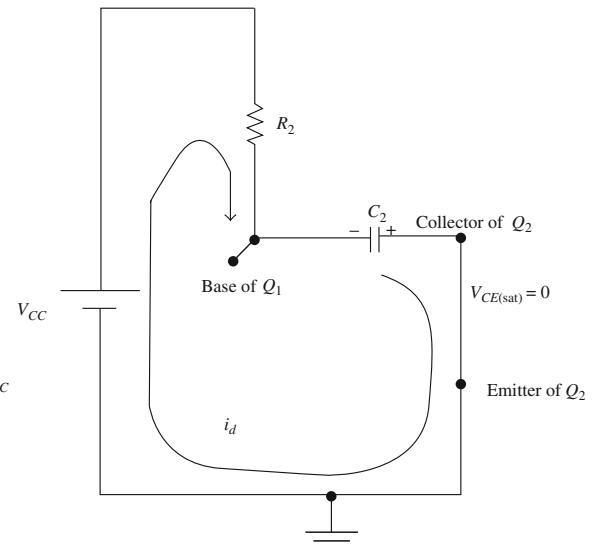
FIGURE 7.1 A collector-coupled astable multivibrator

Let us assume that at the given instant of time Q_1 is OFF and Q_2 is ON and saturated. Then $V_{B2} = V_\sigma$, $V_{C2} = V_{CE(\text{sat})}$ and $V_{C1} = V_{CC}$. With Q_1 OFF and Q_2 ON, C_1 will try to charge to the supply voltage through the collector resistance R_{C1} and the small resistance of Q_2 ($\approx r_{bb'}$), as shown in Fig. 7.2.

However, prior to this condition, Q_2 must have been in the OFF state and Q_1 must have been in the ON state. As a result, C_2 must have been charged through R_{C2} and $r_{bb'}$ of Q_1 , as shown in Fig. 7.3.

When Q_2 suddenly switches from the OFF state into the ON state, the voltage between its collector and emitter terminals is V_{CE} (≈ 0 V). Hence, the collector of Q_2 is at ground potential, i.e., the positive end of the capacitor C_2 is at the ground potential and its negative terminal is connected to the base of Q_1 . As a large negative voltage is now coupled to the base of Q_1 , it is in the OFF state (see Fig. 7.4). However, Q_1 will not remain in the OFF state forever. Now, with Q_2 ON, the charge on the condenser C_2 discharges with a time constant $\tau_2 = R_2 C_2$.

FIGURE 7.2 The charging of the capacitor C_1

FIGURE 7.3 The charging of capacitor C_2 FIGURE 7.4 The discharge of C_2 through R_2

As a result, the voltage at the base of Q_1 goes on changing as a function of time. Once this voltage reaches V_γ , Q_1 starts drawing base current. Hence, there is a collector current. In turn, there is voltage drop across R_{C1} and the voltage at the collector of Q_1 falls. This voltage was earlier V_{CC} and now, it is smaller than V_{CC} . Therefore, the negative step at this collector is coupled to the base of Q_2 through C_1 . As the collector of Q_1 and the base of Q_2 are connected through C_1 and the capacitor will not allow any sudden changes in the voltage, the base of Q_2 undergoes changes that are identical to those that have taken place at the first collector. As a result, the base and collector current of Q_2 drop; so, the collector voltage rises. This positive step change is coupled to the base of Q_1 ; and thus, its base current increases further. And the collector current increases, the voltage at the collector of Q_1 falls still further. This step change is coupled to the base of Q_2 and this process is repeated. Thus, a regenerative action takes place and Q_2 switches to the OFF state and Q_1 goes into the ON state. Hence, the circuit oscillates. As long as the voltage at the base is V_σ , the voltage at the collector is $V_{CE(\text{sat})}$. Once the voltage at the base is negative, the device switches into the OFF state, giving rise to a voltage V_{CC} at its collector. The waveforms at the two bases and the two collectors are shown in Fig 7.5.

When a transistor, say Q_1 , switches from the ON state into the OFF state, its collector voltage is required to abruptly rise to V_{CC} . Consequently, the waveforms at the collectors should have sharp rising edges and flat tops. But when Q_1 goes into the OFF state and Q_2 into the ON, there is a charging current of the condenser C_1 which prevents the sudden rise of the voltage from V_{C1} to V_{CC} . Only when this charging current is zero does the collector voltage reach V_{CC} , as shown in Fig. 7.6. Hence, there is a rounding off of the rising edge of the pulse.

7.2.1 Calculation of the Frequency of an Astable Multivibrator

To calculate the frequency (f), the two time periods T_1 and T_2 are to be calculated. Then:

$$T = T_1 + T_2 \quad \text{and} \quad f = \frac{1}{T}$$

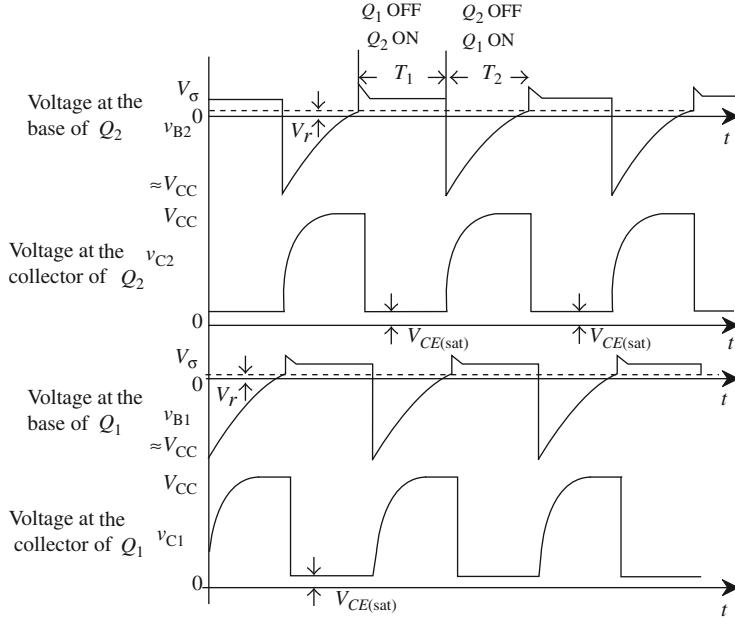


FIGURE 7.5 The waveforms of a collector-coupled astable multivibrator

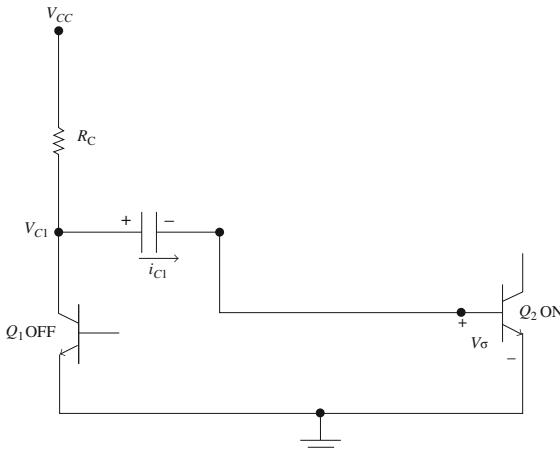
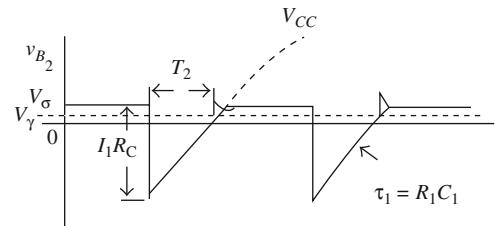
Calculation of the Time Period, T : To calculate T , we calculate T_1 and T_2 . Consider the waveform at the base of Q_2 , as shown in Fig. 7.7.

In general, the voltage variation at the base of Q_2 as a function of time is given by the relation:

$$v_{B2}(t) = v_f - (v_f - v_i)e^{-t/\tau} \quad (7.1)$$

Here, $v_f = V_{CC}$, $v_i = V_\sigma - I_1 R_C$ and the time constant, $\tau_1 = R_1 C_1$.

$$v_{B2}(t) = V_{CC} - (V_{CC} - V_\sigma + I_1 R_C) e^{-t/\tau_1} \quad (7.2)$$


 FIGURE 7.6 V_{C1} rises to V_{CC} only when $i_{C1} = 0$

 FIGURE 7.7 Voltage variation at the base of Q_2

But, at $t = T_2$, $v_{B2}(t) = V_\gamma$

$$\therefore V_\gamma = V_{CC} - (V_{CC} - V_\sigma + I_1 R_C) e^{-T_2/\tau_1}$$

Hence,

$$T_2 = \tau_1 \ln \frac{V_{CC} - V_\sigma + I_1 R_C}{V_{CC} - V_\gamma}. \quad (7.3)$$

Similarly,

$$T_1 = \tau_2 \ln \frac{V_{CC} - V_\sigma + I_2 R_C}{V_{CC} - V_\gamma}. \quad (7.4)$$

where, I_1 and I_2 are the currents in Q_1 and Q_2 when ON. However, here, in the expressions for T_1 and T_2 , the currents I_1 and I_2 are present (for all practical purposes these two currents are the same, if the devices have identical parameters).

A transistor can be said to be in the ON state when it is held in the active region or when it is driven into saturation. When the transistor is in the active region, its current (I_1 or I_2) cannot be maintained at a constant value unless negative feedback is employed to stabilize the current. As there is no such provision in the circuit of Fig. 7.1, I_1 and I_2 are not necessarily stable. Hence, T_1 and T_2 cannot be maintained as constant; and f , the frequency of oscillations is also not stable. To ensure that T_1 and T_2 remain constant, the ON device is preferably driven into saturation. Consider the expression for T_2 from Eq. (7.3):

$$T_2 = \tau_1 \ln \frac{V_{CC} - V_\sigma + I_1 R_C}{V_{CC} - V_\gamma}$$

If Q_1 , in the quasi-stable state, is in saturation, then:

$$I_1 R_C = V_{CC} - V_{CE(\text{sat})} \quad (7.5)$$

$$T_2 = \tau_1 \ln \frac{V_{CC} - V_\sigma + V_{CC} - V_{CE(\text{sat})}}{V_{CC} - V_\gamma} = \tau_1 \ln \frac{2V_{CC} - [V_\sigma + V_{CE(\text{sat})}]}{V_{CC} - V_\gamma}$$

$$T_2 = \tau_1 \ln 2 \times \frac{\left\{ V_{CC} - \frac{[V_\sigma + V_{CE(\text{sat})}]}{2} \right\}}{V_{CC} - V_\gamma}$$

$$\text{But, } \frac{V_\sigma + V_{CE(\text{sat})}}{2} \approx V_\gamma$$

Therefore,

$$T_2 = \tau_1 \ln 2 \frac{V_{CC} - V_\gamma}{V_{CC} - V_\gamma} = \tau_1 \ln 2 + \tau_1 \ln \frac{V_{CC} - V_\gamma}{V_{CC} - V_\gamma} = \tau_1 \ln 2 + \ln 1 = \tau_1 \ln 2 + 0.$$

$$T_2 = 0.69 \tau_1 \quad (7.6)$$

Similarly,

$$T_1 = 0.69 \tau_2 \quad (7.7)$$

T_1 and T_2 are now stable.

Therefore,

$$T = 0.69 (\tau_1 + \tau_2) \quad (7.8)$$

In a symmetric astable multivibrator, $\tau_1 = \tau_2 = \tau$

Therefore,

$$T = 1.4\tau \quad (7.9)$$

and

$$f = \frac{1}{1.4\tau} = \frac{0.7}{\tau} \text{ c/s} \quad (7.10)$$

If the ON device, in the quasi-stable state, is in the active region, then T_1 and T_2 are dependent of currents I_1 and I_2 , which, in the absence of feedback, are not stable. However, from Eqs. (7.6) and (7.7), it is evident that if the ON device is driven into saturation, T_1 and T_2 are independent of I_1 and I_2 ; and hence, will remain stable. We will now derive the condition that ensures that the ON device is saturated as shown in Fig. 7.8(a).

Writing the KVL equations of the base and collector loops, we have:

$$V_{CC} = I_{B2}R + V_\sigma = I_{C2}R_C + V_{CE(\text{sat})}$$

When Q_2 is in saturation, $V_\sigma \approx V_{CE(\text{sat})}$.

Therefore, $I_{B2}R = I_{C2}R_C$

$$R = \frac{I_{C2}}{I_{B2}}R_C = h_{FE}R_C$$

Hence, for the ON device to be in saturation, the following condition has to be satisfied:

$$R \leq h_{FE}R_C \quad (7.11)$$

Recovery Time. From Fig. 7.6, it is seen that when a device is switched into the OFF state, the collector voltage will not abruptly rise to V_{CC} because of a small charging current associated with the condenser. The time taken for this collector voltage to reach 90 per cent of the steady-state value (V_{CC}) is called the recovery time, as shown in Fig. 7.8(b). From the figure it is seen that:

Recovery time $t_{\text{rec}} = t_2 - t_1$

Recovery time

$$t_{\text{rec}} \approx 2.2 \tau' \quad (7.12)$$

where, $\tau' = \approx R_C C$

Therefore,

$$t_{\text{rec}} \approx 2.2 R_C C \quad (7.13)$$

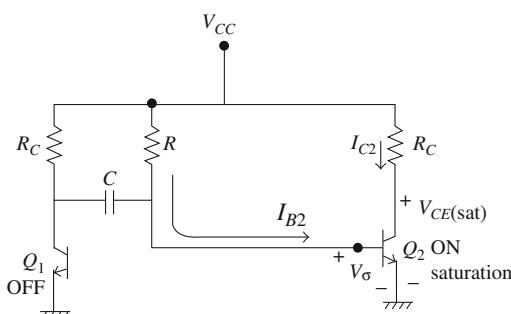


FIGURE 7.8(a) The ON transistor is in saturation

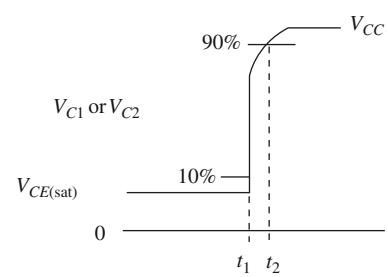


FIGURE 7.8(b) Recovery time

In a symmetric astable multivibrator: $R_1 = R_2 = R$ and $C_1 = C_2 = C$. Hence,

$$\frac{T}{2} = 0.69RC$$

$$\therefore \frac{t_{\text{rec}}}{T/2} = \frac{2.2RCC}{0.69RC} = 3.2 \frac{R_C}{R} \quad (7.14)$$

But, $R \leq h_{FE} R_C$ when the ON transistor is in saturation.

$$\text{Or } \frac{R_C}{R} \geq \frac{1}{h_{FE}}$$

$$\therefore \frac{t_{\text{rec}}}{T/2} \geq \frac{3.2}{h_{FE}} \quad (7.15)$$

As a specific example, if $h_{FE} = 20$,

$$\frac{t_{\text{rec}}}{T/2} = \frac{3.2}{20} \times 100\% = 16\%$$

Thus, the recovery time is 16 per cent of the half period $T/2$. If, alternately, $h_{FE} = 80$, the recovery time is 4 per cent. Thus, for the recovery time to be small, transistors with large h_{FE} may be employed.

Calculation of the Overshoot. When suddenly the transistor switches from the OFF state into the ON state, there could be a small overshoot at this base and at the collector of the transistor which switches from the ON state to the OFF state. To understand this, let us see an analogy. Assume that you are asked to come running and stop at a marked line. Now, due to inertia, instead of stopping at the dotted line you would over step it. Similarly, here the voltage at the base of the device which suddenly switches from the OFF state to the ON state will not just be V_σ , but slightly more. Hence, an overshoot is present at its base and similarly, at the other collector. At the end of the quasi-stable state, let Q_1 go into the OFF state and Q_2 into the ON state and then into saturation. The base-spreading resistance $r_{bb'}$ —the resistance seen between the external base lead and the internal base terminal—is the resistance offered to the recombination current and is accounted by the amount of overshoot. This is typically less than $1 k\Omega$, as shown in Fig. 7.9(a).

From Fig. 7.9(a):

$$I_{B2} = I'_{B2} + I'_R \quad (7.16)$$

$$\text{As } R \gg R_C, I'_R \ll I'_{B2} \quad (7.17)$$

Neglecting the current I'_R , when compared to I'_{B2} , the circuit reduces to that shown in Fig. 7.9(b).

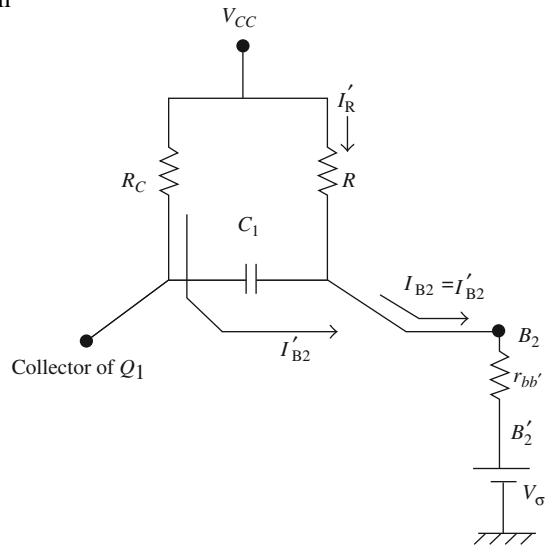


FIGURE 7.9(a) Q_2 at the end of the quasi-stable state

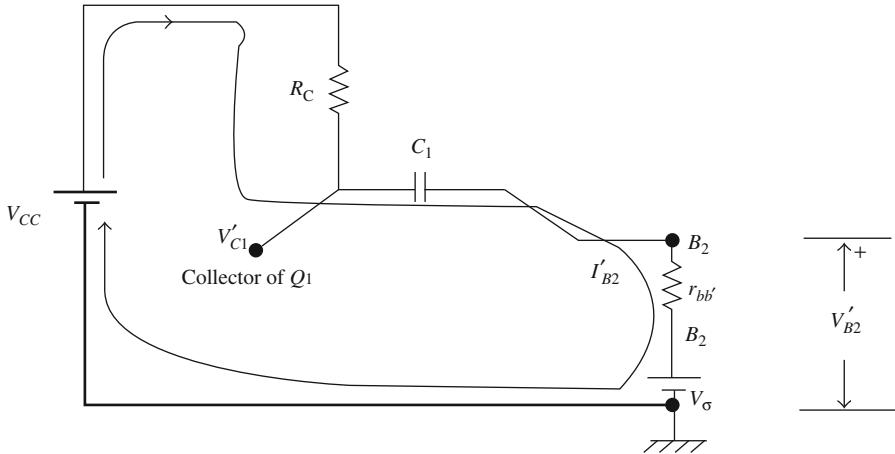


FIGURE 7.9(b) The simplified circuit of Fig. 7.9(a)

The voltages at B_2 and collector of Q_1 are:

$$V'_{B2} = I'_{B2} r_{bb'} + V_\sigma \quad (7.18)$$

$$V'_{C1} = V_{CC} - I'_{B2} R_C \quad (7.19)$$

The overshoot δ at the second base is the variation over and above V_γ .

$$\delta = V'_{B2} - V_\gamma$$

Using Eq. (7.18):

$$\delta = V'_{B2} - V_\gamma = I'_{B2} r_{bb'} + V_\sigma - V_\gamma \quad (7.20)$$

Similarly, the overshoot δ' at the first collector is the variation over and above $V_{CE(\text{sat})}$.

$$\delta' = V'_{C1} - V_{CE(\text{sat})}$$

Using Eq. (7.19):

$$\delta' = V_{CC} - I'_{B2} R_C - V_{CE(\text{sat})} \quad (7.21)$$

As the first collector and the second base are connected through a condenser C_1 which does not allow any sudden changes in voltage, changes, identical to those at the first collector, are required to take place at the second base.

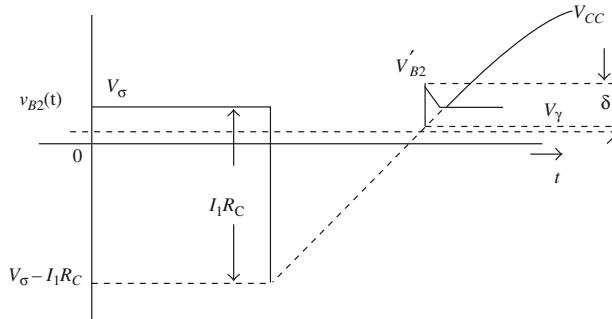
Hence, $\delta = \delta'$.

$$I'_{B2} r_{bb'} + V_\sigma - V_\gamma = V_{CC} - I'_{B2} R_C - V_{CE(\text{sat})}$$

$$I'_{B2} (r_{bb'} + R_C) = V_{CC} - V_{CE(\text{sat})} - V_\sigma + V_\gamma$$

$$I'_{B2} = \frac{V_{CC} - V_{CE(\text{sat})} - V_\sigma + V_\gamma}{r_{bb'} + R_C} \quad (7.22)$$

$$V'_{C1} = V_{CC} - I'_{B2} R_C \quad (7.23)$$

FIGURE 7.9(c) The overshoot at B_2

$$V'_{B2} = I'_{B2} r_{bb'} + V_\sigma \quad (7.24)$$

The overshoot at B_2 is shown in Fig. 7.9(c).

7.2.2 The Design of an Astable Multivibrator

Let us now try to design the astable multivibrator shown in Fig. 7.10.

We are now required to fix the component values of the astable multivibrator shown in Fig. 7.10.

For this to happen, we have to know $h_{FE(\min)}$, $I_{C(\text{sat})}$, $V_{CE(\text{sat})}$, $V_{BE(\text{sat})}$ and the frequency f at which it is expected to oscillate. The value of R_C is calculated as:

$$R_C = \frac{V_{CC} - V_{CE(\text{sat})}}{I_{C(\text{sat})}} \quad (7.25)$$

I_B (min) is now calculated as:

$$I_{B(\text{min})} = \frac{I_{C(\text{sat})}}{h_{FE(\min)}} \quad (7.26)$$

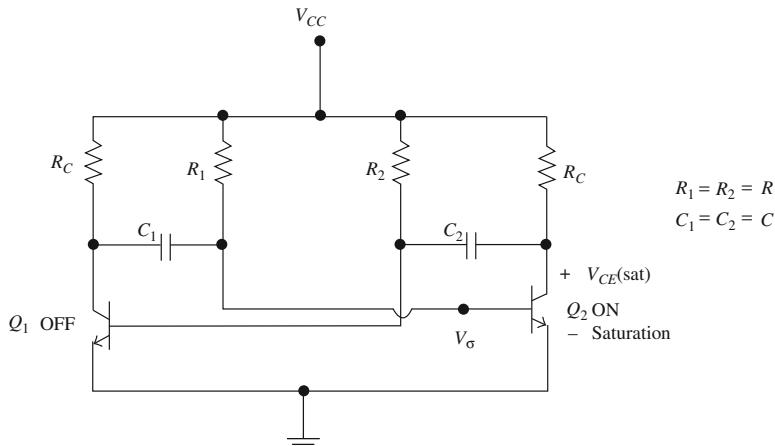


FIGURE 7.10 The design of an astable multivibrator

Now select:

$$I_{B(\text{sat})} = 1.5I_{B(\text{min})} \quad (7.27)$$

to ensure that the ON device is really in saturation:

$$R = \frac{V_{CC} - V_\sigma}{I_{B(\text{sat})}} \quad (7.28)$$

For the ON device to be in saturation, Eq. (7.11) needs to be satisfied. If this condition is satisfied, choose the value of R as obtained in Eq. (7.28); otherwise choose the value of R satisfying Eq. (7.11). For a symmetric astable multivibrator, $f = 0.7/RC$. Using this relation, the value of C can be fixed. Example 7.1 further elucidates the point.

EXAMPLE

Example 7.1: Design an astable multivibrator, assuming that silicon devices with $h_{FE(\text{min})} = 40$ are used. Also assume that $V_{CC} = 10$ V, $I_{C(\text{sat})} = 5$ mA. Let the desired frequency of oscillations be 5 kHz. For transistor used, $V_{CE(\text{sat})} = 0.2$ V, $V_{BE(\text{sat})} = V_\sigma = 0.7$ V.

Solution:

$$R_c = \frac{V_{CC} - V_{CE(\text{sat})}}{I_{C(\text{sat})}} = \frac{10 - 0.2}{5 \text{ mA}} = \frac{9.8}{5 \text{ mA}} = 1.96 \text{ k}\Omega$$

Select $R_C = 2 \text{ k}\Omega$

$$I_{B(\text{min})} = \frac{I_{C(\text{sat})}}{h_{FE(\text{min})}} = \frac{5 \text{ mA}}{40} = 0.125 \text{ mA}$$

Select $I_{B(\text{sat})} = 1.5I_{B(\text{min})} = 1.5 \times 0.125 = 0.187$ mA

$$\therefore R = \frac{V_{CC} - V_\sigma}{I_{B(\text{sat})}} = \frac{10 - 0.7}{0.187 \text{ mA}} = \frac{9.3}{0.187 \text{ mA}} = 49.7 \text{ k}\Omega$$

Select $R = 47 \text{ k}\Omega$

For the ON transistor to be in saturation, the condition is $R \leq h_{FE}R_C$. Verify whether $R \leq h_{FE}R_C$ or not.

$$h_{FE}R_C = 40 \times 2 \text{ k}\Omega = 80 \text{ k}\Omega$$

$R < h_{FE}R_C$, hence, Q_2 is in saturation.

$f = \frac{0.7}{RC}$, for a symmetric astable multivibrator.

We have $f = 5$ kHz

$$5 \times 10^3 = \frac{0.7}{47 \times 10^3 \times C}$$

$$C = \frac{0.7}{5 \times 47 \times 10^{-6}} = 0.003 \mu\text{F}$$

Alternately, if this were to be an un-symmetric astable multivibrator ($T_1 \neq T_2$), then the duty cycle ($= T_1/(T_1 + T_2) = T_1/T$) will have to be specified to fix the component values of R_1 , R_2 , C_1 and C_2 . That is, let $R_1 = R_2 = R$ and duty cycle be specified as 40 per cent. If $f = 5$ kHz, then

$$T = T_1 + T_2 = 0.2 \text{ ms}$$

$$T_1/(T_1 + T_2) = T_1/T = 0.4 \text{ ms}$$

Hence, $T_1 = (0.4) (0.2) = 0.08 \text{ ms}$, $T_2 = 0.2 - 0.08 = 0.12 \text{ ms}$.

From Eq. (7.6) we know that:

$$T_2 = 0.69 \tau_1 = 0.69 RC_1 \quad (0.69)(47k\Omega)C_1 = 0.08 \text{ ms}$$

$$\text{Hence, } C_1 = \frac{0.08 \times 10^{-3}}{0.69 \times 47 \times 10^3} = 2.47 \text{ nF.}$$

Similarly from Eq. (7.7),

$$T_1 = 0.69 \tau_2 = 0.69 RC_2 \quad (0.69)(47k\Omega)C_2 = 0.12 \text{ ms}$$

$$C_2 = \frac{0.12 \times 10^{-3}}{0.69 \times 47 \times 10^3} = 3.7 \text{ nF}$$

The advantages of collector-coupled astable multivibrator in which the ON device is driven into saturation are that it is simple to implement and the dissipation in the ON device ($= V_{CE(\text{sat})} I_{C(\text{sat})}$) as well as that in the OFF device ($V_{CC} I_{CO}$) is negligibly small. So, devices with smaller dissipation capability can be employed. Yet another advantage is that the time durations are stable.

The reduced switching speed is a drawback with this circuit. As the storage time is large, the circuit takes a longer time delay for the ON device, driven into saturation, to be brought back into the OFF state. Further, as the output of one device is connected as the input to the other device through cross-coupling networks, these cross-coupling networks may cause loading. There is a rounding off of the rising edges (because of recovery transients) for the voltages at the two collectors; with the result; this circuit does not generate square waves with sharp rising edges. These factors also add to its disadvantages.

7.2.3 An Astable Multivibrator with Vertical Edges for Collector Waveforms

The square waves generated by an astable multivibrator are required to have sharp rising edges (zero rise time). In the astable multivibrator shown in Fig. 7.1, the collector waveforms have no sharp rising edges (there is a finite rise time, shown in Fig. 7.5) because of the charging current of the condenser flowing through R_C of the OFF device.

The collector waveforms with sharp rising edges and flat tops are used in digital circuits to enable some other circuit either at the rising edge or at the falling edge. If needed we could clip these waveforms using a positive-peak clipper, say at a level, V , as shown in Fig. 7.11. However, this sacrifices the signal amplitude. If on the other hand, the capacitor is provided with an alternate charging path, the voltage at the collector of the OFF device can abruptly rise to V_{CC} , giving rise to pulses with vertical edges. To achieve this, the astable multivibrator circuit shown in Fig. 7.1 is modified as shown in Fig. 7.12.

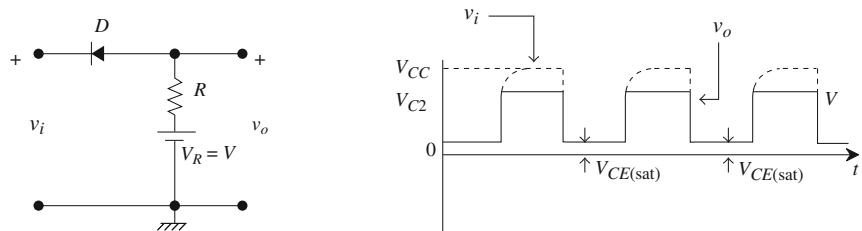


FIGURE 7.11 Deriving a square-wave output using a positive-peak clipper

Here, in this circuit, two diodes D_1 and D_2 and two resistors R_3 and R_4 ($R_3 = R_4$) are added. If Q_2 switches into the OFF state, D_2 is OFF and the voltage at the collector of Q_2 rises to V_{CC} abruptly. At the same time, the charging current of C_2 passes through R_4 and the small input resistance of Q_1 as Q_1 is ON. As this charging current does not pass through R_C of Q_2 , the voltage at this collector rises abruptly to V_{CC} . The amplitude of the square wave is approximately equal to V_{CC} .

7.3 AN ASTABLE MULTIVIBRATOR AS A VOLTAGE-CONTROLLED OSCILLATOR

A voltage-controlled oscillator (VCO) is one in which the frequency of oscillations varies as a function of voltage. The same circuit is also called a voltage-to-frequency converter (VFC) because a given voltage gives rise to a specific frequency. An astable multivibrator is used as voltage-controlled oscillator [see Fig. 7.13(a)]. A comparison of this with the circuit shown in Fig. 7.1 shows that here the two resistors R and R are returned to a separate source V_{BB} rather than to V_{CC} .

When Q_1 is OFF and Q_2 is ON, C_1 charges. When Q_1 is ON, the charge on C_1 decays with a time constant $\tau_1 = RC_1$ as shown in Fig. 7.13(b). As a result, the voltage at the base of Q_2 , V_{B2} varies with time, [see Fig. 7.13(c)].

$$v_{B2}(t) = v_f - (v_f - v_i)e^{-t/\tau_1}$$

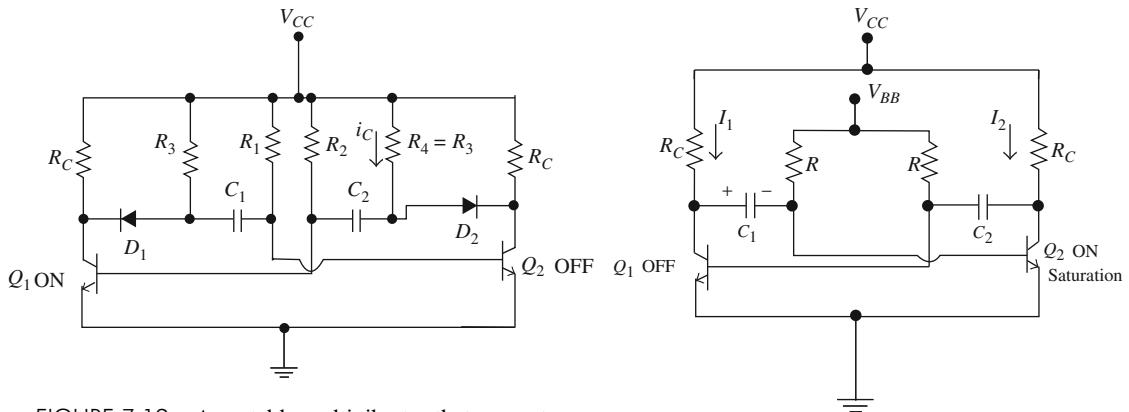


FIGURE 7.12 An astable multivibrator that generates pulses with vertical edges

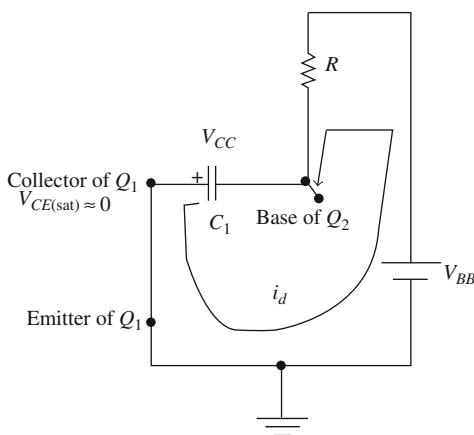


FIGURE 7.13(b) The discharge of condenser C_1 through R

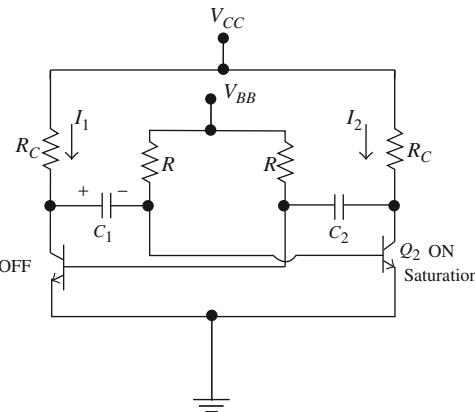


FIGURE 7.13(a) A voltage-to-frequency converter

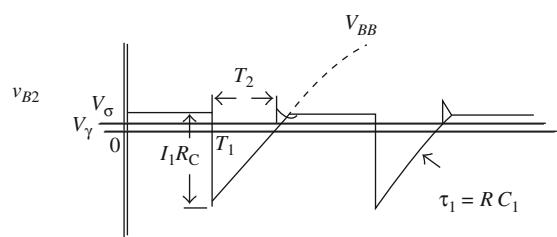


FIGURE 7.13(c) The voltage variation at the base of Q_2

$$v_f = V_{BB} \quad v_i = V_\sigma - I_1 R_C = V_\sigma - V_{CC} + V_{CE(\text{sat})}$$

Since $I_1 R_C = V_{CC} - V_{CE(\text{sat})}$;

$$v_{B2} = V_{BB} - [V_{BB} - V_\sigma + V_{CC} - V_{CE(\text{sat})}]e^{-T_2/\tau_1}$$

At $t = T_2$, $v_{B2}(t) = V_\gamma$

$$\therefore V_\gamma = V_{BB} - [V_{BB} - V_\sigma + V_{CC} - V_{CE(\text{sat})}]e^{-T_2/\tau_1}$$

If the junction voltages are small,

$$0 = V_{BB} - (V_{BB} + V_{CC})e^{-T_2/\tau_1}$$

For a symmetric circuit, $T_1 = T_2 = T/2$ and $\tau_1 = \tau_2 = \tau$

$$T_1 = T_2 = \frac{T}{2} = \tau \ln \left(\frac{V_{BB} + V_{CC}}{V_{BB}} \right) \quad (7.29)$$

Consequently, for a symmetric astable multivibrator:

$$T = 2\tau \ln \left(1 + \frac{V_{CC}}{V_{BB}} \right) \quad (7.30)$$

And, $f = 1/T$. As the frequency of the multivibrator can be varied by simply varying V_{BB} , this circuit is called a voltage-controlled oscillator or voltage-to-frequency converter.

7.4 AN ASTABLE MULTIVIBRATOR AS A FREQUENCY MODULATOR

In communication systems, a modulator is used to transmit information from one end to the other. A modulator is a circuit that changes one of the parameters of the high-frequency signal in accordance with the instantaneous amplitude of the low-frequency signal—that is intelligence. If the frequency of the high-frequency signal, called the carrier, is varied in accordance with the instantaneous amplitude of the low-frequency signal, the process is called frequency modulation.

If the voltage V_{BB} varies in accordance with the amplitude of the modulating signal (say, a sine wave), the frequency of the astable multivibrator varies in accordance with the instantaneous amplitude of the sinusoidal signal as shown in Fig. 7.14. Hence, the circuit may be called a frequency modulator [see Fig. 7.15]. This means that the frequency of the astable multivibrator will vary as per the instantaneous amplitude v_s .

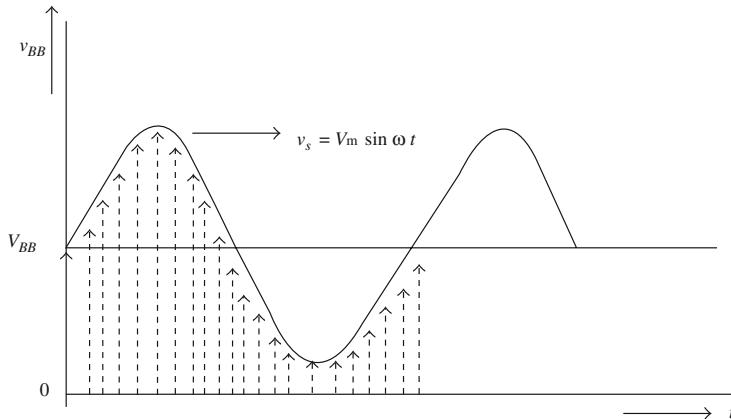


FIGURE 7.14 The instantaneous total voltage (v_{BB}) changes as per the sinusoidal signal v_s

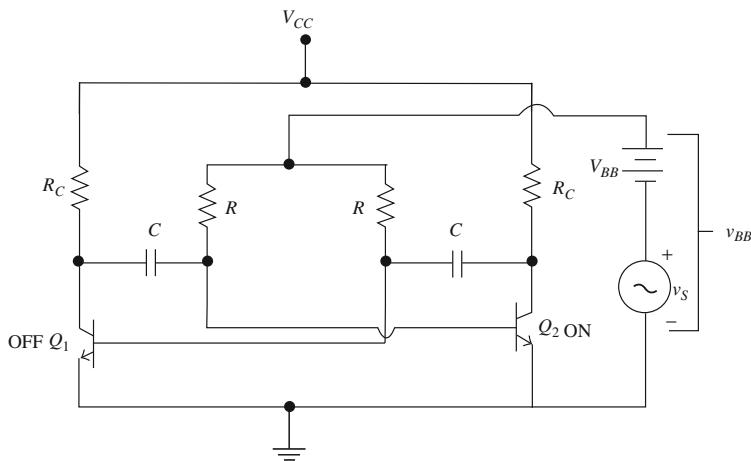


FIGURE 7.15 An astable multivibrator as a frequency modulator

7.5 Emitter-Coupled Astable Multivibrators

The main drawback of a collector-coupled astable multivibrator is that the circuit may not necessarily oscillate when V_{CC} is switched ON. It is possible that both Q_1 and Q_2 may be ON because of the inherent symmetry in the circuit. For oscillations to build up, one device may need to be switched into the OFF state by connecting its base to the emitter for a short duration. This disadvantage can be overcome in an emitter-coupled astable multivibrator as shown in Fig. 7.16(a). The circuit operates in such a fashion that Q_1 switches between cut-off and saturation, and Q_2 switches between the cut-off and active regions.

When Q_1 is OFF, $V_{CN1} = V_{CC1} = V_{BN2}$. If Q_2 (when ON) is to be in the active region, V_{BN2} should be less than V_{CN2} . For this, $V_{CC1} < V_{CC2}$ and to avoid driving Q_1 into saturation, $V_{BB} < V_{CC1}$. Therefore, $V_{BB} < V_{CC1} < V_{CC2}$. The voltages V_{BB} and V_{CC1} are derived from V_{CC2} source using potential divider networks comprising R_1, R_2 and R_3, R_4 , respectively. From Fig. 7.16(a) we have:

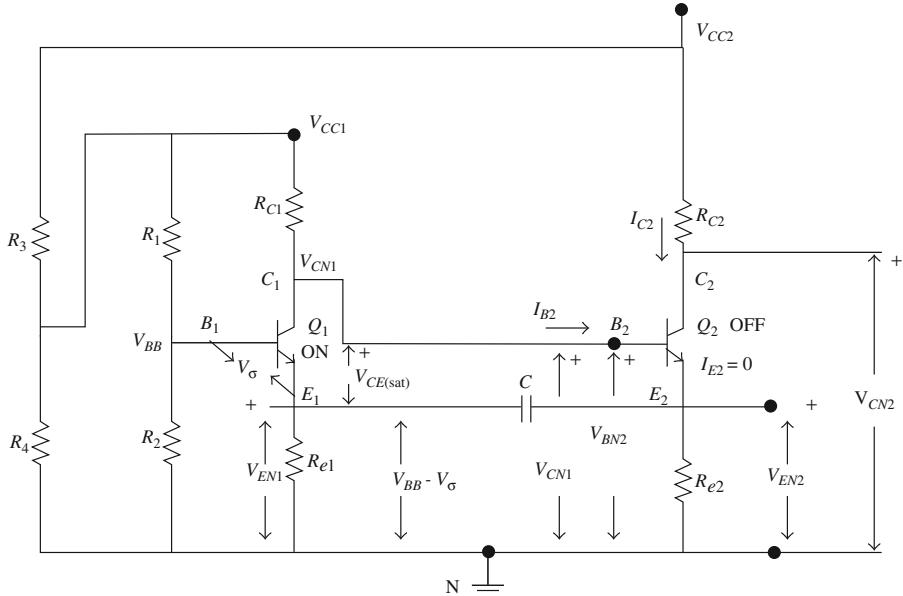


FIGURE 7.16(a) An emitter-coupled astable multivibrator

R_1 and R_2 are chosen such that they do not load the biasing circuit comprising R_3 and R_4 .

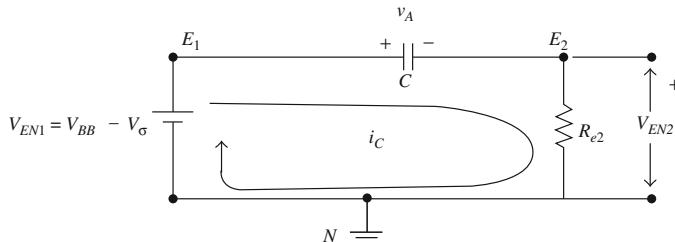
$$V_{CC1} = \frac{V_{CC2} \times R_4}{R_3 + R_4} \quad \text{and} \quad V_{BB} = \frac{V_{CC1} \times R_2}{R_1 + R_2}$$

To understand the operation of the circuit, assume that initially Q_1 is ON and Q_2 is OFF. The voltage $V_{EN1} = V_{BB} - V_\sigma$ and the capacitor C charges from this voltage source, as shown in Fig. 7.16(b).

From Fig. 7.16(b), we have $V_{EN2} = V_{EN1} - V_A$. As the capacitor voltage rises exponentially, V_{EN2} falls exponentially to zero, since V_{EN1} is constant. When $V_{EN2} = V_{BN2} - V_\gamma$, Q_2 begins to conduct. As a result, V_{EN2} rises. As E_1 and E_2 are connected through a condenser, V_{EN1} also rises by the same amount. As V_{EN1} rises further, Q_1 comes out of saturation. Therefore, V_{CN1} rises and so does V_{BN2} . This causes a further increase in the current in Q_2 . Hence, both V_{EN1} and V_{EN2} rise further. Q_1 then goes into the OFF state and Q_2 into the active region. This process is repeated. To plot these waveforms, the voltages are calculated as illustrated here:

When Q_1 is ON and Q_2 is OFF at $t = T_1^-$:

$$V_{CN2}(T_1^-) = V_{CC2} \quad (7.31)$$

FIGURE 7.16(b) Charging of C from V_{EN1} source

$$V_{EN1}(T_1-) = V_{BB} - V_\sigma \quad (7.32)$$

$$V_{CN1}(T_1-) = V_{BN2}(T_1-) = V_{EN1} + V_{CE(\text{sat})} = V_{BB} - V_\sigma + V_{CE(\text{sat})}$$

As the capacitor C charges, the voltage V_{EN2} falls exponentially to zero.

$$V_{EN2}(T_1-) = V_{BN2}(T_1-) - V_\gamma = V_{BB} - V_\sigma + V_{CE(\text{sat})} - V_\gamma \quad (7.33)$$

Q_2 begins to conduct when V_{EN2} falls to $V_{CN1}(T_1-)$.

At $t = T_1+$, Q_2 conducts and Q_1 goes into the OFF state because of the regenerative action.

$$V_{CN2}(T_1+) = V_{CC2} - I_{C2}R_{C2} \quad (7.34)$$

$$V_{CN1}(T_1+) = V_{BN2}(T_1+) = V_{CC1} - I_{B2}R_{C1} \quad (7.35)$$

$$\begin{aligned} V_{EN2}(T_1+) &= V_{BN2}(T_1+) - V_{BE2}(T_1+) \\ &= V_{CC1} - I_{B2}R_{C1} - V_{BE2} \end{aligned} \quad (7.36)$$

$\approx V_{CC1}$, as $I_{B2}R_{C1}$ and V_{BE2} are small when compared to V_{CC1} .

As Q_2 switches into the ON state; V_{EN2} rises by V_D . As E_2 and E_1 are connected through C , V_{EN1} also rises by V_D , where,

$$V_D = V_{EN1}(T_1+) - V_{EN1}(T_1-) = V_{EN2}(T_1+) - V_{EN2}(T_1-)$$

Therefore,

$$V_{EN1}(T_1+) = V_{EN2}(T_1+) + V_{EN1}(T_1-) - V_{EN2}(T_1-) \quad (7.37)$$

Substituting Eqs. (7.32), (7.33) and (7.36) in Eq. (7.37):

$$\begin{aligned} V_{EN1}(T_1+) &= V_{CC1} - I_{B2}R_{C1} - V_{BE2} + V_{BB} - V_\sigma - V_{BB} + V_\sigma - V_{CE(\text{sat})} + V_\gamma \\ &= V_{CC1} - I_{B2}R_{C1} - V_{BE2} - V_{CE(\text{sat})} + V_\gamma = V_1(\text{Say}) \end{aligned} \quad (7.38)$$

$\therefore V_1 \approx V_{CC1}$, if the junction voltages are small and I_{B2} is small.

Therefore,

$$V_{EN1}(T_1+) = V_{EN2}(T_1+) = V_1 \approx V_{CC1}$$

At $t = T_1+$, Q_2 is ON and the current in $R_{e1} = \frac{V_{EN1}(T_1+)}{R_{e1}} \approx \frac{V_{CC1}}{R_{e1}}$

And the current in $R_{e2} = \frac{V_{EN2}(T_1+)}{R_{e2}} \approx \frac{V_{CC1}}{R_{e2}}$

At this time Q_1 is OFF. Hence the sum of these two emitter currents must be supplied by Q_2 .

Hence $I_{E2} \approx I_{C2} = V_{CC1}/R_e$ and $I_{B2} = I_{C2}/h_{FE}$, where R_e is the parallel combination of R_{e1} and R_{e2} .

In the above circuit, $R_{e1} = R_{e2}$ and $R_e = R_{e1}/R_{e2}$.

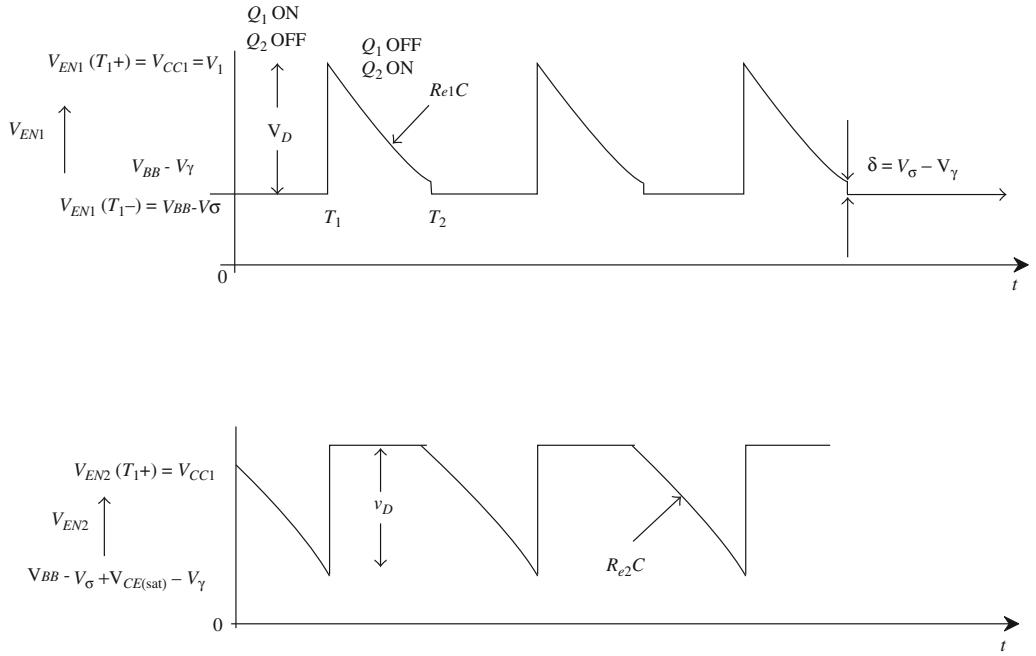


FIGURE 7.16(c) Waveforms of the emitter voltages

$$V_1 = V_{CC1} - I_B R_{C1} - V_{BE2} - V_{CE(sat)} + V_\gamma \quad V_D = V_1 - V_{EN1}(T_1+)$$

Also,

$$V_{CN2}(T_1+) = V_{CC2} - I_C R_{C2}$$

The variations of V_{EN1} and V_{EN2} are plotted as shown in Fig. 7.16(c).

The time periods T_2 and T_1 are calculated as illustrated:

T_2 is the time period for which Q_1 is OFF,

$$\therefore V_{EN1}(t) = v_f - (v_f - v_i)e^{-t/R_{e1}C}$$

$$v_f = 0, v_i = V_1$$

$$\therefore V_{EN1}(t) = V_1 e^{-t/R_{e1}C}$$

At $t = T_1$, $V_{EN1}(T_1) = V_{BB} - V_\sigma$

$$\therefore V_{BB} - V_\sigma = V_1 e^{-T_1/R_{e1}C}$$

From which, if V_σ is small,

$$T_1 = R_{e1}C \ln \frac{V_1}{V_{BB}} \quad (7.39)$$

However, neglecting junction voltages, small currents from Eq. (7.38), we have:

$$V_1 = V_{CC1}$$

$$\therefore T_1 = R_{e1}C \ln \frac{V_{CC1}}{V_{BB}} \quad (7.40)$$

$$\text{Similarly, } T_2 = R_{e2}C \ln \frac{V_{CC1}}{V_{BB}} \quad (7.41)$$

$$T = T_1 + T_2 \quad \text{and} \quad f = \frac{1}{T}$$

If this is a symmetric astable multivibrator, $T_1 = T_2 = T/2$. The operation of this circuit and plotting of the waveforms is better understood by considering an example.

EXAMPLE

Example 7.2: Consider the circuit in Fig. 7.16 (a) with $V_{CC2} = 18 \text{ V}$, $R_1 = 250 \text{ k}\Omega$, $R_3 = 200 \text{ k}\Omega$, $R_2 = R_4 = 1 \text{ M}\Omega$, $R_{e1} = R_{e2} = 3 \text{ k}\Omega$, $R_{C1} = 0.5 \text{ k}\Omega$, $R_{C2} = 0.2 \text{ k}\Omega$, $C = 0.1 \mu\text{F}$ and $h_{FE} = 30$. Si devices are used. Calculate the voltages in the circuit and plot the waveforms to the scale. Also obtain the frequency of oscillations.

Solution:

Given $V_{CC2} = 18 \text{ V}$, $R_3 = 250 \text{ k}\Omega$ and $R_4 = 1 \text{ M}\Omega$

$$V_{CC1} = V_{CC2} \times \frac{R_4}{R_3 + R_4} = 18 \times \frac{1}{1 + 0.200} = 15 \text{ V}$$

$$V_{BB} = V_{CC1} \times \frac{R_2}{R_1 + R_2} = 15 \times \frac{1}{1 + 0.250} = 12 \text{ V}.$$

When Q_1 is ON and Q_2 is OFF at $t = T_1-$

$$V_{CN2}(T_1-) = V_{CC2} = 18 \text{ V} \quad V_{EN1}(T_1-) = V_{BB} - V_\sigma = 12 - 0.7 = 11.3 \text{ V}$$

$$V_{CN1}(T_1-) = V_{BN2}(T_1-) = V_{BB} - V_\sigma + V_{CE(\text{sat})} = 11.3 + 0.3 = 11.6 \text{ V}$$

V_{EN2} exponentially falls to zero.

$$V_{EN2}(T_1-) = V_{BN2}(T_1-) - V_\gamma = 11.6 - 0.5 = 11.1 \text{ V}$$

Q_2 begins to conduct when V_{EN2} falls to 11.1 V.

At $t = T_1+$, Q_2 conducts and Q_1 goes into the OFF state because of the regenerative action. R_e is the parallel combination of R_{e1} and R_{e2} . In the above circuit,

$$R_{e1} = R_{e2} = 3 \text{ k}\Omega \quad R_e = R_{e1}/R_{e2} = \frac{3 \text{ k}\Omega}{2} = 1.5 \text{ k}\Omega$$

$$h_{FE} = 30, \quad I_{C2} = \frac{V_{CC1}}{R_e} = \frac{15 \text{ V}}{1.5 \text{ k}\Omega} = 10 \text{ mA}$$

$$I_{B2} = \frac{I_{C2}}{h_{FE}} = \frac{10 \text{ mA}}{30} = 0.33 \text{ mA} \quad I_{B2}R_{C1} = (0.33 \text{ mA})(0.5 \text{ k}\Omega) = 0.1655 \text{ V}$$

$$I_{C2}R_{C2} = (10 \text{ mA})(0.2 \text{ k}\Omega) = 2 \text{ V}$$

We have $V_\gamma = 0.5 \text{ V}$, $V_{BE2} = 0.6 \text{ V}$, $V_\sigma = 0.7 \text{ V}$, $V_{CE(\text{sat})} = 0.3 \text{ V}$

$$\therefore V_1 = V_{CC1} - I_{B2}R_{C1} - V_{BE2} - V_{CE(\text{sat})} + V_\gamma = 15 \text{ V} - 0.165 \text{ V} - 0.6 \text{ V} - 0.3 \text{ V} + 0.5 \text{ V} = 14.435 \text{ V}$$

$$V_{CN1}(T_1+) = V_{CC1} - I_{B2}R_{C1} = 15 - 0.1655 = 14.8345 \text{ V}$$

$$V_D = V_1 - V_{EN1}(T_1+) = 14.435 - 11.3 = 3.135 \text{ V}$$

$$\therefore V_{CN2}(T_1+) = V_{CC2} - I_{C2}R_{C2} = 18 - 2 = 16 \text{ V}$$

The waveforms are shown in Fig. 7.17.

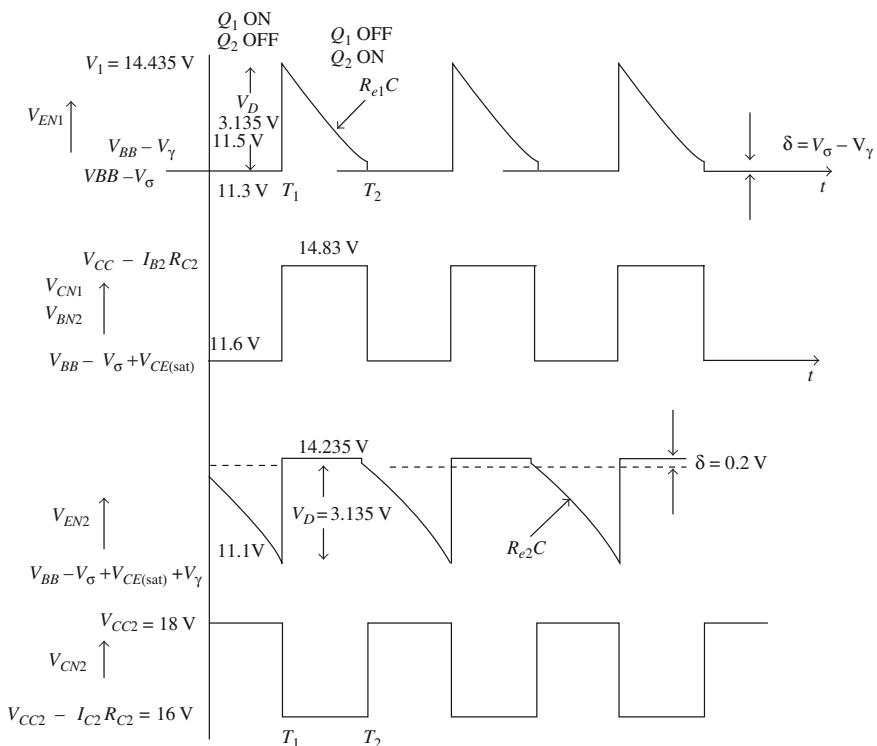


FIGURE 7.17 The waveforms of an emitter-coupled astable multivibrator

We have,

$$R_{e2} = 3 \text{ k}\Omega, C = 0.1 \text{ }\mu\text{F}$$

$$\therefore \frac{T}{2} = 3 \times 10^3 \times 0.1 \times 10^{-6} \ln \frac{15}{12} = 67 \times 10^{-6} \text{ s}$$

$$T = 2 \times \frac{T}{2} = 134 \mu\text{s} \quad f = \frac{1}{T} = \frac{1}{134 \times 10^{-6}} = 7.46 \text{ kHz}$$

7.5.1 Advantages of Emitter-coupled Astable Multivibrators

The advantages of an emitter-coupled astable multivibrator over a collector-coupled astable multivibrator are:

1. The emitter-coupled astable multivibrator starts oscillating the moment power is switched ON. There is no need to induce oscillations.
2. As the second collector is not involved in the regeneration loop, loading is avoided at this collector.
3. The first base again is not involved in the regeneration loop.
4. The pulses at the collectors will have sharp rising edges.
5. The circuit has only one timing capacitance C and thus, it is convenient to adjust the frequency.
6. Q_2 in the quasi-stable state is not driven into saturation but is held in the active region; thereby the storage time is reduced, which enables faster switching.
7. I_{C1} and I_{C2} when Q_1 and Q_2 are ON are stable because of the feedback provided in an emitter-coupled circuit.

7.5.2 Disadvantages of Emitter-coupled Astable Multivibrators

The disadvantages of an emitter-coupled astable multivibrator over a collector-coupled astable multivibrator are:

1. The circuit will not function unless the operating conditions are properly adjusted.
2. Since a single tuning condenser is used, T_1 and T_2 are nearly the same. Unsymmetric operation with variable duty cycle is difficult to implement.
3. This circuit is more complex than a collector-coupled astable multivibrator.
4. When the ON device is held in the active region, the dissipation in the device is large.

S O L V E D P R O B L E M S

Example 7.3: For the astable multivibrator shown in Fig. 7.1:

- (a) Determine the time period and the frequency of oscillations if $R_1 = R_2 = R = 10 \text{ k}\Omega$, $C_1 = C_2 = 0.01 \mu\text{F}$.
- (b) Determine the time period and the frequency of oscillations if $R_1 = 1 \text{ k}\Omega$, $R_2 = 10 \text{ k}\Omega$, $C_1 = 0.01 \mu\text{F}$, $C_2 = 1 \mu\text{F}$.

Solution:

- (a) Given $R_1 = R_2 = R = 10 \text{ k}\Omega$, $C_1 = C_2 = 0.01 \mu\text{F}$.
This is a symmetric astable multivibrator.

$$f = \frac{0.7}{RC} = \frac{0.7}{10 \times 10^3 \times 0.01 \times 10^{-6}} = 7 \text{ kHz.}$$

- (b) Given $R_1 = 1 \text{ k}\Omega$, $R_2 = 10 \text{ k}\Omega$, $C_1 = 0.01 \mu\text{F}$, $C_2 = 0.1 \mu\text{F}$

This is an un-symmetric astable multivibrator:

$$T = 0.69(R_1C_1 + R_2C_2) = 0.69(1 \times 10^3 \times 0.01 \times 10^{-6} + 10 \times 10^3 \times 0.1 \times 10^{-6}) = 0.69 \text{ ms}$$

$$f = \frac{1}{T} = \frac{10^3}{0.69} = 1.45 \text{ kHz}$$

Example 7.4: For the astable multivibrator shown in Fig. 7.1:

- Find the value of C to provide symmetrical oscillations if $R = 10 \text{ k}\Omega$ and $f = 10 \text{ kHz}$.
- Determine the values of capacitors to provide a train of pulses 0.1 ms wide and at a frequency of 1 kHz, if $R_1 = R_2 = 1 \text{ k}\Omega$.
- Find the minimum value of R_C in a symmetric astable if $R = 10 \text{ k}\Omega$ and $h_{FE} = 50$.

Solution:

- Given $R = 10 \text{ k}\Omega$ and $f = 10 \text{ kHz}$, for a symmetrical astable multivibrator.

$$f = \frac{0.7}{RC} \quad C = \frac{0.7}{Rf} = \frac{0.7}{10 \times 10^3 \times 10 \times 10^3} = 0.007 \mu\text{F}$$

- Given $T_1 = \text{duration of the pulse} = 0.1 \text{ ms}$, $f = 1 \text{ kHz}$, for the un-symmetric astable multivibrator:

$$T = \frac{1}{f} = 1 \text{ ms} \quad T_2 = T - T_1 = 1 - 0.1 = 0.9 \text{ ms} \quad R_1 = R_2 = R = 1 \text{ k}\Omega \quad 0.69RC_2 = 0.1 \text{ ms}$$

$$C_2 = \frac{0.1 \times 10^{-3}}{1 \times 10^3 \times 0.69} = 0.145 \mu\text{F} \quad 0.69RC_1 = 0.9 \text{ ms} \quad C_1 = \frac{0.9 \times 10^{-3}}{1 \times 10^3 \times 0.69} = 1.30 \mu\text{F}$$

- We have $R = h_{FE}R_C$

$$R_{C(\min)} = \frac{R}{h_{FE}} = \frac{10 \times 10^3}{50} = 200 \Omega$$

Example 7.5: For the multivibrator shown in Fig. 7.13(a), $V_{CC} = 20 \text{ V}$, $V_{BB} = 10 \text{ V}$, $R_1 = R_2 = R = 10 \text{ k}\Omega$, $C_1 = C_2 = C = 0.01 \mu\text{F}$. Find the time period and the frequency.

Solution:

$$T = 2RC \ln \left(1 + \frac{V_{CC}}{V_{BB}} \right) = 2 \times 10 \times 10^3 \times 0.01 \times 10^{-6} \ln \left(1 + \frac{20}{10} \right) = 0.22 \text{ ms}$$

$$f = \frac{1}{T} = \frac{10^3}{0.22} = 4.54 \text{ kHz}$$

Example 7.6: In an astable multivibrator if $R_2 = 60 \text{ k}\Omega$, $R_1 = 40 \text{ k}\Omega$, $C_1 = C_2 = 2.9 \text{ nF}$, find its frequency and duty cycle.

Solution:

$$T_2 = 0.69 R_1 C_1 = 0.69 \times 40 \times 10^3 \times 2.9 \times 10^{-9} = 80 \mu\text{s} = 0.08 \text{ ms}$$

$$T_1 = 0.69 R_2 C_2 = 0.69 \times 60 \times 10^3 \times 2.9 \times 10^{-9} = 120 \mu\text{s} = 0.12 \text{ ms}$$

$$T = T_1 + T_2 = 0.08 + 0.12 = 0.2 \text{ ms} \quad f = \frac{1}{T} = 5 \text{ kHz}$$

$$\text{Duty cycle} = \frac{T_1}{T} = \frac{0.12 \text{ ms}}{0.2 \text{ ms}} = 0.6$$

Example 7.7: A symmetrical collector-coupled astable multivibrator has the following parameters:

$V_{CC} = 10 \text{ V}$, $R_C = 1 \text{ k}\Omega$, $R = 10 \text{ k}\Omega$, and $C = 0.01 \mu\text{F}$. Silicon transistors with $h_{FE} = 50$ and $r_{bb'} = 0.2 \text{ k}\Omega$ are used. Plot the waveforms and calculate the overshoot. Also plot the waveforms if the circuit uses *p-n-p* transistors.

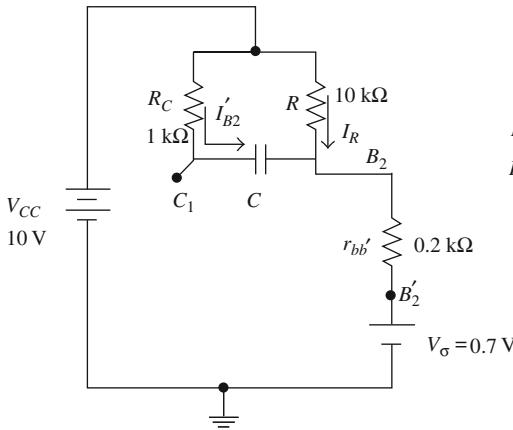
Solution:

Given $V_{CC} = 10 \text{ V}$, $R_C = 1 \text{ k}\Omega$, $R = 10 \text{ k}\Omega$, $C = 0.01 \mu\text{F}$, $r_{bb'} = 0.2 \text{ k}\Omega$ and $h_{FE} = 50$.

Assume $V_\sigma = 0.7 \text{ V}$ and $V_{CE(\text{sat})} = 0.2 \text{ V}$.

Let Q_2 be ON and in saturation, then Q_1 is OFF. After a time interval T_1 , Q_1 is ON and Q_2 is OFF. Suddenly when a device switches from the OFF state into the ON state, there is an overshoot at its base. Similarly, when the device switches its state from ON to OFF there is an overshoot at its collector. To account for these overshoots the base spreading resistance is taken into account. Let Q_2 switch from OFF to ON and Q_1 from ON to OFF, then the equivalent circuit is shown in Fig. 7.18(a).

When $R \gg R_C$, then $I_R \ll I'_{B2}$. Hence, R is omitted in Fig. 7.18(b).



$R \gg R_C$
 $I_R \ll I'_{B2}$

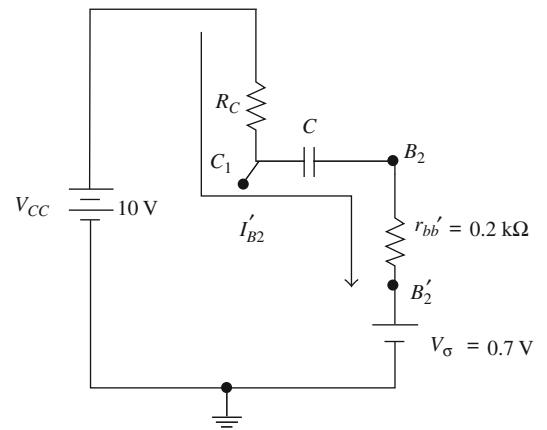


FIGURE 7.18(a) The circuit of the astable multivibrator when Q_2 switches from OFF to ON

FIGURE 7.18(b) The circuit when R is much larger than R_C

Let δ' and δ be the overshoots at the collector of Q_1 and the base of Q_2 .

$$V_\sigma = 0.7 \text{ V} \quad V_\gamma = 0.5 \text{ V} \quad \text{and} \quad V_{CE(\text{sat})} = 0.2 \text{ V}$$

$$\delta = V_{B2} - V_\gamma = I'_{B2} r_{bb'} + V_\sigma - V_\gamma = I'_{B2} r_{bb'} + 0.7 - 0.5$$

But, $\delta = \delta'$, since the collector of Q_1 and the base of Q_2 are connected through a condenser C and identical changes are required to take place at these two nodes.

$$\begin{aligned} \delta' &= V_{C1} - V_{CE(\text{sat})} = V_{CC} - I'_{B2} R_C - V_{CE(\text{sat})} = I'_{B2} r_{bb'} + 0.2 \text{ V} \\ &9.8 \text{ V} - I'_{B2} R_C = I'_{B2} r_{bb'} + 0.2 \text{ V} \end{aligned}$$

$$I'_{B2} (r_{bb'} + R_C) = 9.6 \text{ V} \quad I'_{B2} = \frac{9.6 \text{ V}}{0.2 + 1} = \frac{9.6 \text{ V}}{1.2 \text{ k}\Omega} = 8 \text{ mA}$$

$$\delta = I'_{B2} r_{bb'} + V_\sigma - V_\gamma = 8 \times 10^{-3} \times 0.2 \times 10^3 + 0.7 \text{ V} - 0.5 \text{ V} = 1.6 + 0.2 = 1.8 \text{ V} \quad \delta = \delta'$$

The waveforms are shown in Fig. 7.18(c). For the astable multivibrator circuit using *p*–*n*–*p* transistors, the waveforms are shown in Fig. 7.19.

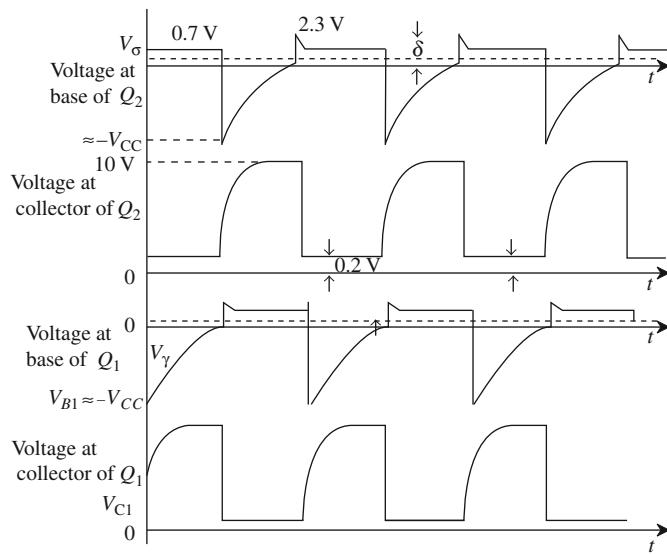


FIGURE 7.18(c) The waveforms of the circuit in Fig. 7.21(a)

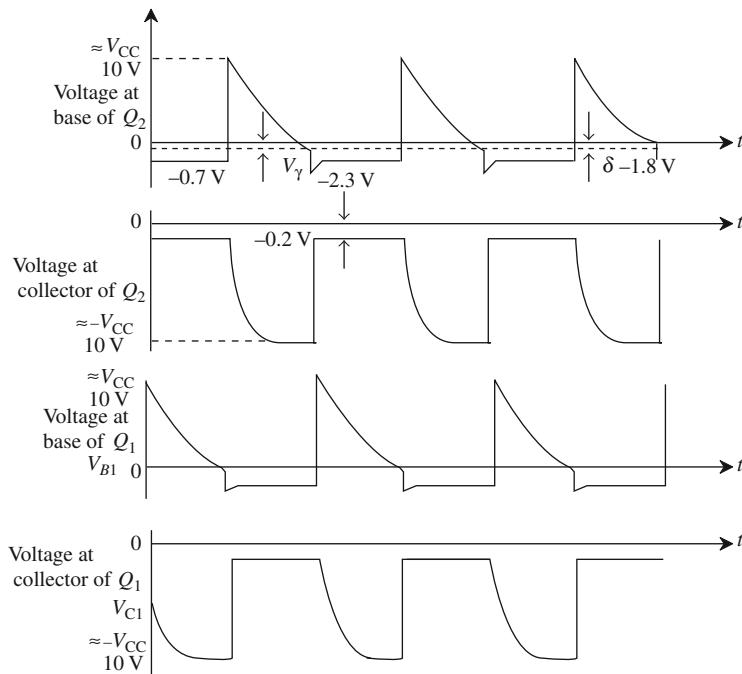


FIGURE 7.19 The Waveforms of the circuit using *p*–*n*–*p* transistors

Example 7.8: A symmetric astable multivibrator with vertical edges (see in Fig. 7.20) has the following parameters, $V_{CC} = 15$ V, $R_C = 3$ k Ω , $R_1 = R_2 = R = 30$ k Ω , $R_3 = 2$ k Ω and silicon transistors with $h_{FE} = 50$ are used. $C_1 = C_2 = C = 0.01$ μ F. Verify whether the ON device is in saturation or not. Find its frequency.

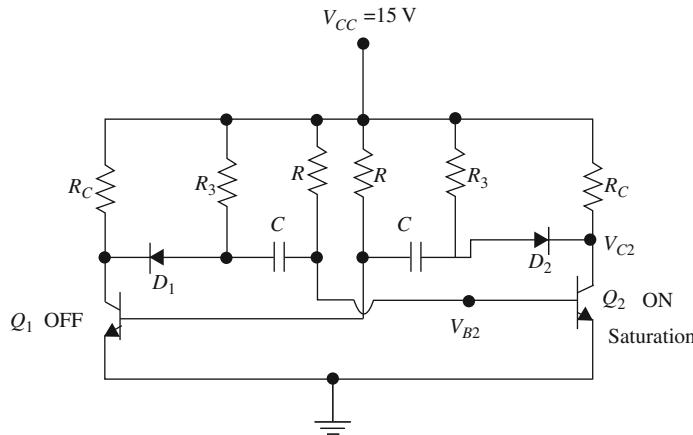


FIGURE 7.20 An astable multivibrator with vertical edges

Assume Q_1 is OFF and Q_2 is ON and in saturation. If Q_2 is ON and in saturation

$V_{C2} = V_{CE(\text{sat})} = 0.2$ V, $V_{B2} = V_\sigma = 0.7$ V then D_2 is ON. The collector load is $R_3 || R_C$.

$$R'_C = R_3 || R_C = \frac{3 \times 2}{5} = 1.2 \text{ k}\Omega \quad I_{C2} = \frac{V_{CC} - V_{CE(\text{sat})}}{R'_C} = \frac{15 - 0.2}{1.2 \text{ k}\Omega} = \frac{14.8 \text{ V}}{1.2 \text{ k}\Omega} = 12.3 \text{ mA}$$

$$I_{B2} = \frac{V_{CC} - V_\sigma}{R} = \frac{15 - 0.7}{30 \text{ k}\Omega} = \frac{14.3 \text{ V}}{30 \text{ k}\Omega} = 0.477 \text{ mA} \quad I_{B2(\text{min})} = \frac{I_{C2}}{h_{FE(\text{min})}} = \frac{12.33 \text{ mA}}{50} = 0.247 \text{ mA}$$

$$I_{B2} \gg I_{B2(\text{min})}$$

Hence, Q_2 is in saturation.

To find, f :

$$\text{For a symmetric astable multivibrator: } f = \frac{0.7}{RC} = \frac{0.7}{30 \times 10^3 \times 0.01 \times 10^{-6}} = 2.33 \text{ kHz}$$

SUMMARY

1. An astable multivibrator is essentially a square-wave generator.
2. An astable multivibrator is used as a clock in digital circuits.
3. If the time periods T_1 and T_2 are not equal, the astable multivibrator is called an un-symmetric astable multivibrator. If $T_1 = T_2 = T/2$, then it is called a symmetric astable multivibrator.
4. The ratio of T_1 to T is called the duty cycle and is expressed as a percentage.
5. In a symmetric astable multivibrator, the frequency is given by $f = 0.7/RC$ cycles/s.
6. There could be rounding-off of the rising edge of a pulse in an astable multivibrator because of a small recharging current associated with the condenser.

7. An astable multivibrator can be used as a voltage-controlled oscillator (VCO) or a voltage-to-frequency converter (VFC).
8. An astable multivibrator can also be used a frequency modulator.
9. An emitter-coupled astable multivibrator starts oscillating the moment power is switched ON.

MULTIPLE CHOICE QUESTIONS

- (1) An astable multivibrator is a:
 - (a) Square-wave generator
 - (b) Sweep generator
 - (c) Ramp generator
 - (d) None of the above
- (2) For the time period of an astable multivibrator to be stable, in the quasi-stable state, the ON device is required to be driven into:
 - (a) Saturation
 - (b) The active region
 - (c) The cut-off region
 - (d) The reverse-biased condition
- (3) The duty cycle of a symmetric multivibrator is:
 - (a) 50%
 - (b) 75%
 - (c) 25%
 - (d) 100%
- (4) The frequency of oscillations of a symmetric astable multivibrator is given as:
 - (a) $\frac{0.7}{\tau}$ c/s
 - (b) 0.7τ c/s
 - (c) 2.2τ c/s
 - (d) None of the above
- (5) To ensure that the ON device is in saturation, the condition that should be satisfied in a symmetric astable multivibrator is given by:
 - (a) $R \leq h_{FE}R_C$
 - (b) $R \geq h_{FE}R_C$
 - (c) R should be infinity
 - (d) R should be zero
- (6) The ratio of $t_{rec}/(T/2)$ of a symmetric astable is given by :
 - (a) $3.2/h_{FE}$
 - (b) $h_{FE}/3.2$
 - (c) $3.2 h_{FE}$
 - (d) h_{FE}
- (7) An astable multivibrator can be used as a:
 - (a) Voltage-controlled oscillator
 - (b) Gating circuit
 - (c) Ramp generator
 - (d) Exponential generator
- (8) An astable multivibrator can also be used as a:
 - (a) Frequency modulator
 - (b) Gating circuit
 - (c) Ramp generator
 - (d) Exponential generator

SHORT ANSWER QUESTIONS

1. Draw the circuit of a collector-coupled astable multivibrator and explain its operation.
2. Explain how an astable multivibrator can be modified to operate as a voltage-controlled oscillator.
3. Explain why in an astable multivibrator the ON device in the quasi-stable state, is required to be driven into saturation.
4. Explain how an astable multivibrator can be used as a frequency modulator.
5. What are the advantages of an emitter-coupled astable multivibrator over a collector-coupled astable multivibrator?

LONG ANSWER QUESTIONS

1. Draw the circuit of a symmetric collector-coupled astable multivibrator using *p*-*n*-*p* devices and explain its operation. Derive the expression for its frequency of oscillation and plot the waveforms.
2. Explain how an astable multivibrator can be modified to operate as a voltage-controlled oscillator. Derive the expression for its frequency of oscillations and plot the waveforms.
3. The output of a collector-coupled astable multivibrator does not have sharp rising edges for the voltages at the collectors. Explain why.
4. Draw the circuit of a collector-coupled astable multivibrator with vertical edges and explain its operation.

UNSOLVED PROBLEMS

1. For the multivibrator in Fig. 7.1, $R_1 = R_2 = R = 47 \text{ k}\Omega$, $C_1 = C_2 = C = 0.01\mu\text{F}$. Find the time period and frequency.
2. For the astable multivibrator in Fig. 7.1, $R_1 = 20 \text{ k}\Omega$, $R_2 = 30 \text{ k}\Omega$, $C_1 = C_2 = C = 0.01\mu\text{F}$. Find the time period, duty cycle and the frequency.
3. For the symmetric astable multivibrator that generates square waves with vertical edges shown in Fig. 7.22, $V_{CC} = 10 \text{ V}$, $R_C = R_3 = 2 \text{ k}\Omega$, $R_1 = R_2 = R = 20 \text{ k}\Omega$, $C = 0.1\mu\text{F}$, $h_{FE(\min)} = 30$. Show that the ON device is in saturation. Also find f . Assume suitable values for $V_{CE(\text{sat})}$ and $V_{BE(\text{sat})}$. Si transistors are used.
4. Design a symmetric collector-coupled astable multivibrator to generate a square wave of 10 kHz having peak-to-peak amplitude of 10 V where $h_{FE(\min)} = 30$, $I_{C(\text{sat})} = 2\text{mA}$.
5. Design an un-symmetric astable multivibrator having duty cycle of 40 per cent. It is required to oscillate at 5 kHz. Ge transistors with $h_{FE} = 40$ are used. The amplitude of the square wave is required to be 20 V, $I_C = 5 \text{ mA}$, $V_{CE(\text{sat})} = 0.1 \text{ V}$ and $V_{BE(\text{sat})} = 0.3 \text{ V}$.
6. For an un-symmetric astable multivibrator $R_1 = 100 \text{ k}\Omega$, $R_2 = 100 \text{ k}\Omega$, $C_1 = 0.02 \mu\text{F}$, $C_2 = 0.01 \mu\text{F}$. Find the frequency of oscillation and the duty cycle.
7. Design an unsymmetrical astable multivibrator shown in Fig. 7p.1 using silicon *n*-*p*-*n* transistors having output amplitude of 12 V. Given data, $I_{C(\text{sat})} = 5 \text{ mA}$, $h_{FE(\min)} = 50$, $f = 5 \text{ kHz}$, duty cycle = 0.6.

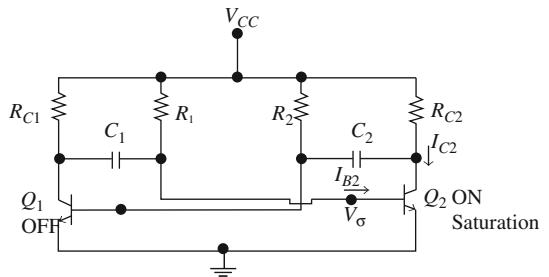


FIGURE 7p.1 Un-symmetric astable multivibrator

8. The voltage-to-frequency converter shown in Fig. 7p.2 generates oscillations at a frequency f_1 when $V_{BB} = V_{CC}$. Find the ratio of V_{CC}/V_{BB} at which the frequency $f_2 = 4f_1$.

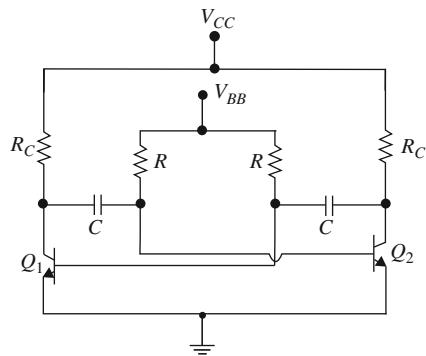


FIGURE 7p.2 The given voltage-to-frequency converter

CHAPTER 8

Monostable Multivibrators

LEARNING OBJECTIVES

After reading this chapter, you will be able to:

- Understand the working of collector-coupled and emitter-coupled monostable multivibrators
 - Derive expressions for the gate width of both emitter-coupled and collector-coupled monostable multivibrators
 - Understand the effect of temperature on the gate width of the monostable multivibrator
 - Realize the need for a commutating condenser in a monostable multivibrator
 - Realize the application of a monostable multivibrator as a voltage-to-time converter
 - Design monostable multivibrator circuits
-

8.1 INTRODUCTION

A monostable multivibrator is one in which there is a stable state and a quasi-stable state. This circuit has two devices Q_1 and Q_2 , one being in the OFF state, say Q_1 , and the other, Q_2 , in the ON state—preferably in saturation. These devices remain in this state forever and only on the application of a trigger, the multivibrator goes into the quasi-stable state, i.e., Q_1 is ON and Q_2 is OFF. After a time interval T , the multivibrator will return to the stable state, i.e., Q_1 is OFF and Q_2 is ON. Thus, this circuit generates a pulse of duration T . Let us consider two types of monostable multivibrators:

1. Collector-coupled monostable multivibrator
2. Emitter-coupled monostable multivibrator

The output of this circuit is a pulse of time duration, T called the pulse duration, pulse width or gate width. Some other circuits can also be controlled with the help of this output for a finite time duration. Its main application is as a gate.

8.2 COLLECTOR-COUPLED MONOSTABLE MULTIVIBRATORS

The collector-coupled monostable multivibrator is shown in Fig. 8.1. When compared to an astable multivibrator as shown in Fig. 7.1, it is evident that the output from the second collector to the first base is through a resistance R_1 . Hence, this circuit has one stable state and one quasi-stable state.

As a negative voltage is connected to the base of the first device, it is possible that Q_1 may be OFF. In the stable state, let Q_1 be OFF and Q_2 be ON and in saturation. Therefore:

$$V_{C1} = V_{CC} \quad V_{C2} = V_{CE(\text{sat})} \quad V_{B2} = V_{BE(\text{sat})} = V_\sigma$$

The capacitor, C now tries to charge to V_{CC} through R_C of Q_1 and a small input resistance of Q_2 , as shown in Fig. 8.2. As $t \rightarrow \infty$, this voltage reaches V_{CC} . To change the state of the devices, a trigger is applied at an appropriate point in the circuit.

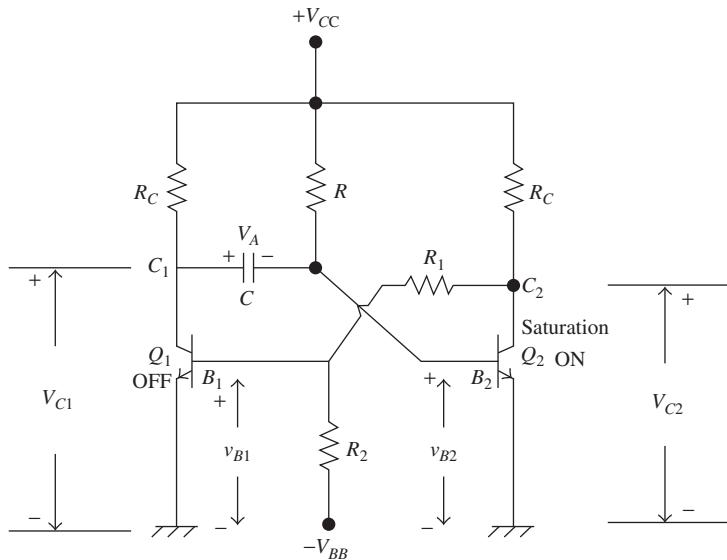


FIGURE 8.1 The collector-coupled monostable multivibrator

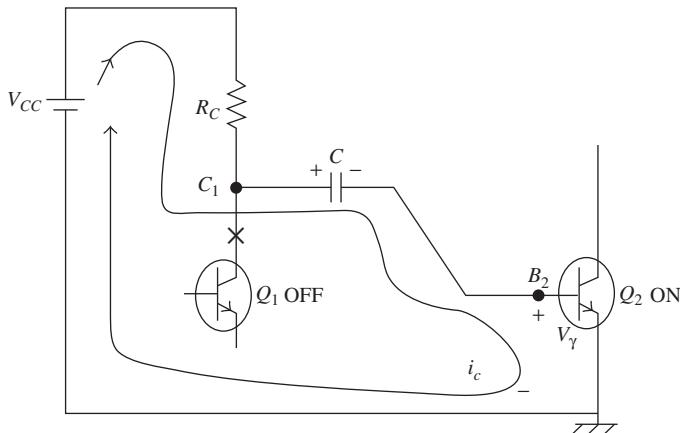


FIGURE 8.2 The charging of capacitor C

8.2.1 Triggering a Monostable Multivibrator

A trigger is a sharp positive or negative pulse of desired amplitude. A negative pulse may be applied at the base of the ON device to drive it into the OFF state or a positive pulse may be applied at the base of the OFF device to drive it into the ON state, as the devices used here are *n-p-n* devices. When a negative trigger is applied to drive an ON device into the OFF state, the instant the trigger is present; the base current of the device begins to reduce. However, when a positive trigger is applied to drive an OFF device into the ON state, the device will not draw any current till the amplitude of the pulse is V_γ . Thus, it is always preferable to drive an ON device into the OFF state rather than trying to drive an OFF device into the ON state, unless warranted otherwise. Obviously, the triggering sensitivity (ability to change state with a smaller pulse) is better if an ON device is driven into the OFF state rather than applying the other option. Therefore, we now try to drive Q_2 into the OFF state by the application of a negative pulse at the base of Q_2 , which is ON and in saturation.

The input resistance of Q_2 is very small and hence, loads the trigger source. To avoid loading, the trigger may be applied as shown in Fig.8.3.

The negative trigger, to drive Q_2 OFF is now applied at the collector of Q_1 through C_i and diode D_1 —which conducts only for negative trigger pulses. R_d is the resistance returned to V_{CC} , which is the input resistance offered by the circuit to the trigger source. If R_d is small, it loads the trigger source. Therefore, here, R_d will have to be large. However, when D_1 is ON, charge is built up on the condenser C_i , which should be quickly removed before the application of the next trigger pulse; thus, R_d should be small on this count. A single resistance cannot satisfy both these conflicting requirements. Hence, in place of the resistance R_d , D_2 is connected, which satisfies both the requirements. When the trigger signal is present, D_2 is OFF and offers large input resistance to the trigger source. When the trigger signal is not there, D_2 conducts, offering negligible resistance so that the accumulated charge on condenser C_i is quickly removed. As C is connected between the first collector and second base, the trigger signal is instantaneously connected to B_2 .

8.2.2 Calculation of the Time Period (T)

On the application of a trigger at $t = 0$, with a negative pulse at B_2 , Q_2 goes into the OFF state and Q_1 is driven into the ON state and preferably into saturation. Hence, there is a current I_1 in Q_1 . V_{C1} is $V_{CE(sat)}$, if $I_1 = I_{C(sat)}$, as shown in Fig. 8.4(a).

The charge on the capacitor C now decays with a time constant $\tau = RC$, as shown in Fig. 8.4(b). Consequently, the voltage at B_2 changes as a function of time and this voltage, V_{B2} at B_2 , reaches V_γ after a time interval T . The moment the voltage at B_2 is once again V_γ , Q_2 has a small base current, which in turn gives rise to collector current. Earlier the voltage at this collector was V_{CC} as Q_2 was OFF. Due to this collector current, the voltage at the collector of Q_2 falls, giving rise to a negative step. This negative step is coupled to the base of Q_1 through R_1 and R_2 and thus, the base current of Q_1 reduces, reducing its collector current. The voltage at the first collector now rises (earlier it was $V_{CE(sat)}$), resulting in a positive step. This change in voltage is coupled to the second base, increasing its base current further. As the collector current increases, the voltage at this collector reduces; this change in the voltage is once again coupled to the first base, reducing its base current further. Its collector current is now reduced, giving rise to a further increase in the voltage at the first collector, which once again is coupled to the second base. It is observed that regeneration takes place and Q_2 is switched ON and Q_1 is switched OFF, thus ending the quasi-stable state (also look at the voltage variation at B_2 of Q_2 shown in Fig. 8.5).

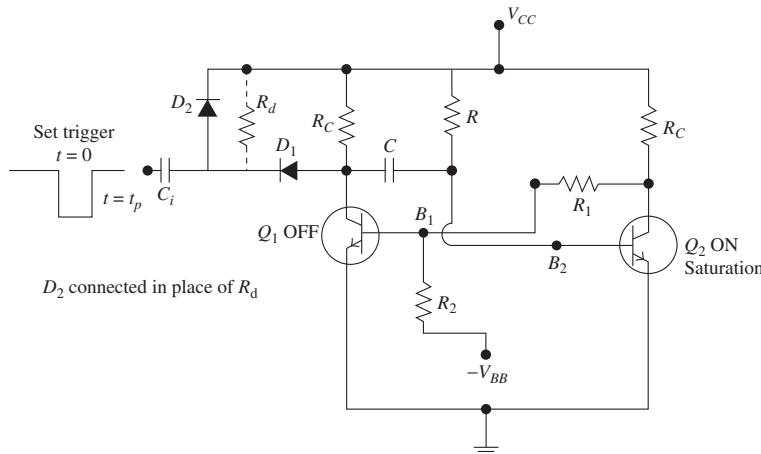
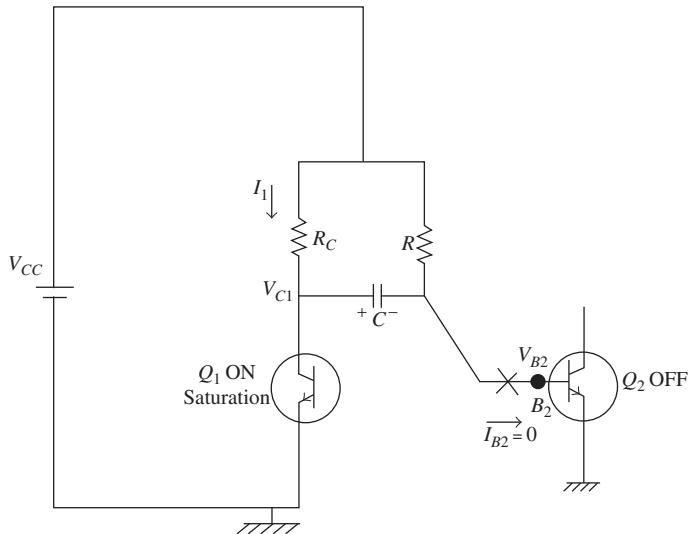
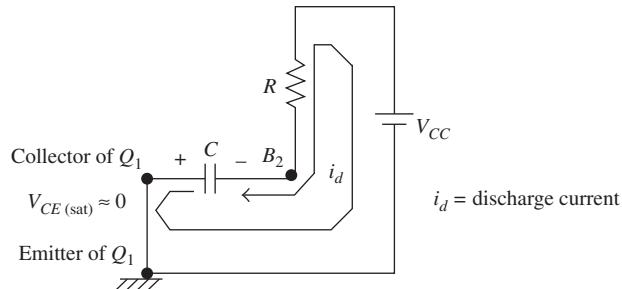
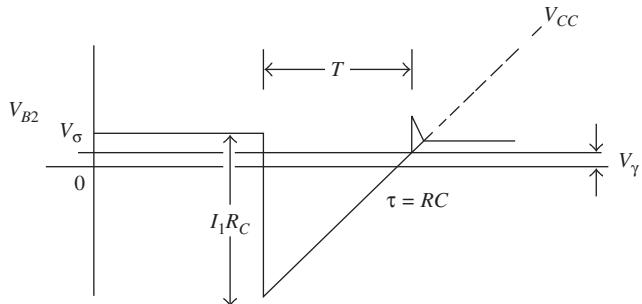


FIGURE 8.3 The triggering of a monostable multivibrator

FIGURE 8.4(a) When Q_1 is ON, in the quasi-stable stateFIGURE 8.4(b) Discharge of C FIGURE 8.5 The voltage variation at the base of Q_2 , in the quasi-stable state

We have from Eq. (7.1),

$$V_{B2}(t) = v_f - (v_f - v_i)e^{-t/\tau}$$

Here, $v_f = V_{CC}$, and if Q_1 is in saturation,

$$v_i = V_{\sigma} - I_1 R_C = V_{\sigma} - [V_{CC} - V_{CE(\text{sat})}] = V_{\sigma} - V_{CC} + V_{CE(\text{sat})}$$

and the time constant, $\tau = RC$

Using Eq. (7.1)

$$V_{B2}(t) = V_{CC} - [V_{CC} - V_\sigma + V_{CC} - V_{CE(\text{sat})}]e^{-t/\tau} \quad (8.1)$$

However, at $t = T$, $V_{B2}(t) = V_\gamma$

$$V_\gamma = V_{CC} - [2V_{CC} - (V_\sigma + V_{CE(\text{sat})})]e^{-T/\tau}$$

$$\text{As } \frac{V_\sigma + V_{CE(\text{sat})}}{2} \approx V_\gamma$$

$$T = \tau \ln 2 \frac{V_{CC} - V_\gamma}{V_{CC} - V_\gamma}$$

$$T = 0.69\tau \quad (8.2)$$

The time period T can be calculated as $T = 0.69 RC$, if Q_1 in the quasi-stable state is in saturation.

8.2.3 The Effect of Temperature on Gate Width

If the temperature effects are not taken into consideration, the gate width of a collector-coupled monostable multivibrator is given as $T = 0.69\tau$. When the temperature changes are taken into consideration, this gate width is likely to change. Consider a transistor which is in the OFF state as shown in Fig. 8.6(a).

Ideally, $I_C = 0$. However, there exists a leakage current called $I_{CBO} = I_{CO}$. The collector cut-off current, I_{CO} is reasonably large in Ge devices, but is small in Si devices. For Si devices at room temperature (25°C), typically I_{CO} is in the order of nanoamperes. However, as the temperature increases I_{CO} also increases, and gets doubled for every 10°C rise in temperature. When $I_C = 0$, $V_{CE} = V_{CC}$. If $I_{CO} = 10 \mu\text{A}$ and $R_C = 2 \text{k}\Omega$, then

$$V_{CE} = V_{CC} - I_{CO} R_C = 10 - (0.01)(2) = 9.98 \text{ V}$$

Thus, the voltage at the collector is 9.98 V instead of 10 V. In normal applications, this may not be important. However, in precision applications, temperature effects will have to be considered. Now consider the collector-coupled monostable multivibrator in Fig. 8.6(b). In the stable state, when capacitor C is fully charged, it behaves as an open circuit for dc. If the multivibrator is now driven into the quasi-stable state, the voltage to which the capacitor is returned is seen to be $V' = V_{CC} + I_{CO}R$, instead of V_{CC} . Hence, when capacitor C discharges, the final voltage $v_f = V'$.

Let us now calculate the time period. We have from Eq. (7.1):

$$V_{B2}(t) = v_f - (v_f - v_i)e^{-t/\tau}$$

Here,

$$v_f = V' = V_{CC} + I_{CO}R \quad (8.3)$$

And if Q_1 is in saturation,

$$v_i = V_\sigma - I_1 R_C = V_\sigma - [(V_{CC} - V_{CE(\text{sat})})] = V_\sigma - V_{CC} + V_{CE(\text{sat})}$$

Neglecting the junction voltages $v_i = -V_{CC}$, and the time constant, $\tau = RC$. Using Eq. (7.1):

$$V_{B2}(t) = V' - (V' + V_{CC})e^{-t/\tau} \quad (8.4)$$

However, at $t = T$, $V_{B2}(t) = V_\gamma \approx 0$.

$$0 = V' - (V' + V_{CC})e^{-T/\tau}$$

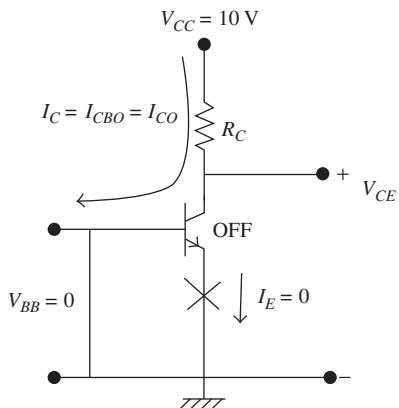
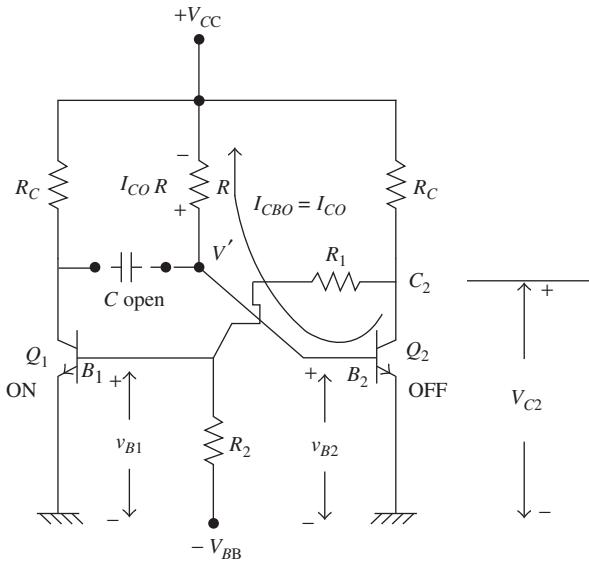


FIGURE 8.6(a) Transistor in the OFF state

FIGURE 8.6(b) The collector-coupled monostable multivibrator considering I_{CO}

$$V' = (V' + V_{CC})e^{-T/\tau} \quad (8.5)$$

$$T = \tau \ln \frac{V' + V_{CC}}{V'} \quad (8.6)$$

Substituting Eq. (8.3) in Eq. (8.6):

$$T = \tau \ln \frac{2V_{CC} + I_{CO}R}{V_{CC} + I_{CO}R} = \tau \ln 2 + \tau \ln \left(\frac{1 + \frac{I_{CO}R}{2V_{CC}}}{1 + \frac{I_{CO}R}{V_{CC}}} \right)$$

If

$$\phi = \frac{I_{CO}R}{V_{CC}} \quad (8.7)$$

$$T = \tau \ln 2 + \tau \ln \left(\frac{1 + \frac{\phi}{2}}{1 + \phi} \right) = \tau \ln 2 - \tau \ln \left(\frac{1 + \phi}{1 + \frac{\phi}{2}} \right) \quad (8.8)$$

The gate width of the monostable multivibrator will now be less than the gate width calculated using Eq. (8.2). This effect can be more pronounced with Ge transistors and at elevated temperatures. Let us consider an example.

EXAMPLE

Example 8.1: Calculate the gate width for the monostable multivibrator given that $R = 100 \text{ k}\Omega$, $V_{CC} = 10 \text{ V}$, $C = 0.01 \mu\text{F}$; (a) when I_{CO} is neglected and (b) when $I_{CO} = 0.01 \text{ mA}$.

Solution:

$$(a) \tau = RC = 100 \times 10^3 \times 0.01 \times 10^{-6} = 1 \text{ ms}$$

When I_{CO} is neglected, the gate width is calculated using Eq. (8.2),

$$T = 0.69 \times 100 \times 10^3 \times 0.01 \times 10^{-6} = 0.69 \text{ ms.}$$

(b) When I_{CO} is considered, from Eq. (8.7),

$$\begin{aligned} \phi &= \frac{0.01 \times 10^{-3} \times 100 \times 10^3}{10} = 0.1 \quad \text{and} \quad \frac{\phi}{2} = 0.05 \\ \frac{1 + \phi}{1 + \frac{\phi}{2}} &= \frac{1 + 0.1}{1 + 0.05} = 1.05 \\ \tau \ln(1.05) &= 1 \times 10^{-3} \times 0.049 = 0.049 \text{ ms} \end{aligned}$$

Therefore, T when the leakage current is considered, using Eq. (8.8) is

$$T = 0.69 - 0.049 = 0.641 \text{ ms.}$$

8.3 CALCULATION OF THE VOLTAGES TO PLOT THE WAVEFORMS

To plot the waveforms at the two collectors and the two bases, the voltages in the circuit are to be calculated; when the multivibrator is in the stable state, when it is driven into the quasi-stable state and finally when it returns to the initial stable state. Consider the collector-coupled monostable multivibrator as shown in Fig. 8.1.

8.3.1 In the Stable State ($t < 0$)

Here, the assumption is that Q_2 is ON and in saturation while Q_1 is OFF. In this situation, the need is to verify whether Q_2 is really in saturation or not and whether Q_1 is in the OFF state.

To Verify that Q_2 is in Saturation. For this we need to calculate I_{C2} and I_{B2} and then verify whether I_{B2} is significantly larger than $I_{B2(\min)}$ or not. If $I_{B2} \gg I_{B2(\min)}$, then Q_2 is really in saturation. To verify this, consider the circuit shown in Fig. 8.7(a). From Fig. 8.7(a),

$$I_2 = \frac{V_{CC} - V_{CE(\text{sat})}}{R_C} \quad (8.9)$$

$$I_3 = \frac{V_{CE(\text{sat})} - (-V_{BB})}{R_1 + R_2} \quad (8.10)$$

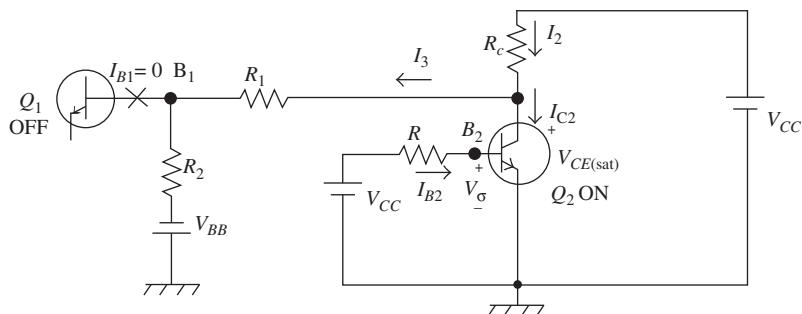


FIGURE 8.7(a) In the stable state Q_1 is OFF and Q_2 is ON

$$\therefore I_{C2} = I_2 - I_3 \quad (8.11)$$

$$I_{B2} = \frac{V_{CC} - V_\sigma}{R} \quad (8.12)$$

$$I_{B2(\min)} = \frac{I_{C2}}{h_{FE(\min)}} \quad (8.13)$$

For Q_2 to be in saturation, I_{B2} should be at least $1.5 I_{B2(\min)}$. If $I_{B2} >> I_{B2(\min)}$, Q_2 is really in saturation, as per the assumption made. Hence $V_{C2} = V_{CE(\text{sat})}$ and $V_{B2} = V_{BE(\text{sat})} = V_\sigma$.

To Verify that Q_1 is OFF. To show that Q_1 is OFF, the voltage V_{B1} at B_1 is to be found out and then checked whether the base-emitter diode is reverse-biased or not. If this diode is reverse-biased, then Q_1 is OFF. To calculate the voltage V_{B1} at B_1 , consider the circuit shown in Fig. 8.7(b). The voltage V_{B1} is due to the two sources; the V_{BB} source and the $V_{CE(\text{sat})}$ source. Use the superposition theorem to calculate V_{B1} , considering one source at a time. Shorting the V_{BB} source, the resultant circuit is as shown in Fig. 8.7(c).

$$V_{B1}(V_{BB} = 0) = V_{CE(\text{sat})} \times \frac{R_2}{R_1 + R_2} \quad (8.14)$$

Now shorting the $V_{CE(\text{sat})}$ source, the resultant circuit is as shown in Fig. 8.7(d).

$$V_{B1}(V_{CE(\text{sat})} = 0) = -V_{BB} \times \frac{R_1}{R_1 + R_2} \quad (8.15)$$

Combining Eqs. (8.14) and (8.15), the net voltage V_{B1} at B_1 due to the two sources $V_{CE(\text{sat})}$ and $-V_{BB}$ is:

$$V_{B1} = V_{CE(\text{sat})} \times \frac{R_2}{R_1 + R_2} + (-V_{BB}) \times \frac{R_1}{R_1 + R_2}. \quad (8.16)$$

If the base of Q_1 is negative with respect to the emitter, the base-emitter diode is reverse-biased. Therefore, Q_1 is OFF, as assumed. Hence, $V_{C1} = V_{CC}$. The voltage across the capacitor terminals is,

$$V_A = V_{C1} - V_{B2} = V_{CC} - V_\sigma \quad (8.17)$$

8.3.2 In the Quasi-stable State ($t = 0+$)

At $t = 0$, a negative pulse of proper amplitude is applied at the base of Q_2 that drives Q_2 into the OFF state. As a result Q_1 goes into the ON state and into saturation as shown in Fig. 8.7(e).

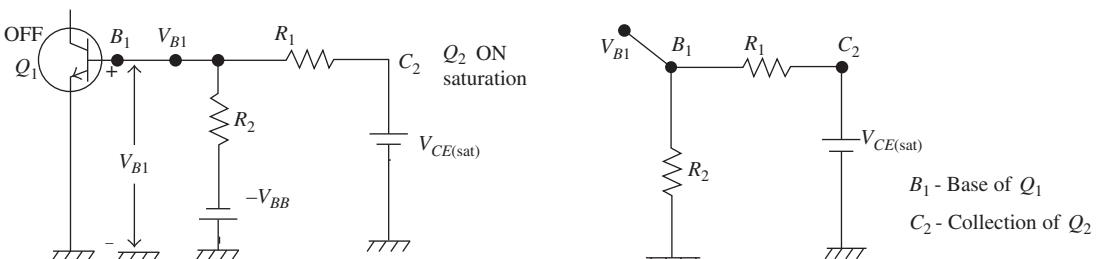


FIGURE 8.7(b) The circuit for calculating V_{B1}

FIGURE 8.7(c) The circuit to calculate V_{B1} due to $V_{CE(\text{sat})}$ source

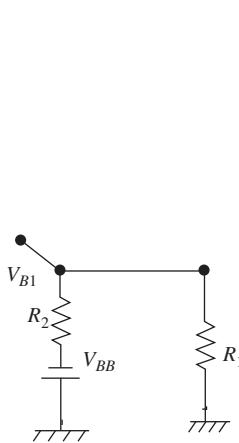


FIGURE 8.7(d) The circuit to calculate V_{B1} due to $-V_{BB}$ source

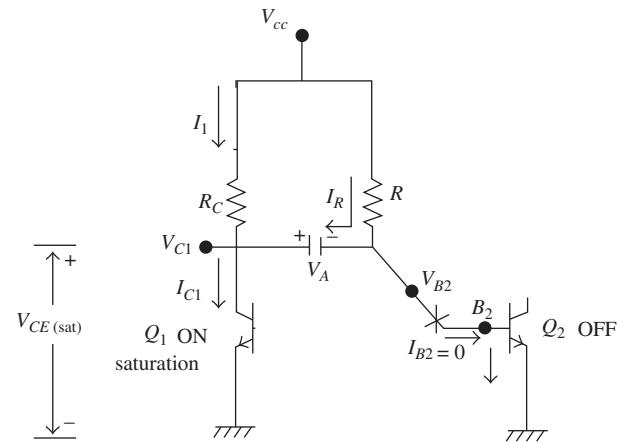


FIGURE 8.7(e) In the quasi-stable state Q_1 is ON and Q_2 is OFF

First let us verify whether Q_1 is really in saturation or not. Let us calculate I_{C1} .

$$I_{C1} = I_1 + I_R \quad (8.18)$$

$$I_1 = \frac{V_{CC} - V_{CE(\text{sat})}}{R_C} \quad (8.19)$$

To calculate I_R , write the KVL equation of the loop consisting of R_C , C and R .

$$I_R R = I_1 R_C + V_A \quad (8.20)$$

Using Eqs. (8.19) and (8.20), we get I_1 and I_R .

Therefore,

$$I_{C1} = I_1 + I_R \quad (8.21)$$

$$I_{B1(\text{min})} = \frac{I_{C1}}{h_{FE(\text{min})}} \quad (8.22)$$

To Calculate I_{B1} . Considering Fig. 8.7(f):

$$I_{B1} = I_3 - I_4 \quad (8.23)$$

$$I_3 = \frac{V_{CC} - V_\sigma}{R_C + R_1} \quad (8.24)$$

$$I_4 = \frac{V_\sigma - (-V_{BB})}{R_2} \quad (8.25)$$

If $I_{B1} \gg I_{B1(\text{min})}$, then Q_1 is in saturation,

$$V_{C2} = V_{CC} - I_3 R_C \quad (8.26)$$

$$V_{B2} = V_{CC} - I_R R \quad (8.27)$$

In the quasi-stable state, only V_{B2} changes and all other voltages remain unaltered. At $t = T$, when $V_{B2} = V_\gamma$, the quasi-stable state ends and the multivibrator returns to the initial stable condition of Q_1 and Q_2 in the OFF and ON states, respectively.

8.3.3 At the End of the Quasi-stable State (at $t = T+$)

At the end of the quasi-stable state, Q_1 goes OFF and Q_2 goes ON and into saturation. In this process, overshoots (increase over and above the expected value) can occur at the base of Q_2 and at the collector of Q_1 , because the voltage change occurs abruptly. The amount of overshoot is accounted for by the base spreading resistance $r_{bb'}$ which is the resistance seen between the external base lead and the internal base terminal and is the resistance offered to a recombination current. This is typically less than $1\text{k}\Omega$, as shown in Fig. 8.7(g).

From Fig. 8.7(g),

$$I_{B2} = I'_{B2} + I'_R \quad (8.28)$$

As

$$R \gg R_C, \quad I'_R \ll I'_{B2}. \quad (8.29)$$

Neglecting the current I_R when compared to I'_{B2} the circuit reduces to as shown in Fig. 8.7(h).

The voltages at B_2 and C_1 are

$$V'_{B2} = I'_{B2}r_{bb'} + V_\sigma \quad (8.30)$$

$$V'_{C1} = V_{CC} - I'_{B2}R_C \quad (8.31)$$

The overshoot δ at the second base is the variation over and above V_γ .

$$\delta = V'_{B2} - V_\gamma$$

Using Eq. (8.30):

$$\delta = V'_{B2} - V_\gamma = I'_{B2}r_{bb'} + V_\sigma - V_\gamma. \quad (8.32)$$

Similarly the overshoot δ' at the first collector is the variation over and above $V_{CE(\text{sat})}$

Therefore,

$$\delta' = V'_{C1} - V_{CE(\text{sat})}.$$

Using Eq. (8.31):

$$\delta' = V_{CC} - I'_{B2}R_C - V_{CE(\text{sat})}. \quad (8.33)$$

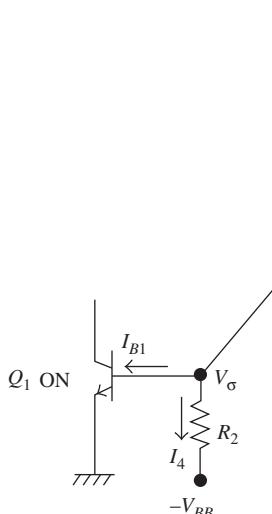


FIGURE 8.7(f) Circuit that is used to calculate I_{B1}

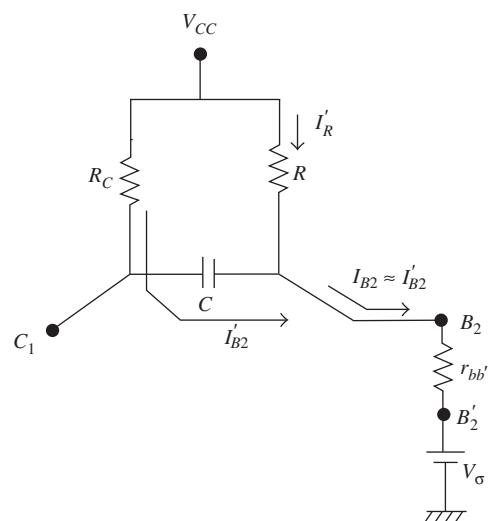


FIGURE 8.7(g) The circuit at the end of the quasi-stable state

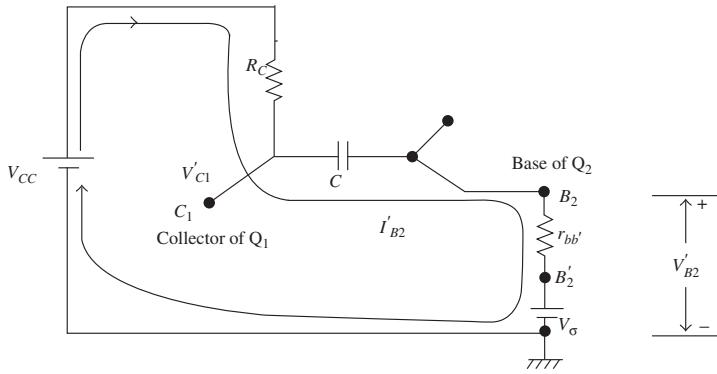


FIGURE 8.7(h) The simplified circuit of Fig. 8.7(g)

The first collector and the second base are connected through a condenser C and as the condenser will not allow any sudden changes in the voltages, whatever is the change that takes place at the first collector an identical change is required to take place at the second base. Hence, $\delta = \delta'$.

$$I'_B2 r_{bb'} + V_\sigma - V_\gamma = V_{CC} - I'_B2 R_C - V_{CE(\text{sat})}$$

$$I'_B2 (r_{bb'} + R_C) = V_{CC} - V_{CE(\text{sat})} - V_\sigma + V_\gamma$$

$$\therefore I'_B2 = \frac{V_{CC} - V_{CE(\text{sat})} - V_\sigma + V_\gamma}{r_{bb'} + R_C} \quad (8.34)$$

$$V'_C1 = V_{CC} - I'_B2 R_C \quad (8.35)$$

$$V'_B2 = I'_B2 r_{bb'} + V_\sigma \quad (8.36)$$

The waveforms can now be plotted. To plot the waveforms of a collector-coupled monostable multivibrator with specific component values mentioned, consider the following example.

EXAMPLE

Example 8.2: Consider the circuit shown in Fig. 8.8(a), which uses an $n-p-n$ silicon transistors with the following specifications: $V_{CC} = 10$ V, $V_{BB} = 10$ V, $R_C = 1$ k Ω , $R_1 = 10$ k Ω = R , $R_2 = 100$ k Ω , $h_{FE(\text{min})} = 30$, $r_{bb'} = 0.2$ k Ω , $V_{CE(\text{sat})} = 0.3$ V, $V_{BE(\text{sat})} = V_\sigma = 0.7$ V. Calculate all the current and voltages and then plot the waveforms.

Solution: (i) In the stable state ($t < 0$)

The assumption made is Q_2 is ON and in saturation and Q_1 is OFF. To verify that Q_2 is ON and in saturation, I_{C2} and I_{B2} of Q_2 are to be calculated. Further check whether $I_{B2} >> I_{B2}(\text{min})$ or not. If $I_{B2} >> I_{B2}(\text{min})$, then Q_2 is really in saturation. Consider the circuit shown in Fig. 8.8(b).

(a) To verify if Q_2 is ON and in saturation:

$$I_{C2} = I_2 - I_3 \quad I_2 = \frac{V_{CC} - V_{CE(\text{sat})}}{R_C} = \frac{10 - 0.3}{1 \text{ k}\Omega} = 9.7 \text{ mA}$$

$$I_3 = \frac{V_{CE(\text{sat})} - (-V_{BB})}{R_1 + R_2} = \frac{10.3}{110 \text{ k}\Omega} = 0.0934 \text{ mA}$$

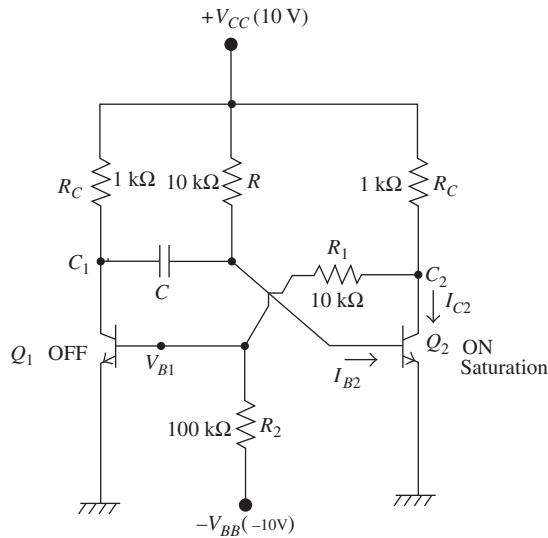
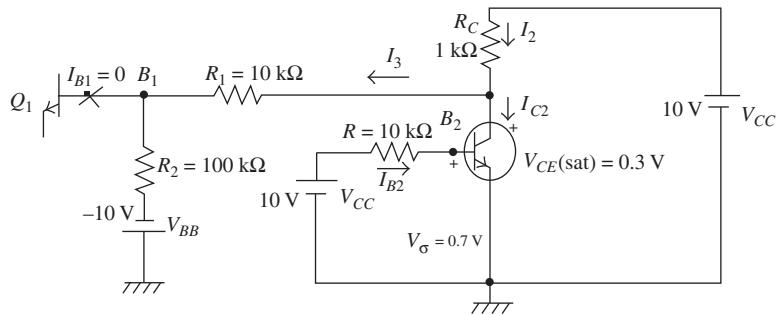


FIGURE 8.8(a) Practical collector-coupled monostable multivibrator

FIGURE 8.8(b) In the stable state, Q_1 is OFF and Q_2 is ON

$$\therefore I_{C2} = I_2 - I_3 = 9.7 \text{ mA} - 0.0934 \text{ mA} = 9.61 \text{ mA}$$

$$I_{B2} = \frac{V_{CC} - V_\sigma}{R} = \frac{10 - 0.7}{10 \text{ k}\Omega} = 0.93 \text{ mA} \quad I_{B2 \text{ (min)}} = \frac{I_{C2}}{h_{FE \text{ (min)}}} = \frac{9.61 \text{ mA}}{30} = 0.32 \text{ mA}$$

For Q_2 to be in saturation, I_{B2} should be at least $1.5 I_{B2 \text{ (min)}}$. Hence, I_{B2} should be selected to keep Q_2 in saturation as

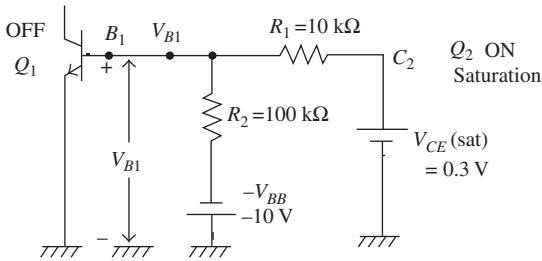
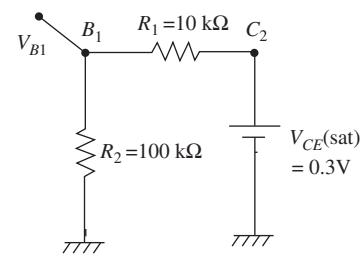
$$I_{B2} = 1.5 \times 0.32 \text{ mA} = 0.48 \text{ mA.}$$

As $I_{B2}(0.93 \text{ mA}) \gg 1.5 I_{B2 \text{ (min)}}(0.48 \text{ mA})$, as per the assumption made Q_2 is really in saturation. Hence,

$$V_{C2} = 0.3 \text{ V, and } V_{B2} = 0.7 \text{ V.}$$

b) To verify that Q_1 is OFF:

To verify whether Q_1 is in the OFF state or not, $V_{B1} = V_{BE1}$ is calculated and seen if it reverse-biases the base-emitter diode. The voltage V_{B1} is due to two sources—the V_{BB} source and the $V_{CE(\text{sat})}$ source, as shown in Fig. 8.8(c). Use the superposition theorem to calculate V_{B1} , considering one source at a time. Considering the $V_{CE(\text{sat})}$ source and shorting the V_{BB} source, the resultant circuit is as shown in Fig. 8.8(d).

FIGURE 8.8(c) The circuit for calculating V_{B1} FIGURE 8.8(d) The circuit to calculate V_{B1} due to $V_{CE(\text{sat})}$ source

$$V_{B1}(V_{BB} = 0) = V_{CE(\text{sat})} \times \frac{R_2}{R_1 + R_2} = 0.3 \times \frac{100}{100 + 10} = \frac{3}{11} = 0.27 \text{ V}$$

Now shorting the $V_{CE(\text{sat})}$ source, the resultant circuit is as shown in Fig. 8.8(e).

$$V_{B1}(V_{CE(\text{sat})} = 0) = -10 \times \frac{10}{110} = \frac{-10}{11} = -0.91 \text{ V}$$

Therefore, the net voltage V_{B1} at B_1 due to the two sources $V_{CE(\text{sat})}$ and $-V_{BB}$ is

$$V_{B1} = 0.27 - 0.91 = -0.64 \text{ V.}$$

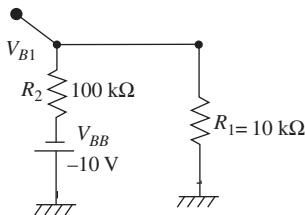
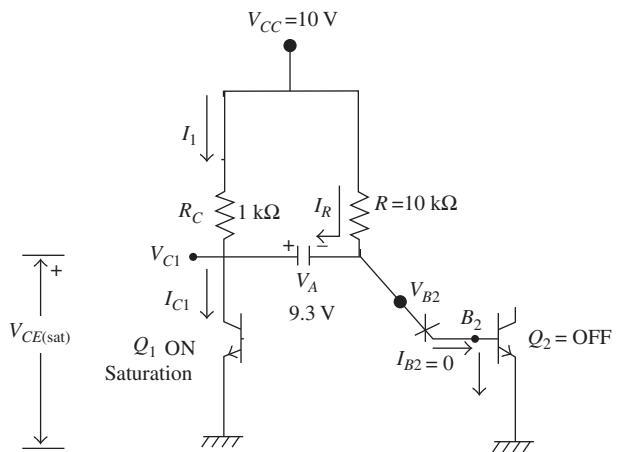
This explains that the base of Q_1 is negative with respect to the emitter by 0.64 V. Hence, the base-emitter diode is reverse-biased. Therefore, Q_1 is OFF, as assumed. Hence, $V_{C1} = V_{CC} = 10 \text{ V}$. The voltage across the capacitor terminals is

$$V_A = V_{C1} - V_{B2} = V_{CC} - V_{\sigma} = 10 \text{ V} - 0.7 \text{ V} = 9.3 \text{ V}$$

In the stable state, the voltages are $V_{B1} = -0.64 \text{ V}$, $V_{C1} = 10 \text{ V}$, $V_{B2} = 0.7 \text{ V}$, $V_{C2} = 0.3 \text{ V}$, $V_A = 9.3 \text{ V}$.

ii) In the quasi-stable state ($t = 0+$)

In the quasi-stable state, Q_2 is driven into the OFF state, by the application of a trigger. Consequently, Q_1 goes into the ON state and into saturation as shown in Fig. 8.8(f).

FIGURE 8.8(e) Circuit to calculate V_{B1} due to $-V_{BB}$ sourceFIGURE 8.8(f) In the quasi-stable state, Q_1 is ON and Q_2 is OFF

a) To verify if Q_1 is ON and in saturation or not

To verify whether Q_1 is really in saturation or not, calculate I_{C1} .

$$I_{C1} = I_1 + I_R \quad I_1 = \frac{V_{CC} - V_{CE(\text{sat})}}{R_C} = \frac{10 - 0.3}{1 \text{ k}\Omega} = 9.7 \text{ mA}$$

To calculate I_R the KVL equation of the loop consisting of R_C , C and R is,

$$I_R R = I_1 R_C + V_A = 9.7 \text{ V} + 9.3 \text{ V} = 19 \text{ V} \quad I_R = \frac{19 \text{ V}}{10 \text{ k}\Omega} = 1.9 \text{ mA}$$

Therefore,

$$I_{C1} = I_1 + I_R = 9.7 \text{ mA} + 1.9 \text{ mA} = 11.6 \text{ mA}$$

$$I_{B1(\text{min})} = \frac{I_{C1}}{h_{FE \text{ min}}} = \frac{11.6 \text{ mA}}{30} = 0.39 \text{ mA}$$

To calculate I_{B1} , consider Fig. 8.8(g).

$$I_{B1} = I_3 - I_4$$

$$I_3 = \frac{V_{CC} - V_\sigma}{R_C + R_1} = \frac{10 - 0.7}{1 + 10} = \frac{9.3 \text{ V}}{11 \text{ k}\Omega} = 0.84 \text{ mA}$$

$$I_4 = \frac{V_\sigma - (-V_{BB})}{R_2} = \frac{0.7 + 10}{100 \text{ k}\Omega} = \frac{10.7 \text{ V}}{100 \text{ k}\Omega} = 0.11 \text{ mA}$$

$$I_{B1} = 0.84 - 0.11 = 0.73 \text{ mA}$$

As already calculated, $I_{B1(\text{min})} = 0.39 \text{ mA}$. Thus,

$$I_{B1} \gg I_{B1(\text{min})}.$$

Hence, Q_1 is in saturation.

$$\therefore V_{C1} = 0.3 \text{ V}, \quad V_{B1} = 0.7 \text{ V},$$

$V_{C2} = V_{CC} - I_3 R_C = 10 - (0.84)(1) = 9.16 \text{ V}$ (But for the current, I_3 , V_{C2} should have been 10 V)

$$V_{B2} = V_{CC} - I_R R = 10 - (1.9)(10) = -9 \text{ V}$$

In the quasi-stable state, except V_{B2} —which changes exponentially as a function of time—all other voltages remain unaltered. At $t = T$, when $V_{B2} = V_\gamma$, the quasi-stable state ends and the multivibrator returns to its initial stable condition. The voltages at the beginning of the quasi-stable state are $V_{C1} = 0.3 \text{ V}$, $V_{B1} = 0.7 \text{ V}$, $V_{C2} = 9.16 \text{ V}$, $V_{B2} = -9 \text{ V}$ initially and varies exponentially.

iii) At the end of the quasi-stable state (at $t = T+$)

At the end of the quasi-stable state Q_1 goes OFF and Q_2 goes ON and into saturation, resulting in overshoots at the base of Q_2 and at the collector of Q_1 . The overshoots are calculated using Fig. 8.8(h).

Neglecting the current I_R when compared to I'_{B2} the circuit reduces to Fig. 8.8(i).

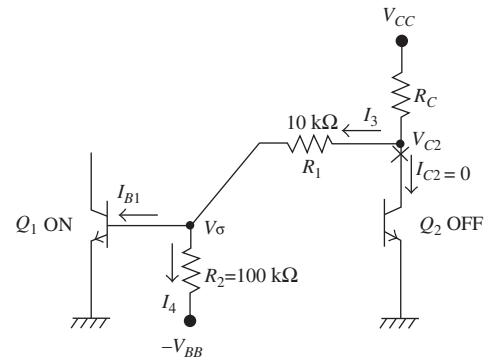


FIGURE 8.8(g) The circuit that is used to calculate I_{B1}

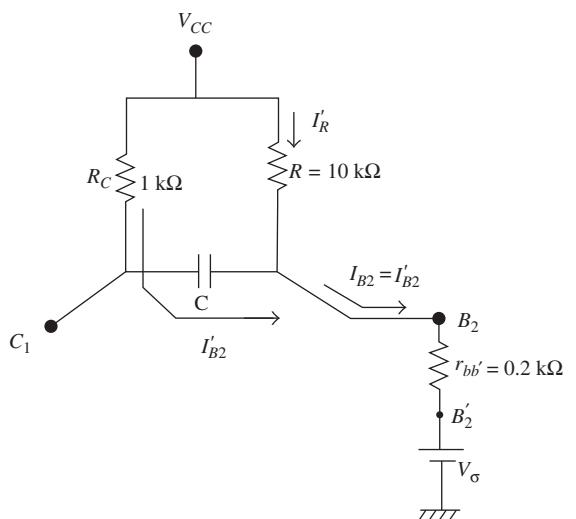


FIGURE 8.8(h) The circuit that is used to calculate I_{B1}

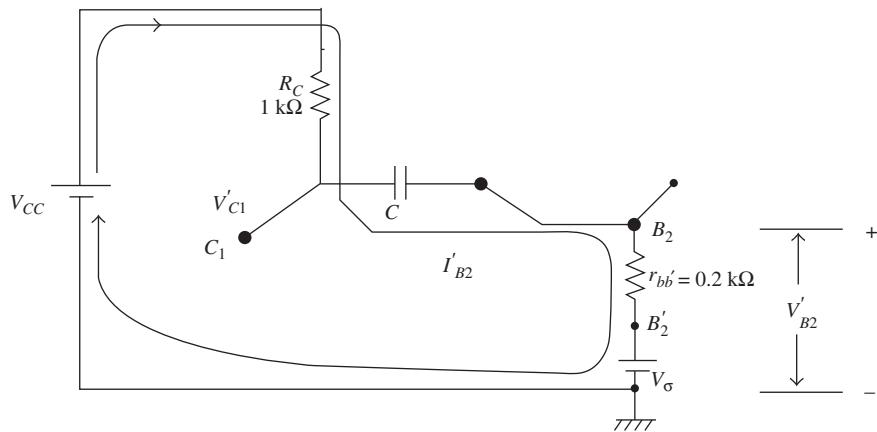


FIGURE 8.8(i) The simplified circuit of Fig. 8.8(h)

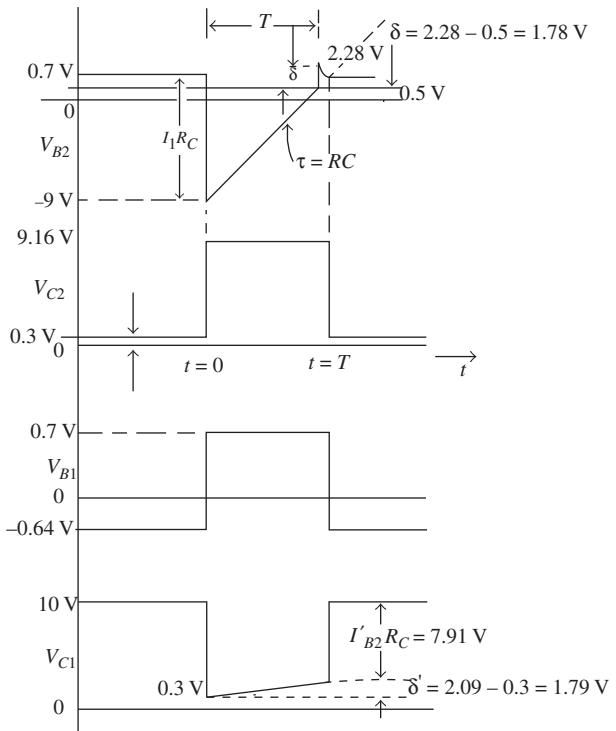


FIGURE 8.8(j) Waveforms of the collector-coupled monostable

Using Eq. (8.34):

$$I'_B2 = \frac{V_{CC} - V_{CE(\text{sat})} - V_\sigma + V_\gamma}{r_{bb'} + R_C}$$

$$= \frac{10 - 0.3 - 0.7 + 0.5}{0.2 + 1} = \frac{9.5 \text{ V}}{1.2 \text{ k}\Omega}$$

$$I'_B2 = 7.91 \text{ mA}$$

$$V'_C1 = V_{CC} - I'_B2 R_C = 10 - (7.91)(1)$$

$$V'_C1 = 2.09 \text{ V}$$

$$V'_B2 = I'_B2 r_{bb'} + V_\sigma$$

$$= (7.91)(0.2) + 0.7 = 1.58 + 0.7$$

$$V'_B2 = 2.28 \text{ V}$$

At $t = T+$, the voltages are $V_{C2} = 0.3 \text{ V}$, $V_{B2} = 2.28 \text{ V}$, $V_{C1} = 10 \text{ V}$, $V_{B1} = -0.64 \text{ V}$. The waveforms are plotted as shown in Fig. 8.8(j).

8.3.4 The Design of a Collector-coupled Monostable Multivibrator

Let us design a collector-coupled monostable multivibrator of Fig. 8.1, having a gate width T . From the circuit of Fig. 8.1 we have,

$$R_C = \frac{V_{CC} - V_{CE(\text{sat})}}{I_{C(\text{sat})}} \quad (8.37)$$

$$I_{B(\text{min})} = \frac{I_{C1(\text{sat})}}{h_{FE(\text{min})}} \quad (8.38)$$

Select $I_{B(\text{sat})} = 2 \times I_{B(\text{min})}$

$$R = \frac{V_{CC} - V_\sigma}{I_{B(\text{sat})}} \quad (8.39)$$

For ON device to be in saturation:

$$R \leq h_{FE} R_C \quad (8.40)$$

On verifying whether the condition in Eq. (8.40) is satisfied or not; the value of R is accepted (if satisfying). If not, the value of R is changed suitably, to satisfy the Eq. (8.40).

Assuming that the current in R_2 is I_2 :

$$I_2 \approx \frac{1}{10} I_C$$

$$R_2 = \frac{V_\sigma + V_{BB}}{I_2}. \quad (8.41)$$

When Q_1 is ON, if I_1 is the current in $(R_C + R_1)$:

$$I_1 = I_{B1} + I_2 \quad (8.42)$$

$$R_C + R_1 = \frac{V_{CC} - V_\sigma}{I_1} \quad (8.43)$$

$$R_1 = (R_C + R_1) - R_C$$

Using the relation, $T = 0.69RC$, the value of C is calculated. To understand the design procedure let us consider an example.

E X A M P L E

Example 8.3: Design a collector-coupled monostable circuit of Fig. 8.1 to generate a pulse of width $100 \mu\text{s}$. Silicon devices with $h_{FE(\text{min})} = 50$ are used. ON device is in saturation.

Given that:

$$V_{CC} = 12 \text{ V}, \quad V_{CE(\text{sat})} = 0.2 \text{ V}, \quad V_{BE(\text{sat})} = 0.7 \text{ V}, \quad I_{B(\text{sat})} = 2 I_{B(\text{min})}, \quad V_{BB} = 12 \text{ V}, \quad I_{C(\text{sat})} = 2 \text{ mA}, \quad T = 100 \mu\text{s}.$$

Solution:

(a) Let Q_2 be ON and Q_1 be OFF.

$$R_{C2} = \frac{V_{CC} - V_{CE(\text{sat})}}{I_{C2(\text{sat})}} = \frac{12 - 0.2}{2 \text{ mA}} = \frac{11.8}{2 \text{ mA}} = 5.9 \text{ k}\Omega \approx 6 \text{ k}\Omega$$

$$I_{B2(\text{min})} = \frac{I_{C2(\text{sat})}}{h_{FE(\text{min})}} = \frac{2 \text{ mA}}{50} = 40 \mu\text{A}$$

$$I_{B2(\text{sat})} = 2 \times I_{B2(\text{min})} = 2 \times 40 = 80 \mu\text{A}$$

$$R = \frac{V_{CC} - V_\sigma}{I_{B2(\text{sat})}} = \frac{12 - 0.7}{80 \mu\text{A}} = \frac{11.3}{80 \times 10^{-6}} = \frac{1130}{8} \times 10^3 = 141 \text{k}\Omega$$

$$h_{FE} R_C = 50 \times 6 = 300 \text{k}\Omega$$

For ON device to be in saturation,

$$R \leq h_{FE} R_C$$

Hence, the condition is verified.

(b) When Q_1 is ON, let I_2 be the current in R_2 .

$$I_2 \approx \frac{1}{10} I_{C(\text{sat})} = 0.2 \text{ mA} \quad R_2 = \frac{V_\sigma + V_{BB}}{I_2} = \frac{12.7}{0.2} = 63.5 \text{k}\Omega$$

Let I_1 be the current in $R_C + R_1$.

$$I_1 = I_{B1} + I_2 = 0.08 + 0.2 = 0.28 \text{ mA}$$

$$R_C + R_1 = \frac{V_{CC} - V_\sigma}{I_1} = \frac{12 - 0.7}{0.28 \text{ mA}} = 40 \text{k}\Omega$$

$$R_1 = (R_C + R_1) - R_C = 40 - 6 = 34 \text{k}\Omega$$

$$T = 0.69 R_C \quad 100 \times 10^{-6} \text{ s} = 0.69 \times 141 \times 10^3 \times C$$

$$C = \frac{100 \times 10^{-6}}{0.69 \times 141 \times 10^3} = \frac{100}{7 \times 14} \times 10^{-9} \approx 1 \text{nF}$$

8.4 COMMUTATING CAPACITORS

In the initial stable state Q_2 is ON and in saturation, Q_1 is OFF. Once a trigger is applied [see Fig. 8.3] to change the state of the devices in the monostable multivibrator, because of the stray capacitances of the devices they may not go into the next state immediately. This is a problem which needs to be overcome.

Now, let a negative pulse be applied at the base Q_2 to drive it into the OFF state and consequently Q_1 into the ON state. Prior to the application of this trigger the voltage at the second collector was $V_{CE(\text{sat})}$. On the application of a trigger at $t = 0$, as Q_2 goes into the OFF state, the voltage at its collector rises from $V_{CE(\text{sat})}$ to V_{CC} . Let the change in voltage at the second collector be v_i , a step voltage. That is,

$$v_i = V_{CC} - V_{CE(\text{sat})} \quad (8.44)$$

This voltage change at the second collector is coupled to the first base through R_1 and R_2 , as shown in Fig. 8.9(a). As a result, Q_1 is expected to switch into the ON state.

If the attenuator is a simple resistive attenuator as seen in Fig. 8.9(a), the moment Q_2 switches into the OFF state, Q_1 quickly switches into the ON state. However, between the input terminals of Q_1 if a stray capacitance C_i is present, then the attenuator circuit in Fig. 8.9(a) gets modified as shown in Fig. 8.9(b).

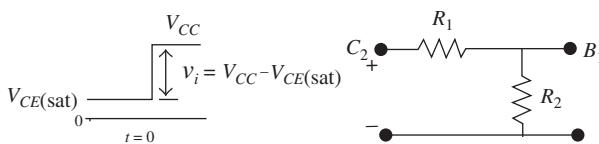


FIGURE 8.9(a) A simple resistive attenuator

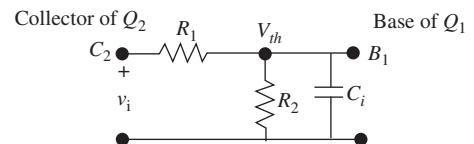


FIGURE 8.9(b) An attenuator considering the stray capacitance

To reduce this two loop network into a single loop network, let us Thévenise the circuit.

$$V_{th} = v_i \frac{R_2}{R_1 + R_2} = \alpha V_i \quad (8.45)$$

where

$$\alpha = \frac{R_2}{R_1 + R_2} \quad (8.46)$$

and

$$R_{th} = R_1 || R_2 \quad (8.47)$$

Then the circuit shown in Fig. 8.9(b) reduces to that shown in Fig. 8.9(c).

Now, only when the voltage at B_1 rises to 90 per cent of its final value, the device Q_1 is assumed to switch from the OFF state into the ON state. This time interval is the rise-time of the circuit.

$$t_r = 2.2R_{th}C_i \quad (8.48)$$

As an example, if $R_1 = R_2 = 1 \text{ M}\Omega$, $R_{th} = 0.5 \text{ M}\Omega$ and if $C_i = 10 \text{ nF}$ then:

$$t_r = 2.2 \times 0.5 \times 10^6 \times 10 \times 10^{-9} = 11 \text{ ms}$$

Having applied a trigger at $t = 0$ so as to switch Q_2 into the OFF state and consequently Q_1 into the ON state, it is understood that Q_1 will not go into the ON state unless a time period of 11 ms elapses from the instant the trigger is applied, which is a large time delay and is not acceptable. Such an attenuator is called uncompensated attenuator. From the above discussion, it is evident that conduction is transferred from Q_2 to Q_1 after a finite time interval (11 ms) from the instant the trigger is applied. This time delay is called the transition time. Transition time is, therefore, defined as the time taken for conduction to be transferred from one device to the other. This means that transition time is the time interval from the instant the trigger is applied at the base of Q_2 which is ON to the instant when Q_1 switches ON. To reduce this transition time condenser C_1 is connected in shunt with resistor R_1 , as shown in Fig. 8.9(d).

Then the attenuator circuit shown in Fig. 8.9(d) is redrawn as shown in Fig. 8.9(e).

The circuit shown in Fig. 8.9(e) is in the form of a bridge comprising of four arms— R_1 , C_1 , R_2 and C_i . The bridge is said to be balanced when $R_1C_1 = R_2C_i$. If this condition is satisfied, then the current in the loop XY is zero and it appears as though there is no physical connection between X and Y , as shown in Fig. 8.9(f). The net result is that the output is calculated independently, either by considering the capacitance combination or the resistance combination.

As discussed in section 3.4.1, at $t = 0+$, C_1 and C_i decides the output and at $t = \infty$, R_1 and R_2 decide. As the voltage at the base of Q_1 abruptly rises, Q_1 goes into the ON state almost instantaneously. Therefore, with this arrangement the moment a trigger is applied, conduction is transferred from Q_2 to Q_1 . Obviously, transition time is drastically reduced by using a compensated attenuator, as shown in Fig. 8.9(f). If the output at $v_o(0+) = v_o(\infty)$ then this attenuator is a perfect attenuator. Here C_2 is the collector of Q_2 and B_1 is the base of Q_1 .

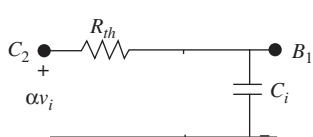


FIGURE 8.9(c) An attenuator circuit with Thévenin source and its internal resistance

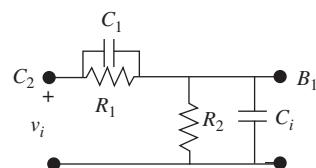


FIGURE 8.9(d) An attenuator circuit with condenser C_1 in shunt with resistor R_1

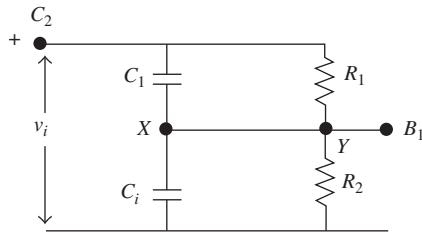


FIGURE 8.9(e) The redrawn circuit of Fig. 8.9(d)

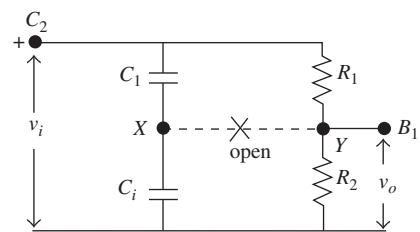


FIGURE 8.9(f) The compensated attenuator

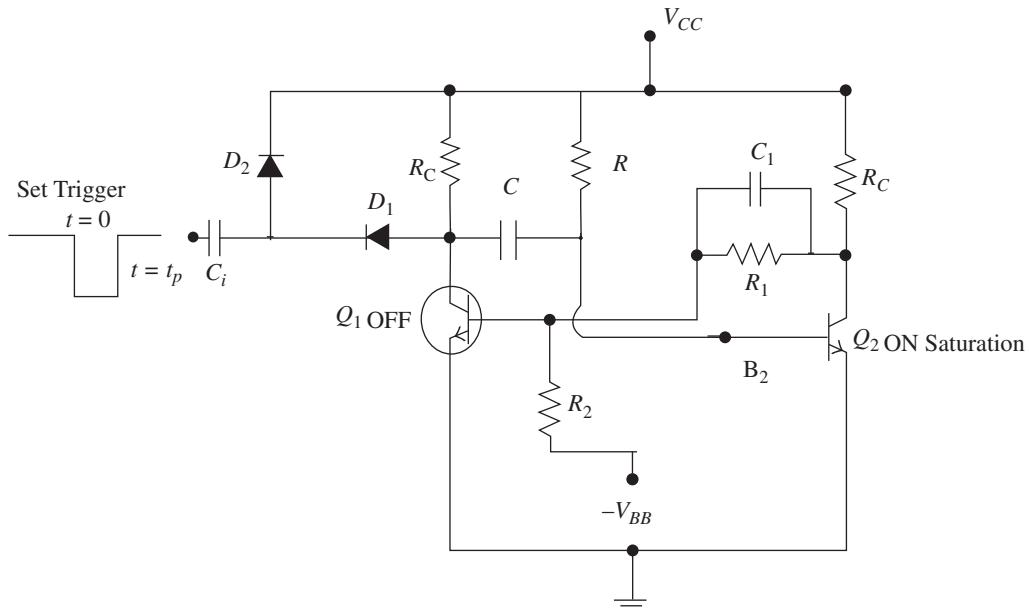


FIGURE 8.9(g) The collector-coupled monostable multivibrator using commutating condenser

As the capacitor C_1 is connected in shunt with resistor R_1 it helps in reducing the transition time, this capacitor is called the speed-up capacitor, commutating condenser or transpose capacitor. The collector-coupled monostable multivibrator using commutating condenser is shown in Fig. 8.9(g).

8.4.1 Calculation of the Value of the Commutating Condenser

If C_1 is the commutating condenser then,

$$C_1 = \frac{R_2}{R_1} C_i \quad (8.49)$$

where, C_i is the stray capacitance at the input of the transistor and using Eq. (8.49), C_1 can be calculated. In the absence of any specification of C_i , $R_1 C_1$ is typically chosen as $1 \mu\text{s}$.

8.4.2 A Monostable Multivibrator as a Voltage-to-time Converter

A monostable multivibrator can be used as a voltage-to-time converter, in which the time duration is a function of voltage, as shown in Fig. 8.10(a). The time, T for which Q_1 , in the quasi-stable state, is ON and Q_2 is OFF is calculated. Now, consider the voltage variations at B_2 , as shown in Fig. 8.10(b).

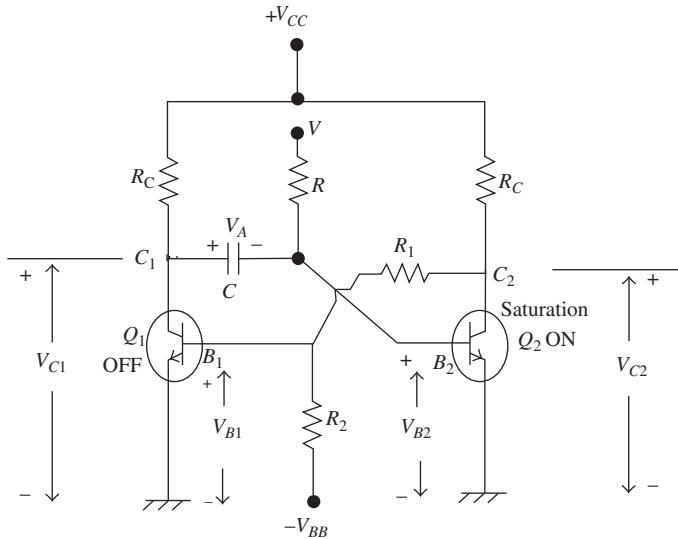
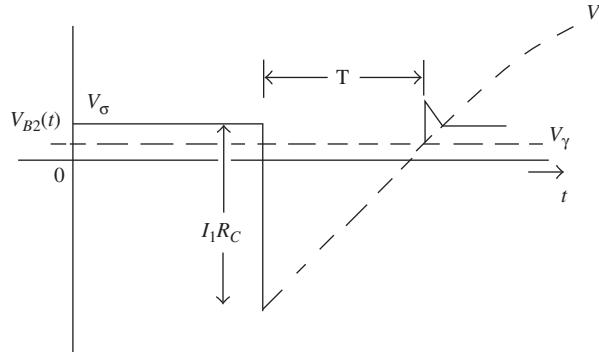


FIGURE 8.10(a) The monostable multivibrator as a voltage-to-time converter

FIGURE 8.10(b) Voltage variation at B_2

$$V_{B2}(t) = v_f - (v_f - v_i)e^{-t/\tau} \quad v_f = V \quad v_i = V_\sigma - I_1 R_C$$

If Q_1 is in saturation,

$$I_1 R_C = V_{CC} - V_{CE(\text{sat})} \quad v_i = V_\sigma - V_{CC} + V_{CE(\text{sat})}$$

$$V_{B2}(t) = V - [V - V_\sigma + V_{CC} - V_{CE(\text{sat})}] e^{-t/\tau} \quad (8.50)$$

At $t = T$,

$$V_{B2}(t) = V_\gamma \quad V_\gamma = V - [V - V_\sigma + V_{CC} - V_{CE(\text{sat})}] e^{-T/\tau}$$

As V_γ , V_σ and $V_{CE(\text{sat})}$ are small when compared to V and V_{CC} ,

$$0 = V - (V + V_{CC}) e^{-T/\tau}$$

$$T = \tau \ln \frac{(V + V_{CC})}{V} \quad T = \tau \ln \left(1 + \frac{V_{CC}}{V}\right) \quad (8.51)$$

Thus, to change T , V can be varied. As the pulse width is a function of V , the monostable multivibrator is called a voltage-to-time converter.

8.5 Emitter-Coupled Monostable Multivibrators

In the collector-coupled monostable circuit, for the gate width T to be stable, the ON device, in the quasi-stable state, is required to be driven into saturation [see Eq. (8.2)]. Once a device is driven into saturation the storage time becomes longer. Hence, the switching speed of the multivibrator is reduced, which is considered as the main limitation of this circuit.

Further, as there is a cross-coupling from the second collector to the first base in the collector-coupled monostable multivibrator, if the cross-coupling network loads the collector circuit, the voltage change at this collector may not necessarily be V_{CC} . This reduced voltage change at the second collector may not in turn drive Q_1 into saturation, in the quasi-stable state. These limitations can be eliminated in an emitter-coupled monostable multivibrator, as shown in Fig. 8.11(a).

In this circuit, there is no cross-coupling from the second collector to the first base. Hence, the second collector is not loaded by this cross-coupling network. Therefore, the second collector is an appropriate point at which the output can be taken.

The first base is not involved in regeneration and hence, becomes a suitable point at which the trigger can be injected. When Q_1 is driven into the ON state in the quasi-stable state of a collector-coupled monostable multivibrator, the current I_1 in Q_1 cannot be stable and thus, Q_1 is preferably driven into saturation to make gate width, T stable. However, in the emitter-coupled monostable multivibrator when Q_1 goes ON, the current I_1 in Q_1 can be maintained stable because of a substantial emitter resistance (provides negative feedback), even if the device is in the active region. This reduces the storage time and hence, improves the switching speed of the multivibrator. The operation of the multivibrator in Fig. 8.11(a) is explained in the following paragraphs.

In the stable state, let Q_1 be OFF and Q_2 be ON and in saturation, as shown in Fig 8.11(b). During this period, the capacitor C charges through R_{C1} , and the input resistance between the base and reference terminal, R_{i2} . The charging time constant is $(R_{C1} + R_E + r_{bb'}) C$.

To drive the multivibrator into the quasi-stable state, a positive pulse of proper magnitude is applied at the base of Q_1 , as shown in Fig. 8.11(d). As a result, Q_1 is driven into the active region and Q_2 into the OFF state.

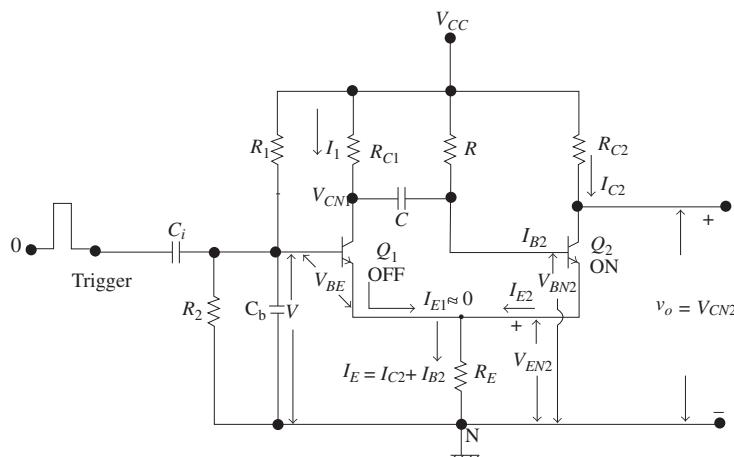
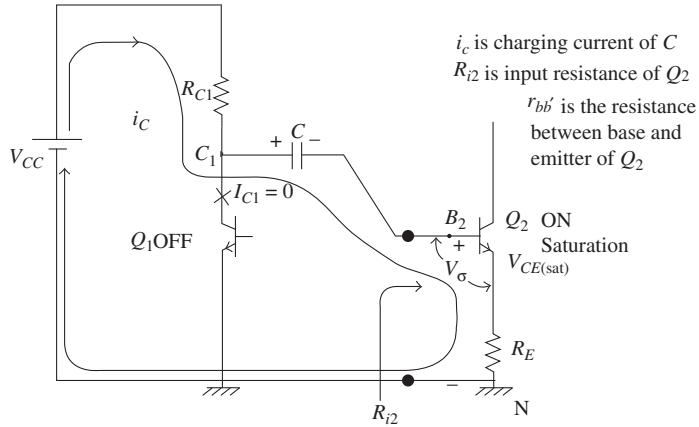
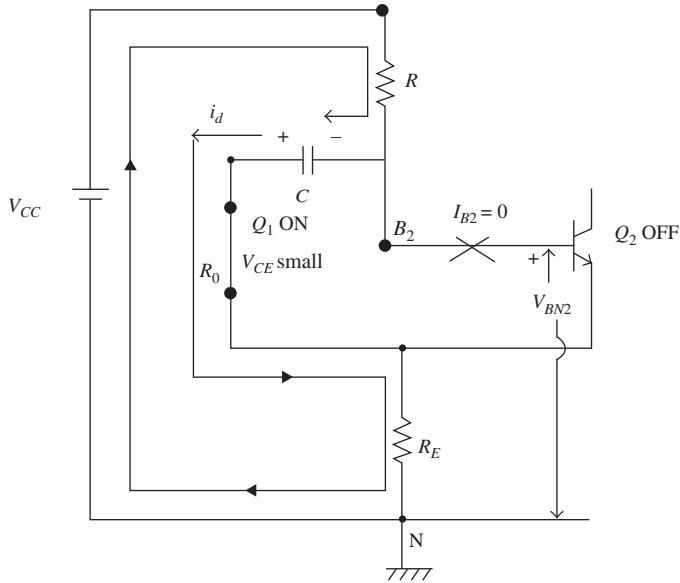


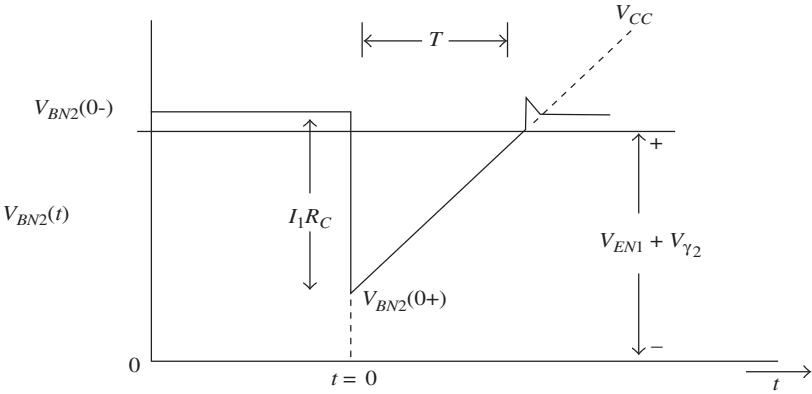
FIGURE 8.11(a) The emitter-coupled monostable multivibrator

FIGURE 8.11(b) In the stable state, Q_1 is OFF and Q_2 is ONFIGURE 8.11(c) Discharge of capacitor C in the quasi-stable state when Q_1 is ON and Q_2 is OFF

Now, the capacitor C discharges through the small resistance between the collector and emitter terminals of Q_1 , R_E and R . As a result, the voltage at B_2 varies as a function of time. When the voltage at B_2 is such that it drives Q_2 into the ON state, the multivibrator comes back into the initial stable condition of Q_1 OFF and Q_2 ON. The discharging time constant is $C(R_o + R_E + R) \approx RC$ as $R >> (R_E + R_o)$.

8.5.1 To Calculate the Gate Width (T)

To calculate the gate width T , consider the voltage variation at the base of Q_2 , as shown in Fig. 8.11(d). In the stable state, Q_1 is OFF and Q_2 is ON and in saturation. Let $V_{BN2}(0-)$ be the voltage at B_2 in the stable state. At $t = 0$, a trigger is applied, Q_1 goes ON and the voltage at its collector falls by $I_1 R_C$. A similar change in the voltage occurs at the second base. Therefore, V_{BN2} also falls by $I_1 R_C$. Now the charge on the capacitor

FIGURE 8.11(d) Voltage variation at the base of Q_2

C discharges with a time constant $\tau \approx RC$. The moment the voltage at the second base is $(V_{EN1} + V_{\gamma_2})$, Q_2 again goes into the ON state and Q_1 into the OFF state, thus ending the quasi-stable condition. The voltage at the base of Q_2 at any given time, after the application of a trigger, is given by:

$$V_{BN2}(t) = v_f - (v_f - v_i)e^{-t/\tau}$$

$$v_f = V_{CC}$$

$$v_i = V_{BN2}(0-) - I_1 R_{C1}$$

$$V_{BN2}(t) = V_{CC} - (V_{CC} - V_{BN2}(0-) + I_1 R_{C1})e^{-t/\tau}$$

At $t = T$, $V_{BN2}(T) = V_{EN1} + V_{\gamma_2}$

Therefore,

$$V_{EN1} + V_{\gamma_2} = V_{CC} - (V_{CC} - V_{BN2}(0-) + I_1 R_{C1})e^{-T/\tau}$$

$$T = \tau \ln \frac{V_{CC} - V_{BN2}(0-) + I_1 R_{C1}}{V_{CC} - V_{EN1} - V_{\gamma_2}} \quad (8.52)$$

The gate width T can be calculated using Eq. (8.52). To plot the waveforms of an emitter-coupled monostable multivibrator, we calculate the voltages in the stable state, in the quasi-stable state and when the multivibrator returns to its original stable state.

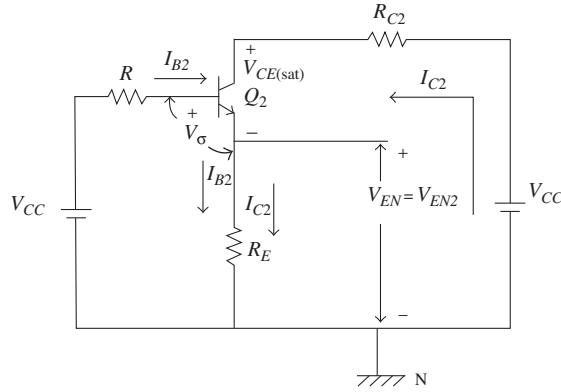
8.5.2 To Calculate the Voltages

Consider the emitter-coupled monostable multivibrator shown in Fig. 8.11(a).

In the Stable State ($t < 0$). Q_1 is OFF and Q_2 is ON and in saturation. To verify this, the base current and collector current of Q_2 are calculated. For this, calculations are made assuming Q_2 is in saturation. When Q_2 is ON and Q_1 is OFF, the circuit shown in Fig. 8.11(a) reduces to the circuit as shown in Fig. 8.12(a).

Writing the KVL equations of the input and output loops, we calculate I_{B2} and I_{C2} and find out $I_{B2(\min)}$ using the relation, $I_{B2(\min)} = I_{C2}/h_{FE(\min)}$. For Q_2 to be in saturation, select $I_{B2(\text{sat})} = 1.5 I_{B2(\min)}$. If $I_{B2} >> I_{B2(\text{sat})}$, Q_2 is in saturation. Hence, the assumption made that Q_2 is in saturation is verified. If Q_2 is in saturation, the voltage between the collector and the emitter is $V_{CE(\text{sat})}$ and the voltage between the base and the emitter is $V_{BE(\text{sat})} = V_{\sigma}$. Therefore:

$$V_{EN} = V_{EN2} = (I_{B2} + I_{C2})R_E \quad (8.53)$$

FIGURE 8.12(a) Circuit when Q_2 is ON and Q_1 is OFF

Is Q_1 OFF or not?

$$V_{BE1} = V_{BN1} - V_{EN2} \quad (8.54)$$

If V_{BE1} reverse-biases the base emitter diode then Q_1 is OFF; if Q_1 is really OFF, then in the stable state

$$V_{CN1} = V_{CC}$$

$$V_{CN2} = V_{EN2} + V_{CE(sat)} \quad (8.55)$$

$$V_{BN2} = V_{EN2} + V_\sigma \quad (8.56)$$

The voltage across the capacitor, V_A is:

$$V_A = V_{CN1} - V_{BN2} \quad (8.57)$$

Calculations at $t = 0+$. At the beginning of the quasi-stable state, at $t = 0$, when a trigger is applied, Q_1 goes ON and into the active region and Q_2 goes OFF. The equivalent circuit with which the calculations are made is shown in Fig. 8.12(b).

If Q_1 is in the active region, $V_\gamma < V_{BE1} < V_\sigma$, $V_{EN} = V_{EN1} = V - V_{BE1}$.

$$I_{B1} + I_{C1} = \frac{V_{EN1}}{R_E} \quad (8.58)$$

Also:

$$I_{B1} + I_{C1} = I_{C1} \left(1 + \frac{I_{B1}}{I_{C1}} \right) = I_{C1} \left(1 + \frac{1}{h_{FE}} \right)$$

Using Eqs. (8.58) and (8.59):

$$\frac{V_{EN1}}{R_E} = I_{C1} \left(\frac{1 + h_{FE}}{h_{FE}} \right) \quad (8.59)$$

$$\therefore I_{C1} = \frac{V_{EN1}}{R_E} \left(\frac{h_{FE}}{1 + h_{FE}} \right) \quad (8.60)$$

Also, we have:

$$I_{C1} = I_1 + I_R \quad (8.61)$$

Writing the KVL equation of the loop containing R_{C1} , C and R in terms of I_1 and I_R :

$$I_R R = I_1 R_C + V_A \quad (8.62)$$

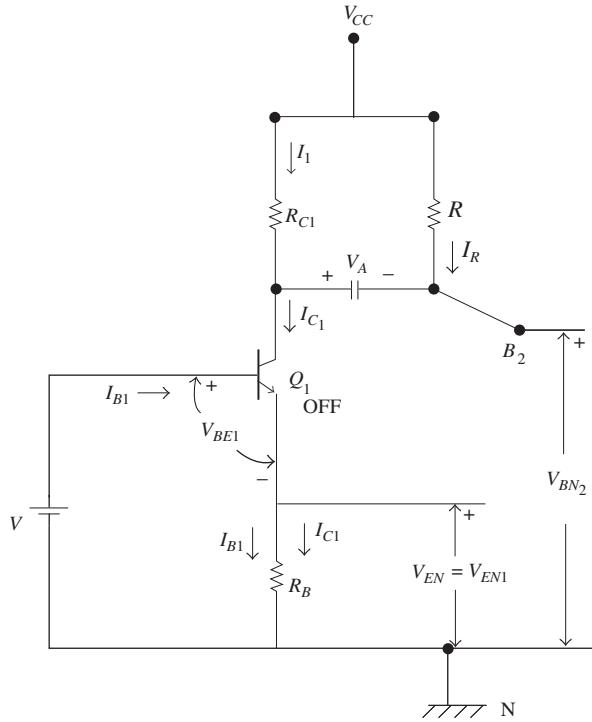


FIGURE 8.12(b) Equivalent Circuit in the Quasi-stable state

Solving Eqs. (8.61) and (8.62), we get the values of I_1 and I_R . Therefore, at $t = 0+$, we have,

$$V_{CN2} = V_{CC} \quad V_{CN1} = V_{CC} - I_1 R_{C1}$$

$$V_{EN} = V_{EN1}$$

$$V_{BN2} = V_{CC} - I_R R \quad V_{BN2} = V_{BN2}(0+)$$

Is Q_1 in the active state as assumed? To verify this, V_{CB1} is to be found out and seen whether this voltage reverse-biases the collector base diode by a reasonable amount or not.

$$V_{CB1} = V_{CN1} - V_{BN1}$$

If V_{CB1} reverse-biases the base collector diode, Q_1 is in the active region as assumed.

Calculations at $t = T-$ (Just Prior to the Completion of the Quasi-stable state). During the quasi-stable state V_{CN2} , V_{EN1} and I_{C1} remain constant and V_{BN2} varies. At $t = T-: V_{BN2} = V_{EN1} + V_{\gamma 2}$.

Therefore,

$$I_R = \frac{V_{CC} - V_{BN2}(T-)}{R} \quad (8.63)$$

As I_{C1} is constant:

$$I_1 = I_{C1} - I_R$$

Therefore,

$$V_{CN1} = V_{CC} - I_1 R_{C1}. \quad (8.64)$$

The voltage across the capacitor V_A at $t = T-$ is

$$V_A(T-) = V_{CN1} - V_{BN2}. \quad (8.65)$$

At the End of the Quasi-stable State (At $t = T+$). At $t = T+$, Q_1 is switched OFF and Q_2 is switched ON and will be in saturation. The equivalent circuit is shown in Fig 8.12(c). As $R \gg R_{C1}, I'_{B2} \gg I_R$, therefore, $I'_{B2} + I_R \approx I'_{B2}$.

Thus, the circuit shown in Fig. 8.12(c) reduces to that shown in Fig. 8.12(d). Writing the KVL equations of the input and output loops:

$$V_{CC} - (V_A + V_\sigma) = I'_{B2}(R_{C1} + r_{bb'} + R_E) + I'_{C2}R_E \quad (8.66)$$

$$V_{CC} - V_{CE(\text{sat})} = I'_{B2}R_E + I'_{C2}(R_{C2} + R_E) \quad (8.67)$$

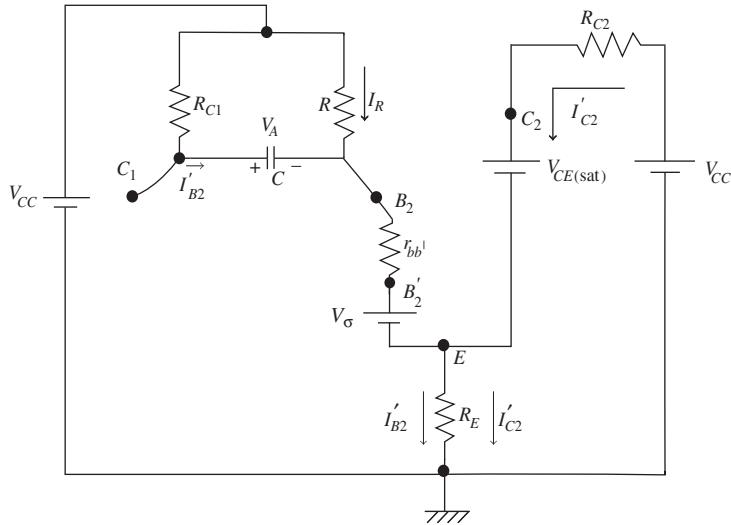


FIGURE 8.12(c) The equivalent circuit at the end of the quasi-stable state

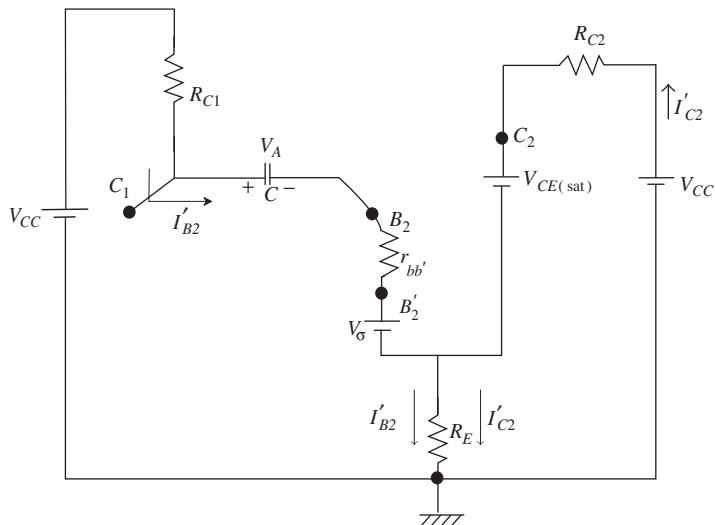


FIGURE 8.12(d) The simplified circuit of Fig. 8.12(c)

Solving Eqs. (8.66) and (8.67), we get I'_{B2} and I'_{C2} . The voltages at $t = T+$ are

$$V_{EN} = V'_{EN2} = (I'_{B2} + I'_{C2})R_E \quad (8.68)$$

$$V_{CN2} = V'_{EN2} + V_{CE(\text{sat})} \quad (8.69)$$

$$V_{CN1} = V_{CC} - I'_{B2}R_{C1} \quad (8.70)$$

$$V_{BN2} = V'_{EN2} + V_\sigma + I'_{B2}r_{bb'} \quad (8.71)$$

Using these calculations, the waveforms can be plotted. To understand the procedure of calculating the voltages and plot the waveforms to scale, let us consider an example.

EXAMPLE

Example 8.4: For the emitter-coupled monostable multivibrator shown in Fig. 8.11(a), $V_{CC} = 15$ V, $R = 100$ k Ω , $R_{C1} = 5$ k Ω , $R_{C2} = 5$ k Ω , $V = 6$ V, $h_{FE} = 40$. Calculate the voltages, and plot the waveforms to scale. Calculate the gate width.

Solution:

(a) In the stable state ($t < 0$) :

The equivalent circuit in the stable state is as shown in Fig. 8.13(a). Let silicon transistors be used for which,

$$V_{BE(\text{sat})} = V_\sigma = 0.7 \text{ V} \quad h_{FE(\text{min})} = 40$$

$$V_{CE(\text{sat})} = 0.2 \text{ V} \quad r_{bb'} = 0.1 \text{ k}\Omega$$

Writing the KVL equations of the input and output loops

$$15 - 0.7 = 104 I_{B2} + 4 I_{C2}$$

$$15 - 0.2 = 4 I_{B2} + 9 I_{C2}$$

Solving these two equations:

$$I_{B2} = 0.075 \text{ mA} \quad I_{C2} = 1.61 \text{ mA}$$

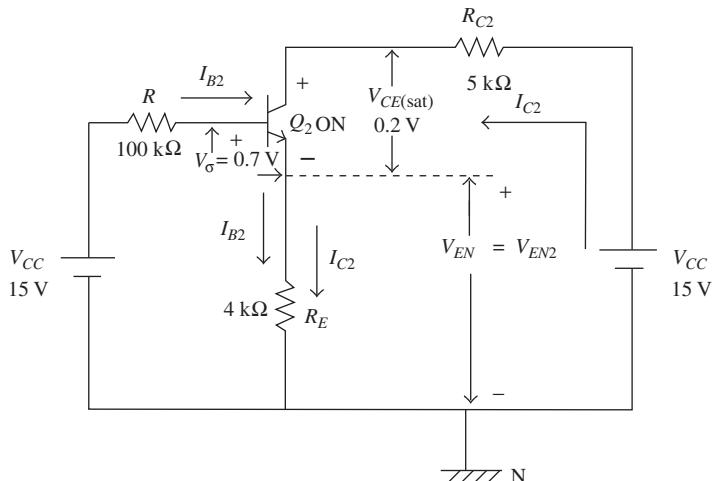


FIGURE 8.13(a) Circuit when Q_2 is ON and Q_1 is OFF

$$I_{B2(\min)} = \frac{I_{C2}}{h_{FE}(\min)} = \frac{1.61 \text{ mA}}{40} = 0.040 \text{ mA}$$

For Q_2 to be in saturation let $I_{B2(\text{sat})} = 1.5I_{B2(\min)}$.

Therefore, $I_{B2(\text{sat})} = 1.5 \times 0.04 = 0.06 \text{ mA}$

As $I_{B2} \gg I_{B2(\text{sat})}$, Q_2 is in saturation. Hence, the assumption made, that Q_2 is in saturation is verified.

$$\therefore V_{EN} = V_{EN2} = (I_{B2} + I_{C2})R_E = (0.075 + 1.61)4 = 6.74 \text{ V}$$

Is Q_1 OFF or not?

$$V_{BE1} = V_{BN1} - V_{EN2} = 6 \text{ V} - 6.74 \text{ V} = -0.74 \text{ V}$$

Hence, Q_1 is OFF. Therefore,

$$V_{CN1} = 15 \text{ V}$$

$$V_{CN2} = V_{EN2} + V_{CE(\text{sat})} = 6.74 + 0.2 = 6.94 \text{ V}$$

$$V_{BN2} = V_{EN2} + V_\sigma = 6.74 + 0.7 = 7.44 \text{ V}$$

The voltage across the capacitor, V_A is,

$$V_A = V_{CN1} - V_{BN2} = 15 - 7.44 = 7.56 \text{ V}$$

The voltages in the stable state are:

$$V_{EN2} = 6.74 \text{ V}, \quad V_{CN1} = 15 \text{ V}, \quad V_{CN2} = 6.94 \text{ V}, \quad V_{BN2} = 7.44 \text{ V}$$

(b) Calculations at $t = 0+$:

At $t = 0$, when a trigger is applied, Q_1 goes ON and into active region and Q_2 goes OFF. The equivalent circuit is as shown in Fig. 8.13(b). If Q_1 is in the active region,

$$V_{BE1} = 0.6 \text{ V}$$

$$V_{EN} = V_{EN1} = 6 - 0.6 = 5.4 \text{ V}$$

$$I_{B1} + I_{C1} = \frac{V_{EN1}}{R_E} = \frac{5.4 \text{ V}}{4 \text{ k}\Omega} = 1.35 \text{ mA}$$

$$I_{B1} + I_{C1} = I_{C1} \left(1 + \frac{I_{B1}}{I_{C1}} \right) = I_{C1} \left(1 + \frac{1}{h_{FE}} \right) = I_{C1} \left(\frac{1 + h_{FE}}{h_{FE}} \right)$$

$$I_{C1} \left(\frac{1 + h_{FE}}{h_{FE}} \right) = 1.35 \text{ mA} \quad I_{C1} = 1.35 \times \frac{40}{41} \approx 1.3 \text{ mA}$$

Therefore, $I_1 + I_R = 1.3 \text{ mA}$

(1)

Writing the KVL equation of the loop containing R_{C1} , C and R :

$$100I_R = 5I_1 + V_A \quad 5I_1 - 100I_R = -V_A \quad 5I_1 - 100I_R = -7.56 \text{ V} \quad (2)$$

Solving Eqs (1) and (2) for I_1 and I_R ,

$$I_R = 0.134 \text{ mA}, \quad I_1 = 1.166 \text{ mA}$$

Therefore, at $t = 0+$,

$$V_{CN2} = V_{CC} = 15 \text{ V}$$

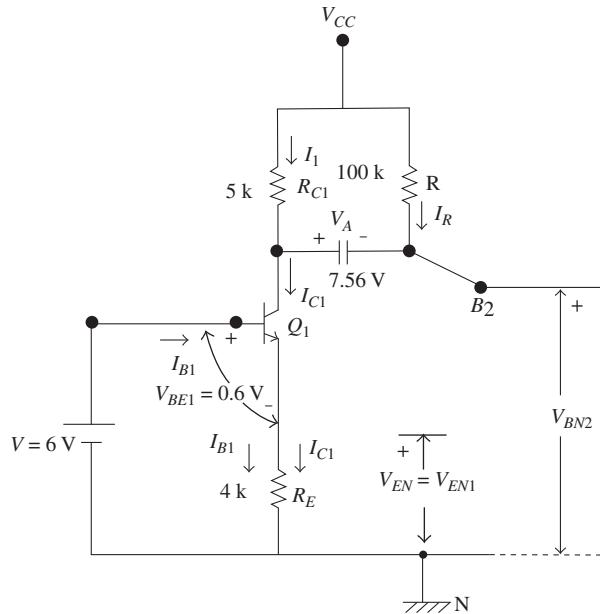


FIGURE 8.13(b) The equivalent circuit in quasi-stable state

$$V_{CN1} = V_{CC} - I_1 R_{C1} = 15 - (1.166)(5) = 15 - 5.83 = 9.17 \text{ V}$$

$$V_{BN2} = V_{CC} - I_R R = 15 - (0.134)(100) = 1.6 \text{ V}$$

$$V_{BN2} = V_{BN2}(0+) = 1.6 \text{ V}$$

Is Q_1 in the active as assumed? To verify this, V_{CB1} is to be found out and seen whether this voltage reverse-biases the collector base diode by a reasonable amount or not.

$$V_{CB1} = V_{CN1} - V_{BN1} = 9.17 - 6 = 3.17 \text{ V}$$

Hence, Q_1 is in the active region. The voltages at the beginning of the quasi-stable are:

$$V_{BN2} = 1.6 \text{ V}, \quad V_{EN} = 5.4 \text{ V}, \quad V_{CN1} = 9.17 \text{ V}, \quad V_{CN2} = 15 \text{ V}$$

(c) Calculations at $t = T-$ (i.e., just prior to the completion of the quasi-stable state):

During the quasi-stable state V_{CN2} , V_{EN1} and I_{C1} remain constant and V_{BN2} varies.

At $t = T-$

$$V_{BN2}(T-) = V_{EN1} + V_{\gamma 2} = 5.4 \text{ V} + 0.5 \text{ V} = 5.9 \text{ V}$$

Therefore,

$$I_R = \frac{V_{CC} - V_{BN2}(T-)}{R}$$

$$\frac{15 - 5.9}{100 \text{ k}\Omega} = 0.091 \text{ mA}$$

As I_{C1} is constant,

$$I_1 = I_{C1} - I_R = 1.3 \text{ mA} - 0.091 \text{ mA} = 1.209 \text{ mA}$$

$$V_{CN1} = V_{CC} - I_1 R_{C1} = 15 - (1.209)5 = 15 - 6.04 = 8.96 \text{ V}$$

The voltage across the capacitor V_A at $t = T -$ is:

$$V_A(T-) = V_{CN1} - V_{BN2} = 8.96 - 5.9 = 3.06 \text{ V.}$$

(d) At $t = T +$ i.e., at the end of the quasi-stable state:

At $t = T+$, Q_1 is switched OFF and Q_2 is switched ON and will be in saturation. The equivalent circuit is shown in Fig. 8.13(c). Writing the KVL equations of the input and output loops:

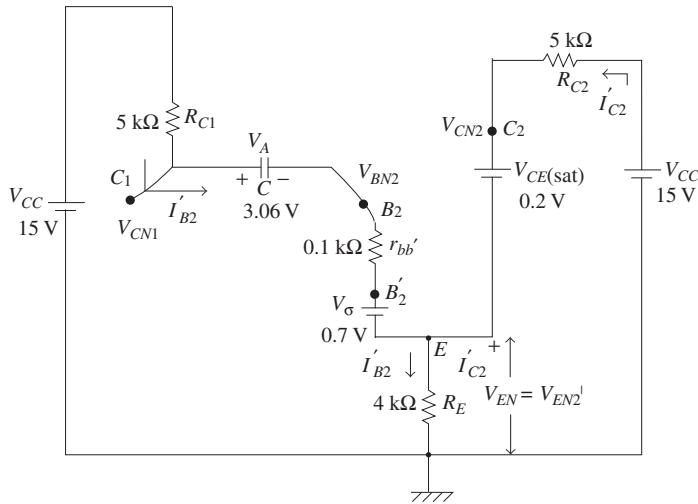


FIGURE 8.13(c) The simplified circuit

$$15 - 3.06 - 0.7 = 9.1I'_{B2} + 4I'_{C2} \quad 15 - 0.2 = 4I'_{B2} + 9I'_{C2}$$

$$11.24 = 9.1I'_{B2} + 4I'_{C2} \quad 14.8 = 4I'_{B2} + 9I'_{C2}$$

Solving for I'_{B2} and I'_{C2} :

$$I'_{B2} = 0.668 \text{ mA}, \quad I'_{C2} = 1.29 \text{ mA}$$

$$\therefore V_{EN} = V'_{EN2} = (I'_{B2} + I'_{C2})R_E = (0.668 + 1.29)4 = 7.832 \text{ V}$$

$$V_{CN2} = V'_{EN2} + V_{CE(\text{sat})} = 7.832 + 0.2 = 8.032 \text{ V}$$

$$V_{CN1} = V_{CC} - I_{B2}' R_{C1} = 15 - 0.668 \times 5 = 11.66 \text{ V}$$

$$V_{BN2} = V'_{EN2} + V_\sigma + I'_{B2} r_{bb'} = 7.832 + 0.7 + (0.668 \times 0.1) = 8.599 \text{ V}$$

If $C = 0.01 \mu\text{F}$, gate width using Eq. (8.52) is:

$$\begin{aligned} T &= \tau \ln \left(\frac{15 - 7.44 + 5.83}{15 - 5.4 - 0.5} \right) = \tau \ln \left(\frac{13.39}{9.1} \right) \\ &= 100 \times 10^3 \times 0.01 \times 10^{-6} \ln \left(\frac{13.39}{9.1} \right) = 0.386 \text{ ms} \end{aligned}$$

The voltages at the end of the quasi-stable state are $V_{CN1} = 11.66 \text{ V}$, $V_{CN2} = 8.032 \text{ V}$, $V_{EN} = 7.832 \text{ V}$, $V_{BN2} = 8.599 \text{ V}$. The waveforms are shown in Fig. 8.13(d).

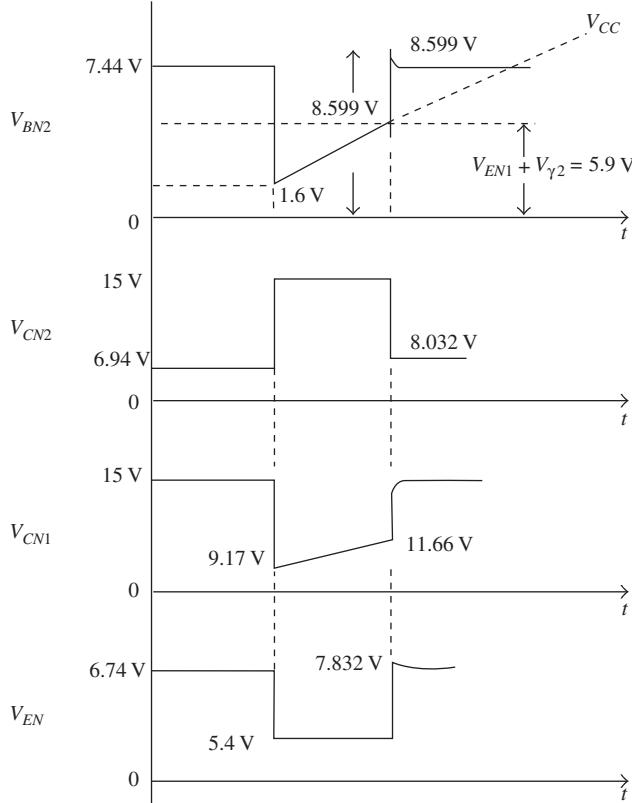


FIGURE 8.13(d) Waveforms of an emitter-coupled monostable multivibrator

8.5.3 The Design of an Emitter-coupled Monostable Multivibrator

Now, in the design of an emitter-coupled monostable multivibrator, we fix the component values of the monostable multivibrator shown in Fig. 8.11(a). To begin with, choose V , $I_C(\text{sat})$. The choice of V is based on the following considerations:

i) V should be sufficiently large to keep Q_1 OFF in the stable state. As, in the stable state Q_2 is in saturation, its emitter current I_{E2} develops a voltage in R_E , $V_{EN} = V_{EN2}$. Q_1 can be ON only when $V_{BN1} > V_{EN2} + V_\gamma$. Therefore, the maximum value of V , say, $V_{(\text{max})}$ can be:

$$V_{(\text{max})} = V_{EN2} + V_\gamma. \quad (8.72)$$

ii) The collector current in Q_1 , when in the quasi-stable state, should be large so as to be able to drive Q_2 into the OFF state. To derive this maximum collector current, the bias voltage for Q_1 should be minimum, say $V_{(\min)}$, given by the equation:

$$V_{(\min)} = V_{EN1(\min)} + V_{BE1} \quad (8.73)$$

where, $V_{EN1(\min)}$ is the minimum voltage at the emitters when Q_1 is ON. V should lie between $V_{(\max)}$ and $V_{(\min)}$. V should be appropriately chosen. Now to fix the component values, assume Q_1 is OFF, Q_2 is ON and in saturation, in the stable state.

Let

$$V_{EN} = V_{EN2} = \frac{V_{CC}}{2}$$

Therefore,

$$V_{BE1} = V - V_{EN2}$$

If V_{BE1} reverse-biases, the emitter diode of Q_1 is OFF.

$$R_E = \frac{V_{EN2}}{I_E} \quad (8.74)$$

$$R_{C1} = R_{C2} = \frac{V_{CC} - V_{CE(\text{sat})} - V_{EN2}}{I_{C2}} \quad (8.75)$$

$$I_{B2(\min)} = \frac{I_{C2}}{h_{FE(\min)}}$$

Let $I_{B2} = 1.5 \times I_{B2(\min)}$

$$R = \frac{V_{CC} - V_{\sigma} - V_{EN2}}{I_{B2}}. \quad (8.76)$$

Using the Eqs. (8.72) to (8.76) it is possible to design the circuit. Now consider the Example 8.5 to illustrate the design procedure.

EXAMPLE

Example 8.5: Design the monostable multivibrator shown in Fig. 8.11(a) having $V_{CC} = 18$ V and $V = 6$ V, $h_{FE} = 50$, $I_{C(\text{sat})} = 5$ mA.

Solution:

For V to be 6 V, choose $R_1 = 200$ k Ω , $R_2 = 100$ k Ω , (to avoid loading the dc source) and $C_b = 10 \mu\text{F}$ (bypass condenser). Given that $I_{C(\text{sat})} = 5$ mA, assume Q_1 is OFF and Q_2 is ON and in saturation, in the stable state.

Let

$$V_{EN} = V_{EN2} = \frac{V_{CC}}{2} = 9 \text{ V}$$

Therefore,

$$V_{BE1} = V - V_{EN2} = 6 - 9 = -3 \text{ V}$$

Hence, Q_1 is OFF.

$$R_E = \frac{V_{EN2}}{I_E} = \frac{9 \text{ V}}{5 \text{ mA}} = 1.8 \text{ k}\Omega$$

Choose $R_E = 2$ k Ω

$$R_{C1} = R_{C2} = \frac{V_{CC} - V_{CE}(\text{sat}) - V_{EN2}}{I_{C2}} = \frac{18 - 0.2 - 9}{5 \text{ mA}} = \frac{8.8 \text{ V}}{5 \text{ mA}} = 1.75 \text{ k}\Omega$$

$$I_{B2(\text{min})} = \frac{I_{C2}}{h_{FE}(\text{min})} = 0.1 \text{ mA}$$

Let

$$I_{B2} = 1.5 \times I_{B2(\text{min})} = 0.15 \text{ mA}$$

$$R = \frac{V_{CC} - V_{\sigma} - V_{EN2}}{I_{B2}} = \frac{18 - 0.7 - 9}{0.15 \text{ mA}} = \frac{8.3 \text{ V}}{0.15 \text{ mA}} \approx 55 \text{ k}\Omega$$

Choose $R \approx 60 \text{ k}\Omega$

8.5.4 Free-running Operation of an Emitter-coupled Monostable Multivibrator

Equation (8.72) says that for the circuit shown in Fig. 8.11(a) to work as a monostable multivibrator, the bias voltage V cannot be more than $V_{(\text{max})}$. If $V > V_{(\text{max})}$, Q_1 may not remain in the OFF state, with the result, the multivibrator might operate in the astable mode. From the waveforms shown in Fig. 8.13(d), for the voltages V_{BN2} and V_{EN} , if Q_1 is in the ON state, Q_2 is OFF. However, the voltage V_{BN2} varies as a function of time and reaches $(V_{EN1} + V_{\gamma 2})$, after a time interval T ; Q_2 goes into the ON state and the voltages V_{BN2} and V_{EN} suddenly rise to a reasonably large value. Subsequently, these voltages decay. When the voltage V_{EN} reaches $[V_{(\text{max})} - V_{\gamma 1}]$, Q_1 again goes into the ON state as $V > V_{(\text{max})}$ and Q_2 into the OFF state and this process is repeated. Hence, this circuit operates as a free-running multivibrator.

S O L V E D P R O B L E M S

Example 8.6: For the monostable multivibrator shown in Fig. 8.1, $R_1 = R_2 = R = 20 \text{ k}\Omega$, $C = 0.01 \mu\text{F}$, $R_C = 2 \text{ k}\Omega$, $V_{CC} = 12 \text{ V}$, $V_{BB} = -12 \text{ V}$. Find the time period T .

Solution:

$$\text{Time period } T = 0.69RC = 0.69 \times 20 \times 10^3 \times 0.01 \times 10^{-6} = 138 \mu\text{s}$$

Example 8.7: A monostable multivibrator is used as a voltage-to-time converter. Find the time period if $R = 10 \text{ k}\Omega$, $C = 0.01 \mu\text{F}$ and $V_{BB}/V_{CC} = 0.25$.

Solution:

$$\text{Given } V_{CC}/V_{BB} = 4$$

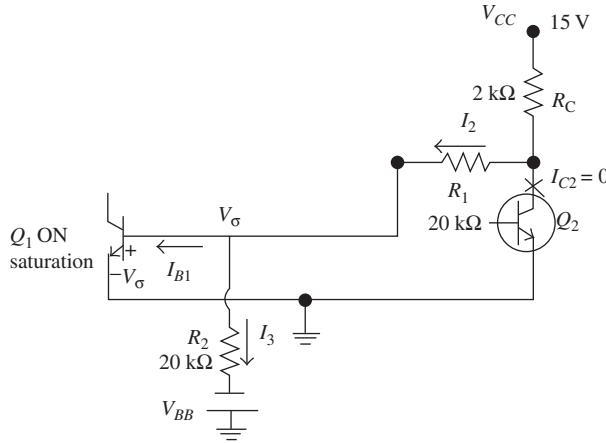
Time period T is given by $T = RC \ln (1 + V_{CC}/V_{BB})$

$$= 10 \times 10^3 \times 0.01 \times 10^{-6} \ln (1 + 4) = 0.1 \times 10^{-3} \times (1.61) = 0.161 \text{ ms} = 161 \mu\text{s}$$

Example 8.8: For a collector-coupled monostable multivibrator circuit shown in Fig. 8.1, $R_1 = R_2 = R = 20 \text{ k}\Omega$, $C = 0.001 \mu\text{F}$, $R_C = 2 \text{ k}\Omega$, $V_{CC} = 15 \text{ V}$, $h_{FE} = 20$. In the quasi-stable state Q_1 is in the active region with collector current of 4 mA. Find the time period and the value of V_{BB} . Neglect junction voltages.

Solution:

The circuit, when Q_1 is ON in the quasi-stable state, is shown in Fig. 8.14(a).

FIGURE 8.14(a) In the quasi-stable state, Q_1 is ON

$$I_2 = \frac{V_{CC} - V_\sigma}{R_C + R_1} = \frac{V_{CC}}{R_C + R_1} = \frac{15}{2 + 20} = 0.68 \text{ mA.}$$

$$I_3 = \frac{V_\sigma + V_{BB}}{R_2} \approx \frac{V_{BB}}{R_2} = \frac{V_{BB}}{20} \text{ mA}$$

The collector current of Q_1 , $I_{C1} = 4 \text{ mA}$

Therefore,

$$I_{B1(\min)} = \frac{I_{C1}}{h_{FE}} = \frac{4}{20} = 0.2 \text{ mA}$$

From Fig. 8.14(a), $I_{B1} = I_2 - I_3$

$$0.2 = 0.68 - \frac{V_{BB}}{20} \quad \frac{V_{BB}}{20} = 0.48 \quad V_{BB} = 9.6 \text{ V}$$

$$T = \tau \ln \frac{V_{CC} + I_{C1}R_C - V_\sigma}{V_{CC} - V_\gamma} = \tau \ln \frac{V_{CC} + I_{C1}R_C}{V_{CC}} = \tau \ln \left[\frac{15 + (4)(2)}{15} \right]$$

$$= 20 \times 10^3 \times 0.001 \times 10^{-6} \times 0.425 = 8.5 \mu\text{s}$$

Example 8.9: Design a collector-coupled monostable multivibrator shown in Fig. 8.15(a) to obtain an output pulse of amplitude 10 V. Given that $I_{C(\text{sat})} = 10 \text{ mA}$, $I_{B2} = 2I_{B2(\min)}$, $V_{CE(\text{sat})} = 0.1 \text{ V}$, $V_{BE(\text{sat})} = 0.3 \text{ V}$, $h_{FE(\min)} = 40$ and a pulse of duration 1000 μs is required. $V_{BE(\text{cut-off})} = -1 \text{ V}$

Solution:

As the pulse amplitude is 10 V, choose $V_{CC} = 10 \text{ V}$.

$$R_C = \frac{V_{CC} - V_{CE(\text{sat})}}{I_{C(\text{sat})}} = \frac{10 - 0.1}{10 \text{ mA}} = \frac{9.9 \text{ V}}{10 \text{ mA}} = 990 \Omega$$

Choosing $R_C = 1 \text{ k}\Omega$:

$$R = \frac{V_{CC} - V_\sigma}{I_{B2}}$$

$$I_{B2(\min)} = \frac{I_{C(\text{sat})}}{h_{FE(\min)}} = \frac{10 \text{ mA}}{40} = 0.25 \text{ mA}$$

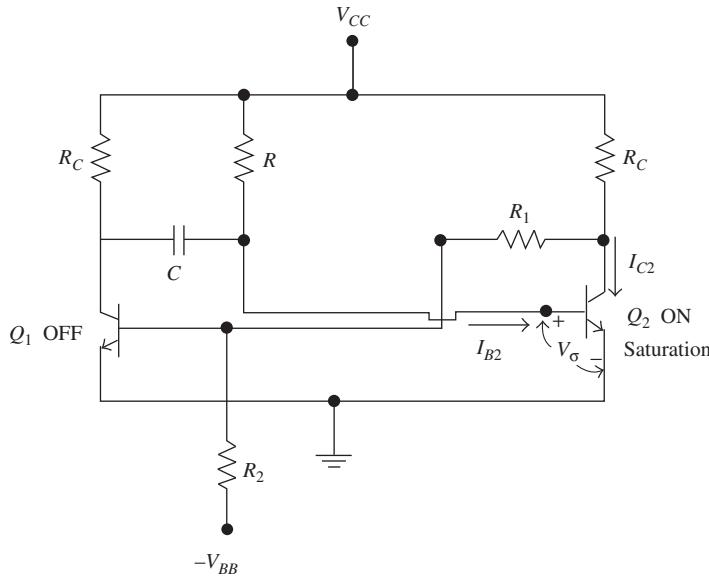


FIGURE 8.15(a) The given circuit of the monostable multivibrator

We want,

$$I_{B2} = 2 \times I_{B2(\min)} = 2 \times 0.25 = 0.5 \text{ mA}$$

Therefore,

$$R = \frac{10 - 0.3}{0.5} = \frac{9.7 \text{ V}}{0.5 \text{ mA}} = 19.4 \text{ k}\Omega$$

Choose $R = 20 \text{ k}\Omega$

$$T = 0.69RC$$

$$1000 \times 10^{-6} = 0.69 \times 20 \times 10^3 \times C$$

Therefore,

$$C = \frac{10^{-6}}{13.8} = 0.072 \mu\text{F}$$

For the value of V_{BB} to be fixed, consider the Fig. 8.15(b).

If

$$V_{BE(\text{cut-off})} = -1 \text{ V} \quad I_2 = \frac{V_{CE(\text{sat})} - (-V_{BB})}{R_1 + R_2}$$

If

$$R_1 = R_2 = R \quad I_2 = \frac{0.1 + V_{BB}}{2R}$$

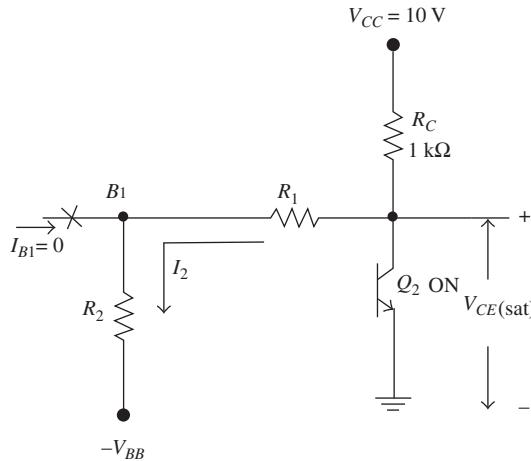
Also:

$$I_2 = \frac{V_{B1} - (-V_{BB})}{R_2} \quad I_2 = \frac{-1 + V_{BB}}{R_2}$$

$$\therefore \frac{0.1 + V_{BB}}{2R} = \frac{-1 + V_{BB}}{R} \quad 0.1 + V_{BB} = 2(-1 + V_{BB})$$

$$0.1 + V_{BB} = -2 + 2V_{BB} \quad V_{BB} = 2.1 \text{ V}$$

To find $R_1 = R_2$,

FIGURE 8.15(b) The circuit to calculate V_{BB}

$$I_2 = \frac{1}{10} I_{C(\text{sat})} = \frac{10}{10} = 1 \text{ mA}$$

Therefore,

$$R_1 + R_2 = \frac{V_{CE(\text{sat})} + V_{BB}}{I_2} = \frac{0.1 + 2.1}{1 \text{ mA}} = 2.2 \text{ kΩ}$$

$$R_1 = R_2 = 1.1 \text{ kΩ}.$$

Example 8.10: Design the circuit for the collector-coupled monostable multivibrator shown in Fig. 8.16. Given that: $I_{C(\text{sat})} = 5 \text{ mA}$, $V_{B(\text{OFF})} = -1.5 \text{ V}$, $C_i = 20 \text{ pF}$. It is required to generate a pulse having a width of $5000 \text{ } \mu\text{s}$. $I_{B(\text{sat})} = 1.5 \times I_{B(\text{min})}$. Neglect junction voltages and assume $h_{FE}(\text{min}) = 20$.

Solution: We have

$$R_C = \frac{V_{CC} - V_{CE(\text{sat})}}{I_{C(\text{sat})}} = \frac{V_{CC}}{I_{C(\text{sat})}} = \frac{15}{5} = 3 \text{ kΩ}$$

$$I_{B2(\text{min})} = \frac{I_{C2(\text{sat})}}{h_{FE}} = \frac{5}{20} = 0.25 \text{ mA}.$$

$$I_{B2(\text{sat})} = 1.5 \times I_{B2(\text{min})} = 1.5 \times 0.25 = 0.375 \text{ mA}$$

$$R = \frac{V_{CC} - V_{\sigma}}{I_{B2(\text{sat})}} = \frac{V_{CC}}{I_{B2(\text{sat})}} = \frac{15}{0.375} = 40 \text{ kΩ}$$

$$R = 40 \text{ kΩ}$$

Given

$$T = 5000 \text{ } \mu\text{s} \quad \text{and} \quad T = 0.69RC$$

$$C = \frac{T}{0.69 \times R} = \frac{5000 \times 10^{-6}}{0.69 \times 40 \times 10^3} = 181.16 \text{ nF}$$

Given that

$$V_{B1(\text{OFF})} = -1.5 \text{ V} :$$

$$V_{B1(\text{OFF})} = \frac{V_{CE(\text{sat})} \times R_2}{R_1 + R_2} + \frac{(V_{BB})R_1}{R_1 + R_2} = \frac{(V_{BB})R_1}{R_1 + R_2} \quad \text{as the first term is small.}$$

$$-1.5 = V_{BB} \times \frac{40}{40 + 40} = 0.5 V_{BB}$$

Therefore,

$$V_{BB} = -3 \text{ V}$$

In the quasi-stable state when Q_1 goes into saturation:

$$I_{B1(\text{sat})} = I_1 - I_2$$

Since junction voltages are negligible:

$$I_{B1(\text{sat})} = \frac{V_{CC} - V_\sigma}{R_C + R_1} - \frac{V_\sigma + V_{BB}}{R_2} = \frac{V_{CC}}{R_C + R_1} - \frac{V_{BB}}{R_2}$$

Since $R_1 = R_2$, the above equation reduces to:

$$0.375 = \frac{15}{3 + R_1} - \frac{3}{R_1}$$

$$\therefore 0.375R_1^2 - 10.875R_1 + 9 = 0$$

$$R_1 = \frac{10.8 \pm \sqrt{(10.8)^2 - (4 \times 0.375 \times 9)}}{2 \times 0.375}$$

From this $R_1 = 28 \text{ k}\Omega$ or $0.85 \text{ k}\Omega$.

Choose $R_1 = R_2 = 28 \text{ k}\Omega$.

Further, given that $C_i = 20 \text{ pF}$:

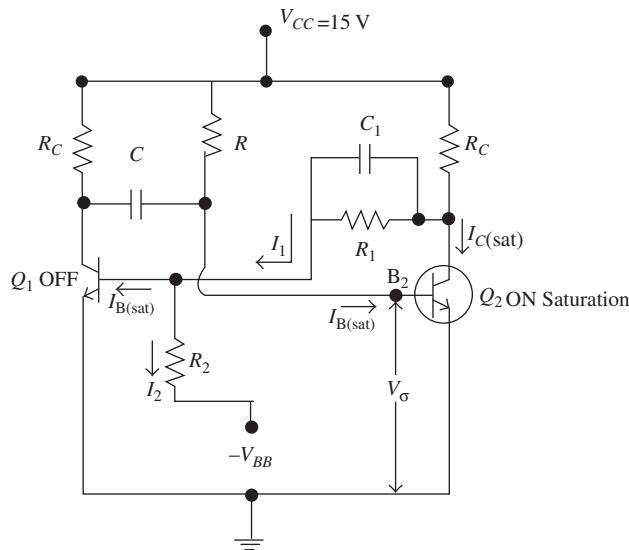


FIGURE 8.16 Monostable multivibrator

Therefore,

$$C_1 = \frac{R_2 C_i}{R_1} = 20 \text{ pF.}$$

In the absence of any specification of C_i , C_1 is calculated as $R_1 C_1 = 1 \mu\text{s}$.

In which case,

$$C_1 = \frac{1 \times 10^{-6}}{40 \times 10^3} = 25 \text{ pF}$$

SUMMARY

- A monostable multivibrator has one stable state and one quasi-stable state.
- The main application of a monostable multivibrator is as a gate that generates a pulsed output.
- The gate width of collector-coupled monostable multivibrator is liable to change with temperature variations.
- A monostable multivibrator can be used as a voltage-to-time converter.
- In a collector-coupled monostable multivibrator, to ensure that the gate width remains constant, the ON device is required to be driven into saturation, in the quasi-stable state.
- The emitter-coupled monostable multivibrator may operate as a free-running multivibrator if $V > V_{(\text{max})}$.
- In an emitter-coupled monostable multivibrator, even if the ON device is held in the active region; in the quasi-stable state, because of a substantial emitter-resistance which stabilizes the current, the gate width can be maintained stable.

MULTIPLE CHOICE QUESTIONS

- (1) A monostable multivibrator is also known by the name:
 - Flip-flop
 - Free-running multivibrator
 - One-shot multivibrator
 - Schmitt trigger
- (2) A monostable multivibrator can be used as a:
 - Voltage-to-time converter
 - Clock
 - Squaring circuit
 - Flip-flop
- (3) The gate width of a collector-coupled monostable multivibrator in which the ON device, in the quasi-stable state, is in saturation is given by the relation:
 - $T = 0.69 RC$
 - $T = 69 RC$
 - $T = \sqrt{0.69RC}$
 - $T = \sqrt{69RC}$
- (4) The multivibrator that can be used as a gating circuit is:
 - Bistable multivibrator
 - Schmitt trigger
 - Monostable multivibrator
 - Astable multivibrator
- (5) The gate width of an emitter-coupled multivibrator is:
 - Independent of temperature variation
 - Varies with temperature
 - Varies with variation of device parameters
 - None of the above
- (6) The expression for the gate width of collector-coupled monostable multivibrator, considering I_{CO} is given by:
 - $T = 0.69RC$
 - $T = \sqrt{0.69RC}$
 - $T = 69RC$
 - $T = \tau \ln 2 - \tau \ln [(1 + \phi)/(1 + \phi/2)]$

SHORT ANSWER QUESTIONS

- (1) The main application of a monostable multivibrator is as a gating circuit, explain.
 - (2) Explain, how you can use a monostable multivibrator as a voltage-to-time converter.
 - (3) The expression for the gate width of a collector-coupled monostable multivibrator is given as $T = \tau \ln (V_{CC} - V_\sigma + I_1 R_C) / (V_{CC} - V_\gamma)$ where I_1 is the current in Q_1 , when ON in the quasi-stable

- state. If the ON device is driven into saturation, show that $T = 0.69\tau$.

 - (4) What is the main advantage of an emitter-coupled monostable multivibrator over collector-coupled monostable multivibrator?
 - (5) Draw the circuit of an emitter-coupled monostable multivibrator and explain its operation.

LONG ANSWER QUESTIONS

- (1) Draw the circuit of a collector-coupled monostable multivibrator and explain its operation. Obtain the expression for its gate width and show that the gate width can be stable if the ON device is driven into saturation, in the quasi-stable state. Draw the waveforms.

- (2) Draw the circuit of a voltage-to-time converter and obtain the expression for the time period.
 - (3) With the help of a circuit diagram and waveforms, explain the working of an emitter-coupled monostable multivibrator. Derive the expression for its gate width.

UNSOLVED PROBLEMS

- (1) A monostable multivibrator is used as a voltage-to-time converter. Find the time period if $R = 10 \text{ k}\Omega$, $C = 0.01 \mu\text{F}$, $V_{BB}/V_{CC} = 0.5$.
 - (2) Design a collector-coupled monostable multivibrator using an $n-p-n$ silicon transistor with $h_{FE(\min)} = 40$, $V_{BE(\text{cut Off})} \approx 0 \text{ V}$ and $I_{B(\text{sat})} = 1.5I_{B(\min)}$. Given that: $V_{CC} = 10 \text{ V}$, $I_{C(\text{sat})} = 5 \text{ mA}$, $R_{C1} = R_{C2} = R_C$, $V_{CE(\text{sat})} = 0.2 \text{ V}$ and $V_{BE(\text{sat})} = 0.7 \text{ V}$. If the pulse width required is 1 ms, calculate the value of C .
 - (3) A collector-coupled monostable multivibrator shown in Fig. 8p.1 using Ge $n-p-n$ transistors has the following parameters: $V_{CC} = 9 \text{ V}$, $V_{BB} = 9 \text{ V}$, $R_C = 2 \text{ k}\Omega$, $R_1 = 10 \text{ k}\Omega$, $R_2 = 20 \text{ k}\Omega$, $R = 10 \text{ k}\Omega$, $h_{FE} = 40$, $r_{bb'} = 0.2 \text{ k}\Omega$, $C = 0.001 \mu\text{F}$, $V_{CE(\text{sat})} = 0.1 \text{ V}$ and $V_\sigma = 0.3\text{V}$.
 - (a) Calculate and plot the waveforms.
 - (b) Find the pulse width.

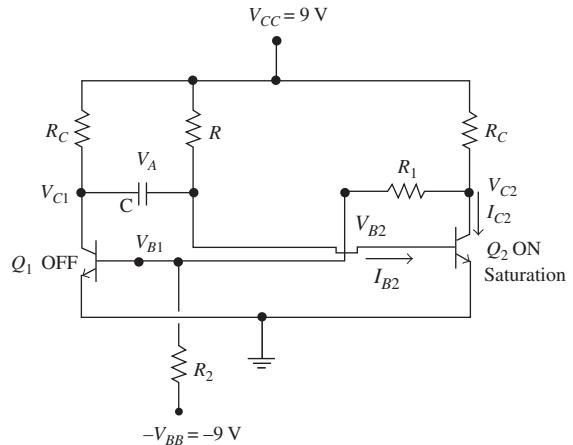


FIGURE 8p.1 The given circuit of the monostable multivibrator

- (4) For a collector-coupled monostable multivibrator circuit shown in Fig. 8.1, $R_1 = R_2 = R = 10 \text{ k}\Omega$, $C = 0.01 \mu\text{F}$, $R_C = 1 \text{ k}\Omega$, $V_{CC} = 10 \text{ V}$, $h_{FE} = 20$. In the quasi-stable state Q_1 is in the active region with collector current of 2 mA. Find the time period and the value of V_{BB} . Neglect junction voltages. $I_B(\text{sat}) = 1.5 I_B(\text{min})$.

- (5) An emitter-coupled monostable multivibrator shown in Fig. 8p.2 has the following parameters: $V_{CC} = 6 \text{ V}$, $R_{C1} = R_{C2} = R_E = 3 \text{ k}\Omega$, $R = 50 \text{ k}\Omega$, $V = 2.8 \text{ V}$ and $C = 0.01 \mu\text{F}$ and $n-p-n$ silicon transistors with $h_{FE} = 50$ and $r_{bb'} = 100 \Omega$ are used. A trigger is applied at $t = 0$.

- (a) Assume that Q_1 is OFF and Q_2 is ON at $t = 0-$. Calculate the node voltages. Using your calculated values verify that Q_1 is indeed OFF and Q_2 is in saturation.
- (b) Assume that Q_1 is in the active region and Q_2 is OFF at $t = 0+$. Calculate the node voltage and verify that Q_1 is indeed in the active region and Q_2 is OFF.
- (c) Calculate the node voltages at $t = T-$.
- (d) Calculate the node voltages at $t = T+$.

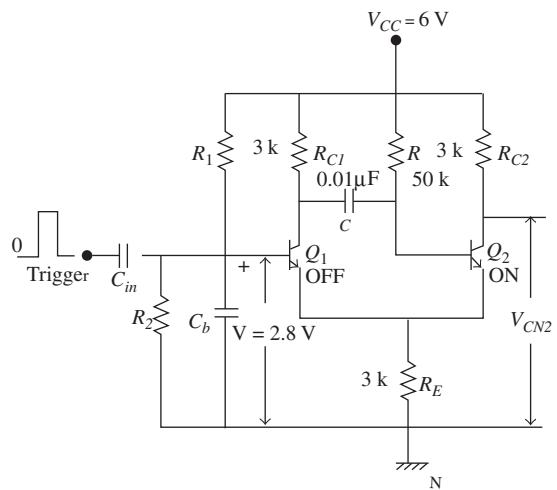


FIGURE 8p.2 Emitter-coupled monostable multivibrator

- (6) An emitter-coupled monostable multivibrator has the following parameters: $V_{CC} = 15 \text{ V}$, $R_{C1} = R_{C2} = R_E = 4 \text{ k}\Omega$, $R = 100 \text{ k}\Omega$, $V = 5 \text{ V}$ and $C = 0.01 \mu\text{F}$ and an $n-p-n$ silicon transistor with $h_{FE(\text{min})} = 40$ and $r_{bb'} = 100 \Omega$ is used. Calculate and plot the waveforms to scale.

Bistable Multivibrators

LEARNING OBJECTIVES

After reading this chapter, you will be able to:

- Analyse fixed-bias and self-bias bistable multivibrators
 - Design bistable multivibrator circuits
 - Realize the need for commutating condensers in a bistable multivibrator
 - Find out the resolution time and the maximum switching speed of a bistable multivibrator
 - Analyse and design emitter-coupled bistable multivibrator, also called Schmitt triggers
 - Describe the applications of bistable multivibrator circuits
-

9.1 INTRODUCTION

A bistable multivibrator has two stable states and this circuit also employs two devices, Q_1 and Q_2 . If one device is ON, the other device is required to be OFF. If initially Q_1 is OFF, the voltage at the collector of Q_1 is $V_{C1} = V_{CC}$; and when Q_2 is ON, the voltage at this collector $V_{C2} \approx 0$ V. This is the initial stable state for the bistable multivibrator. The circuit is flipped from one stable state to other (i.e driving into the other stable state in which Q_1 is ON and Q_2 is OFF) by an external trigger. On the application of a trigger, Q_1 switches ON ($V_{C1} \approx 0$ V) and Q_2 switches OFF ($V_{C2} = V_{CC}$) and the states of Q_1 and Q_2 are flipped only when another trigger is applied. If V_{CC} is taken to represent “1” in binary and 0 V represents “0”. So “1” level remains as “1” and “0” level remains as a “0” till the application of a trigger signal. Hence, this type of circuit is used as a one-bit memory element in digital circuits. An array of such circuits can be used to write or store a string of binary digits (0 s or 1 s), called a register. This becomes the basic memory unit in digital computers. This circuit is also known by many names such as binary, flip-flop, scale-of-two circuit and Eccles–Jordan circuit. If the ON device is driven to saturation, the binary is called a saturating binary. If, on the other hand, the ON device is held in the active region, the binary is called a non-saturating binary. An emitter-coupled binary is called a Schmitt trigger. This circuit, in addition to operating as a binary, can also be used as an amplitude comparator and as a squaring circuit.

9.2 BISTABLE MULTIVIBRATOR CIRCUITS

The two types of bistable multivibrator circuits considered here are fixed-bias bistable and self-bias bistable multivibrators. In the first circuit, two separate sources are used for biasing the devices whereas in the second one self-bias is used to derive the biasing voltage.

Besides the two circuits, there is a third variation of bistable multivibrators, namely, the Schmitt trigger. This circuit, in addition to being used as a bistable, can also be used for other applications like waveshaping, comparators, etc

9.2.1 Fixed-bias Bistable Multivibrators

The circuit shown in Fig. 9.1(a) is called a fixed-bias bistable multivibrator as two separate dc sources are used to bias the transistors. The circuit consists of two inverters, the output of one is connected as the input to the other.

Let it be arbitrarily assumed that initially Q_1 is OFF and Q_2 is ON and in saturation. Then the voltage at the first collector is V_{CC} (the binary equivalent of which is 1) and the voltage at the second collector is $V_{CE(sat)}$ (the binary equivalent being 0). If a negative trigger is applied at the base of the ON device (Q_2), Q_2 goes into the OFF state and its collector voltage rises to V_{CC} . Consequently Q_1 goes into the ON state and its collector voltage falls to $V_{CE(sat)}$. Let us now verify whether Q_1 is really OFF and Q_2 is really ON and in saturation.

To Verify that Q_2 is ON and in Saturation. For this, we have to calculate its base current I_{B2} and its collector current I_{C2} to ensure that the base current is significantly higher than the minimum so that Q_2 is really in saturation. To calculate I_{B2} using Fig. 9.1(b), we begin by assuming that Q_2 is in saturation and Q_1 is OFF and justify the assumption made.

To find I_{B2} , we calculate I_1 and I_2 .

$$I_1 = \frac{V_{CC} - V_\sigma}{R_C + R_1} \quad (9.1)$$

$$I_2 = \frac{V_\sigma - (-V_{BB})}{R_2} \quad (9.2)$$

$$I_{B2} = I_1 - I_2 \quad (9.3)$$

To calculate I_{C2} , we use the circuit shown in Fig. 9.1(c).

$$I_3 = \frac{V_{CC} - V_{CE(sat)}}{R_C} \quad (9.4)$$

$$I_4 = \frac{V_{CE(sat)} - (-V_{BB})}{R_1 + R_2} \quad (9.5)$$

$$I_{C2} = I_3 - I_4 \quad (9.6)$$

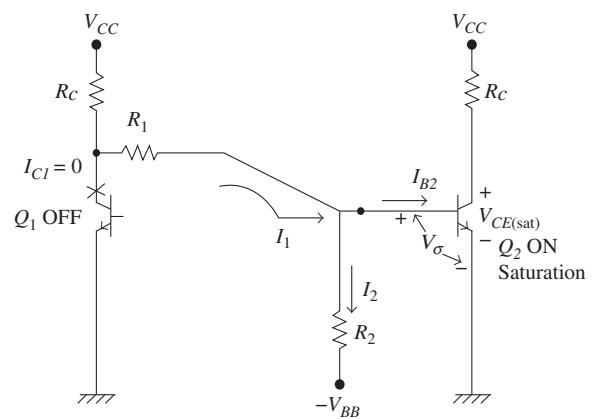
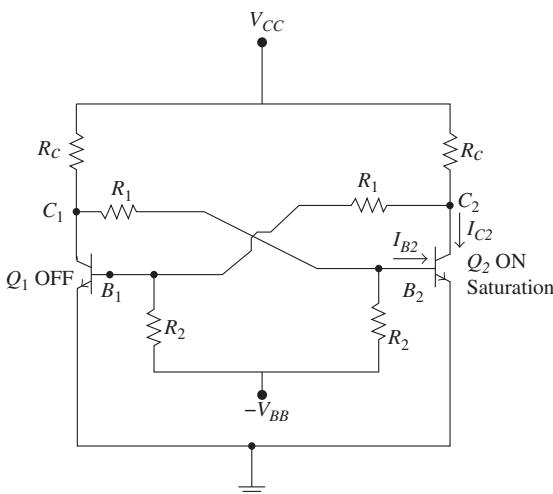
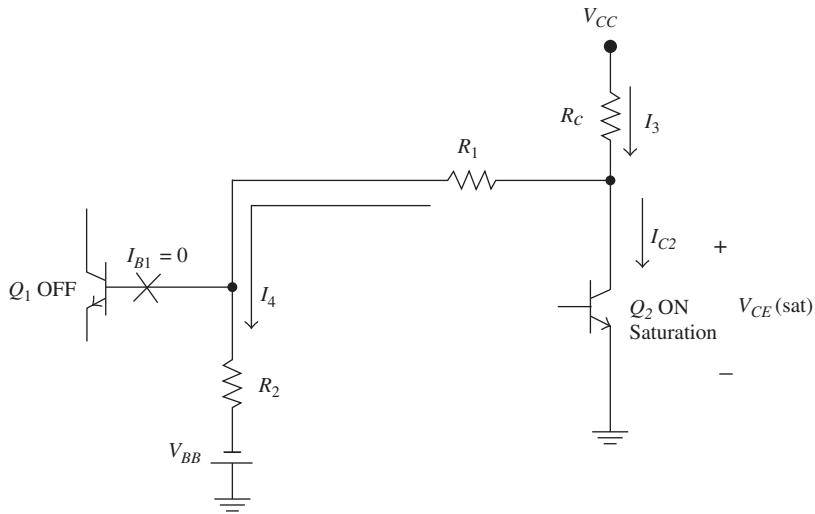


FIGURE 9.1(a) The fixed-bias bistable multivibrator FIGURE 9.1(b) The circuit that enables the calculation of I_{B2}

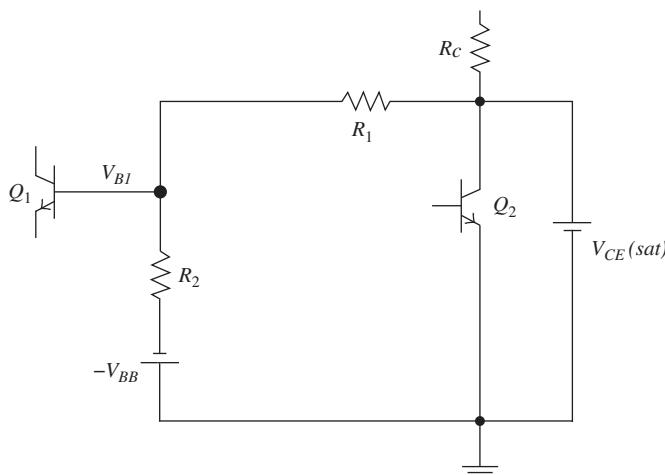
FIGURE 9.1(c) The circuit that enables calculation of I_{C2}

Now find $I_{B2(\min)}$ using the relation:

$$I_{B2(\min)} = \frac{I_{C2}}{h_{FE(\min)}}$$

If $I_{B2} \gg I_{B2(\min)}$, then Q_2 is in saturation, as assumed.

To Verify that Q_1 is OFF. The transistor Q_1 is OFF if its base-emitter diode is reverse-biased. To verify this, we calculate the voltage V_{B1} at the base of Q_1 using the circuit shown in Fig. 9.1(d) and check whether it reverse-biases the emitter diode or not. If the emitter diode is reverse-biased, the transistor is indeed in the OFF state.

FIGURE 9.1(d) The circuit to calculate V_{B1}

The voltage V_{B1} at the base of Q_1 is due to the two sources: $-V_{BB}$ and $V_{CE(\text{sat})}$. Using the superposition theorem:

$$V_{B1} = V_{CE(\text{sat})} \frac{R_2}{R_1 + R_2} + (-V_{BB}) \frac{R_1}{R_1 + R_2} \quad (9.7)$$

If the voltage between the base and emitter terminals of Q_1 reverse-biases the base-emitter diode, then Q_1 is OFF and $V_{C1} = V_{CC}$. However, V_{C1} is not exactly V_{CC} as it should be when Q_1 is OFF. Instead, it is smaller than this, because of the cross-coupling network comprising R_1 and R_2 . There is a current I_1 through R_1 and R_C . Therefore, the actual voltage at the first collector is not necessarily V_{CC} , but somewhat lower than V_{CC} .

$$V_{C1} = V_{CC} - I_1 R_C \quad (9.8)$$

The currents and voltages in the initial stable state are calculated, using Eqs. (9.1) to (9.8). Sometimes the output of the bistable multivibrator is required to drive some other circuit. Let the voltage V_{CC} at the collector of the OFF device drive another circuit, as shown in Fig. 9.1 (e). If the circuit to be driven, offers an input resistance R_i , this becomes the load ($= R_L$) for the bistable multivibrator. The effective load resistance at the collector, $R_C//R_L$, will be now small if R_L is small and the collector voltage falls to a value less than V_{CC} . If this falls appreciably, the ON device may not be driven into saturation as required. Therefore, we have to ensure that the voltage at the collector of the OFF device is not allowed to fall below a threshold level. Hence, R_L is chosen such that R_L is $R_{L(\text{min})}$ for which I_L is $I_{L(\text{max})}$, but at the same time making sure that Q_2 is in saturation. $R_{L(\text{min})}$ is called as the heaviest load and $I_{L(\text{max})}$ as the corresponding load current [see Fig. 9.1(f)]. When I_{B2} drops to $I_{B2(\text{min})}$, the corresponding R_L is considered as the heaviest load.

$$I_{B2(\text{min})} = \frac{I_{C2}}{h_{FE(\text{min})}}$$

Then,

$$I_{1(\text{min})} = I_{B2(\text{min})} + I_2 \quad (9.9)$$

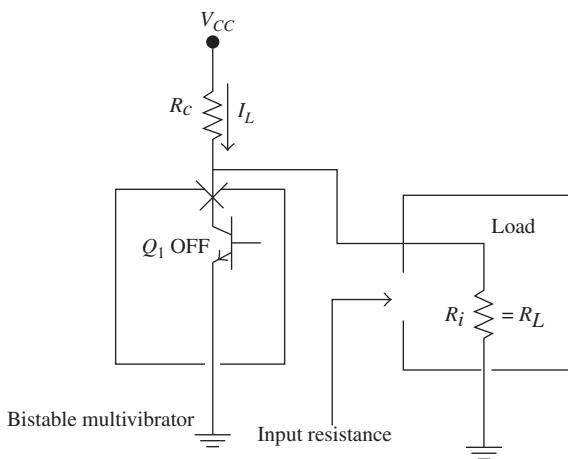


FIGURE 9.1(e) The output of the bistable multivibrator driving another circuit

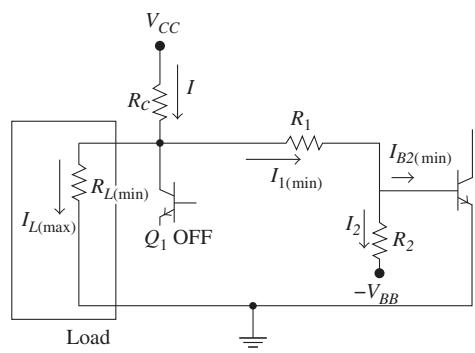


FIGURE 9.1(f) The calculation of the heaviest load

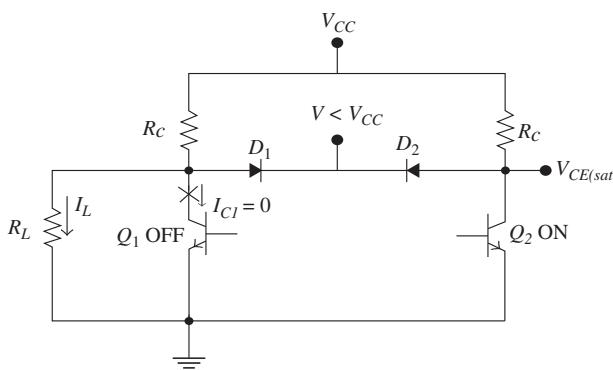


FIGURE 9.1(g) The use of collector catching diodes

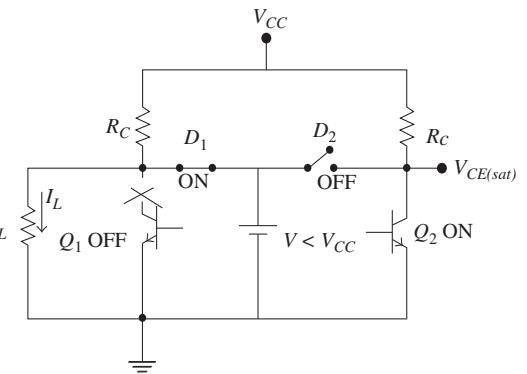


FIGURE 9.1(h) The simplified circuit of Fig. 9.1(g)

Therefore, the new value of V_{C1} is

$$V_{C1(\min)} = I_{1(\min)}R_1 + V_{B2} \quad (9.10)$$

Earlier V_{C1} was given by Eq. (9.8). Due to R_L , V_{C1} has now fallen to $V_{C1(\min)}$ as given by Eq. (9.10).

$$I = \frac{V_{CC} - V_{C1(\min)}}{R_C} \quad (9.11)$$

$$I_{L(\max)} = I - I_{1(\min)} \quad (9.12)$$

$$R_{L(\min)} = \frac{V_{C1(\min)}}{I_{L(\max)}} \quad (9.13)$$

This is the minimum value of R_L that can be connected as load. It is seen that by connecting the load to a bistable multivibrator the voltage at the collector of the OFF device falls, if there is a loading on the collector. To ensure that the voltage does not fall below a specified threshold, diodes D_1 and D_2 , called collector catching diodes, are used along with a source V , as shown in Fig. 9.1(g).

V_{C1} , was the voltage, prior to connecting the load R_L at the first collector. Let $V < V_{C1}$. Then, D_1 conducts and during this period D_2 is OFF, as $V_{C2} = V_{CE(\text{sat})}$. When D_1 is ON, it simply acts as a switch and hence, V is directly connected to the first collector. A simplified circuit of Fig. 9.1(g) is shown in Fig. 9.1(h). As V is a source that can deliver a large current, the loading (drawing more current) at this collector can be eliminated. As D_1 and D_2 clamp the collectors to V (hold the collector voltage at V), when the respective devices (Q_1 or Q_2) are OFF, these diodes are called collector catching diodes. To calculate the stable-state currents and voltages, let us consider Example 9.1.

EXAMPLE

Example 9.1: The circuit shown in Fig. 9.2(a) uses an $n-p-n$ silicon transistor having $h_{FE(\min)} = 50$, $V_{CE(\text{sat})} = 0.3$ V, $V_{BE(\text{sat})} = 0.7$ V, $V_{CC} = 12$ V, $V_{BB} = 12$ V, $R_C = 1\text{ k}\Omega$, $R_1 = 10\text{ k}\Omega$, $R_2 = 20\text{ k}\Omega$. Calculate the stable-state currents and voltages and also calculate the heaviest load the multivibrator can handle.

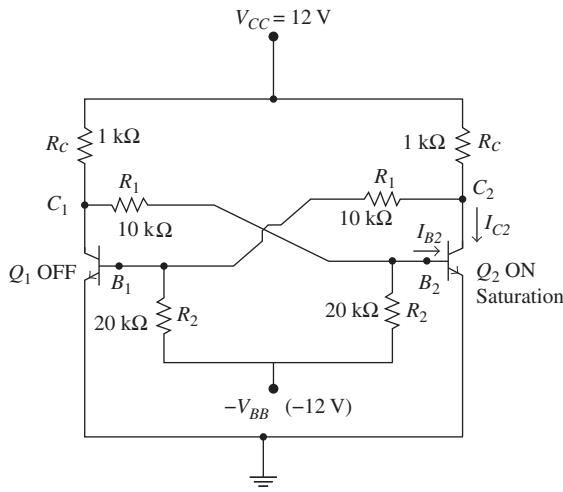


FIGURE 9.2(a) The fixed-bias bistable multivibrator

Solution:

(a) To calculate I_{B2} and I_{C2} :

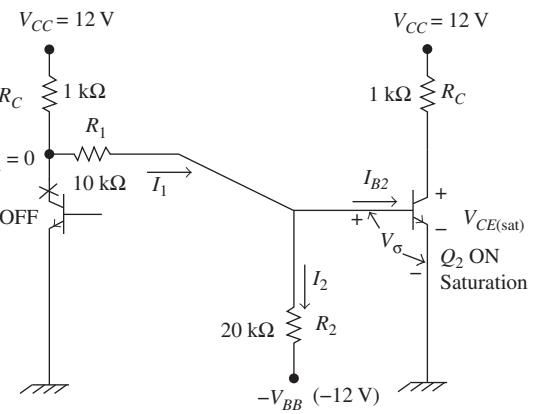
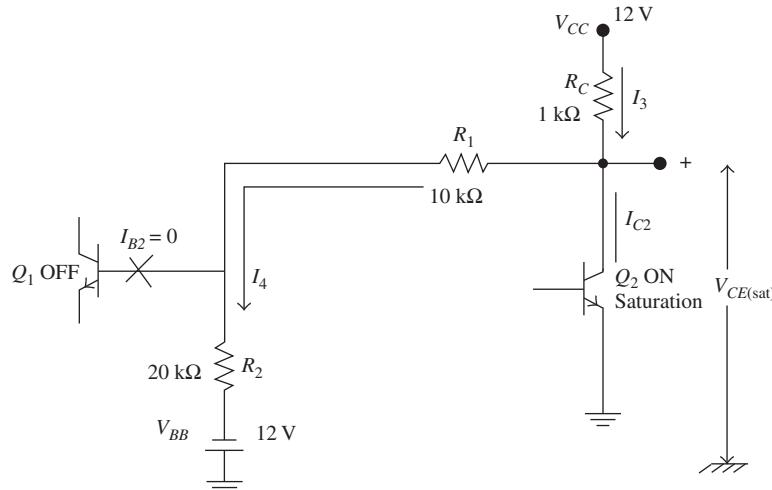
Consider the Fig. 9.2(b), in which the cross-coupling network from the first collector to the second base is represented, to calculate I_{B2} .

On the assumption that Q_2 is in saturation and Q_1 is OFF calculations are made and justified. To find I_{B2} , we calculate I_1 and I_2 .

Then, $I_{B2} = I_1 - I_2$

$$I_1 = \frac{V_{CC} - V_\sigma}{R_C + R_1} = \frac{12 - 0.7}{1 + 10} = \frac{11.3}{11 \text{ k}\Omega} = 1 \text{ mA} \quad I_2 = \frac{V_\sigma - (-V_{BB})}{R_2} = \frac{0.7 - (-12)}{20 \text{ k}\Omega} = 0.635 \text{ mA}$$

$$I_{B2} = I_1 - I_2 = 1 \text{ mA} - 0.635 \text{ mA} = 0.365 \text{ mA}$$

FIGURE 9.2(b) The circuit that enables the calculation of I_{B2} FIGURE 9.2(c) The circuit that enables the calculation of I_{C2}

To calculate I_{C2} , consider the cross-coupling network from the second collector to the first base as shown in Fig. 9.2(c).

$$I_3 = \frac{V_{CC} - V_{CE(\text{sat})}}{R_C} = \frac{12 - 0.3}{1 \text{ K}} = 11.7 \text{ mA}$$

$$I_4 = \frac{V_{CE(\text{sat})} - (-V_{BB})}{R_1 + R_2} = \frac{12 + 0.3}{30 \text{ K}} = \frac{12.3}{30 \text{ K}} = 0.41 \text{ mA}$$

$$I_{C2} = I_3 - I_4 = 11.7 - 0.41 = 11.29 \text{ mA}$$

(b) To Verify Q_2 is in saturation:

$$I_{B2(\text{min})} = \frac{I_{C2}}{h_{FE(\text{min})}} = \frac{11.29 \text{ mA}}{50} = 0.226 \text{ mA}$$

For Q_2 to be saturation:

$$I_{B2} \cong 1.5I_{B2\text{min}}$$

$$I_{B2} = 1.5 \times 0.226 \text{ mA} = 0.339 \text{ mA}$$

Actually, $I_{B2} = 0.365 \text{ mA}$, i.e., $I_{B2} \gg I_{B2(\text{min})}$. Hence, Q_2 is in saturation. Therefore, $V_{C2} = 0.3 \text{ V}$, $V_{B2} = 0.7 \text{ V}$.

(c) To verify whether Q_1 is OFF or not:

For verifying whether Q_1 is OFF or not, voltage V_{B1} is calculated, using the circuit shown in Fig.9.2(d). To calculate the voltage V_{B1} at the base of Q_1 due to $-V_{BB}$ and $V_{CE(\text{sat})}$ sources,use Eq. (9.7).

$$V_{B1} = V_{CE(\text{sat})} \frac{R_2}{R_1 + R_2} + (-V_{BB}) \frac{R_1}{R_1 + R_2} = 0.3 \times \frac{20}{30} - 12 \times \frac{10}{30} = 0.2 - 4 = -3.8 \text{ V.}$$

As voltage V_{B1} reverse-biases the emitter diode, Q_1 is OFF and hence, $V_{C1} = V_{CC} = 12 \text{ V}$. However, V_{C1} is not exactly 12 V—as it should be when Q_1 is OFF—but, is smaller than this because of the current I_1 in R_1 . The actual voltage at the first collector is,

$$V_{C1} = V_{CC} - I_1 R_C = 12 - (1 \text{ mA})(1 \text{ K}) = 11 \text{ V}$$

Hence, the voltages in the initial stable state are $V_{C1} = 11 \text{ V}$, $V_{B1} = -3.8 \text{ V}$, $V_{C2} = 0.3 \text{ V}$, $V_{B2} = 0.7 \text{ V}$. The maximum allowable load current can be found out from the circuit shown in Fig. 9.2(e).

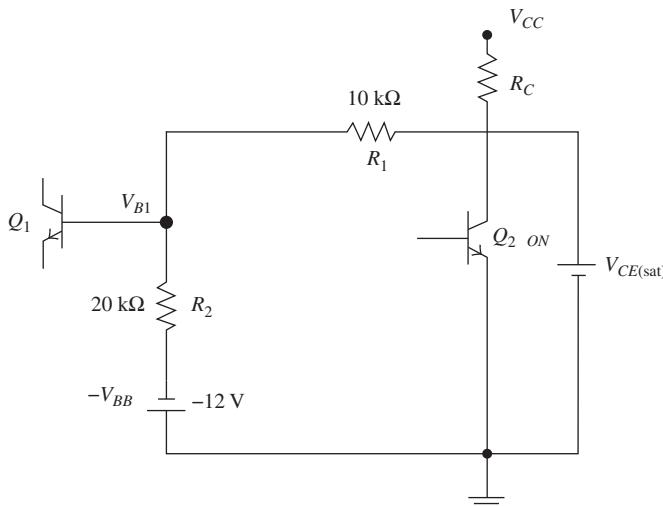


FIGURE 9.2(d) The circuit to calculate V_{B1}

When I_{B2} drops to $I_{B2(\min)}$, the corresponding R_L is considered as the heaviest load.

$$I_{B2(\min)} = \frac{I_{C2}}{h_{FE(\min)}} = \frac{11.29 \text{ mA}}{50} = 0.226 \text{ mA}$$

$$I_2 = 0.635 \text{ mA}$$

$$I_{1(\min)} = I_{B2(\min)} + I_2 = 0.226 + 0.635 = 0.861 \text{ mA}$$

Therefore $V_{C1(\min)} = I_{1(\min)} R_1 + V_{B2}$

$$= (0.861 \text{ mA})(10 \text{ k}\Omega) + 0.7 \text{ V} = 8.61 + 0.7 \text{ V} = 9.31 \text{ V}$$

The voltage, V_{C1} in the initial stable state was 11 V. Due to the resistance R_L , V_{C1} has now fallen to 9.31 V.

$$I = \frac{V_{CC} - V_{C1(\min)}}{R_C} = \frac{12 - 9.31}{1 \text{ k}\Omega} = 2.69 \text{ mA}$$

$$I_{1(\min)} = 0.861 \text{ mA}$$

$$I_{L(\max)} = I - I_{1(\min)} = 2.69 - 0.861 = 1.829 \text{ mA}$$

$$R_{L(\min)} = \frac{V_{C1(\min)}}{I_{L(\max)}} = \frac{9.31 \text{ V}}{1.829 \text{ mA}} = 5.0 \text{ k}\Omega$$

This is the minimum value of the resistance R_L that can be connected as a load.

The Design of a Fixed-bias Bistable Multivibrator. The fixed-bias bistable multivibrator shown in Fig. 9.1(a) can be designed by using the given supply voltages V_{CC} and V_{BB} ; $n-p-n$ silicon devices and assuming I_C and $h_{FE(\min)}$. The design equations are:

R_C is calculated as

$$R_C = \frac{V_{CC} - V_{CE(\text{sat})}}{I_{C2}} \quad (9.14)$$

R is calculated as

$$R_2 = \frac{V_{\sigma} - (-V_{BB})}{I_2} \quad (9.15)$$

Choose $I_2 \approx \frac{1}{10} I_{C2}$

$$I_{B2(\min)} = \frac{I_{C2}}{h_{FE(\min)}} \quad (9.16)$$

For Q_2 to be in saturation $I_{B2} \gg I_{B2(\min)}$

$$I_1 = I_2 + I_{B2} \quad (9.17)$$

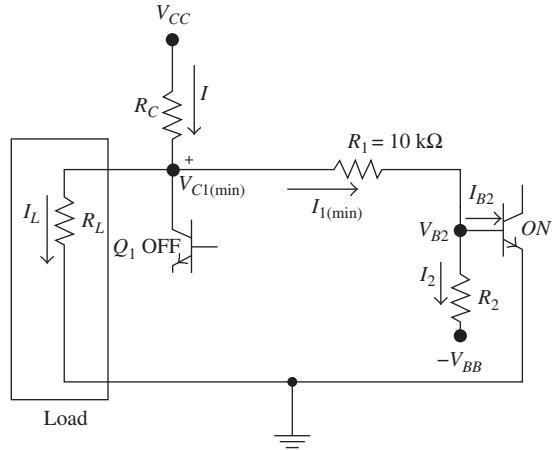


FIGURE 9.2(e) The circuit for calculation of the heaviest load

$$R_C + R_1 = \frac{V_{CC} - V_\sigma}{I_1} \quad (9.18)$$

$$R_1 = (R_C + R_1) - R_C \quad (9.19)$$

After the design is complete, there is a need to verify whether Q_2 is in saturation and Q_1 is OFF or not. To understand the design procedure let us consider an example.

E X A M P L E

Example 9.2: Design a fixed-bias bistable multivibrator shown in Fig. 9.1(a) with supply voltages ± 12 V, an $n-p-n$ silicon device having $V_{CE(\text{sat})} = 0.2$ V, $V_{BE(\text{sat})} = V_\sigma = 0.7$ V and $h_{FE(\text{min})} = 50$ are used. Assume $I_C = 5$ mA.

Solution:

From Eq. (9.14),

$$R_C = \frac{V_{CC} - V_{CE(\text{sat})}}{I_{C2}} = \frac{12 - 0.2 \text{ V}}{5 \text{ mA}} = \frac{11.8 \text{ V}}{5 \text{ mA}} = 2.36 \text{ k}\Omega \approx 2.2 \text{ k}\Omega \text{ (standard resistance).}$$

From Eq. (9.15),

$$R_2 = \frac{V_\sigma - (-V_{BB})}{I_2}$$

$$\text{Choose } I_2 \approx \frac{1}{10} I_{C2} = 0.5 \text{ mA}$$

$$\therefore R_2 = \frac{0.7 + 12}{0.5} = \frac{12.7 \text{ V}}{0.5 \text{ mA}} = 25.4 \text{ k}\Omega \approx 22 \text{ k}\Omega$$

$$I_{B2(\text{min})} = \frac{I_{C2}}{h_{FE(\text{min})}} = \frac{5 \text{ mA}}{50} = 0.1 \text{ mA}$$

If Q_2 is in saturation:

$$I_{B2(\text{sat})} = 1.5 I_{B2(\text{min})} = 0.15 \text{ mA}$$

$$I_1 = I_2 + I_{B2(\text{sat})} = 0.5 \text{ mA} + 0.15 \text{ mA} = 0.65 \text{ mA}$$

From Eq. (9.18)

$$R_C + R_1 = \frac{V_{CC} - V_\sigma}{I_1} = \frac{12 - 0.7}{0.65 \text{ mA}} = \frac{11.3 \text{ V}}{0.65 \text{ mA}} = 17.38 \text{ k}\Omega$$

from Eq. (9.19)

$$R_1 = (R_C + R_1) - R_C = 17.38 - 2.36 = 15.02 \text{ k}\Omega$$

Choose $R_1 = 15 \text{ k}\Omega$

The circuit, so designed, with component values indicated is shown in Fig. 9.3.

After the design is complete and as the components chosen are of standard values, there is a need to verify whether Q_2 is in saturation and Q_1 is OFF or not. For this, we calculate I_{C2} and I_{B2} and verify whether Q_2 is in saturation or not. Afterwards, the voltage V_{B1} is calculated to check whether this voltage reverse-biases the base-emitter diode of Q_1 or not.

$$I_{C2} \approx \frac{V_{CC} - V_{CE(\text{sat})}}{2.2 \text{ k}\Omega} = \frac{12 - 0.2 \text{ V}}{2.2 \text{ k}\Omega} = \frac{11.8 \text{ V}}{2.2 \text{ k}\Omega} = 5.36 \text{ mA}$$

$$I_{B2(\text{min})} = \frac{5.36 \text{ mA}}{50} = 0.107 \text{ mA}$$

$$I_2 = \frac{V_\sigma + V_{BB}}{R_2} = \frac{12.7}{22 \text{ k}\Omega} = 0.58 \text{ mA}$$

$$I_1 = \frac{V_{CC} - V_\sigma}{R_C + R_1} = \frac{12 - 0.7}{2 + 10} = \frac{11.3}{12} = 0.94 \text{ mA}$$

$$I_{B2} = I_1 - I_2 = 0.94 \text{ mA} - 0.58 \text{ mA} = 0.36 \text{ mA}$$

$$I_{B2} \geq I_{B2\text{min}}$$

Hence, Q_2 is in saturation.

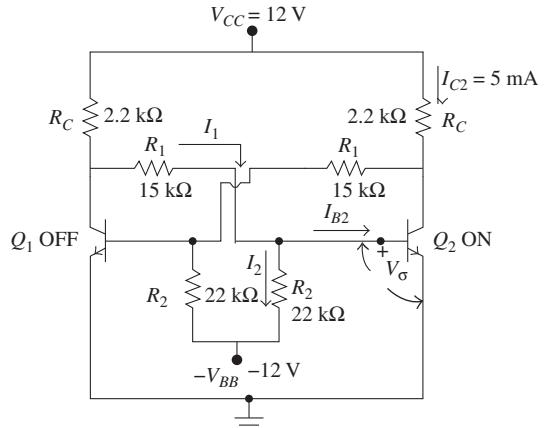


FIGURE 9.3 The designed fixed-bias bistable multivibrator with component values

$$V_{B1} = V_{CE(\text{sat})} \frac{R_2}{R_1 + R_2} - V_{BB} \frac{R_1}{R_1 + R_2} = 0.2 \times \frac{22}{15 + 22} - 12 \times \frac{10}{15 + 22} = 0.118 - 4.86 = -4.742 \text{ V}$$

The voltage, V_{B1} reverse-biases the base-emitter diode of Q_1 . Hence, Q_1 is OFF.

Commutating Condensers. In Section 8.4, we learnt that a commutating condenser is connected across R_1 to reduce the transition time. As in a bistable multivibrator there are two cross-coupling resistances R_1 and R_1 , C_1 and C_1 need to be connected across these resistances to transfer conduction from one device to the other, soon after the application of the trigger. Hence, the bistable multivibrator is modified as shown in Fig. 9.4.

However, the moment the commutating condensers are connected to reduce the transition time, voltages of value V_A and V_B exist across the two capacitors. When Q_1 is OFF and Q_2 is ON, the values of these two voltages can be calculated using the following equations:

$$V_A = V_{C1} - V_{B2} = V_{CC} - V_\sigma \quad (9.20)$$

$$V_B = V_{C2} - V_{B1}$$

$$= V_{CE(\text{sat})} - V_{B1} \text{ (a small negative voltage)} \quad (9.21)$$

If a trigger is applied to change the state of the devices, Q_1 quickly goes into the ON state when Q_2 switches into the OFF state as the transition time is negligible. However, the voltages across the two capacitors will not switch instantaneously. The multivibrator is said to have settled down in its new state completely only when the capacitor voltages also switch. The next trigger, to once again change the state of the two devices, can be applied only then. The interval during which the capacitor voltages interchange is called the settling time. Thus, settling time is defined as the time taken for the capacitor voltages to interchange after conduction is transferred from one device to the other, on the application of a trigger.

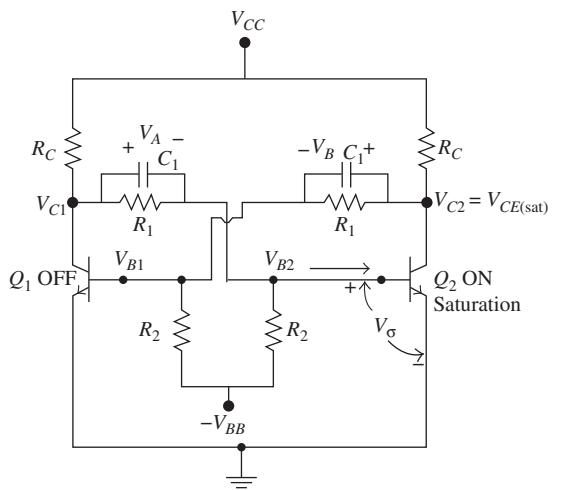


FIGURE 9.4 A fixed-bias bistable multivibrator with commutating condensers

9.2.2 The Resolution Time and the Maximum Switching Speed of a Bistable Multivibrator

The sum of transition time and settling time is called the resolution time of the bistable multivibrator.

$$t_{\text{res}} = t_{\text{trans}} + t_{\text{settling}} \approx t_{\text{settling}}, \text{ as } t_{\text{trans}} \text{ is small.} \quad (9.22)$$

where, t_{res} is the resolution time, t_{trans} is the transition time, and t_{settling} is the settling time.

Thus, the resolution time is the minimum time interval required between successive trigger pulses to reliably drive the multivibrator from one state to the other. The reciprocal of the resolution time is called the maximum switching speed of a bistable multivibrator.

$$f_{(\text{max})} = \frac{1}{t_{\text{res}}} \quad (9.23)$$

Equation (9.23) tells us as to how fast we can switch the bistable multivibrator from one stable state to the other. To be able to reliably trigger the bistable multivibrator from one stable state to the other, we have to wait for a time interval t_{res} . The transition time, as we have seen, is appreciably reduced by connecting commutating condensers. As a result, the resolution time is approximately equal to the settling time, during which period the voltages across the two commutating condensers interchange. The recharging time constants associated with the two condensers, C_1 and C'_1 shown in Fig. 9.5(a) are used to calculate the resolution time t_{res} .

In order to distinguish between the two capacitors in the circuit, they are labelled differently as C_1 and C'_1 , though in actuality the two capacitors are equal i.e, $C_1 = C'_1$. To find the recharging time constant associated with the capacitor C'_1 , consider the circuit shown in Fig. 9.5(b).

As Q_2 is ON and in saturation, $r_{bb'}$ appears between its base and emitter terminals. The net resistance in the circuit is R' , as shown in Fig. 9.5(c).

$$R' = R_1 \parallel (R_C + R_i) = R_1 \parallel (R_C + r_{bb'}) \approx R_1 \parallel R_C \quad (9.24)$$

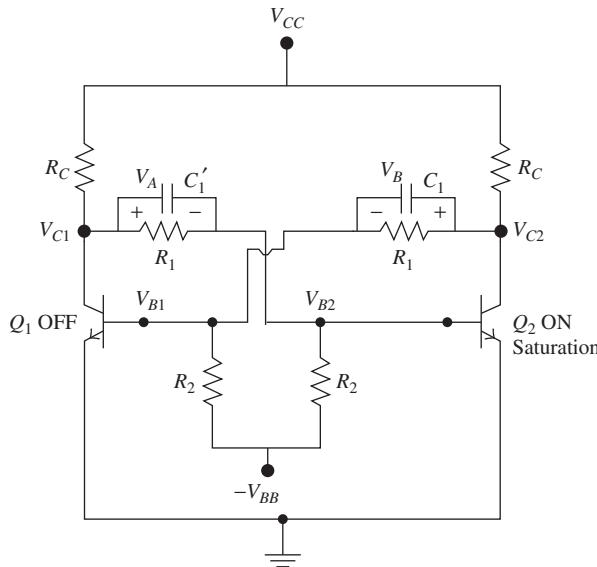


FIGURE 9.5(a) The bistable multivibrator with commutating condensers C'_1 and C_1

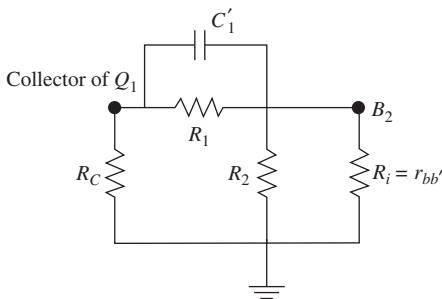


FIGURE 9.5(b) The circuit to calculate the recharging time constant of capacitor C'_1

$R_i \approx r_{bb'}$
 $R_2 \gg R_i$ and the effective resistance $R_2 \parallel R_i$ is R_i

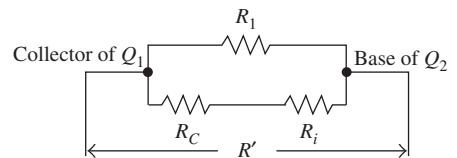


FIGURE 9.5(c) The calculation of the effective resistance, R'

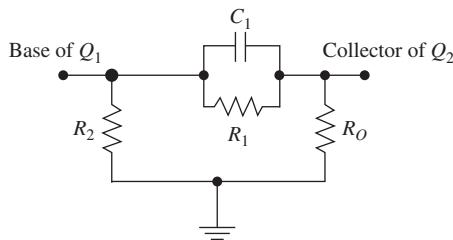


FIGURE 9.5(d) The circuit to calculate the recharging time constant of C_1

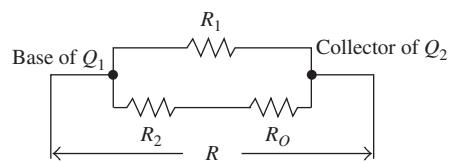


FIGURE 9.5(e) The calculation of the effective resistance, R

Hence, the recharging time constant associated with this condenser C'_1 is,

$$\tau' = R' C'_1 \quad (9.25)$$

To find the recharging time constant associated with C_1 , the corresponding circuit is shown in Fig. 9.5(d). R_o is the output resistance of Q_2 (in saturation) taking R_C also into account, which is small. The net resistance in the circuit is R , as shown in Fig. 9.5(e).

$$R = R_1 \parallel (R_2 + R_o)$$

$$R = R_1 \parallel R_2 \text{ as } R_o \text{ is small.} \quad (9.26)$$

The recharging time constant associated with $C_1 = \tau$ is calculated from Fig. 9.5(f).

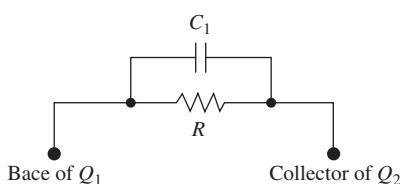
$$\tau = R C_1 \quad (9.27)$$

From Eqs. (9.25) and (9.27) it is evident that $\tau > \tau'$.

After conduction is transferred from one device to the other, it is assumed that voltages across the capacitors interchange in a time period $(\tau + \tau')$. However as $\tau > \tau'$, if the resolution time is taken to be 2τ , the voltages across these capacitors would certainly interchange before the application of the next trigger. Hence,

$$t_{res} = 2\tau = 2 \times \frac{R_1 R_2 C_1}{R_1 + R_2} \quad (9.28)$$

FIGURE 9.5(f) The circuit to calculate τ



And the reciprocal of it is,

$$f_{(\max)} = \frac{R_1 + R_2}{2R_1R_2C_1} \quad (9.29)$$

Methods of Improving the Resolution Time of a Bistable Multivibrator. The resolution time, as given by Eq. (9.28), is $t_{\text{res}} = 2C_1(R_1 // R_2)$. For reducing the resolution time and hence, improving the switching speed, the following considerations have to be taken into account:

- (1) A finite transition time exists mainly because of stray capacitances of the transistor. Commutating condensers are used, to reduce the transition time, and once they are used there is a settling time. If devices with negligible stray capacitances are used, the problem of settling time does not arise at all. Similarly, to reduce the resolution time the devices with negligible stray capacitances called as switching devices are chosen.
- (2) However, for the devices chosen, if the influence of stray capacitances can not be neglected, then invariably commutating condensers (C_1 and C_1) need to be used. For t_{res} to be small, C_1 must be small. Though, if C_1 is smaller, transition time is lengthened. Alternately, if C_1 is larger, settling time is lengthened. For perfect compensation, C_1 is chosen satisfying the requirement of a compensated attenuator, as discussed in Section 3.3.2 and is given by $C_1 = C_i(R_2/R_1)$, where C_i is the stray input capacitance of the transistor.
- (3) If t_{res} is to be smaller, a third option could be to have smaller values of R_1 and R_2 . However, smaller values of R_1 and R_2 will load the collector of the OFF device, resulting in a reduced voltage at its collector. It is possible that this reduced voltage may not be able to drive the ON device into saturation, as desired. Secondly, smaller values of R_1 and R_2 tend to draw larger current from the dc sources, thereby, increasing the drain on the batteries.

Hence, to improve the resolution time, the transistors should be chosen carefully and a compromise should be arrived at in view of the points discussed in this section.

9.2.3 Methods of Triggering a Bistable Multivibrator

To switch the bistable multivibrator from one stable state to the other, a trigger of proper polarity and magnitude is applied at an appropriate point in the circuit. The purpose of a trigger is to change the state of the devices. The trigger can be a dc trigger or a pulse trigger. However, in circuits like counters (which we are going to consider later), the trigger is normally a pulse train. Here, the focus is on pulse triggering only. There are two methods of triggering a bistable multivibrator using pulses:

- (1) Unsymmetric triggering
- (2) Symmetric triggering.

Unsymmetric Triggering. In this method of triggering, one trigger pulse, taken from a source, is applied at one point in the circuit. The next trigger pulse taken from a different source is applied at a different point in the circuit [see Fig. 9.6(a)]. It has been mentioned earlier that the trigger is applied at the base of the ON device. However, since commutating condensers are connected in this circuit, the trigger pulse is not connected to the base of Q_2 directly, but is applied at the collector of Q_1 through a condenser. As the capacitor behaves as a short circuit when there is a sudden change in voltage, the negative pulse applied at the collector of Q_1 is coupled to the base of Q_2 .

Let the set trigger be applied to the circuit at $t = 0$. If Q_1 is OFF, the voltage at this collector is V_{CC} . Therefore, D_1 is ON and this negative pulse appears at the base of Q_2 as the first collector and the second base are connected through C_1 . Q_2 goes into the OFF state and Q_1 into the ON state.

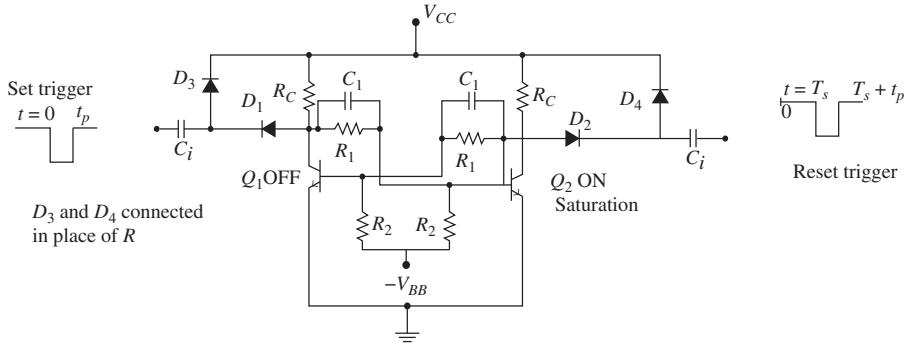


FIGURE 9.6(a) The unsymmetric triggering of a bistable multivibrator

The next trigger pulse, i.e., the reset pulse, is applied through D_2 at the second collector which is coupled to the first base through C_1 . Q_1 now goes into the OFF state and Q_2 into the ON state. Let us look at the voltages at the two collectors as shown in Fig. 9.6(b).

The set trigger pulse applied at $t = 0$ sets the voltage at the second collector to V_{CC} . The reset pulse applied after a time interval T_s , resets the voltage at the second collector to $V_{CE(sat)}$. Hence, a pulse is generated at this collector and similarly at the first collector. The duration of this pulse is equal to the spacing between successive trigger pulses. Hence, unsymmetric triggering is used to generate a gated output, the width of this gate being the spacing between two successive triggers.

As discussed in Section 8.2.1, diodes D_3 and D_4 are used in place of a resistance R . When a negative trigger pulse appears, the diode is OFF (D_3 or D_4); the large reverse resistance of the diode avoids loading the trigger source. When the trigger is absent, the diode is ON and offers a negligible resistance so that the charge on the capacitor C_i can be quickly removed.

Symmetric Triggering. In symmetric triggering, successive trigger pulses taken from the same source and applied at the same point in the circuit will cause the multivibrator to change from one stable state to the other. This method of triggering is normally used in counters, as shown in Fig. 9.7(a).

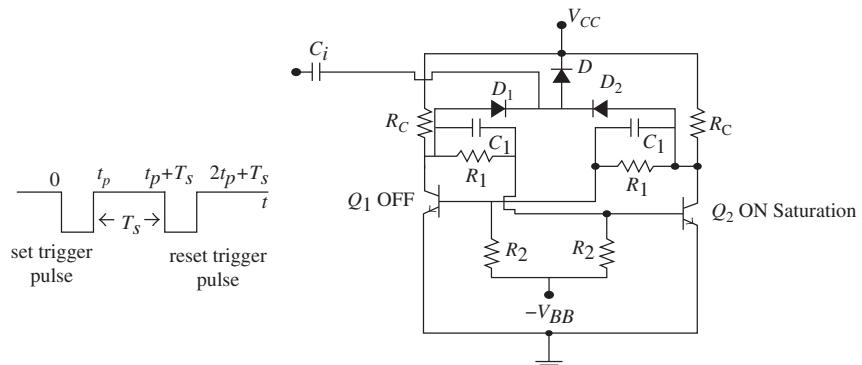


FIGURE 9.7(a) The symmetric triggering of a bistable multivibrator

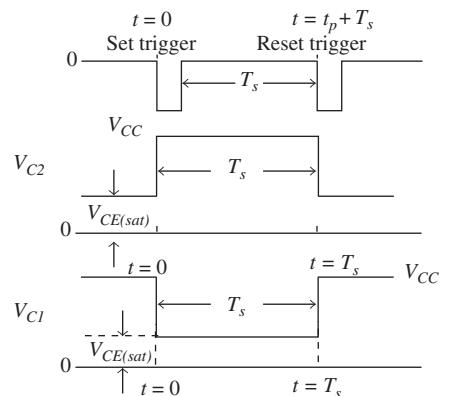


FIGURE 9.6(b) The voltages at the two collectors on the application of trigger pulses

In the circuit shown in Fig. 9.7(a) the purpose of D is similar to the diodes D_3 and D_4 used in Fig. 9.6(a). The first trigger pulse (Set pulse) makes D_1 conduct and this pulse is coupled to the base of Q_2 and drives Q_2 into the OFF state and Q_1 into the ON state. The next trigger pulse (Reset pulse) applied at $t = t_1$ is coupled to the first base as D_2 is now ON. Hence, Q_1 again goes into the OFF state and Q_2 into the ON state. D_1 and D_2 are called steering diodes as these diodes steer the trigger to the appropriate base.

A bistable multivibrator is represented by a block having a trigger input and the outputs Q and \bar{Q} (collectors of Q_1 and Q_2), as shown in Fig. 9.7(b).

From the above waveforms, it is seen that for every two trigger pulses, there is one pulse at Q and \bar{Q} . Hence, a bistable multivibrator is also called a scale-of-two circuit.

9.2.4 Non-saturating Bistable Multivibrators

In the bistable multivibrator shown in Fig. 9.4, the ON device is driven into saturation. As a result, the storage time becomes longer. To reduce the storage time and ensure faster switching of the device, the ON device is held in the active region. Such a bistable multivibrator in which the ON device is in the active region is called a non-saturating bistable multivibrator. To hold the ON device in the active region, the circuit of Fig. 9.4 is modified as shown in Fig. 9.8(a). Of the four diodes used in the circuit shown in Fig. 9.8(a); two (D_1 and D_3) are semiconductor diodes and the other two, (D_2 and D_4) are Zener diodes.

When a transistor is in saturation, the emitter as well as the collector diodes are forward-biased. However, when it is in the active region, the emitter diode is forward-biased but the collector diode is reverse-biased by a suitable voltage. Hence, when Q_2 is ON, to hold it in the active region, the collector diode is reverse-biased by V_Z , the breakdown potential of the Zener diode.

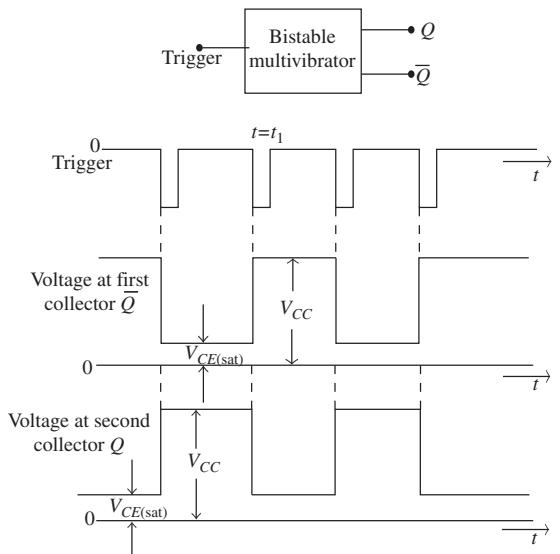


FIGURE 9.7(b) The trigger and outputs with symmetrical triggering of a bistable multivibrator

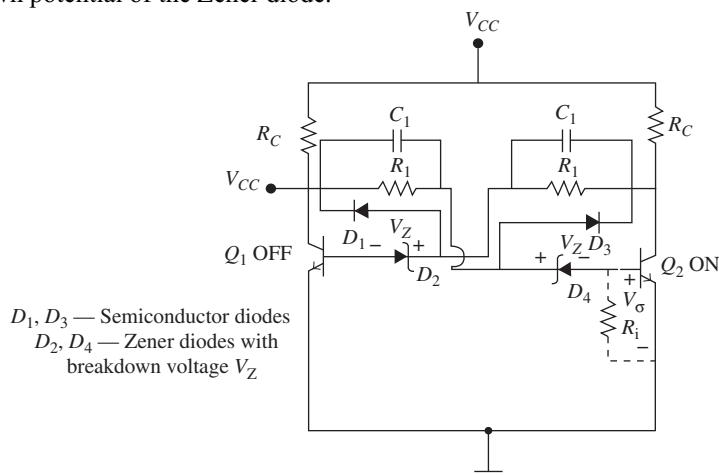


FIGURE 9.8(a) A non-saturating bistable multivibrator

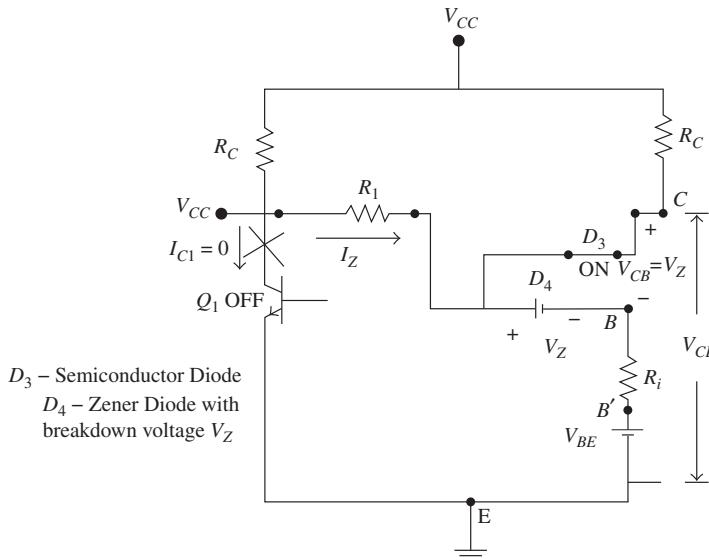


FIGURE 9.8(b) The simplified circuit of Fig. 9.8(a) when Q_1 is OFF and Q_2 is ON

When Q_1 is OFF and Q_2 is ON, D_4 (Zener diode) conducts. As a result, with the polarity shown in Fig. 9.8(b), a voltage V_Z is available at the anode of D_3 , and a relatively small voltage V_{CE} at its cathode. As $V_Z > V_{CE}$, D_3 is ON. Now the collector of Q_2 is positive with respect to the base by a value equal to V_Z . Hence, the collector diode is reverse-biased; this being an $n-p-n$ device. Therefore, the device Q_2 is in the active region. If, on the other hand Q_2 is OFF and Q_1 is ON, a voltage V_Z between the collector and the base of Q_1 holds Q_1 in the active region.

The main advantage of a non-saturating bistable multivibrator is that it does not allow the ON device to go into saturation, thereby reducing the storage time, and thus enabling faster switching speeds. However, the complexity of the circuit may be a possible disadvantage. Also the dissipation in the device becomes large. The limitations of a fixed-bias bistable multivibrator are that the circuit uses two separate sources, V_{CC} and V_{BB} which add to the cost; and also here, the currents and voltages change with temperature variations. These problems are circumvented in a self-bias bistable multivibrator, discussed in the following section.

9.3 SELF-BIAS BISTABLE MULTIVIBRATORS

In a self-bias bistable multivibrator, the negative V_{BB} source can be removed by including an emitter resistor R_E in the emitter lead. The voltage drop across R_E is used to derive the other voltage needed. The resistance R_E in a self-bias bistable multivibrator provides stability to the currents and voltages. Here, a self-bias bistable multivibrator in which the ON transistor is driven into saturation is considered. Hence, this circuit is called a saturating bistable multivibrator. One major advantage of a saturating bistable multivibrator is that the power dissipation in devices either when ON or when OFF is so small that transistors with lesser power dissipation capability can be employed. However, its major limitation is larger storage time which tends to reduce the switching speed. Consider the self-bias bistable multivibrator shown in Fig. 9.9(a).

Let it be assumed that Q_2 is ON and in saturation, in the initial stable state. As a result, I_{B2} and I_{C2} flow through R_E developing a voltage V_{EN} . The voltage between the base-emitter terminals of Q_1 is V_{BE1} and is given by:

$$V_{BE1} \equiv V_{BN1} - V_{EN}$$

If this voltage reverse-biases the emitter diode of Q_1 , then Q_1 is indeed in the OFF state. To calculate the stable-state currents and voltages, assume that Q_1 is OFF and Q_2 is ON and in saturation. As Q_1 is OFF, $I_{E1} = 0$. To verify whether Q_2 is in saturation or not, the collector and base loops of the circuit are drawn by Thevenizing at the collector and base terminals.

$$V_{thb} = V_{CC} \times \frac{R_2}{R_C + R_1 + R_2} \quad (9.30)$$

and

$$R_{thb} = R_2 // (R_C + R_1) = \frac{R_2(R_C + R_1)}{R_2 + R_C + R_1} \quad (9.31)$$

$$V_{thc} = V_{CC} \times \frac{(R_1 + R_2)}{R_C + R_1 + R_2} \quad (9.32)$$

$$R_{thc} = (R_1 + R_2) || R_C \quad (9.33)$$

The base and collector loops of Q_2 are drawn as shown in Fig. 9.9(b). Writing the KVL equations of the input and output loops we get:

$$V_{thb} - V_\sigma = I_{B2}(R_{thb} + R_E) + I_{C2}R_E \quad (9.34)$$

$$V_{thc} - V_{CE(\text{sat})} = I_{B2}R_E + I_{C2}(R_{thc} + R_E) \quad (9.35)$$

Solving Eqs. (9.34) and (9.35), we get I_{B2} and I_{C2} :

$$I_{B2(\min)} = \frac{I_{C2}}{h_{FE}}$$

If $I_{B2} \gg I_{B2(\min)}$, Q_2 is in saturation.
Therefore,

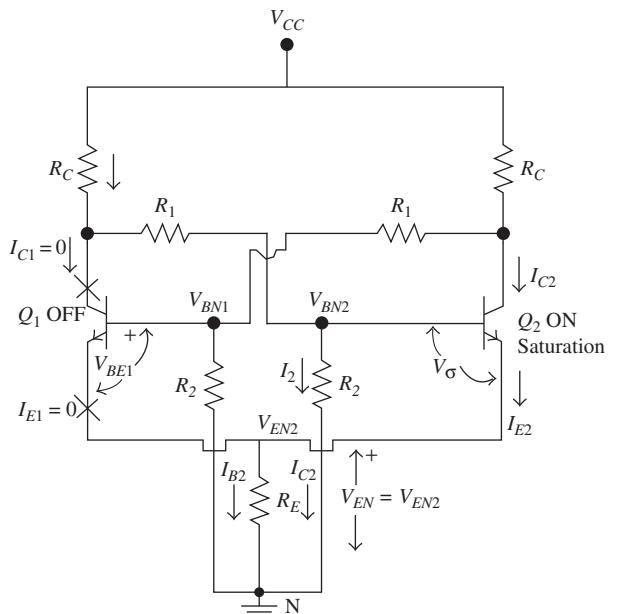


FIGURE 9.9(a) The self-bias bistable multivibrator

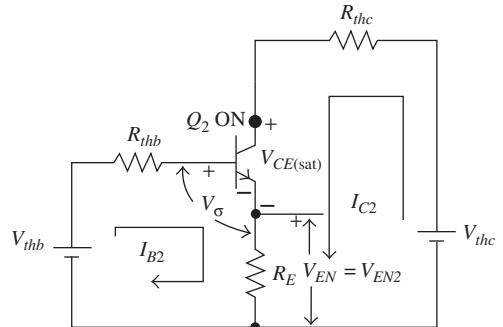


FIGURE 9.9(b) The circuit to calculate the base and collector currents of Q_2

$$V_{EN} = V_{EN2} = (I_{B2} + I_{C2})R_E \quad (9.36)$$

$$V_{CN2} = V_{EN2} + V_{CE(\text{sat})} \quad (9.37)$$

$$V_{BN2} = V_{EN2} + V_\sigma \quad (9.38)$$

$$V_{BN1} = V_{CN2} \times \frac{R_2}{R_1 + R_2} \quad (9.39)$$

$$V_{BE1} = V_{BN1} - V_{EN2} \quad (9.40)$$

If this voltage reverse-biases the emitter diode, Q_1 is OFF.

$$I_1 = \frac{V_{CC} - V_{BN2}}{R_C + R_1} \quad (9.41)$$

$$V_{CN1} = V_{CC} - I_1 R_C \quad (9.42)$$

9.3.1 The Heaviest Load Driven by a Self-bias Bistable Multivibrator

In the stable state, Q_1 is OFF and Q_2 is ON. If the output at the first collector, which is approximately V_{CC} , is to drive a load, the maximum permissible load current I_L (or minimum value of R_L) without disrupting the stable-state conditions is called the heaviest load. To find the value of the maximum permissible load, consider the circuit shown in Fig. 9.9(c).

Q_2 is ON and is in saturation even with $I_{B2} = I_{B2(\min)}$

$$\text{Therefore, } I_{1(\min)} = I_2 + I_{B2(\min)} \quad (9.43)$$

$$V_{CN1(\min)} = I_{1(\min)} R_1 + V_{BN2} \quad (9.44)$$

$$I = \frac{V_{CC} - V_{CN1(\min)}}{R_C} \quad (9.45)$$

$$I_L = I_{L(\max)} = I - I_{1(\min)} \quad (9.46)$$

Hence,

$$R_{L(\min)} = \frac{V_{CN1(\min)}}{I_{L(\max)}} \quad (9.47)$$

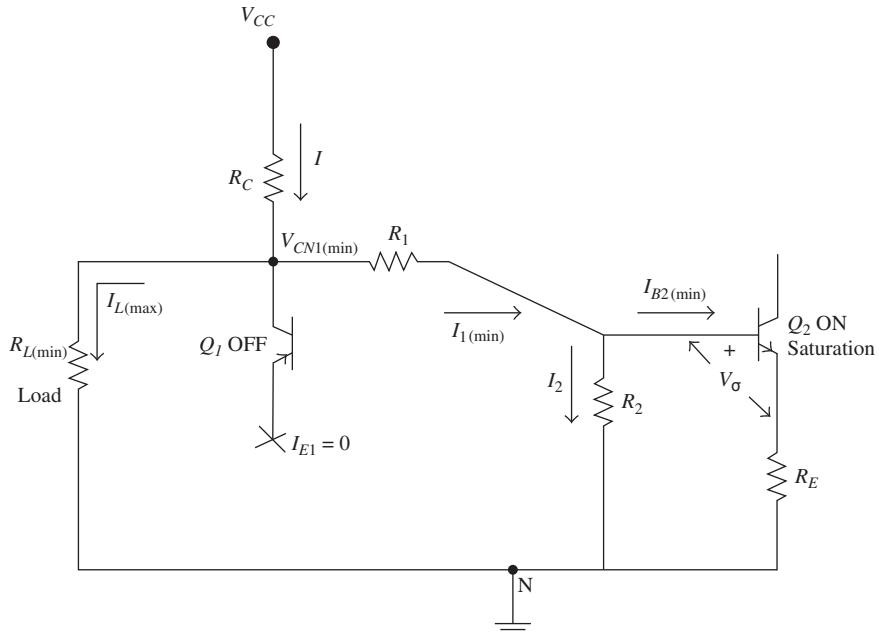


FIGURE 9.9(c) The circuit showing the maximum allowable load current or the minimum load resistance

To calculate the stable-state voltages and currents of a self-biased bistable multivibrator and the heaviest load it can support, let us consider Example 9.3.

EXAMPLE

Example 9.3: Calculate the stable-state currents and voltages for the circuit of Fig. 9.10(a) in which *n*-*p*-*n* silicon transistors are used. Given that $V_{BE(sat)} = 0.7$ V, $V_{CE(sat)} = 0.3$ V and $h_{FE(\min)} = 50$. Take $V_{CC} = 20$ V, $R_C = 4.7$ k Ω , $R_1 = 30$ k Ω and $R_2 = 15$ k Ω , $R_E = 400$ Ω .

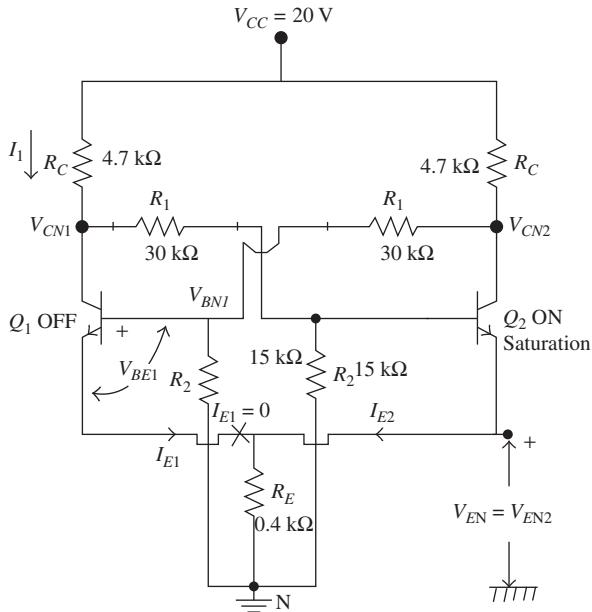


FIGURE 9.10(a) A self-bias bistable multivibrator with component values specified

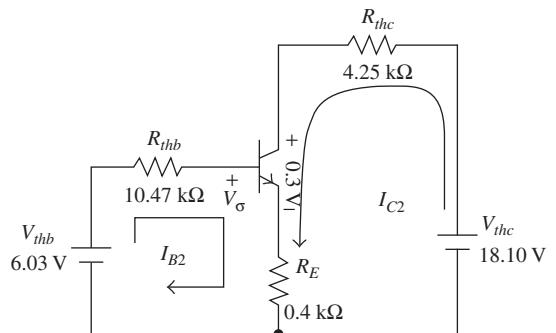


FIGURE 9.10(b) The circuit to calculate the base and collector currents

Let Q_1 be OFF and Q_2 be ON and in saturation. To verify whether Q_2 is in saturation or not, draw the collector loop and base loop of the circuit by Thévenising at the collector and base terminals of Q_2 .

$$V_{thb} = V_{CC} \times \frac{R_2}{R_C + R_1 + R_2} = 20 \times \frac{15}{4.7 + 30 + 15} = 6.03 \text{ V}$$

and

$$R_{thb} = R_2 \quad || \quad (R_C + R_1) = \frac{R_2(R_C + R_1)}{R_2 + R_C + R_1} = \frac{(15)(30 + 4.7)}{4.7 + 30 + 15} = 10.47 \text{ k}\Omega$$

$$V_{thc} = V_{CC} \times \frac{(R_1 + R_2)}{R_C + R_1 + R_2} = \frac{20 \times (30 + 15)}{4.7 + 30 + 15} = 18.10 \text{V}$$

$$R_{thc} = (R_1 + R_2) \parallel R_C = \frac{(30 + 15)(4.7)}{30 + 15 + 4.7} = 4.25 \text{ k}\Omega$$

The base and collector loops of Q_2 are drawn as shown in Fig. 9.10(b).

Writing the KVL equations of the input and output loops:

$$6.03 - 0.7 = (10.47 + 0.4) I_{B2} + 0.4 I_{C2} \quad 18.10 - 0.3 = 0.4 I_{B2} + (4.25 + 0.4) I_{C2}$$

That is,

$$5.33 \text{ V} = 10.87 I_{B2} + 0.4 I_{C2} \quad (1)$$

$$17.80 \text{ V} = 0.4 I_{B2} + 4.65 I_{C2} \quad (2)$$

Solving Eqs. (1) and (2):

$$I_{B2} = 0.35 \text{ mA} \quad I_{C2} = 3.79 \text{ mA}$$

$$I_{B2\min} = \frac{I_{C2}}{h_{FE}} = \frac{3.79 \text{ mA}}{50} = 0.075 \text{ mA} \quad I_{B2} \gg I_{B2(\min)}$$

Hence, Q_2 is saturation.

$$V_{EN} = V_{EN2} = (I_{B2} + I_{C2})R_E \quad V_{EN2} = (0.35 + 3.79)(0.4) = 1.656 \text{ V}$$

$$V_{CN2} = V_{EN2} + V_{CE(\text{sat})} = (1.656 \text{ V} + 0.3 \text{ V}) = 1.956 \text{ V} \quad V_{BN2} = V_{EN2} + V_\sigma = (1.656 \text{ V} + 0.7 \text{ V}) = 2.356 \text{ V}$$

$$V_{BN1} = V_{CN2} \times \frac{R_2}{R_1 + R_2} = \frac{1.956 \times 15}{15 + 30} = 0.652 \text{ V}$$

$$V_{BE1} = V_{BN1} - V_{EN2} = (0.652 \text{ V} - 1.656) = -1.004 \text{ V}$$

As this voltage reverse-biases the emitter diode, Q_1 is OFF.

$$I_1 = \frac{V_{CC} - V_{BN2}}{R_C + R_1} = \frac{20 - 2.356}{4.7 + 30} = 0.508 \text{ mA}$$

$$V_{CN1} = V_{CC} - I_1 R_C = 20 - (0.508)(4.7) = 17.61 \text{ V}$$

The stable-state voltages are:

$$V_{CN1} = 17.61 \text{ V}, \quad V_{BN1} = 0.652 \text{ V}, \quad V_{CN2} = 1.956 \text{ V}, \quad V_{BN2} = 2.356 \text{ V}, \quad V_{EN} = 1.656 \text{ V}$$

To find out the maximum permissible load current I_L (or minimum value of R_L), consider the circuit shown in Fig. 9.10(c).

$$V_{BN2} = 2.356 \text{ V} \quad I_2 = \frac{2.356}{15 \text{ k}\Omega} = 0.157 \text{ mA}$$

Q_2 is ON and is in saturation even when $I_{B2} = I_{B2(\min)}$

Therefore,

$$I_{1(\min)} = I_2 + I_{B2(\min)} = 0.157 + 0.075 = 0.232 \text{ mA}$$

Therefore,

$$V_{CN1(\min)} = I_{1(\min)} R_1 + V_{BN2} = (0.232)(30) + (2.356) = 9.316 \text{ V}$$

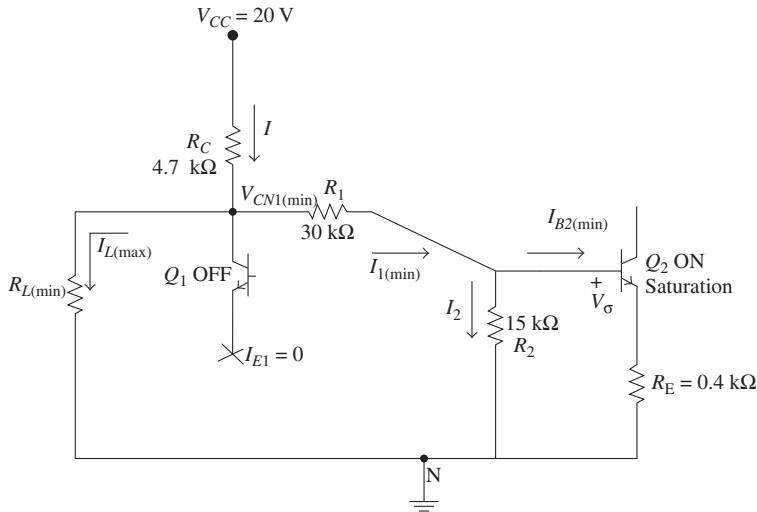


FIGURE 9.10(c) The maximum allowable load current or minimum load resistance

$$I = \frac{V_{CC} - V_{CN1(\min)}}{R_C} = \frac{20 - 9.316}{4.7 \text{ k}\Omega} = 2.27 \text{ mA}$$

$$I_L = I_{L(\max)} = I - I_{1(\min)} = 2.27 - 0.232 = 2.038 \text{ mA}$$

Hence,

$$R_{L(min)} = \frac{V_{CN1(min)}}{I_{L(max)}} = \frac{9.316 \text{ V}}{2.038 \text{ mA}} = 4.57 \text{ k}\Omega$$

9.3.2 The Design of a Self-bias Bistable Multivibrator

Let us try to design a self-bias bistable multivibrator as given in Fig. 9.9(a) using silicon $n-p-n$ transistors whose junction voltages are $V_{CE(\text{sat})}$, $V_{BE(\text{sat})}$, $V_{BE(\text{cut-off})}$ and $h_{FE(\text{min})}$. V_{CC} , I_C are specified.

Assume

$$V_{EN} = \frac{1}{3} V_{CC} \quad (9.48)$$

to ensure that Q_1 is OFF.

$$I_{B2(\min)} = \frac{I_{C2}}{h_{FE(\min)}}$$

Choose $I_{B2} = 1.5I_{B2(\min)}$: The design equations are:

$$R_E = \frac{V_{EN2}}{I_{C2} + I_{B2}} \quad (9.49)$$

$$R_C = \frac{V_{CC} - V_{CE(\text{sat})} - V_{EN2}}{I_C} \quad (9.50)$$

$$\text{Let } I_2 = \frac{1}{10} I_{C2} \quad V_{BN2} = V_{EN2} + V_\sigma$$

$$R_2 = \frac{V_{BN2}}{I_2} \quad (9.51)$$

Find I_2 again if R_2 is chosen as the nearest standard resistance.

$$I_2 = \frac{V_{BN2}}{R_2}$$

$$R_C + R_1 = \frac{V_{CC} - V_{BN2}}{I_2 + I_{B2}} \quad (9.52)$$

$$R_1 = (R_C + R_1) - R_C \quad (9.53)$$

Having fixed the component values, once again verify whether Q_2 is really in saturation or not and Q_1 is OFF or not.

Calculation of the Commutating Condenser Value:

(i) If C is the commuting condenser then,

$$C = \frac{R_2}{R_1} \times C_i \quad (9.54)$$

where, C_i is the stray input capacitance of the transistor. Using Eq. (9.54), C is calculated:

- (ii) In the absence of any specification of C_i , $CR \approx 1\mu s$, where $R = R_1 // R_2$.
- (iii) Another alternative is to use Eq. (9.28) when t_{res} is given or use Eq. (9.29) if $f_{(\max)}$ is given. To understand this design procedure let us consider an example.

E X A M P L E

Example 9.4: Design a self-bias bistable multivibrator shown in Fig. 9.9(a) using silicon $n-p-n$ transistors whose junction voltages are $V_{CE(\text{sat})} = 0.3$ V, $V_{BE(\text{sat})} = 0.7$ V, $V_{BE(\text{cut-off})} = 0$ V and $h_{FE(\min)} = 50$, $V_{CC} = V_{BB} = 9$ V, $I_C = 4$ mA.

Solution:

$$\text{Assume } V_{EN} = \frac{1}{3}V_{CC} = \frac{1}{3} \times 9 = 3 \text{ V} \quad \text{and} \quad I_{C2} = 4 \text{ mA}$$

$$I_{B2(\min)} = \frac{4 \text{ mA}}{50} = 0.08 \text{ mA}$$

$$\text{Choose } I_{B2} = 1.5 I_{B2(\min)} = 0.12 \text{ mA}$$

$$(I_{C2} + I_{B2}) = 4 + 0.12 = 4.12 \text{ mA} \quad R_E = \frac{V_{EN2}}{I_{C2} + I_{B2}} = \frac{3 \text{ V}}{4.12 \text{ mA}} = 0.728 \text{ k}\Omega$$

$$\text{Select } R_E \approx 500 \Omega$$

$$R_C = \frac{V_{CC} - V_{CE(\text{sat})} - V_{EN2}}{I_C} = \frac{9 - 0.3 - 3}{4 \text{ mA}} = \frac{5.7 \text{ V}}{4 \text{ mA}} = 1.425 \text{ k}\Omega$$

$$\text{Choose } R_C = 1 \text{ k}\Omega$$

Let

$$I_2 = \frac{1}{10}I_{C2} = \frac{1}{10} \times 4 \text{ mA} = 0.4 \text{ mA} \quad V_{BN2} = V_{EN2} + V_\sigma = 3 + 0.7 = 3.7 \text{ V}$$

$$R_2 = \frac{V_{BN2}}{I_2} = \frac{3.7 \text{ V}}{0.4 \text{ mA}} = 9.25 \text{ k}\Omega$$

Choose $R_2 = 10 \text{ k}\Omega$ and then find I_2 for this R_2 .

$$I_2 = \frac{V_{BN2}}{R_2} = \frac{3.7 \text{ V}}{10 \text{ k}\Omega} = 0.37 \text{ mA}$$

$$R_C + R_1 = \frac{V_{CC} - V_{BN2}}{I_2 + I_{B2}} = \frac{9 - 3.7}{0.37 + 0.12} = \frac{5.3 \text{ V}}{0.49 \text{ mA}} = 10.8 \text{ k}\Omega$$

$$(R_C + R_1) = 10.8 \text{ k}\Omega \quad (R_C + R_1) - R_C = 10.8 - 1 = 9.8 \text{ k}\Omega$$

Now, choose $R_1 = 10 \text{ k}\Omega$. The circuit with the component values is shown in Fig. 9.11.

Verifying whether Q_2 is really in saturation or not and Q_1 is OFF, with the designed component values; when calculated,

$$I_{B2} = 0.149 \text{ mA}, I_{C2} = 5.46 \text{ mA}, I_{B2(\min)} = 0.109 \text{ mA}, V_{EN2} = 2.8 \text{ V},$$

$$V_{CN2} = 3.1 \text{ V}, V_{BN1} = 1.55 \text{ V}, V_{BE1} = V_{BN1} - V_{EN2} = -1.25 \text{ V}.$$

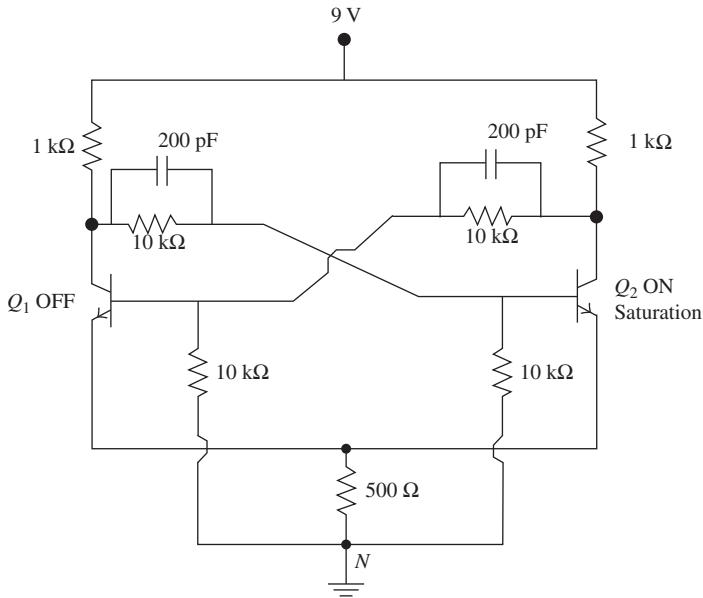


FIGURE 9.11 A self-bias bistable multivibrator with designed component values

These values show that Q_1 is OFF and Q_2 is in saturation.

$$R = R_1 \parallel R_2 \quad R_1 = R_2 = 10 \text{ k}\Omega \quad R = 5 \text{ k}\Omega$$

$$RC = 1 \times 10^{-6} \text{ sec} \quad C = \frac{1 \times 10^{-6}}{5 \times 10^3} = 200 \text{ pF}$$

If t_{res} or $f_{(\text{max})}$ is given, we may use either Eq. (9.28) or Eq. (9.29) to calculate C .

9.4 SCHMITT TRIGGERS

An emitter-coupled bistable multivibrator is also called a Schmitt trigger, named after the designer of the vacuum tube version. In addition to being used as a bistable multivibrator, it has some more important applications.

In the Schmitt trigger circuit shown in Fig. 9.12(a), it is seen that the output of the first transistor is connected to the input of the second transistor through a potential divider network comprising R_1 and R_2 . This is simply an attenuator circuit. Normally R_1 and R_2 are reasonably large resistors so as to avoid loading the collector of Q_1 . Further, the emitter resistance R_E stabilizes the currents and voltages. Note that the second collector and the first emitter are not involved in the regenerative loop (there is no cross-coupling from the second collector to the first base). So, when used as a bistable multivibrator, there is no loading on the second collector and the trigger is applied at the first base and the output is taken from the second collector.

As long as the battery voltage v_i is small, Q_1 is OFF. The voltage at this collector is approximately V_{CC} . This voltage is coupled to the second base through R_1 and R_2 . As a result, Q_2 can conduct. If Q_2 conducts, it can operate in the active region or it may be driven into saturation.

Let it be assumed that Q_2 is in the active region. The base current I_{B2} and collector current I_{C2} flows through R_E . Therefore, a voltage $V_{EN} = V_{EN2}$ is developed in R_E . As $V_{BE1} = V_{BN1} - V_{EN2}$ and if V_{BE1} reverse-biases the emitter diode of Q_1 , then as assumed Q_1 is OFF.

If V_{BN1} (v_i) is increased, at a value $(V_{EN2} + V_{\gamma 1})$, Q_1 begins to conduct. As a result, the voltage at the second base decreases, hence the base current of Q_2 decreases, its collector current also reduces and consequently the voltage at the second collector rises. If the input is increased further, Q_1 goes into the ON state and Q_2 into the OFF state. If the loop gain is less than unity (this condition can be satisfied by reducing the collector load of Q_1), there exists a region of linearity in the transfer characteristic. In this region an incremental change at the input Δv_i will cause a proportional change in the output, Δv_o as shown in Fig. 9.12(b). If the loop gain is made equal to 1 by adjusting R_{C1} and R_{C2} , the transfer characteristic is as shown in Fig. 9.12(c).

If on the other hand, the loop gain is made greater than 1, the transfer characteristic is an S-shaped characteristic, as shown in Fig. 9.12(d). When the input is increased from 0 to a larger value, at a voltage V_1 , the output suddenly jumps from a smaller value to V_{CC} as shown in Fig. 9.13(a). Even if the input is increased further, the output remains at V_{CC} .

If on the other hand, the input is decreased, then at a voltage V_2 the output falls from V_{CC} to a smaller value, as shown in Fig. 9.13(b). If these two curves are combined together, the resultant transfer characteristic, that gives the relation between the input and the output, is shown in Fig. 9.13(c).

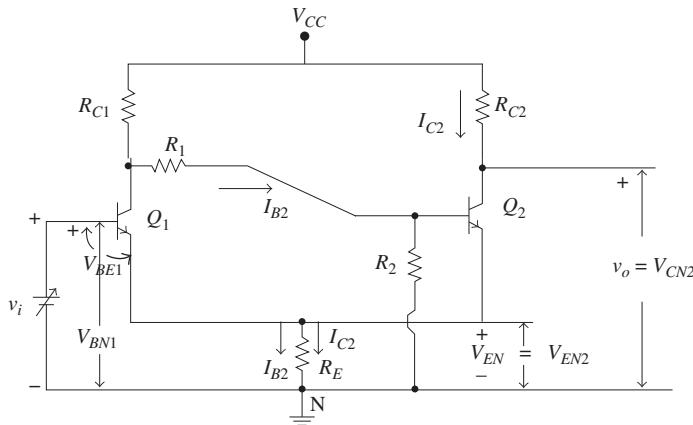


FIGURE 9.12(a) The Schmitt trigger

V_1 is called the upper trip point (UTP) and V_2 is called the lower trip point (LTP). The closed loop in Fig. 9.13(c) is termed the hysteresis loop and the difference in voltages V_1 and V_2 is called the hysteresis voltage, V_H . Thus, $V_H = V_1 - V_2$.

It is seen from the above discussion that a Schmitt trigger exhibits hysteresis, i.e., when the input v_i is increased to reach a voltage V_1 it is required to first pass through a point, V_2 at which the reverse transition takes place. Similarly, when the input now is reduced to reach V_2 it has to pass through the point V_1 . This is called hysteresis. This characteristic of the Schmitt trigger is used to an advantage in waveshaping applications.

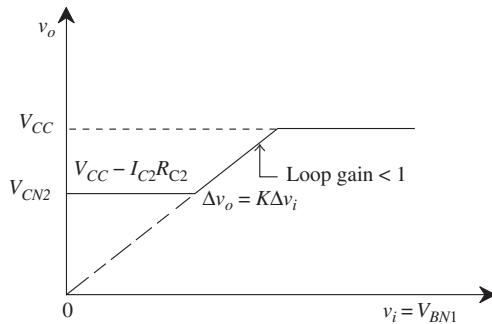


FIGURE 9.12(b) The transfer characteristic of a Schmitt trigger when the loop gain < 1

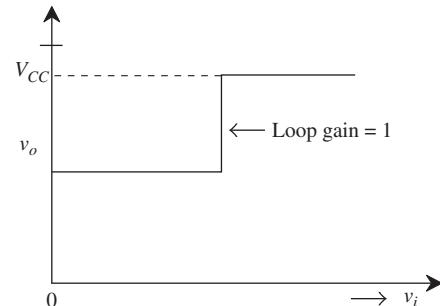


FIGURE 9.12(c) The transfer characteristic of a Schmitt trigger when the loop gain is 1

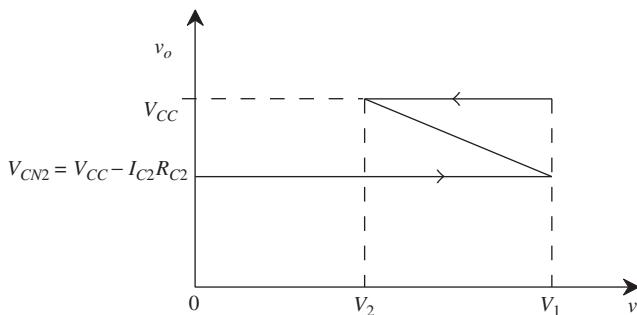


FIGURE 9.12(d) The transfer characteristic of a Schmitt trigger when the loop gains > 1

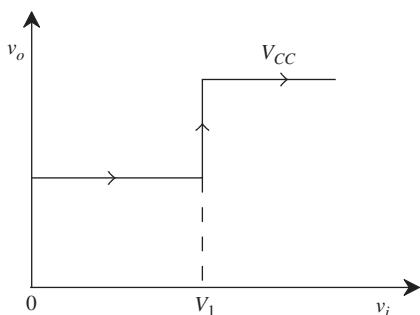


FIGURE 9.13(a) The output rises suddenly to V_{CC}

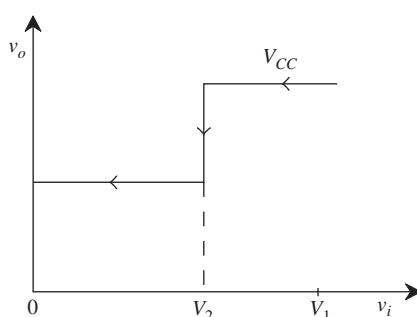


FIGURE 9.13(b) When the input is decreased the output falls from V_{CC}

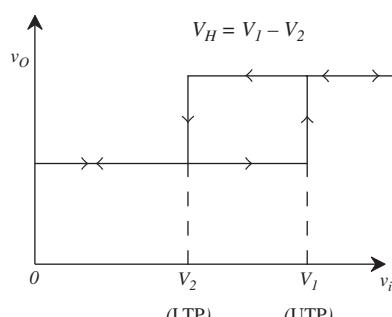


FIGURE 9.13(c) The transfer characteristic of a Schmitt trigger

9.4.1 Calculation of the Upper Trip Point (V_1)

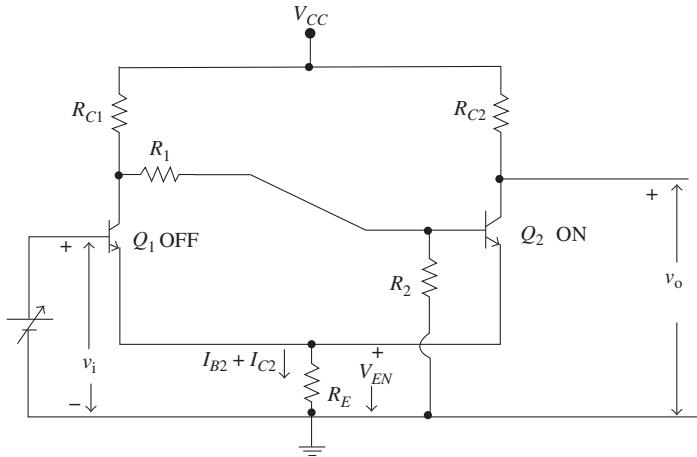


FIGURE 9.14 The Schmitt trigger circuit

In the Schmitt trigger circuit, shown in Fig. 9.14, when the input is increased, till V_1 is reached Q_1 is OFF and Q_2 is ON. As a result, I_{B2} and I_{C2} flow through R_E developing a voltage V_{EN} in R_E . Now, if the input is such that its value is $(V_{EN} + V_{y1}) = V_1$ (UTP), Q_1 switches into the ON state and Q_2 switches into the OFF state.

If the circuit shown in Fig. 9.14 is Thévenised at the base of Q_2 , the Thévenin voltage source is,

$$V' = V_{CC} \times \frac{R_2}{R_{C1} + R_1 + R_2} \quad (9.55)$$

And its internal resistance R' is given by the relation:

$$R' = R_2 || (R_{C1} + R_1) \quad (9.56)$$

The resultant simplified circuit is shown in Fig. 9.15(a).

$$I_{E2} = I_{B2} + I_{C2} = I_{B2} \left(1 + \frac{I_{C2}}{I_{B2}} \right) = I_{B2} (1 + h_{FE}) \quad (9.57)$$

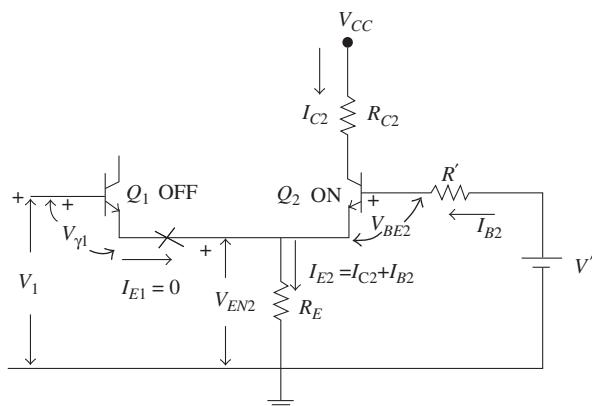


FIGURE 9.15(a) The circuit that enables computation of V_1

The total current in R_E is $I_{B2}(1+h_{FE})$ and the current in R' is I_{B2} . As far as I_{B2} is concerned, R_E is seen to have increased by a factor $(1+h_{FE})$. The net voltage in the base loop is, $(V' - V_{BE2})$ and is equal to the sum of the voltage drops across R' and $(1+h_{FE})R_E$, as shown in Fig. 9.15(b).

$$\begin{aligned}\therefore V_{EN2} &= (V' - V_{BE2}) \frac{R'_E}{R' + R'_E} \\ &= (V' - V_{BE2}) \frac{R_E(1+h_{FE})}{R' + R_E(1+h_{FE})} \quad (9.58)\end{aligned}$$

In Eq. (9.58), as:

$$R' \ll R_E(1+h_{FE}) \quad R' + R_E(1+h_{FE}) \cong R_E(1+h_{FE})$$

Then Eq. (9.58) reduces to:

$$\therefore V_{EN2} = (V' - V_{BE2}) \frac{R_E(1+h_{FE})}{R_E(1+h_{FE})} \quad (9.59)$$

$$= V' - V_{BE2} \quad (9.60)$$

From Fig. 9.15(a), using Eq. (9.60):

$$V_1 = V_{EN2} + V_{\gamma_1} \quad (9.61)$$

The calculation of V_1 is made based on the assumption that Q_2 is in the active region. Now, to verify whether Q_2 is in the active region, V_{CB2} is calculated and checked if this reverse-biases the collector diode by a reasonable voltage or not. If it does, the device Q_2 is indeed in the active region.

From the circuit in Fig. 9.15(a), we have:

$$V_{CB2} = V_{CE2} - V_{BE2} \quad \text{and} \quad V_{CE2} = V_{CC} - I_{C2}R_{C2} - V_{EN2}$$

$$\therefore V_{CB2} = V_{CC} - I_{C2}R_{C2} - V_{EN2} - V_{BE2} \quad (9.62)$$

To calculate V_{CB2} using Eq. (9.62), we have to find I_{C2} .

$$\begin{aligned}V_{EN2} &= (I_{B2} + I_{C2})R_E = I_{C2} \left(1 + \frac{1}{h_{FE}}\right)R_E \\ V_{EN2} &= I_{C2}R''_E \quad (9.63)\end{aligned}$$

where,

$$R''_E = \left(1 + \frac{1}{h_{FE}}\right)R_E \quad (9.64)$$

Substituting Eq. (9.63) in Eq. (9.61) we get:

$$V_1 = I_{C2}R''_E + V_{\gamma_1} \quad (9.65)$$

where R''_E is given by Eq. (9.64). From Eq. (9.63) I_{C2} is given as:

$$I_{C2} = \frac{V_{EN2}}{R''_E} \quad (9.66)$$

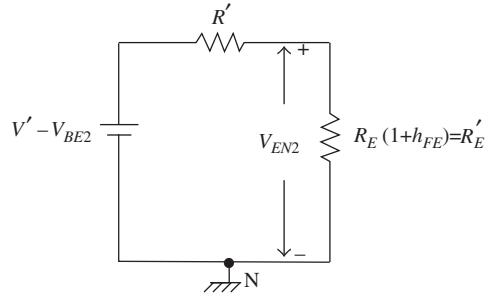


FIGURE 9.15(b) The circuit to calculate V_{EN2}

These calculations were made based on the assumption that Q_2 is in the active region. Having made the calculations, we once again verify whether Q_2 is really in the active region or not, to justify the validity of the calculations made. V_{CB2} is calculated using Eq. (9.62). If the base–collector diode is reverse-biased, then Q_2 is in the active region as assumed.

9.4.2 Calculation of the Lower Trip Point (V_2)

At the voltage V_1 (UTP), Q_1 is ON and Q_2 is OFF. Now if the input is reduced, till voltage V_2 is reached, Q_1 is ON and Q_2 is still OFF. However, when the voltage at the input is V_2 then the voltage at the second base is $V_{EN1} + V_{\gamma 2}$. Q_2 again switches into the ON state and Q_1 into the OFF state.

Consider the Schmitt trigger circuit shown in Fig. 9.14. The Thévenin voltage source at the first collector is:

$$V_t = V_{CC} \frac{R_1 + R_2}{R_{C1} + R_1 + R_2} \quad (9.67)$$

And its internal resistance R_t is,

$$R_t = R_{C1} // (R_1 + R_2) \quad (9.68)$$

The first collector and the second base are connected through R_1 and R_2 , as shown in Fig. 9.16.

$$\therefore V_{BN2} = V_{CN1} \frac{R_2}{R_1 + R_2} = \alpha V_{CN1} \quad (9.69)$$

where

$$\alpha = \frac{R_2}{R_1 + R_2} \quad (9.70)$$

$$R_t = \frac{R_{C1}(R_1 + R_2)}{R_{C1} + R_1 + R_2} \quad (9.71)$$

The circuit that enables us to calculate V_2 is shown in Fig. 9.17.

Writing the KVL equation for the base loop of Q_2 :

$$\alpha V_{CN1} = V_{\gamma 2} + (I_{B1} + I_{C1})R_E \quad V_{CN1} = V_t - I_{C1}R_t$$

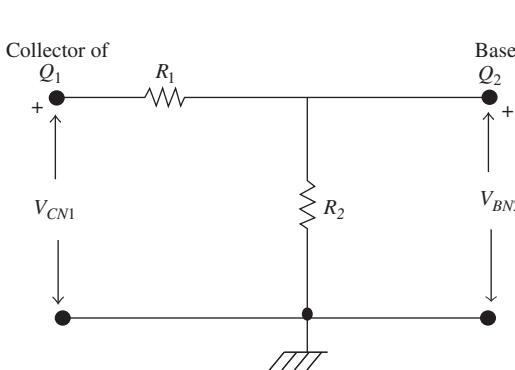


FIGURE 9.16 The coupling network from the first collector to the second base

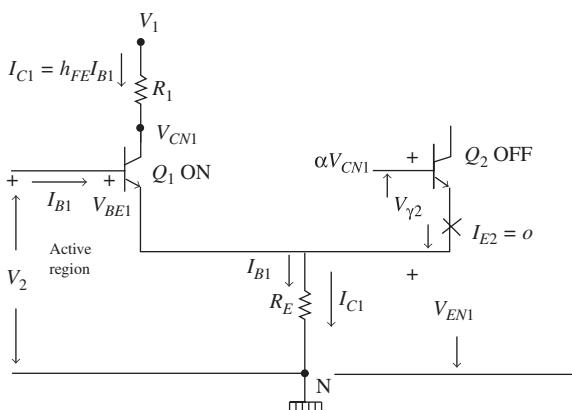


FIGURE 9.17 The circuit to calculate V_2

$$\alpha(V_t - I_{C1}R_t) = V_{\gamma_2} + I_{C1} \left(1 + \frac{1}{h_{FE}}\right) R_E$$

Let:

$$R''_E = \left(1 + \frac{1}{h_{FE}}\right) R_E \quad (9.72)$$

$$\alpha V_t - I_{C1} \alpha R_t = V_{\gamma_2} + I_{C1} R''_E \quad I_{C1} (\alpha R_t + R''_E) = \alpha V_t - V_{\gamma_2}$$

$$I_{C1} = \frac{(\alpha V_t - V_{\gamma_2})}{(\alpha R_t + R''_E)} \quad (9.73)$$

However, we have:

$$\alpha V_t = V_{CC} \frac{(R_1 + R_2)}{(R_{C1} + R_1 + R_2)} \times \left(\frac{R_2}{R_1 + R_2} \right) = V_{CC} \frac{R_2}{(R_{C1} + R_1 + R_2)} = V' \quad (9.74)$$

Therefore, from Eq. (9.73)

$$I_{C1} = \frac{(V' - V_{\gamma_2})}{(\alpha R_t + R''_E)} \quad (9.75)$$

$$V_2 = V_{BE1} + I_{C1} R''_E \quad (9.76)$$

Using Eqs. (9.72), (9.74) and (9.75), V_2 is calculated. To understand the method of calculation for V_1 and V_2 , let us consider Example 9.5.

EXAMPLE

Example 9.5: For the Schmitt trigger circuit shown in Fig. 9.18(a), calculate V_1 and V_2 .

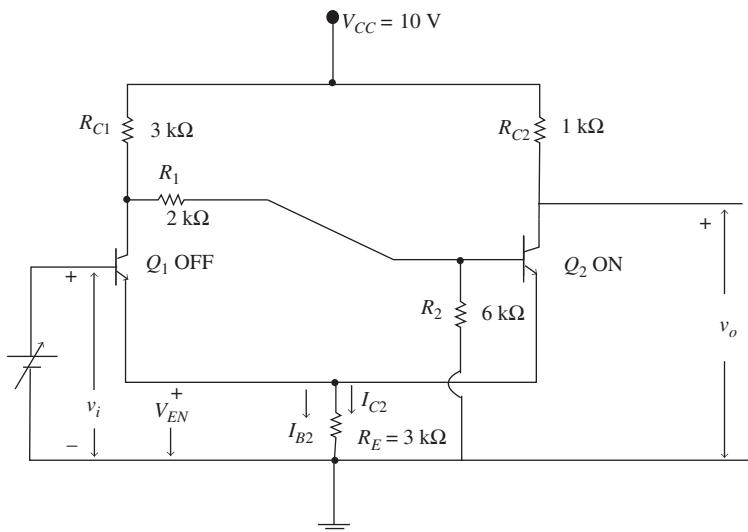


FIGURE 9.18(a) The Schmitt trigger with components mentioned

Solution:

a) Calculation of V_1 :

Consider the Schmitt trigger circuit, shown in Fig. 9.18(a). From Eq. (9.55):

$$V' = V_{CC} \times \frac{R_2}{R_{C1} + R_1 + R_2} = 10 \times \frac{6}{3 + 2 + 6} = 5.45 \text{ V}$$

R' the internal resistance of this Thévenin source, as given by Eq. (9.56), is:

$$R' = R_2 // (R_{C1} + R_1) = 6 // (3 + 2) = \frac{6 \times 5}{6 + 5} = 2.73 \text{ k}\Omega$$

The resultant circuit is shown in Fig. 9.18(b).

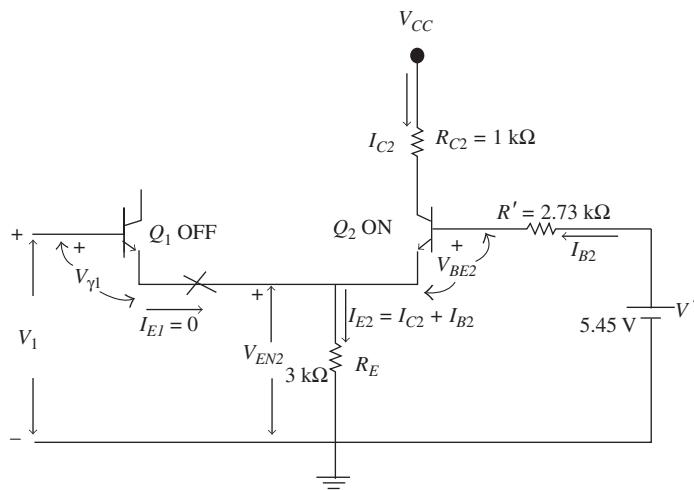


FIGURE 9.18(b) The circuit that enables computation of V_1

From Eq. (9.58):

$$V_{EN2} = (V' - V_{BE2}) \frac{R_E(1 + h_{FE})}{R' + R_E(1 + h_{FE})}$$

If Q_2 is in the active region, typically, for silicon $V_{BE2} = 0.6 \text{ V}$ and let $h_{FE} = 50$,

$$R_E(1 + h_{FE}) = 3(1 + 50) = 153 \text{ k}\Omega$$

Therefore,

$$V_{EN2} = (5.45 - 0.6) \times \frac{153}{2.73 + 153} = 4.85 \times \frac{153}{155.73} = 4.76 \text{ V}$$

Therefore,

$$V_1 = V_{EN2} + V_{BE2} = 4.76 + 0.6 = 5.36 \text{ V.}$$

The calculation of V_1 is made based on the assumption that Q_2 is in the active region. To find out whether Q_2 is in the active region or not, we calculate V_{CB2} .

$$V_{CB2} = V_{CC} - I_{C2}R_{C2} - V_{EN2} - V_{BE2}.$$

From Eq. (9.72)

$$R_E'' = (1 + \frac{1}{h_{FE}})R_E = (1 + \frac{1}{50})3 = \frac{51}{50} \times 3 = 3.06 \text{ k}\Omega$$

$$\text{Hence } I_{C2} = \frac{V_{EN2}}{R''_E} = \frac{4.76 \text{ V}}{3.06 \text{ k}\Omega} = 1.56 \text{ mA}$$

$$V_{CB2} = 10 - (1.56 \times 1) - 4.76 - 0.6 = 10 - 6.92 = 3.08 \text{ V}$$

As the collector of Q_2 is positive with respect to the base by 3.08 V the collector diode is reverse-biased. Hence, Q_2 is in the active region, as assumed.

(b) Calculation of V_2 :

The circuit that enables us to calculate V_2 is shown in Fig. 9.18(c). From the circuit values:

$$\alpha = \frac{R_2}{R_1 + R_2} = \frac{6}{2+6} = 0.75 \quad R_t = \frac{3(2+6)}{3+2+6} = \frac{24}{11} = 2.18 \text{ k}\Omega$$

$$\alpha R_t = 0.75 \times 2.18 \text{ k}\Omega = 1.64 \text{ k}\Omega \quad R_E'' = 3.06 \text{ k}\Omega \quad V_2 = V_{BE1} + I_{C1} R_E''$$

$$I_{C1} = \frac{(V' - V_{\gamma 2})}{\alpha R_t + R_F''} = \frac{(5.45 - 0.5)}{1.64 + 3.06} = \frac{4.95}{4.7} = 1.05 \text{ mA}$$

$$\therefore V_2 = 0.6 \text{ V} + (1.05 \text{ mA})(3.06 \text{ k}\Omega) = 0.6 \text{ V} + 3.22 \text{ V} = 3.82 \text{ V}$$

Hence, for the given Schmitt trigger:

$$V_1 = 5.36 \text{ V} \quad V_2 = 3.82 \text{ V} \quad V_H = V_1 - V_2 = 5.36 - 3.82 = 1.54 \text{ V}$$

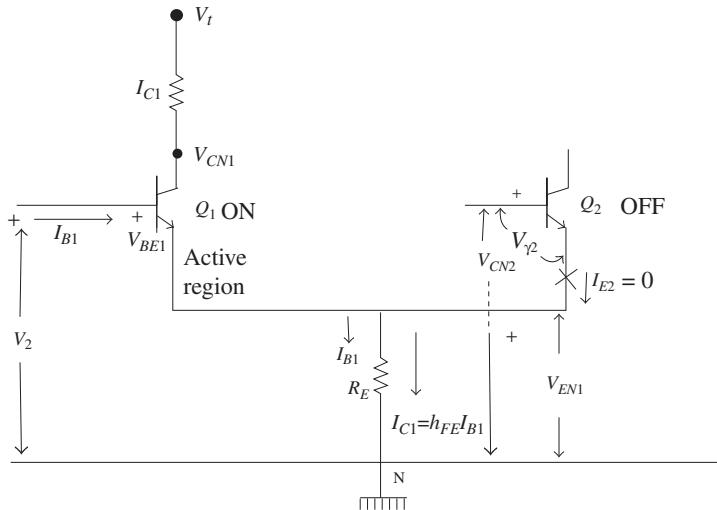


FIGURE 9.18(c) The circuit to calculate V_2

9.4.3 Methods to Eliminate Hysteresis in a Schmitt Trigger

It is evident from Fig. 9.13(c), that hysteresis is present in a Schmitt trigger because the loop gain is not exactly unity, but is greater than 1. Hysteresis is needed when a schmitt trigger used as a histable multitrigger and also when converting a time-varying signal into a square wave. But when it used as a comparator, hysteresis needs to be eliminated. The following schemes can be implemented to eliminate hysteresis in a Schmitt trigger:

- (i) V_1 and V_2 are made to coincide with the proper choice of R_1 and R_2 . However, by this method, though, it is not possible to make V_1 identical to V_2 , they can be brought close to each other in practice.
- (ii) Another method to eliminate hysteresis is by introducing a resistance R_{e2} in series with the emitter terminal of Q_2 , as shown in Fig. 9.19(a).

R_{e2} will change V_1 , but has no effect on V_2 . Therefore, by including R_{e2} in series with the emitter of Q_2 , it is possible to reduce V_1 to the level of V_2 , (V_1 is made equal to V_2), thereby reducing hysteresis. The method to calculate R_{e2} , for the circuit shown in Fig. 9.19(b), calculate V' and R' as illustrated in Section 9.4.1, as shown in Fig. 9.15(a).

From Fig. 9.19(b), we have:

$$V_{EN} = V_{EN2} = (V' - V_{BE2}) \frac{(1 + h_{FE})R_E}{R' + (1 + h_{FE})(R_{e2} + R_E)} \quad (9.77)$$

$$\text{And } V_1 = V_{EN2} + V_{\gamma 1} = (V' - V_{BE2}) \frac{(1 + h_{FE})R_E}{R' + (1 + h_{FE})(R_{e2} + R_E)} + V_{\gamma 1} \quad (9.78)$$

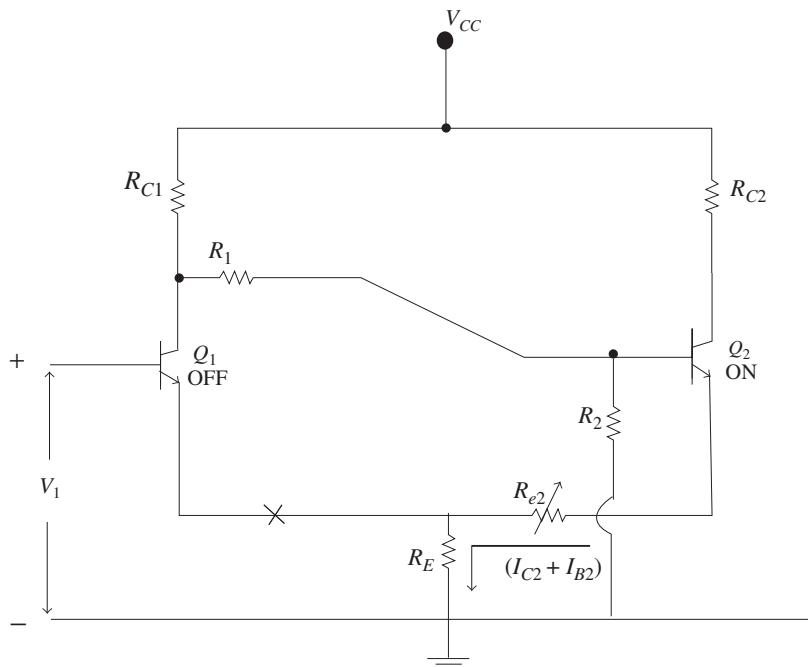
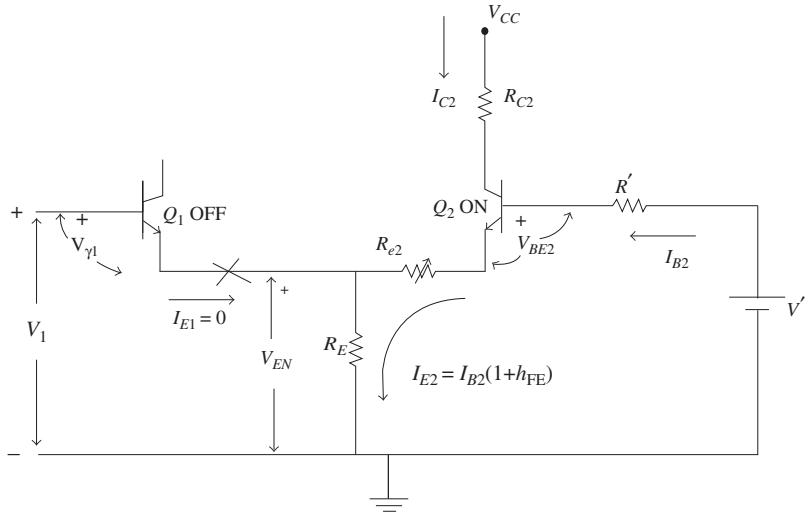


FIGURE 9.19(a) An alternate method to eliminate hysteresis

FIGURE 9.19(b) The circuit to calculate R_{e2}

To eliminate hysteresis, V_1 should be made equal to V_2 , which means that in Eq. (9.78) V_1 is replaced by V_2

$$(V' - V_{BE2}) \frac{(1 + h_{FE})R_E}{R' + (1 + h_{FE})(R_{e2} + R_E)} + V_{\gamma 1} = V_2 \quad (9.79)$$

R_{e2} that eliminates hysteresis is calculated using Eq. (9.79). To further understand the procedure let us consider Example 9.6.

EXAMPLE

Example 9.6: From the problem in Example 9.5, we have $V_1 = 5.36$ V, $V_2 = 3.82$ V, $V' = 5.45$ V, $R' = 2.73$ k Ω , $R_E = 3$ k Ω , $h_{FE} = 50$, $V_{BE2} = 0.6$ V. Find the value of R_{e2} that ensures $V_1 = V_2 = 3.82$ V and eliminates hysteresis.

Solution: We have from Eq. (9.79):

$$(V' - V_{BE2}) \frac{(1 + h_{FE})R_E}{R' + (1 + h_{FE})(R_{e2} + R_E)} + V_{\gamma 1} = V_2$$

$$(5.45 - 0.6) \frac{(1 + 50)3}{2.73 + (1 + 50)(R_{e2} + 3)} + 0.5 = 3.82$$

$$\frac{742.05}{155.73 + 51R_{e2}} + 0.5 = 3.82$$

Therefore,

$$R_{e2} = \frac{742.05 - 517.02}{169.32} = \frac{225.03}{169.32} = 1.33 \text{ k}\Omega$$

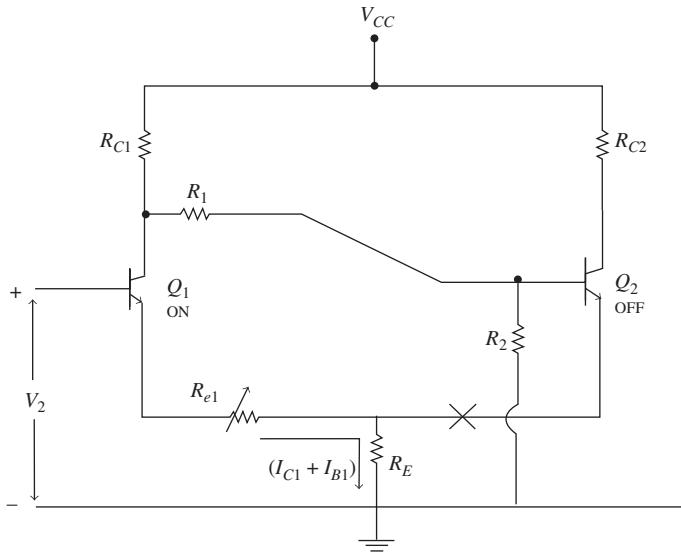


FIGURE 9.19(c) Another method to eliminate hysteresis

(iii) Another method to eliminate hysteresis is to introduce a resistance R_{e1} in series with the emitter terminal of Q_1 , as shown in Fig. 9.19(c).

R_{e1} is not going to change V_1 but will only influence V_2 . To eliminate hysteresis, R_{e1} is chosen such that V_2 is increased to the level of V_1 . To achieve this, we must ensure that V_2 plus the voltage drop across R_{e1} is V_1 .

$$V_1 = V_2 + R_{e1}(I_{C1} + I_{B1}) \quad (1)$$

From Eq. (1):

$$R_{e1} = \frac{V_1 - V_2}{I_{C1} + I_{B1}} = \frac{V_H}{I_{C1} + I_{B1}} \quad (2)$$

$$I_{C1} + I_{B1} = I_{C1} \left(1 + \frac{1}{h_{FE}}\right) = I_{C1} \frac{(1 + h_{FE})}{h_{FE}} \quad (3)$$

Substituting Eq. (3) in Eq. (2), we get:

$$R_{e1} = \frac{V_H}{I_{C1}} \times \frac{h_{FE}}{(1 + h_{FE})} \quad (4)$$

To understand the procedure to calculate R_{e1} , let us consider an example.

EXAMPLE

Example 9.7: From the problem in Example 9.5, we have $V_1 = 5.36$ V, $V_2 = 3.82$ V, $I_{C1} = 1.05$ mA, $h_{FE} = 50$. Find the value of R_{e1} .

Solution:

Using Eq. (9.83),

$$R_{e1} = \frac{(5.36 - 3.82)}{1.05} \times \frac{50}{51} = 1.43 \text{ k}\Omega$$

9.4.4 Applications of a Schmitt Trigger

The following are some applications of a Schmitt trigger:

(a) An emitter-coupled bistable multivibrator is called the Schmitt trigger. Hence, a Schmitt trigger can be used as a bistable multivibrator. Consider the transfer characteristic, shown in Fig. 9.20(a).

To use this circuit as a bistable multivibrator, the first device Q_1 is biased to have a voltage V at its base. Initially, let the output be at 0 level ($V_{CC} - I_{C2}R_{C2}$). To change this to 1(V_{CC}) apply a positive pulse at the base of Q_1 , whose magnitude is more positive than ($V_1 - V$) as shown in Fig. 9.20(b).

To once again change the output to a 0 level, apply a pulse at the base of Q_1 , which is negative with respect to V and whose magnitude is more negative than ($V_2 - V$) as shown in Fig. 9.20(c).

(b) A Schmitt trigger can be used as an amplitude comparator. In an amplitude comparator, the amplitude of a time varying signal is compared with a reference and it tells us the time instant at which the input has reached this set reference level. For example, consider the diode comparator circuit shown in Fig. 9.21(a). As long as $v_i < V_R$, D is OFF and $v_o = v_i$. When $v_i \geq V_R$, D is ON and $v_o = V_R$.

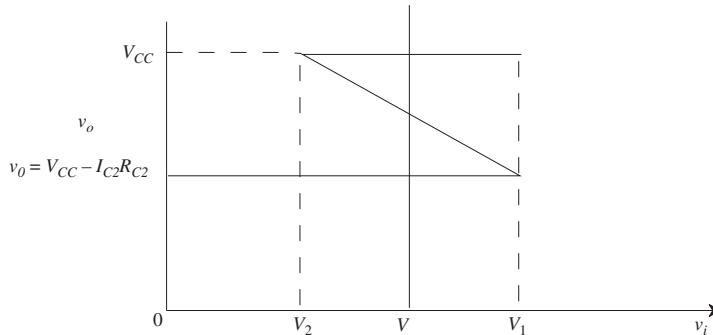


FIGURE 9.20(a) The transfer characteristic of a Schmitt trigger

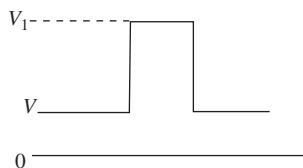


FIGURE 9.20(b) The trigger to change the output from 0 to 1 level

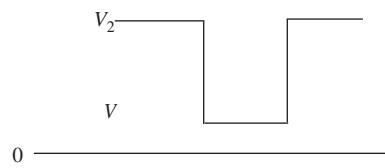


FIGURE 9.20(c) The trigger to change the output from 1 to 0 level

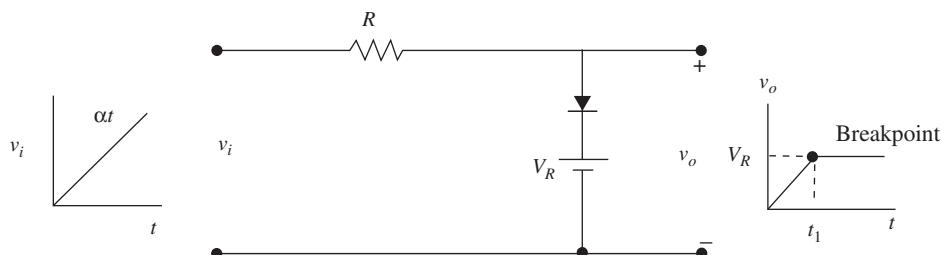


FIGURE 9.21(a) A diode comparator

The output follows the input till $t = t_1$ and then the slope of the output abruptly changes. This is called the break point, and t_1 is the time instant at which v_i has reached V_R .

Now consider the Schmitt trigger (in which hysteresis is eliminated) as a comparator with input and output shown in Fig. 9.21(b). A relatively small dc voltage is there at the output till $V_1 (= V_2)$ is reached at the input. The moment the input is V_1 , the output abruptly jumps to V_{CC} . The slope of the input has no relation to the slope of the signal at the output. Thus, a Schmitt trigger can be used as a better amplitude comparator.

(c) A Schmitt trigger can be used as a waveshaping circuit (or a squaring circuit). It can be used to convert any arbitrarily time varying signal into a square-wave output. The only condition to be satisfied is that the input signal has amplitude more than V_1 and also less than V_2 . Consider the input for which the output is plotted as shown in Fig. 9.22.

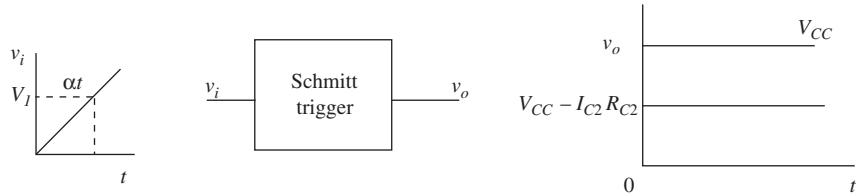


FIGURE 9.21(b) A Schmitt trigger as a comparator

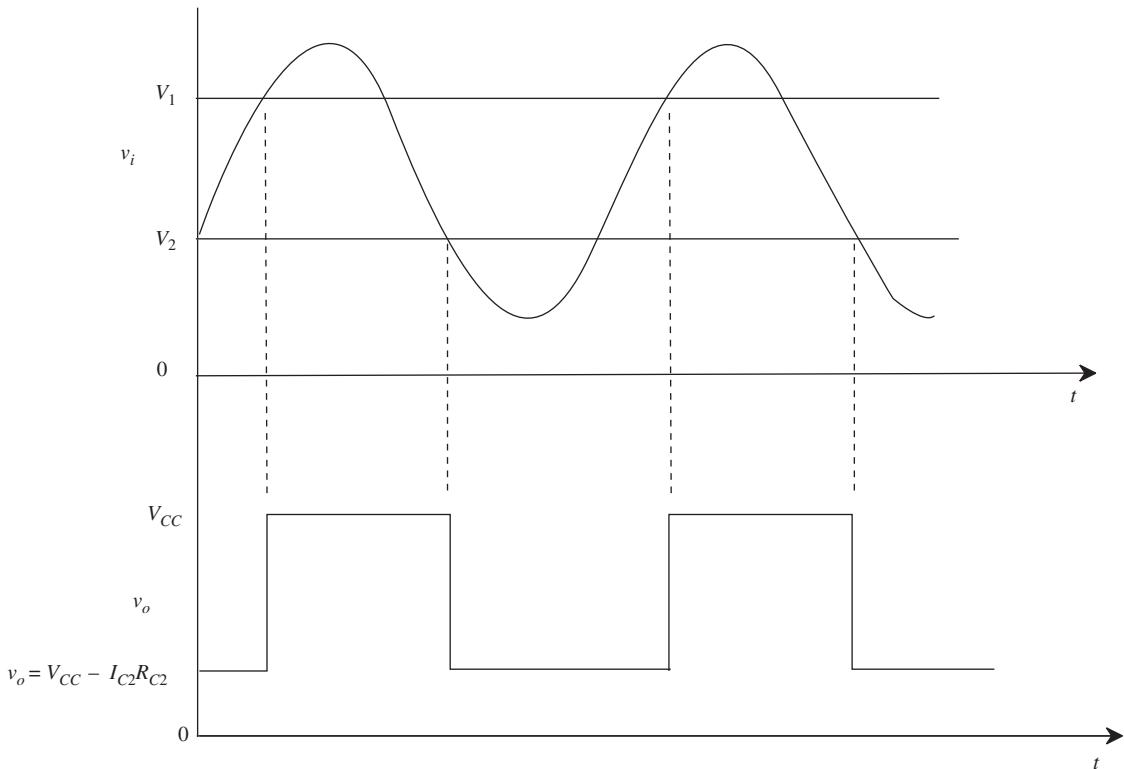


FIGURE 9.22 The Schmitt trigger as a squaring circuit

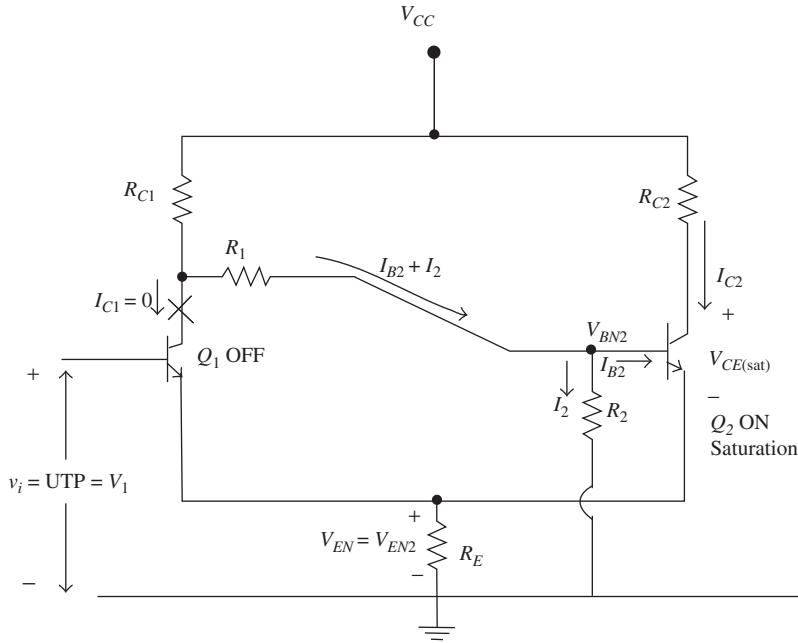


FIGURE 9.23(a) A Schmitt trigger circuit

9.4.5 The Design of a Schmitt Trigger

In this section, the procedure to design a Schmitt trigger is presented. For designing the Schmitt trigger shown in Fig. 9.23(a), UTP (V_1) and LTP (V_2) values, h_{FE} , desired I_C and V_{CC} are to be specified.

(a) Till UTP is reached Q_1 is OFF and Q_2 is ON and in saturation. Just at V_1 (UTP), Q_1 goes ON and Q_2 goes OFF.

Therefore, $V_1 = \text{UTP} = V_{BN2}$ and $I_E = I_C$ is specified. Therefore:

$$R_E = \frac{V_1 - V_{BE2}}{I_E} \quad (9.80)$$

R_E is chosen using Eq. (9.80). If Q_2 is in saturation, $V_{CE} = V_{CE(\text{sat})}$. From the circuit shown in Fig. 9.23(a), we have $I_{C2}R_{C2} = V_{CC} - V_{CE(\text{sat})} - V_{EN2}$

Therefore,

$$R_{C2} = \frac{V_{CC} - V_{CE(\text{sat})} - V_{EN2}}{I_{C2}} \quad (9.81)$$

R_{C2} is calculated using Eq. (9.81).

Assume that

$$I_2 = \frac{I_{C2}}{10} \quad (9.82)$$

Using Eq. (9.82):

$$R_2 = \frac{V_{BN2}}{I_2} = \frac{V_1}{I_2} \quad (9.83)$$

Using the value of h_{FE} specified, we can now calculate $I_{B2(\min)}$ as:

$$I_{B2(\min)} = \frac{I_{C2}}{h_{FE}} \quad (9.84)$$

For Q_2 to be in saturation $I_{B2(\text{sat})}$ must be larger than $I_{B2(\min)}$, choose

$$I_{B2(\text{sat})} = 1.5 \times I_{B2(\min)} \quad (9.85)$$

Using Eq. (9.82) and (9.85), we can calculate $(I_2 + I_{B2})$.

From the circuit shown in Fig. 9.23(a):

$$R_{C1} + R_1 = \frac{V_{CC} - V_{BN2}}{I_2 + I_{B2}} = R \quad (9.86)$$

R is calculated using Eq. (9.86).

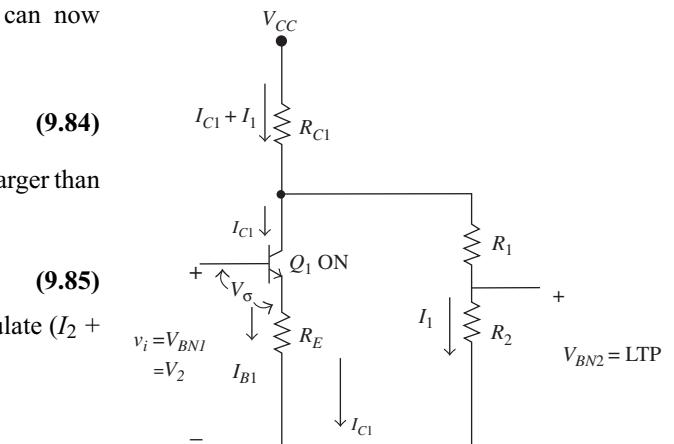


FIGURE 9.23(b) The circuit at LTP

$$R_1 = R - R_{C1} \quad (9.87)$$

R_1 is chosen using Eq. (9.87).

(b) At $LTP = V_2$, consider the circuit shown in Fig. 9.23(b).

$$V_{BN2} = V_{BN1} = LTP = V_2$$

Let I_1 be the current in R_2 ,

$$I_1 = \frac{V_{BN2}}{R_2} = \frac{V_2}{R_2} \quad (9.88)$$

$$I_{C1} = I_{E1} = \frac{V_2 - V_\sigma}{R_E} \quad (9.89)$$

Writing the KVL equation of the outer loop consisting of R_{C1} , R_1 and R_2 :

$$V_{CC} = (I_{C1} + I_1)R_{C1} + I_1(R_1 + R_2)$$

Using Eq. (9.87):

$$V_{CC} = (I_{C1} + I_1)R_{C1} + I_1(R - R_{C1} + R_2)$$

Therefore,

$$V_{CC} = I_{C1}R_{C1} + I_1(R + R_2) \quad (9.90)$$

From Eq. (9.90),

$$R_{C1} = \frac{V_{CC} - I_1(R + R_2)}{I_{C1}} \quad (9.91)$$

R_{C1} is calculated using Eq. (9.95),

$$R_1 = R - R_{C1}$$

All the components of the Schmitt trigger are fixed. The procedure to design a Schmitt trigger is presented in the Example 9.8.

EXAMPLE

Example 9.8: Design a Schmitt trigger shown in Fig. 9.24(a) with UTP of 6 V and LTP of 3 V. Ge transistors with $h_{FE(\min)} = 50$ and $I_C = 4 \text{ mA}$ are used. The supply voltage is 15 V.

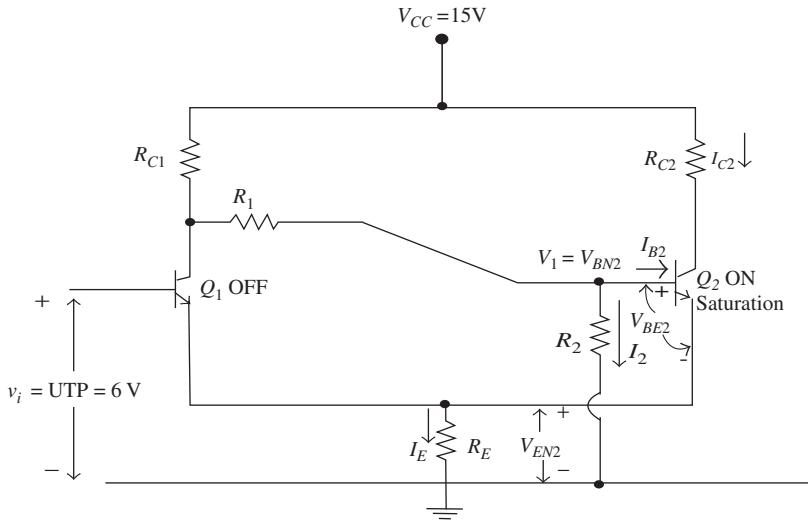


FIGURE 9.24(a) The Schmitt trigger circuit

Solution:

Till UTP is reached, Q_1 is OFF and Q_2 is ON and in saturation. Just at V_1 (UTP) Q_1 goes ON and Q_2 goes OFF. Therefore, $V_1 = \text{UTP} = V_{BN2} = 6 \text{ V}$

$$I_E = I_C = 4 \text{ mA}$$

$$R_E = \frac{V_1 - V_{BE2}}{I_E} = \frac{V_{EN2}}{I_E} = \frac{6 - 0.3}{4 \text{ mA}} = \frac{5.7 \text{ V}}{4 \text{ mA}} = 1.425 \text{ k}\Omega$$

Choose $R_E = 1 \text{ k}\Omega$

If Q_2 is in saturation $V_{CE(\text{sat})} = 0.1 \text{ V}$, $V_\sigma = 0.3 \text{ V}$, so

$$I_C R_{C2} = V_{CC} - V_{CE(\text{sat})} - V_{EN2}$$

Therefore,

$$R_{C2} = \frac{15 - 0.1 - 5.7}{4 \text{ mA}} = \frac{9.2 \text{ V}}{4 \text{ mA}} = 2.3 \text{ k}\Omega$$

Choose $R_{C2} = 2.2 \text{ k}\Omega$

$$I_2 = \frac{1}{10} I_{C2} = 0.4 \text{ mA} \quad R_2 = \frac{V_{BN2}}{I_2} = \frac{6 \text{ V}}{0.4 \text{ mA}} = 15 \text{ k}\Omega$$

$$I_{B2(\min)} = \frac{I_{C2}}{h_{FE(\min)}} = \frac{4 \text{ mA}}{50} = 0.08 \text{ mA} \quad I_{B2} = 1.5 \times I_{B2(\min)} = 1.5 \times 0.08 = 0.12 \text{ mA}$$

$$I_{B2} + I_2 = 0.12 \text{ mA} + 0.4 \text{ mA} = 0.52 \text{ mA} \quad (R_{C1} + R_1) = \frac{V_{CC} - V_{BN2}}{(I_{B2} + I_2)} = \frac{15 - 6}{0.52} = \frac{9}{0.52} = 17.31 \text{ k}\Omega$$

$$R_1 = 17.31 \text{ k}\Omega - R_{C1}$$

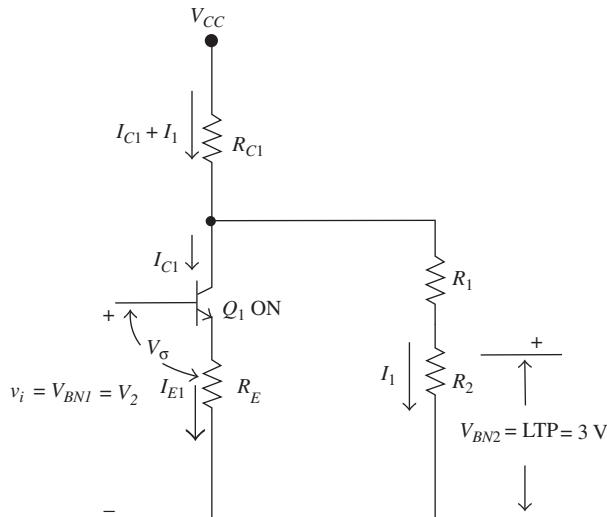


FIGURE 9.24(b) The circuit at LTP

At LTP = 3 V, consider the circuit shown in Fig. 9.24(b).

$$V_{BN2} = V_{BN1} = 3 \text{ V} = \text{LTP} = V_2$$

Let I_1 be the current in R_2 ,

$$I_1 = \frac{V_{BN2}}{R_2} = \frac{3 \text{ V}}{15 \text{ k}\Omega} = 0.2 \text{ mA} \quad I_{C1} = I_{E1} = \frac{V_2 - V_\sigma}{R_E} = \frac{3 - 0.3}{1 \text{ k}\Omega} = 2.7 \text{ mA}$$

Writing the KVL equation of the outer loop:

$$V_{CC} = (I_{C1} + I_1)R_{C1} + I_1(R_1 + R_2) = (I_{C1} + I_1)R_{C1} + I_1(17.31 - R_{C1} + R_2)$$

$$V_{CC} = I_{C1}R_{C1} + I_1(17.31 + R_2)$$

$$R_{C1} = \frac{V_{CC} - I_1(17.31 + R_2)}{I_{C1}} = \frac{15 - 0.2(17.31 + 15)}{2.7} = \frac{8.54}{2.7} = 3.16 \text{ k}\Omega$$

$$R_{C1} = 3 \text{ k}\Omega \quad R_1 = 17.31 - R_{C1} = 17.31 - 3 = 14.31 \text{ k}\Omega$$

Choose $R_1 = 15 \text{ k}\Omega$.

The designed Schmitt trigger circuit is shown in Fig. 9.24(c) with all the component values.

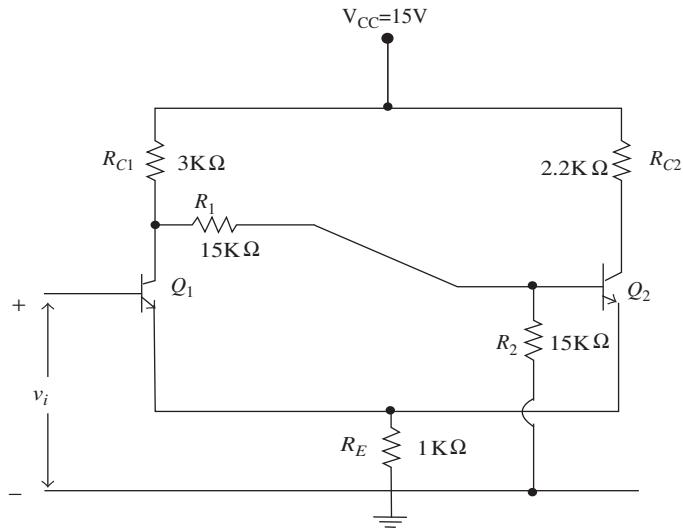


FIGURE 9.24(c) The designed Schmitt trigger

SOLVED PROBLEMS

Example 9.9: Design a fixed-bias bistable multivibrator shown in Fig. 9.25 using $p-n-p$ Ge transistors having $h_{FE(min)} = 50$, $V_{CC} = -10$ V, $V_{BB} = 10$ V, $V_{CE(sat)} = -0.1$, $V_{BE(sat)} = -0.3$ and $I_{C(sat)} = -5$ mA. Assume $I_C = -5$ mA.

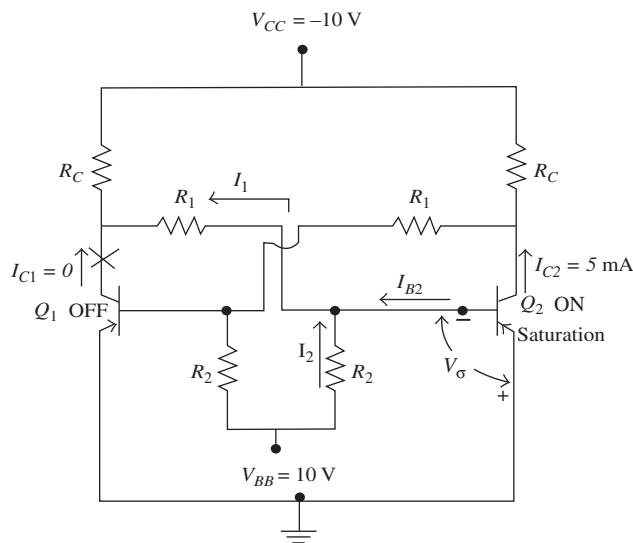


FIGURE 9.25 The fixed-bias bistable multivibrator

Solution:

$$R_C = \frac{V_{CC} - V_{CE(\text{sat})}}{I_{C2}} = \frac{-10 + 0.1V}{-5 \text{ mA}} = \frac{-9.9 \text{ V}}{-5 \text{ mA}}$$

$$R_C = 1.98 \text{ k}\Omega \approx 2.2 \text{ k}\Omega \text{ (standard resistance).}$$

$$R_2 = \frac{-V_\sigma - (V_{BB})}{I_2} \quad I_2 \approx \frac{1}{10} I_{C2} = -0.5 \text{ mA}$$

$$R_2 = \frac{-0.3 - 10}{-0.5} = \frac{-10.3 \text{ V}}{-0.5 \text{ mA}} = 20.6 \text{ k}\Omega \approx 20 \text{ k}\Omega$$

$$I_{B2(\min)} = \frac{I_{C2}}{h_{FE(\min)}} = \frac{-5 \text{ mA}}{50} = -0.1 \text{ mA}$$

If Q_2 is in saturation,

$$I_{B2} = 1.5 I_{B2(\min)} = -0.15 \text{ mA} \quad I_1 = I_2 + I_{B2} = -0.5 \text{ mA} - 0.15 \text{ mA} = -0.65 \text{ mA}$$

$$R_C + R_1 = \frac{-V_{CC} + V_\sigma}{I_1} = \frac{-10 + 0.3}{-0.65 \text{ mA}} = \frac{-9.7 \text{ V}}{-0.65 \text{ mA}} = 14.92 \text{ k}\Omega$$

$$R_1 = (R_C + R_1) - R_C = 14.92 - 1.98 = 12.94 \text{ k}\Omega$$

Choose $R_1 \approx 13 \text{ k}\Omega$

Note: Choose the nearest standard values.

Example 9.10: For a fixed-bias bistable multivibrator using Si transistors, shown in Fig. 9.26(a), $h_{FE} = 20$, $V_{CE(\text{sat})} = 0.3 \text{ V}$, $V_\sigma = 0.7 \text{ V}$.

- Calculate the stable-state currents and voltages.
- $I_{CO} = I_{CBO} = 15 \mu\text{A}$ at 25°C . I_{CBO} gets doubled for every 10°C rise in temperature. The OFF transistor remains OFF only till the net voltage at its base is 0 V. Find the maximum value of I_{CBO} and the temperature up to which the OFF transistor will remain OFF and the multivibrator operates normally.
- If the commutating condenser is 100 pF , find the maximum switching speed of the bistable multivibrator
- The maximum switching frequency is 50 kHz . Find the value of the commutating condenser.

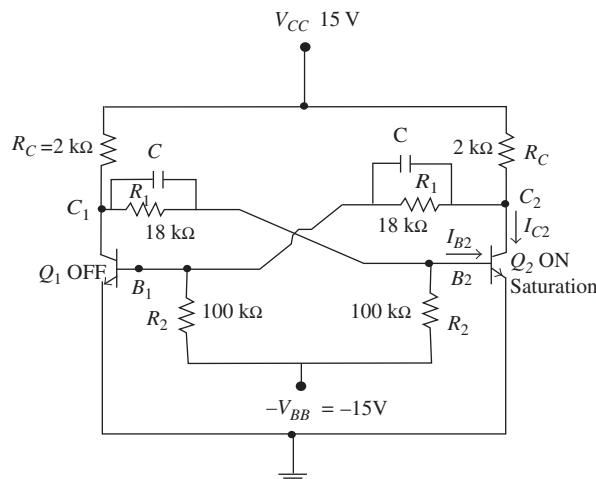


FIGURE 9.26(a) The given fixed-bias bistable multivibrator

Solution:

(a)

(i) If Q_2 is ON and in saturation, to find its base current I_{B2} , consider the base circuit shown in Fig. 9.26(b).

From Fig. 9.26(b),

$$\begin{aligned} I_1 &= \frac{V_{CC} - V_\sigma}{R_C + R_1} \\ &= \frac{15 - 0.7}{2 + 18} = 0.715 \text{ mA} \\ I_2 &= \frac{V_\sigma + V_{BB}}{R_2} \\ &= \frac{0.7 + 15}{100} = 0.157 \text{ mA} \end{aligned}$$

$$\begin{aligned} I_{B2} &= I_1 - I_2 \\ &= 0.715 - 0.157 = 0.558 \text{ mA} \end{aligned}$$

(ii) To calculate I_{C2} consider the collector circuit of Q_2 , shown in Fig. 9.26(c).

From Fig. 9.26(c),

$$\begin{aligned} I_3 &= \frac{V_{CC} - V_{CE(\text{sat})}}{R_C} = \frac{15 - 0.3}{2} = 7.35 \text{ mA} \\ I_4 &= \frac{V_{CE(\text{sat})} + V_{BB}}{R_1 + R_2} = \frac{0.3 + 15}{100 + 18} = 0.13 \text{ mA} \end{aligned}$$

$$I_{C2} = I_3 - I_4 = 7.35 - 0.13 = 7.22 \text{ mA}$$

Given $h_{FE} = 20$.

Therefore,

$$I_{B2(\text{min})} = \frac{I_{C2}}{h_{FE}} = \frac{7.22}{20} = 0.361 \text{ mA}$$

$$I_{B2(\text{sat})} = 1.5 I_{B2(\text{min})} = 1.5 \times 0.361 = 0.54 \text{ mA}$$

As $I_{B2} = 0.558 \text{ mA}$, Q_2 is in saturation.

$$V_{B1} = V_{CE(\text{sat})} \frac{R_2}{R_1 + R_2} + (-V_{BB}) \frac{R_1}{R_1 + R_2} = (0.3) \frac{100}{118} + (-15) \frac{18}{118} = 0.254 - 2.288 = -2.034 \text{ V}$$

Hence, Q_1 is OFF.

$$V_{C1} = V_{CC} - I_1 R_C = 15 - (0.715)2 = 13.57 \text{ V}$$

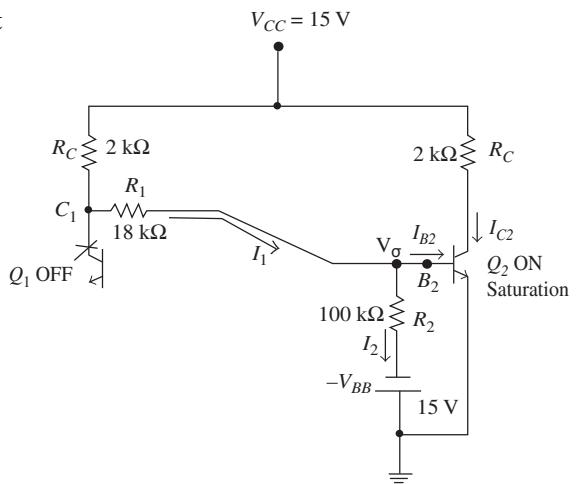


FIGURE 9.26(b) The circuit to calculate I_{B2}

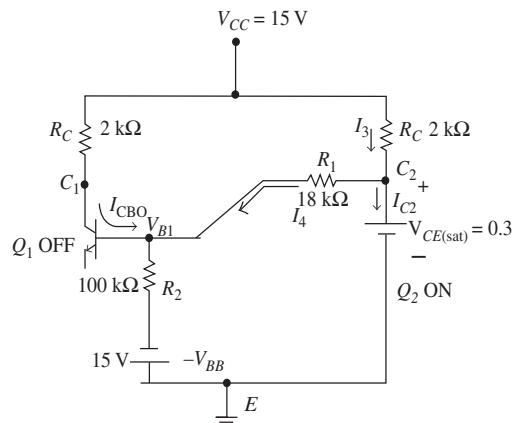


FIGURE 9.26(c) The circuit to calculate I_{C2}

(b) $I_{CO} = I_{CBO} = 15 \mu A$ at $25^\circ C$.

To calculate the positive voltage that I_{CBO} develops at B_1 , the base of the OFF device, short $V_{CE(\text{sat})}$ and V_{BB} sources, shown in Fig. 9.26(d). We see that I_{CBO} flows through the parallel combination of R_1 and R_2 . If R_B is the effective resistance of R_1 and R_2 in parallel, then,

$$R_B = R_1 \parallel R_2 = \frac{18 \times 100}{18 + 100} = 15.25 \text{ k}\Omega$$

V_{B1} was calculated earlier.

$$V_{B1} = -2.034 \text{ V}$$

When $I_{CBO} R_B = V_{B1}$, the net voltage at B_1 is zero. Till that instant Q_1 is OFF. If $I_{CBO} R_B > V_{B1}$, the voltage at B_1 becomes positive and Q_1 will not be in the OFF state. Therefore, for Q_1 to be OFF,

$$R_B I_{CBO(\max)} = V_{B1}$$

Therefore,

$$I_{CBO(\max)} = \frac{V_{B1}}{R_B} = \frac{2.034}{15.25} = 133 \mu\text{A}$$

$$\frac{I_{CBO(\max)}}{I_{CBO}} = 2^{(T_2 - 25)/10} = 2^{\Delta T/10} = 2^n$$

where, T_2 is the temperature at which $I_{CBO} = I_{CBO(\max)}$.

$$\frac{133}{15} = 2^n \quad n = \frac{\log 8.87}{\log 2} = 3.15$$

$$\text{As } n = \frac{\Delta T}{10}$$

$$\frac{\Delta T}{10} = 3.15 \quad \Delta T = 31.5$$

$$\Delta T = T_2 - 25 \quad T_2 - 25 = 31.5 \quad T_2 = 31.5 + 25 = 56.5^\circ\text{C}$$

$$(c) f_{(\max)} = \frac{1}{2\tau} = \frac{(R_1 + R_2)}{2CR_1R_2}.$$

Given $C = 100 \text{ pF}$.

Therefore

$$f_{(\max)} = \frac{(100 + 18) \times 10^3}{2 \times 100 \times 10^{-12} (100 \times 10^3 \times 18 \times 10^3)} = 327 \text{ kHz}$$

(d) Given $f_{(\max)} = 50 \text{ kHz}$.

$$C = \frac{(R_1 + R_2)}{2f_{(\max)}R_1R_2} = \frac{(100 + 18) \times 10^3}{2 \times 50 \times 10^3 \times 100 \times 10^3 \times 18 \times 10^3} = 655 \text{ pF}$$

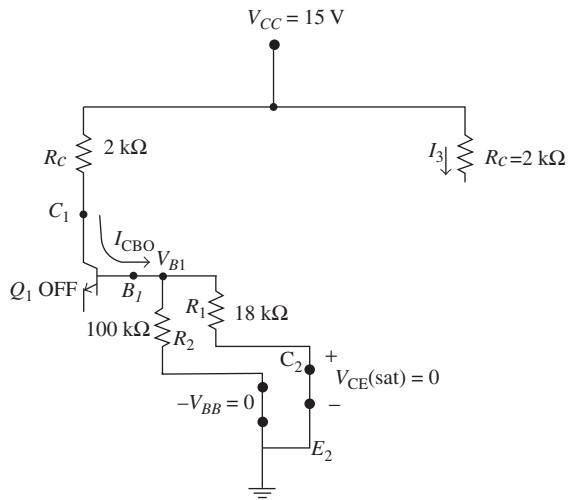


FIGURE 9.26(d) The circuit to calculate R_B and $I_{CBO(\max)}$

Example 9.11: The self-bias transistor bistable multivibrator shown in Fig. 9.27(a) uses a *n*-*p*-*n* Ge transistor. Given that $V_{CC} = 15$ V, $V_{CE(\text{sat})} = 0.1$ V, $V_\sigma = 0.3$ V, $R_C = 2 \text{ k}\Omega$, $R_1 = 30 \text{ k}\Omega$, $R_2 = 10 \text{ k}\Omega$, $R_E = 500 \Omega$.

Find:

- Stable-state currents and voltages and the h_{FE} needed to keep the ON device in saturation
- The value of C_1 needed to ensure a resolution time of 0.02 ms.
- The maximum value of I_{CBO} that will still ensure one device OFF and the other ON.
- The maximum temperature up to which the multivibrator can work normally if I_{CBO} at 25 °C = 10 μ A.

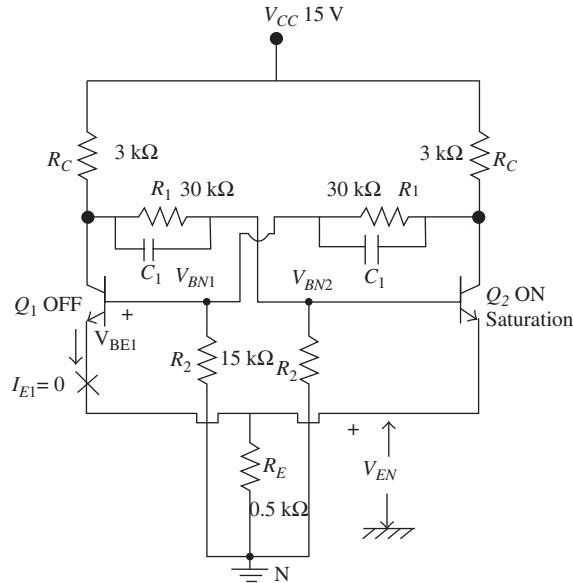


FIGURE 9.27(a) The self-bias bistable multivibrator

Solution: (a)

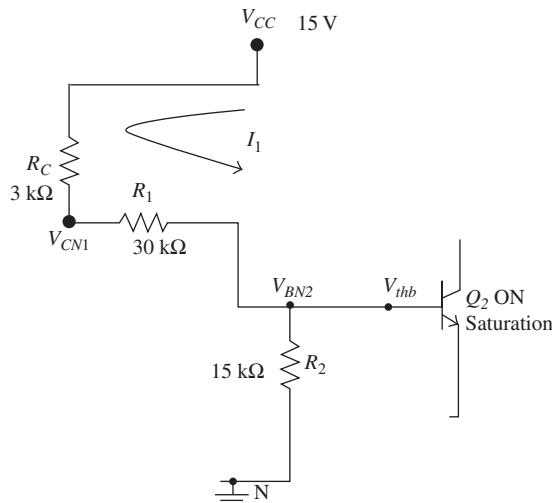


FIGURE 9.27(b) The circuit to calculate V_{thb} and R_{thb} of Q_2

(i) To calculate I_{B2} , consider the base circuit of Q_2 , shown in Fig. 9.27(b).

From Fig. 9.27(b),

$$V_{thb} = V_{CC} \frac{R_2}{R_C + R_1 + R_2} = \frac{15 \times 15}{3 + 30 + 15} = \frac{225}{48} = 4.69 \text{ V}$$

$$R_{thb} = R_2 \parallel (R_C + R_1) = \frac{15 \times (3 + 30)}{3 + 30 + 15} = \frac{495}{48} = 10.31 \text{ k}\Omega$$

(ii) To calculate I_{C2} , consider the collector circuit of Q_2 , Fig. 9.27(c).

$$V_{thc} = V_{CC} \frac{R_1 + R_2}{R_C + R_1 + R_2} = \frac{15 \times (30 + 15)}{3 + 30 + 15} = \frac{675}{48} = 14.06 \text{ V}$$

$$R_{thc} = R_C \parallel (R_1 + R_2) = \frac{3 \times 45}{48} = \frac{135}{48} = 2.81 \text{ k}\Omega$$

Now let us draw the base and collector circuits of Q_2 , shown in Fig. 9.27(d).

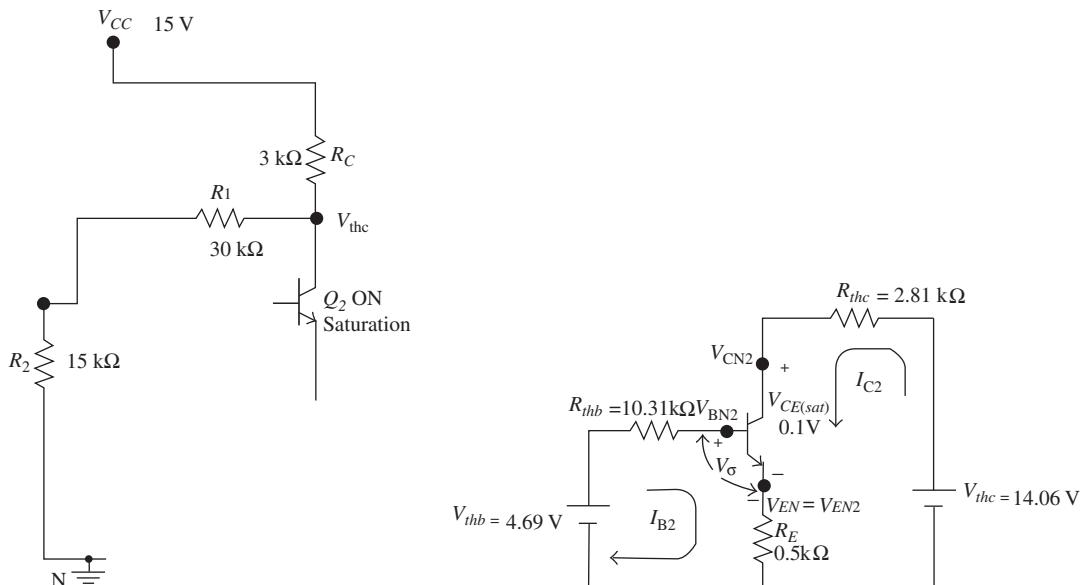


FIGURE 9.27(c) The circuit to calculate V_{thc} and R_{thc} of Q_2

FIGURE 9.27(d) The circuit to calculate I_{B2} and I_{C2}

Writing the KVL equations of the input and output loops:

$$4.69 - 0.3 = (10.31 + 0.5) I_{B2} + 0.5 I_{C2} \quad (1)$$

$$14.06 - 0.1 = 0.5 I_{B2} + (2.81 + 0.5) I_{C2} \quad (2)$$

Eqs. (1) and (2) are simplified as:

$$4.39 = 10.81 I_{B2} + 0.5 I_{C2} \quad (3)$$

$$13.96 = 0.5 I_{B2} + 3.31 I_{C2} \quad (4)$$

Solving Eqs. (3) and (4) for I_{B2} and I_{C2} we get,

$$I_{B2} = 0.212 \text{ mA} \quad I_{C2} = 4.18 \text{ mA}$$

Therefore, $h_{FE} = 4.18/0.212 = 19.7$.

The h_{FE} that keeps the ON device in saturation is 20.

$$V_{EN2} = (I_{B2} + I_{C2}) R_E = (4.18 + 0.212) 0.5 = 2.196 \text{ V}$$

$$V_{CN2} = V_{EN2} + V_{CE(\text{sat})} = 2.196 + 0.1 = 2.296 \text{ V}$$

$$V_{BN2} = V_{EN2} + V_\sigma = 2.196 + 0.3 = 2.496 \text{ V}$$

$$V_{BN1} = V_{CN2} \frac{R_2}{R_1 + R_2} = \frac{2.296 \times 15}{15 + 30} = \frac{2.296}{3} = 0.765 \text{ V}$$

$$V_{BE1} = V_{BN1} - V_{EN2} = 0.765 - 2.196 = -1.431 \text{ V}$$

Hence, Q_1 is OFF.

Therefore, V_{CN1} should be V_{CC} , but actually it is less than V_{CC} .

We have from Fig. 9.27(b),

$$I_1 = \frac{V_{CC} - V_{BN2}}{R_C + R_1} = \frac{15 - 2.496}{3 + 30} = 0.379 \text{ mA}$$

$$V_{CN1} = V_{CC} - I_1 R_C = 15 - (0.379) (3) = 13.86 \text{ V}$$

$$(b) t_{\text{res}} = \frac{2R_1 R_2 C_1}{(R_1 + R_2)}$$

$$0.02 \times 10^{-3} = \frac{2 \times 30 \times 10^3 \times 15 \times 10^3 C_1}{(15 + 30) 10^3} \quad C_1 = \frac{0.02 \times 10^{-3} \times 45 \times 10^3}{900 \times 10^6} = \frac{0.9}{900} \times 10^{-6} = 1 \text{ nF}$$

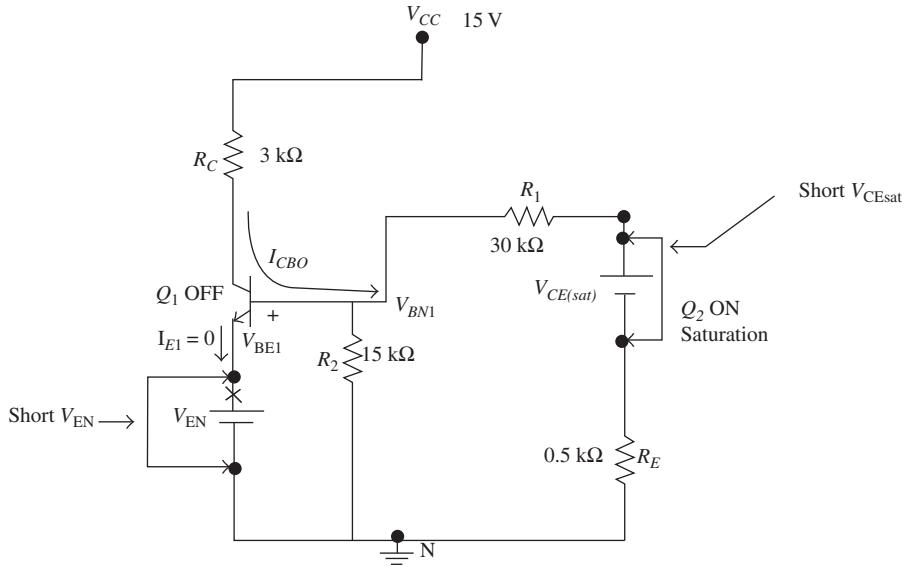
(c) V_{BE1} was calculated as -1.431 V . This voltage exists at the base of Q_1 to keep Q_1 OFF. Till such time the voltage at B_1 of Q_1 is 0 V , let us assume that Q_1 is OFF, as shown in Fig. 9.27(e). To calculate R_B and hence $I_{CB0} R_B$, short V_{EN} (though $I_{E1} = 0$, there exists a voltage V_{EN} at the first emitter) and $V_{CE(\text{sat})}$ sources. From Fig. 9.27(e), it is seen that R_B is the parallel combination of R_2 and $(R_1 + R_E)$.

$$R_B = R_2 \parallel (R_1 + R_E) = 15 \parallel (30.5) = \frac{15 \times 30.5}{15 + 30.5} = 10.05 \text{ k}\Omega$$

Until $I_{CB0(\text{max})} R_B = V_{BE1}$, Q_1 will be OFF.

Therefore,

$$I_{CB0(\text{max})} = \frac{1.431 \text{ V}}{10.05 \text{ K}} = 0.142 \text{ mA} = 142 \mu\text{A}$$

FIGURE 9.27(e) The circuit to calculate $I_{CBO}R_B$ d) I_{CB0} at $25^\circ\text{C} = 10 \mu\text{A}$

$$\frac{I_{CB0max}}{I_{CB0}} = \frac{142}{10} = 14.2 \quad 14.2 = 2^n$$

$$n = \frac{\log 14.2}{\log 2} = \frac{1.15}{0.3} = 3.83$$

$$\frac{\Delta T}{10} = n \quad \frac{T_2 - 25}{10} = 3.83 \quad T_2 = 25 + 38.3 = 63.3^\circ\text{C}$$

Example 9.12: Consider the Schmitt trigger circuit designed, shown in Fig. 9.28(a). R_{e2} is now included to eliminate hysteresis, as shown in Fig. 9.28(a). For this circuit $V_1 = 8 \text{ V}$ and $V_2 = 4 \text{ V}$ and $h_{FE} = 40$. Calculate R_{e2} such that $V_1 = V_2 = 4 \text{ V}$.

Solution:

$$V' = \frac{V_{CC}R_2}{R_{C1} + R_1 + R_2} = \frac{18 \times 16}{4.5 + 10 + 16} = 9.44 \text{ V}$$

$$R' = R_2 / (R_{C1} + R_1) = \frac{16 \times 14.5}{30.5} = 7.60 \text{ k}\Omega$$

From Eq. (9.79), we have:

$$(V' - V_{BE2}) \frac{(1 + h_{FE})R_E}{R' + (1 + h_{FE})(R_{e2} + R_E)} + V_\gamma = V_2$$

$$(9.44 - 0.6) \frac{41 \times 1.5}{7.60 + (41)(R_{e2} + 1.5)} + 0.5 = 4 \text{ V}$$

$$143.5R_{e2} = 301.81 \quad R_{e2} = 2.10 \text{ k}\Omega$$

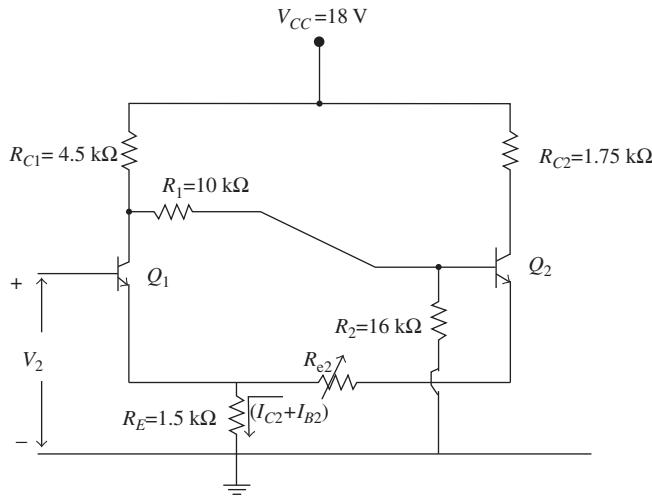


FIGURE 9.28(a) R_{e2} is connected to eliminate hysteresis

S U M M A R Y

- A bistable multivibrator has two stable states. Initially if the multivibrator is in one of the stable states (say Q_1 is ON and Q_2 is OFF), change of state (Q_1 is OFF and Q_2 is ON) occurs only after the application of an external trigger.
- A bistable multivibrator is also known by many names, namely, binary, flip-flop, scale-of-two circuit and Eccles–Jordan circuit.
- A bistable multivibrator can be used for storing and counting of binary information. It can also be used for generating pulsed output.
- The output of a bistable multivibrator, if connected to some other circuit, could cause loading on the bistable multivibrator, which in turn will reduce the output swing.
- To ensure that the output of a bistable multivibrator does not fall below a specified threshold, the collector of the OFF transistor is clamped to a dc voltage using collector catching diodes.
- The time taken for conduction to transfer from one device to the other is called the transition time.
- Once conduction is transferred from one device to the other, an additional time, known as the settling time, is required to elapse before the voltages across the commutating condensers interchange. Only then do we say that the multivibrator has settled down in its new state completely.
- Commutating condensers help in reducing the transition time.
- The resolution time of a bistable multivibrator is the minimum time interval required between successive trigger pulses to be reliably able to drive the multivibrator from one stable state to the other.
- The reciprocal of the resolution time is the maximum switching speed of the bistable multivibrator.
- Unsymmetric triggering is a method of pulse triggering in which one trigger pulse taken from one source is applied at point in the circuit. The next trigger pulse is taken from a different source and is applied at a different point in the circuit to cause a change of state in both the devices. This method of triggering is used to generate a gated output; the duration of gate being dependent on the time interval between these trigger pulses.
- Symmetric triggering is a method of pulse triggering in which successive trigger pulses taken from the same source and applied at the same point in the circuit will

cause a change of state in either direction. This method of triggering is used in counters.

- An emitter-coupled bistable multivibrator is called a Schmitt trigger.
- When the loop gain is greater than 1, the Schmitt trigger exhibits hysteresis.
- Hysteresis in a Schmitt trigger can be eliminated by including a suitable resistance in series with either the first emitter (R_{e1}) or the second emitter (R_{e2}).

- A Schmitt trigger can also be used as a comparator and squaring circuit in addition to being used as a bistable multivibrator.
- The input voltage at which the output voltage of a Schmitt trigger goes high is called the upper trip point (UTP).
- The input voltage at which the output voltage of a Schmitt trigger goes low is called the lower trip point (LTP).

MULTIPLE CHOICE QUESTIONS

- (1) Unless an external trigger is applied, the state of a bistable multivibrator:
 - Remains unaltered
 - Changes automatically
 - Goes into the quasi-stable state
 - None of the above
- (2) When a trigger is applied to a bistable multivibrator, conduction is transferred from one device to the other. The time taken for conduction to transfer from one device to the other is called:
 - Delay time
 - Rise time
 - Transition time
 - Fall time
- (3) The time taken for the voltages across the commutating condensers to interchange is called:
 - Transition time
 - Rise time
 - Recovery time
 - Settling time
- (4) Resolution time of a bistable multivibrator is the sum of the:
 - Rise time and fall time
 - Delay time and rise time
 - Transition time and settling time
 - Storage time and fall time
- (5) The reciprocal of the resolution time of the bistable multivibrator is called:
 - Maximum switching speed of the bistable multivibrator
 - Minimum switching speed of the bistable multivibrator
- (6) If the commutating condensers are large:
 - Transition time decreases and the settling time increases
 - Transition time increases and the settling time decreases
 - Both, transition time and settling time increase
 - Both transition time and settling time decrease
- (7) An emitter-coupled bistable multivibrator is also called as:
 - Astable multivibrator
 - Monostable multivibrator
 - Schmitt trigger
 - None of the above
- (8) A Schmitt trigger can be used as a:
 - Comparator
 - Astable multivibrator
 - Monostable multivibrator
 - None of the above
- (9) If the loop gain is greater than 1, a Schmitt trigger exhibits:
 - Oscillations
 - Hysteresis
 - Instability
 - None of the above
- (10) When symmetric pulse triggering is used in a bistable multivibrator, its application is in:
 - Astable multivibrators
 - Monostable multivibrators
 - Counters
 - Schmitt trigger

- (11) R_{e2} connected in series with the second emitter in a Schmitt trigger influences:
- V_2 but not V_1
 - V_1 but not V_2
 - Both V_1 and V_2
 - None of the above
- (12) R_{e1} connected in series with the first emitter in a Schmitt trigger influences:
- V_2 but not V_1
 - V_1 but not V_2
 - Both V_1 and V_2
 - None of the above

SHORT ANSWER QUESTIONS

- What is a bistable multivibrator? What are the other names by which it is called? Explain, in short, how a bistable multivibrator can be used as a memory element?
- What is meant by loading in a bistable multivibrator? How can you make the output swing constant?
- What is the purpose served by a collector catching diodes?
- What is the use of commutating condensers in a bistable multivibrator?
- Define transition time? Suggest how to minimize it.
- What is meant by the resolution time of a bistable multivibrator? Suggest simple methods to improve it.
- What do you understand by unsymmetric triggering? What is its application?
- What do you understand by symmetric triggering? What is its application?
- What is a Schmitt trigger? Mention some of its applications.
- Suggest simple methods to eliminate hysteresis in a Schmitt trigger.
- A Schmitt trigger can be used as a regenerative comparator – justify.

LONG ANSWER QUESTIONS

- With the help of a neat circuit diagram explain the working of a fixed-bias bistable multivibrator. Derive the expression for the resolution time and maximum switching speed of a bistable multivibrator.
- With the help of a neat circuit diagram explain the working of a self-bias bistable multivibrator. List the advantages of this circuit over a fixed-bias bistable multivibrator.
- With the help of a suitable circuit diagram, explain the methods of symmetric and unsymmetric triggering of a bistable multivibrator.
- Draw the circuit of a Schmitt trigger and explain its operation. Derive the expressions for (i) UTP and (ii) LTP.
- Explain with the help of waveforms how a Schmitt trigger can be used as a:
 - Bistable multivibrator;
 - Squaring circuit; and
 - Amplitude comparator.

UNSOLVED PROBLEMS

- Design a fixed-bias bistable multivibrator using Ge transistors having $h_{FE}(\text{min}) = 50$, $V_{CC} = 10$ V and $V_{BB} = 10$ V, $V_{CE(\text{sat})} = 0.1$ V, $V_{BE(\text{sat})} = 0.3$ V, $I_{C(\text{sat})} = 5$ mA and assume $I_{B(\text{sat})} = 1.5I_{B(\text{min})}$.
- For a fixed-bias bistable multivibrator shown in Fig. 9p.1 using $n-p-n$ Ge transistor $V_{CC} = 10$ V, $R_C = 1$ $k\Omega$, $R_1 = 10$ $k\Omega$, $R_2 = 20$ $k\Omega$, $h_{FE(\text{min})} = 40$, $V_{BB} = 10$ V. Calculate:

- (a) Stable-state currents and voltages assuming Q_1 is OFF and Q_2 is ON and in saturation. Verify whether Q_1 is OFF and Q_2 is ON or not.
- (b) The maximum load current.

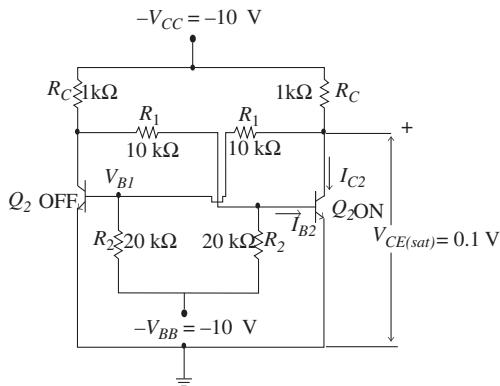


FIGURE 9p.1 The fixed-bias bistable multivibrator

- (3) Design a self-bias bistable multivibrator shown in Fig. 9p.2 with a supply voltage of -12 V. A $p-n-p$ silicon transistor with $h_{FE}(\min) = 50$, $V_{CE}(\text{sat}) = -0.3$ V, $V_{BE}(\text{sat}) = -0.7$ V and $I_{C2} = -4$ mA is used.

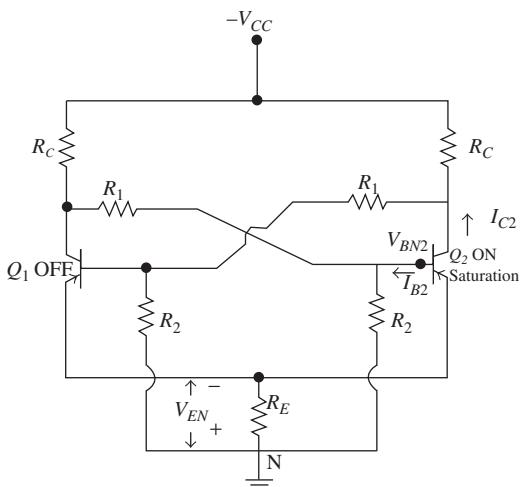


FIGURE 9p.2 The given self-bias bistable multivibrator

- (4) A self-bias bistable multivibrator uses Si transistors having $h_{FE}(\min) = 50$. $V_{CC} = 18$ V, $R_1 = R_2$, $I_{C(\text{sat})} = 5$ mA. Fix the component values R_E , R_C , R_1 and R_2 .

- (5) For the Schmitt trigger in Fig 9p.4 using $n-p-n$ silicon transistors having $h_{FE}(\min) = 40$, the following are the circuit parameters: $V_{CC} = 15$ V, $R_S = 0$, $R_{C1} = 4$ kΩ, $R_{C2} = 1$ kΩ, $R_1 = 3$ kΩ, $R_2 = 10$ kΩ and $R_E = 6$ kΩ. Calculate V_1 and V_2 .

- (6) The self-bias transistor bistable multivibrator shown in Fig. 9p.3 uses $n-p-n$ Si transistors. Given that $V_{CC} = 15$ V, $V_{CE}(\text{sat}) = 0.2$ V, $V_\sigma = 0.7$ V, $R_C = 3$ kΩ, $R_1 = 20$ kΩ, $R_2 = 10$ kΩ, $R_E = 500$ Ω. Find:
- Stable-state currents and voltages and the h_{FE} needed to keep the ON device in saturation.
 - $f_{(\max)}$, if $C_1 = 100$ pF.
 - The maximum value of I_{CBO} that will ensure one device is OFF and the other is ON.
 - The maximum temperature up to which the multivibrator can work normally if I_{CBO} at $25^\circ\text{C} = 20$ μA.

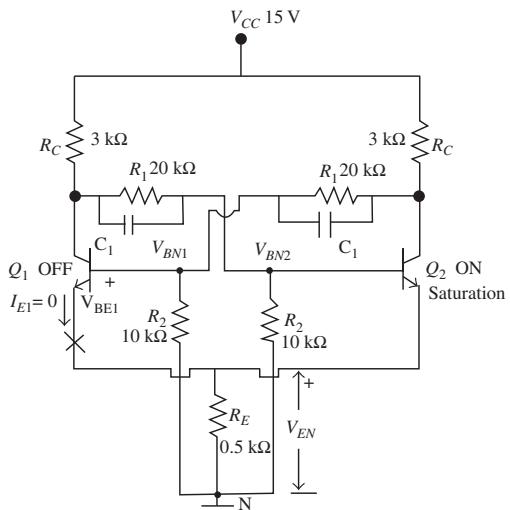


FIGURE 9p.3 The given self-bias bistable multivibrator

- (7) Design a Schmitt trigger shown in Fig. 9p.4 with UTP of 8 V and LPT of 4 V. Si transistors with $h_{FE} = 40$ and $I_C = 5$ mA are used. The supply voltage is 18 V. The ON transistor is in the active region for which $V_{BE} = 0.6$ V, $V_{CE} = 2.0$ V. (b) Calculate R_{e1} for eliminating hysteresis.

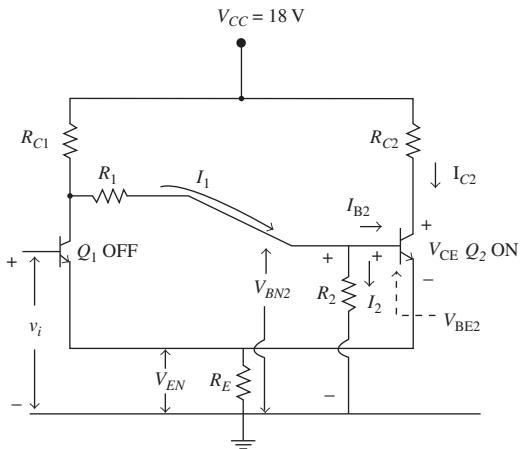


FIGURE 9p.4 The Schmitt trigger circuit

- (8) Design a Schmitt trigger in Fig. 9p.5 with UTP of 8 V and LTP of 4 V. Si transistors with $h_{FE} = 40$ and $I_C = 4$ mA are used. The supply voltage is 12 V. The

ON transistor is in saturation for which $V_{BE} = 0.7$ V, $V_{CE(sat)} = 0.2$ V.

- (ii) Calculate R_{e1} for eliminating hysteresis.
 - (iii) Find R_{e2} to eliminate hysteresis.

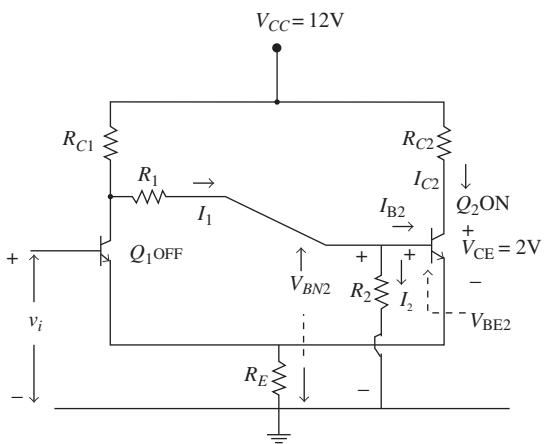


FIGURE 9p.5 The given Schmitt trigger circuit

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Logic Gates

LEARNING OBJECTIVES

After reading this chapter, you will be able to:

- Describe AND, OR (or NAND, NOR) logic gates
 - Realize logic gates belonging to different logic families such as DTL, TTL and CMOS
 - Understand the factors that define the performance of a logic gate
 - Compare the performance of the various logic families
 - Interface gates belonging to TTL and CMOS families
-

10.1 INTRODUCTION

In digital applications, data is in the form of binary bits—0s and 1s. A logic gate is a digital circuit that gives a specific discrete output (0 or 1) depending on the input conditions. These logic gates can be wired using discrete components such as resistors, diodes, transistors, FETs, and their combinations. The simplest logic gate, say a two-input AND / OR gate (diode–resistance logic gate), may be constructed using two diodes, a resistance and a dc source. The important logic families are diode–transistor logic (DTL), transistor–transistor logic (TTL), *p*-channel and *n*-channel MOSFET logic (PMOS and NMOS) and complementary MOSFET logic (CMOS). The TTL family is further subdivided into open-collector TTL, emitter-coupled logic (ECL) or integrated injection logic (I^2L). TTL and CMOS are the two most important logic families. TTL gates are preferred where there is a need for faster switching speed and CMOS gates are used where the requirement is lower power dissipation per gate. The suitability of a logic gate, for a specific application, is evaluated in terms of the number of requirements. This chapter presents the relative performance of these gates. Also, sometimes, it becomes necessary to connect the output of one type of gate (say, a TTL gate which operates with a 5 V supply) to the input of another gate (say, a CMOS gate that operates with a 30 V supply). In such cases, the output requirements of the driving gate should be compatible with the input requirements of the driven gate. Hence, interfacing methods are also discussed. Normally, designing and constructing logic gates using discrete components is meaningful only for small circuits. As the complexity increases, these circuits are best fabricated on a chip called the digital integrated circuit. Depending on the level of integration, these are classified as under:

- (a) Small-scale integration (SSI): 1 to 20 gates or transistors per package
- (b) Medium-scale integration (MSI): 20 to 200 gates or transistors per package
- (c) Large-scale integration (LSI): 200 to 200,000 gates or transistors per package
- (d) Very large-scale integration (VLSI): More than 1million gates or transistors
- (e) Ultra large-scale integration (ULSI): 1 billion gates or transistors

10.2 LOGIC GATES

A logic gate is a circuit that gives either ‘0’ (LOW) level or ‘1’ (HIGH) level at the output, depending on the input conditions. The basic logic gates can be wired using discrete components such as resistors, diodes, transistors and FETs. The wiring of a complex gate circuit is unthinkable using discrete components. When

the complexity of the gate circuit increases, it is preferable to wire the logic gate in an integrated circuit form. In this section, we basically describe the different types of logic gates using discrete components only, in order to understand the principle of operation of logic circuits of different logic families.

10.2.1 Simple Diode Gates

AND and OR are the two basic gates from which NAND and NOR gates can be derived. Here, we describe two types of diode gates—diode AND gates and diode OR gates.

Diode AND Gates. An AND gate is a digital circuit which gives a high output only when all the inputs are simultaneously high (1), otherwise the output is low (0). Consider a simple two-input AND gate using diodes (See Fig. 10.1).

Assuming D_1 and D_2 to be ideal diodes, the following cases are possible:

- Both the inputs are zero, the diodes are ON and $V_o = 0$.
- $V_1 = 0, V_2 = 1, D_1$ is ON, D_2 is OFF, $V_o = 0$.
- $V_1 = 1, V_2 = 0, D_1$ is OFF, D_2 is ON, $V_o = 0$.
- $V_1 = 1, V_2 = 1, D_1$ and D_2 are OFF, $V_o = 1$.

The truth table for the gate is given in Table 10.1. The schematic representation of the AND gate is shown in Fig 10.2(a).

The timing diagram for the two-input AND gate is shown in Fig 10.2(b). As mentioned in the preceding section, in an AND gate, the output is 1 only when all the inputs are 1 and, 0 if any one of the inputs is 0. Hence, in Fig. 10.2(b), at the instant T_0 , when both the inputs V_1 and V_2 are 0, the output $V_o = 0$. At T_1 , $V_1 = 0$ and $V_2 = 1$. Since one of the inputs is zero, the output $V_o = 0$. At the instant $T_3, V_1 = 1$ and $V_2 = 1$. Since both the inputs are 1, the output $V_o = 1$ and so on. In general, there can be a large number of inputs to a gate. A NOT gate, also called an inverter in digital circuits, is schematically represented as in Fig. 10.2(c). Figure 10.2(d) shows the timing diagram for a NOT gate.

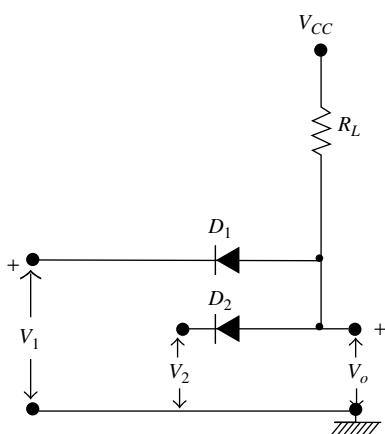


FIGURE 10.1 A two-input AND gate

TABLE 10.1 The truth table for the AND gate

V_1	V_2	V_o
0	0	0
0	1	0
1	0	0
1	1	1

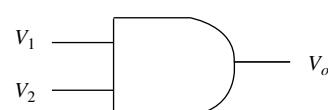


FIGURE 10.2(a) The schematic diagram for the two-input AND gate

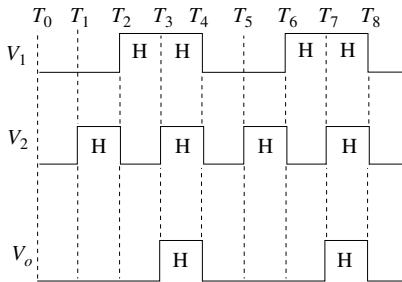


FIGURE 10.2(b) The timing diagram for two-input AND gate

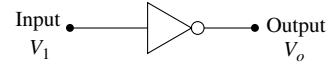


FIGURE 10.2(c) A NOT gate

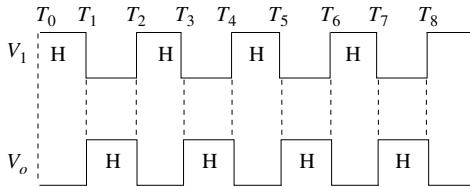


FIGURE 10.2(d) The timing diagram for a NOT gate

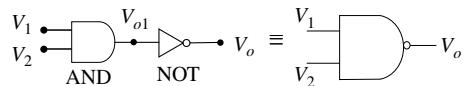


FIGURE 10.3(a) A NAND gate

In a NOT gate, the output is the complement of the input. This means, that if the input is 1, the output is 0; and if the input is 0, the output is 1. At T_0 , the input $V_1 = 1$; therefore, the output $V_o = 0$. At T_1 , the input $V_1 = 0$ and output $V_o = 1$ and so on.

An AND gate cascaded with a NOT gate is called a NAND gate. Figures 10.3(a) and (b) show the schematic representation and the timing diagram of a NAND gate, respectively.

In a NAND gate, the output is 0 only when all the inputs are 1. If any one of the inputs is 0, the output is 1. As shown in Fig. 10.3(b), at the instant T_0 , both the inputs V_1 and V_2 are 0 and therefore, the output V_o is 1. At T_1 , $V_1 = 0$ and $V_2 = 1$. Since one of the inputs is 0, the output V_o is 1. At T_3 both the inputs V_1 and V_2 are equal to 1 and therefore the output $V_o = 0$.

Diode OR Gates. An OR gate is a digital circuit which gives a high output when either one or all the inputs are high (1). In other words, the output is low (0) only when both the inputs are low. A two-input diode OR gate is shown in Fig. 10.4. Here too, we assume the diodes to be ideal. The following cases are possible:

- (i) $V_1 = V_2 = 0$, D_1 and D_2 are OFF, $V_o = 0$
- (ii) $V_1 = 0$, $V_2 = 1$, D_1 is OFF, D_2 is ON, $V_o = 1$
- (iii) $V_1 = 1$, $V_2 = 0$, D_1 is ON, D_2 is OFF, $V_o = 1$
- (iv) $V_1 = 1$, $V_2 = 1$, D_1 and D_2 are ON and $V_o = 1$

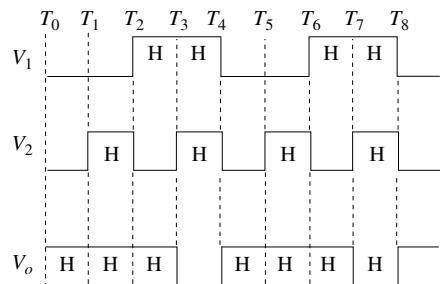


FIGURE 10.3(b) The timing diagram for a NAND gate

The truth table for an OR gate is shown in Table 10.2. An OR gate is schematically represented as in Fig. 10.5(a).

The timing diagram for a two-input OR gate is shown in Fig. 10.5(b). In an OR gate, when any one of the inputs is 1, the output is 1. It is 0 only if all the inputs are 0. Hence, in Fig. 10.5(b), at the instant T_0 , both the inputs V_1 and V_2 are 0; therefore, the output V_o is 0. At T_1 , V_1 is 0 whereas $V_2 = 1$. Since one of the inputs is 1, the output $V_o = 1$. At the instant T_3 , V_1 is 1 and V_2 is 1. Since both the inputs are 1, the output $V_o = 1$. An OR gate cascaded with a NOT gate is called a NOR gate, as represented in Fig. 10.6(a). Its timing diagram is shown in Fig. 10.6(b).

The output of a NOR gate is 1 when all the inputs are 0. When any one of the inputs is 1, the output is 0. Therefore, in Fig. 10.5(b), at the instant T_0 , when both the inputs V_1 and V_2 are 0, the output of the NOR gate is $V_o = 1$. At T_1 , $V_1 = 0$ and $V_2 = 1$; since one of the inputs is 1, the output V_o is 0. At T_3 , both the inputs V_1 and V_2 are equal to 1; therefore, the output V_o is 0.

TABLE 10.2 The truth table for an OR gate

V_1	V_2	V_o
0	0	0
0	1	1
1	0	1
1	1	1

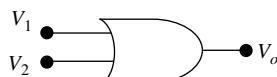


FIGURE 10.5(a) An OR gate

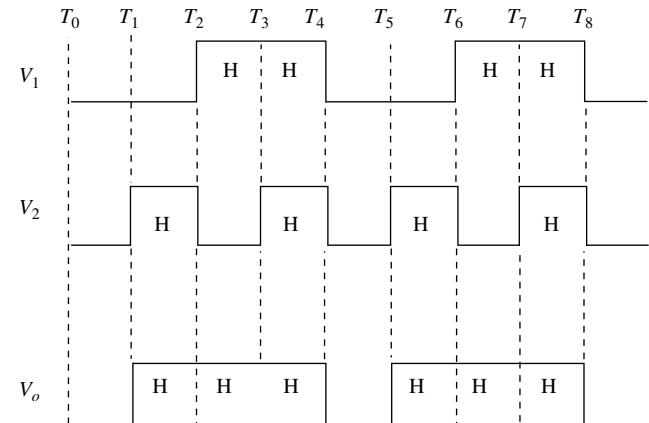


FIGURE 10.5(b) The timing diagram for a two-input OR gate

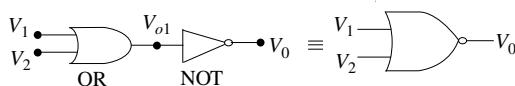


FIGURE 10.6(a) A NOR gate

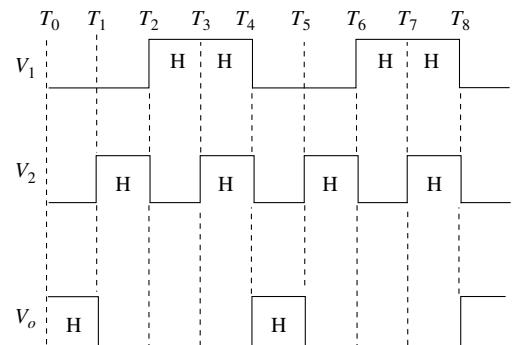


FIGURE 10.6(b) The timing diagram for a NOR gate

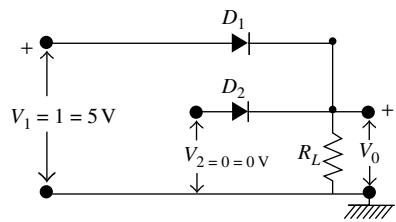


FIGURE 10.4 The two-input diode OR gate

EXAMPLE

Example 10.1: The three-input AND gate shown in Fig. 10.7(a) is driven by the outputs of a bistable multivibrator. Transistors are capable of taking an additional current of 1 mA when in saturation. Fix the value of R_1 and find the output for different input conditions.

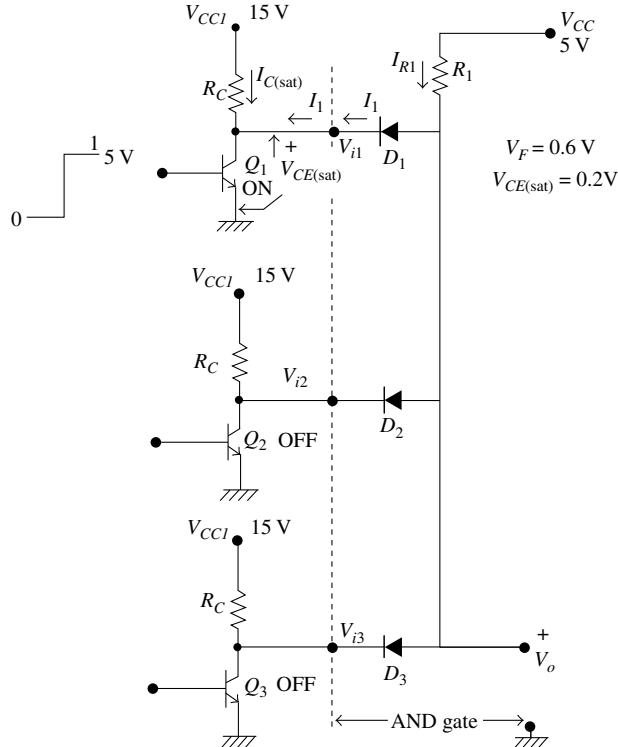


FIGURE 10.7(a) The given three -input AND gate

Solution:

When Q_1 is in saturation, Q_2 and Q_3 are OFF as shown in Fig. 10.14(b).

$$V_{CC} = I_{R1}R_1 + V_F + V_{CE(\text{sat})}$$

Therefore,

$$\begin{aligned} R_1 &= \frac{V_{CC} - V_F - V_{CE(\text{sat})}}{I_{R1}} = \frac{5 - 0.6 - 0.2}{1 \text{ mA}} \\ &= \frac{4.2 \text{ V}}{1 \text{ mA}} = 4.2 \text{ k}\Omega \end{aligned}$$

This is the value of R_1 to limit the additional current to 1 mA.

$$V_o(\text{low}) = V_{CE(\text{sat})} + V_F = 0.2 + 0.6 = 0.8 \text{ V}$$

When all the inputs to the AND are 1, diodes are OFF ;

$$V_o(\text{high}) = V_{CC} = 5 \text{ V}$$

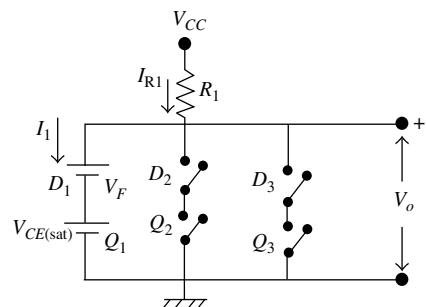


FIGURE 10.7(b) The circuit of Fig. 10.7(a) when Q_1 is ON, Q_2 and Q_3 are OFF

EXAMPLE

Example 10.2: For the three-input OR gate shown in Fig. 10.8(a), the supply voltage is 15 V. The inputs to the gate are supplied by bistable multivibrators. The output voltage is required to be 12 V for the logic level 1. Given $V_F = 0.6$ V. Fix the value of R_1 .

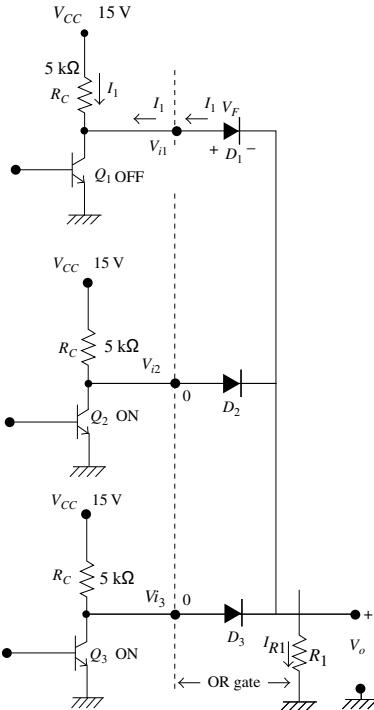


FIGURE 10.8(a) The three-input OR gate

Let the inputs be 1, 0 and 0 for D_1 , D_2 and D_3 , respectively. This means Q_1 is OFF and Q_2 and Q_3 are ON. Then D_1 is ON and D_2 and D_3 are OFF, as shown in Fig. 10.8(b).

$$V_{CC} = I_1 R_C + V_F + V_o \quad I_1 R_C = V_{CC} - V_F - V_o$$

V_o for 1 level required to be 12 V.

Therefore,

$$I_1 = \frac{15 - 0.6 - 12}{R_C} = \frac{2.4}{5 \text{ k}\Omega} \quad I_1 = I_{R1} = 0.48 \text{ mA}$$

Therefore

$$V_o = I_{R1} R_1 \quad R_1 = \frac{12}{0.48 \text{ mA}} = 25 \text{ k}\Omega$$

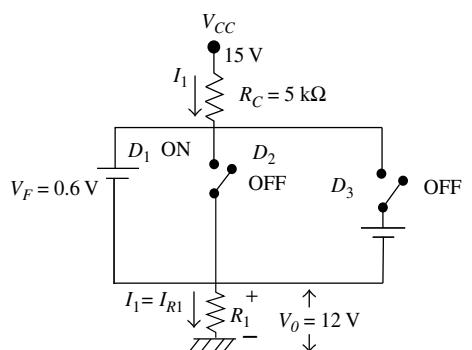


FIGURE 10.8(b) The circuit of Fig. 10.8(a) when Q_1 is OFF Q_2 and Q_3 are ON

10.2.2 Resistor-Transistor Logic Gates

An RTL gate uses the resistances and transistors for its operation. Figure 10.9 shows a resistor-transistor logic (RTL) NOR gate. If both the inputs V_1 and V_2 are 0, Q_1 and Q_2 are OFF and $V_o = V_{CC}$ (1 level). If any or both the inputs are 1, $V_o = V_{CE(sat)}$ (0 level). Hence, this is a NOR gate.

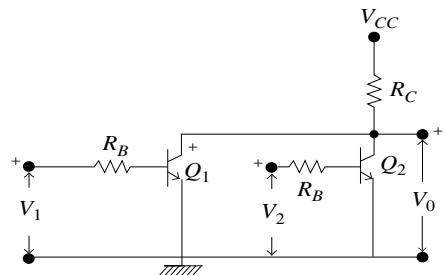


FIGURE 10.9 An RTL NOR Gate

E X A M P L E

Example 10.3: Verify that the alternate form of RTL gate in Fig. 10.10(a) is a NOR gate.

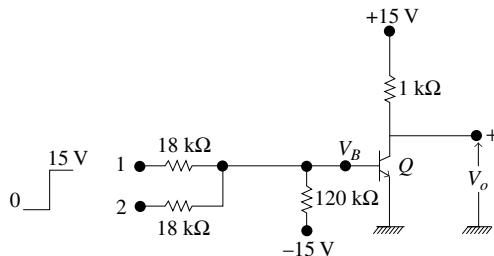


FIGURE 10.10(a) An RTL NOR gate

Solution:

(i) If both the inputs are 0 V, the resultant circuit is shown in Fig. 10.10(b).

$$V_B = \frac{-15 \times 9}{9 + 120} = -1.05 \text{ V}$$

As this voltage at the base of Q reverse-biases the emitter diode, Q is OFF:

$$V_o = 15 \text{ V} \text{ (1 level).}$$

If both the inputs are at 1 level (15 V), as shown in fig.10.10(c)

$$V_B = \frac{15 \times 120}{120 + 9} + (-15) \times \frac{9}{120 + 9} = 13.95 - 1.05 = 12.9 \text{ V}$$

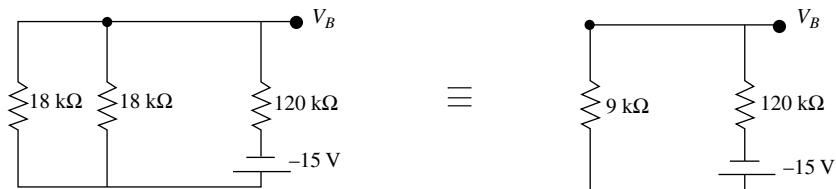


FIGURE 10.10(b) The resultant circuit of Fig. 10.10(a) when both the inputs are 0

Hence, Q is in saturation.

$$V_o = 0 \text{ V}(0 \text{ level})$$

If any one input is 1 (say 1) and the other input is 0 (say 2), the resultant circuit is shown in Fig. 10.10(d).

Thevenizing,

$$V_{th} = \frac{15 \times 18}{18 + 18} = 7.5 \text{ V} \quad R_{th} = \frac{18 \times 18}{18 + 18} = 9 \text{ k}\Omega$$

$$V_B = \frac{7.5 \times 120}{120 + 9} + (-15) \times \frac{9}{120 + 9} = 6.98 - 1.05 = 5.93 \text{ V}$$

This voltage at the base of Q , drives the transistor into saturation. Thus, if any or both the inputs are 1, $V_o = 0$ level; with both the inputs 0, $V_o = 1$ level. Hence, the truth table is as shown in Table 10.3. Therefore, the RTL gate is a NOR gate.

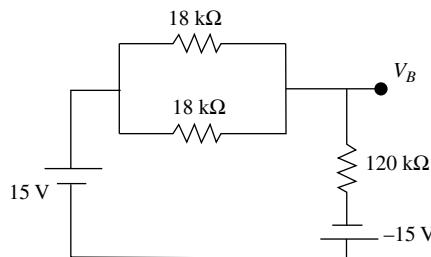


FIGURE 10.10(c) The resultant circuit of Fig. 10.10(a) when both the inputs are 1

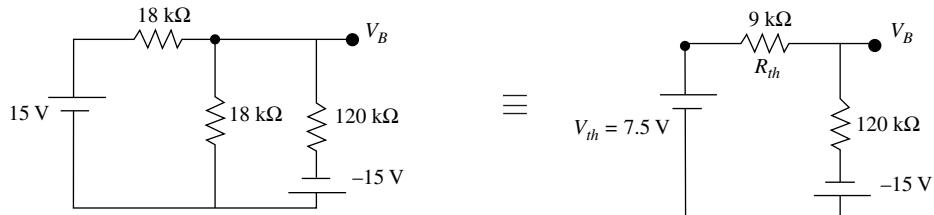


FIGURE 10.10(d) The resultant circuit of Fig. 10.10(a) when input 1 is 1 and input 2 is 0

TABLE 10.3 The truth table for a NOR gate

1	2	V_o
0	0	1
0	1	0
1	0	0
1	1	0

10.2.3 Diode–Transistor Logic Gates

In the diode–transistor logic family (DTL), diodes and transistors are used as the basic building blocks. In this family, we consider the two basic gates—NAND and NOR.

DTL NAND Gates. A diode AND gate followed by a transistor inverter is a DTL NAND gate, as shown in Fig. 10.11. Here, we assume that the input at 1 is grounded. Diode D_1 conducts. Then the voltage at A, $V_A = V_F$, the diode forward voltage. With this voltage (approximately equal to 0.7 V), diodes D_3 and D_4 will not conduct as they require a minimum voltage of 1.4 V to conduct. Hence, Q is OFF. Thus, if any one of the inputs to the NAND gate is zero, Q is OFF and $V_o = V_{CC}$ (1 level).

If, on the other hand, both the inputs are 1, then diodes D_1 and D_2 are reverse-biased and behave as open circuits. Diodes D_3 and D_4 then conduct and the voltage at the base of Q can drive it into saturation. Therefore, the output $V_o = V_{CE(sat)}$ (0 level). This gate produces a 0 output level when all the inputs are 1 and the 1 level at the output if any of the inputs is 0 (NAND gate). D_3 and D_4 are provided to derive noise immunity. In the NAND gate shown in Fig. 10.11, when D_3 is replaced by a Zener diode (anode and cathode reversed) with a break-down voltage of 3.8 V, this gate gives an even better noise immunity. However, this requires high supply voltages. Such a gate is called a high-threshold logic (HTL) NAND gate. HTL is also sometimes referred to as HNIL (high noise immunity logic).

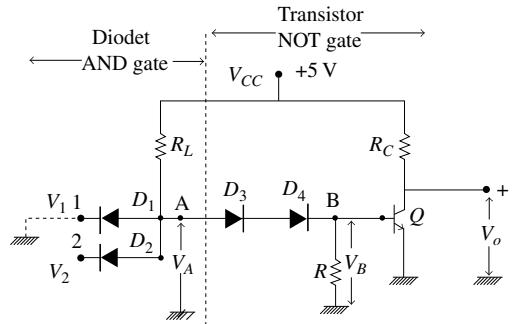


FIGURE 10.11 A DTL NAND gate

E X A M P L E

Example 10.4: Verify that the alternate form of the DTL circuit shown in Fig. 10.12(a) is a NAND gate. What is the minimum value of h_{FE} to keep Q in saturation?

Solution:

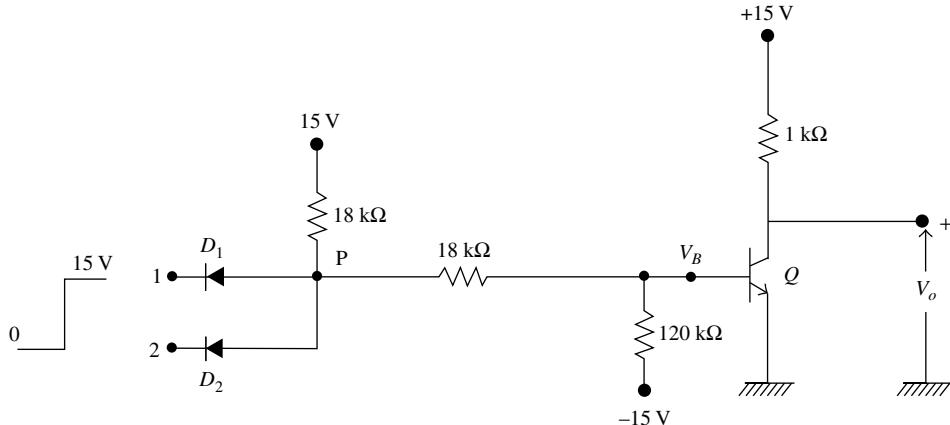


FIGURE 10.12(a) A DTL NAND gate

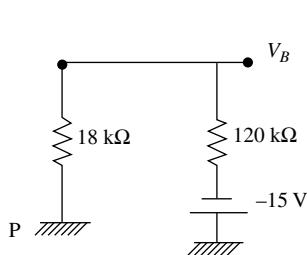


FIGURE 10.12(b) The resultant circuit of Fig. 10.12(a) when the input 1 is 0 and the other is 1

To verify that the circuit shown in Fig. 10.12(a) is a NAND gate, let us assume that input 1 is 0 V and input 2 is at level 1, i.e., 15 V. Then D_1 conducts as the voltage at the anode of D_2 is $V_F \approx 0$ V and that at the cathode is 15 V, D_2 is OFF and is open circuited. The voltage at P is 0 V, as shown in Fig. 10.12(b).

$$V_B = \frac{-15 \times 18}{18 + 120} = -1.96 \text{ V}$$

As V_B reverse-biases the emitter diode, Q is OFF and $V_o = 15$ V (1 level). If all the inputs are 15 V (1 level), both the diodes are OFF.

$$V_B = \frac{15 \times 120}{120 + 36} + (-15) \times \frac{36}{120 + 36} = 11.54 - 3.46 = 8.08 \text{ V}$$

Hence, Q is in saturation. Consequently, $V_o = 0$ V (0 level). The truth table for this is shown in Table 10.4. Hence, the circuit is a NAND gate.

(ii) Calculating the minimum value of h_{FE} to keep Q in saturation

Consider the equivalent circuit of Fig. 10.12 (a). When Q is in saturation, $V_{CE(\text{sat})} = 0$, $V_{BE(\text{sat})} = 0$ when compared to the supply voltages of 15 V, as shown in Fig. 10.12(d).

$$I_1 = I_2 + I_B \quad I_B = I_1 - I_2$$

$$I_B = \frac{15 \text{ V}}{36 \text{ k}\Omega} - \frac{15 \text{ V}}{120 \text{ k}\Omega} = 0.42 - 0.125 = 0.295 \text{ mA}$$

$$I_C = \frac{15 \text{ V}}{1 \text{ k}\Omega} = 15 \text{ mA}$$

And

$$h_{FE}(\text{min}) = \frac{I_C}{I_B} = \frac{15}{0.295} = 50$$

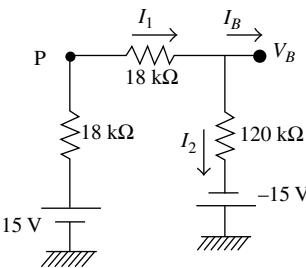


FIGURE 10.12(c) The resultant circuit of Fig. 10.12(a) when both the inputs are 1

TABLE 10.4 The truth table for a NAND gate

1	2	V_o
0	0	1
0	1	1
1	0	1
1	1	0

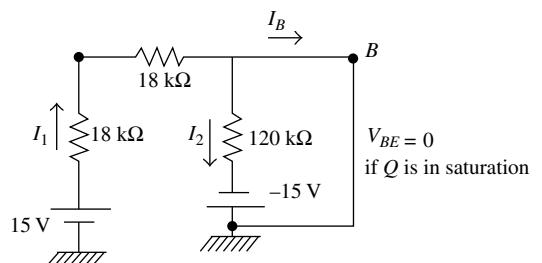


FIGURE 10.12(d) The resultant circuit of Fig. 10.12(a) when Q is in saturation

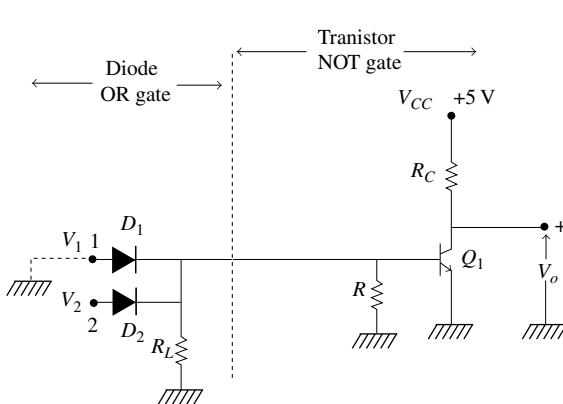


FIGURE 10.13 A DTL NOR gate

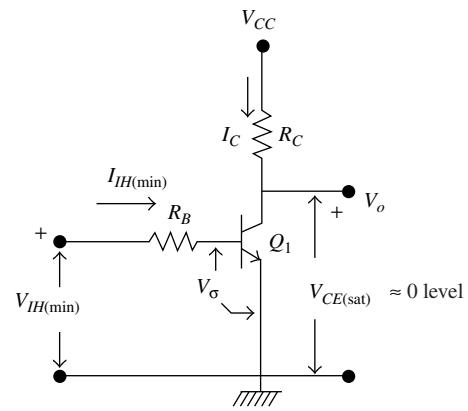


FIGURE 10.14 A transistor inverter with an output low

DTL NOR Gates. A DTL NOR gate comprises a diode OR gate followed by a transistor inverter, as shown in Fig. 10.13. When both the inputs V_1 and V_2 are 0, Q_1 is OFF and $V_o = V_{CC}$ (1 level). If any input, say V_1 is 1, D_1 is ON and the voltage at the base of Q_1 is 5 V. Consequently, Q_1 is in saturation and $V_o = V_{CE(\text{sat})}$ (0 level).

10.3 FACTORS DEFINING THE PERFORMANCE OF LOGIC GATES

The following factors define the performance of a logic gate:

Supply voltage: TTL IC logic gates are normally designed to operate with a supply voltage of 5 V whereas CMOS gates can operate in the range of 1–30 V. When a supply voltage of 5 V is specified for a gate, it is expected that the voltage variation remains within ± 0.25 V of 5 V for reliable gate operation.

Input voltages and currents: For a gate to operate properly, it should have minimum high-input voltage, $V_{IH(\text{min})}$, which represents the logic 1 input level.

As an example, let $V_{IH(\text{min})} = 2$ V for a gate. It means that the output of the gate changes only when the input is greater than or equal to 2 V. Consider the transistor inverter shown in Fig. 10.14.

Let Q_1 be OFF in which case the voltage at its collector is V_{CC} (1 level). To switch this output to a 0 level, the minimum high-input voltage is given as:

$$V_{IH(\text{min})} = I_{IH(\text{min})} R_B + V_\sigma$$

where, I_{IH} is the high-level input current sufficient enough to drive the transistor into saturation.(Typically, this value is 1mA.)

Similarly, each type of gate has a maximum low-input voltage, $V_{IL(\text{max})}$, which is the highest voltage acceptable as the logic 0 input. Consider the circuit shown in Fig. 10.15. $V_{IL(\text{max})}$, therefore, must be much smaller than V_γ . For silicon transistors, $V_{IL(\text{max})}$ is typically 0.2 V. Any voltage above this level will not be accepted as a low-level input by the logic circuit. $I_{IL(\text{max})}$ is the current that flows into an input when $V_{IL(\text{max})}$ is applied at the input. The low-level input current I_{IL} occurs when Q_2 is OFF. In actuality, the junction leakage current is less than 1 μ A

Output currents and voltages: The output current from a gate is termed as a high-level output current, I_{OH} , when the gate output voltage, V_{OH} , is high. Consider the circuit shown in Fig. 10.16.

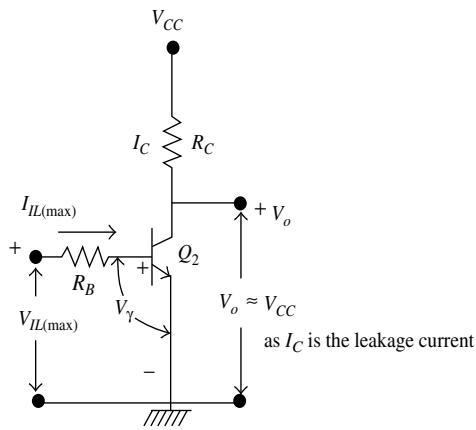


FIGURE 10.15 A transistor inverter with a high output

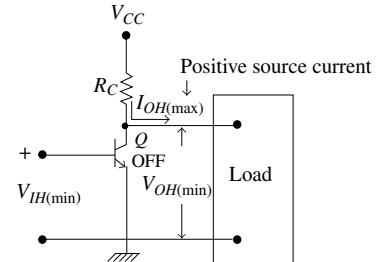


FIGURE 10.16 The output voltage and current when the gate output is high

Here, the device Q is OFF and $I_{OH(\max)}$ is the maximum high-level output current through the load. $I_{OH(\max)}$ is a positive quantity and the current flows out of the gate terminal. The gate is now said to source the output current and is called a current source. The minimum output voltage for a logic 1 level is called $V_{OH(\min)}$, given by the relation:

$$V_{OH(\min)} = V_{CC} - I_{OH(\max)}R_C.$$

Sometimes the output of a gate is required to drive the inputs of several gates. This requirement stipulates that the minimum logic 1 output voltage of a driving gate should be greater than or equal to the minimum logic 1 input of the driven gates, that is, $V_{OH(\min)} \geq V_{IH(\min)}$. The output current when the gate output voltage is low is called the low-level output current I_{OL} and the corresponding voltage V_{OL} is the low-level output voltage.

Consider the output of the gate shown in Fig. 10.17. Here, the low-level output current, I_{OL} , is generally a negative quantity. In other words, the current flows into the output terminal. The gate is now said to sink this current and the output is called a current sink. For the circuit shown in Fig. 10.17, $V_{OL(\max)} = V_{CE(\text{sat})} = 0.2 \text{ V}$. If this gate is required to drive the input of several gates, $V_{OL(\max)}$ has to be lower than $V_{IL(\max)}$.

Fan-out: The output of a logic gate may have to drive inputs of several similar logic gates. The maximum number of inputs (to several gates) that the output of any one gate can drive is called fan-out or loading factor of the gate. For example, if the fan-out of a logic gate is specified as five, it means that the gate can drive five inputs from the same family.

$$\text{Generally, fan-out} = \frac{I_{OL(\max)}}{I_{IL(\max)}}.$$

The fan-out, when the output of a gate is at logic level 1, is indicated in Fig. 10.18(a).

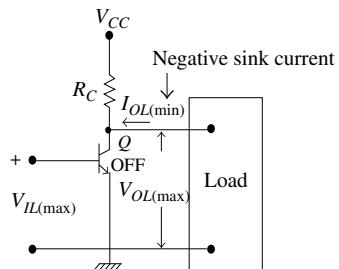


FIGURE 10.17 The output voltage and current when the gate output is low

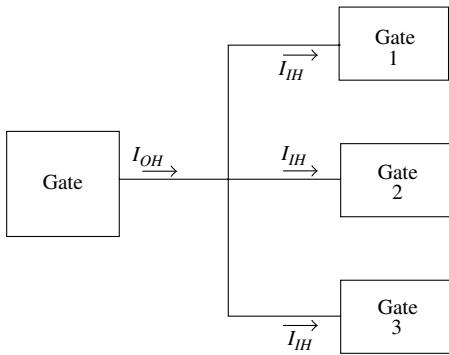


FIGURE 10.18(a) The fan-out when the output of a gate is at logic level 1

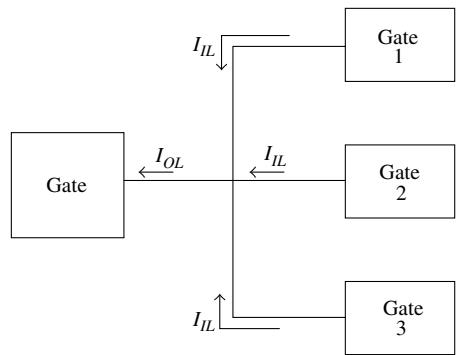


FIGURE 10.18(b) The fan-out when the output of a gate is at 0 level

The fan-out when the output of a gate is high is:

$$\text{Fan-out} = \frac{|I_{OH(\max)}|}{|I_{IH(\max)}|}$$

For standard TTL, $I_{OH(\max)} = 400 \mu\text{A}$ and $I_{IH(\max)} = 40 \mu\text{A}$

$$\text{Therefore, fan-out} = \frac{400 \mu\text{A}}{40 \mu\text{A}} = 10$$

This means, that the standard TTL gate can drive the inputs of 10 other identical gates. The fan-out, when the output of a gate is at 0 level, is shown in Fig. 10.18(b).

The fan-out when the output of a gate is low,

$$\text{Fan-out} = \frac{|I_{OL(\max)}|}{|I_{IL(\max)}|}$$

For standard TTL, where $I_{OL(\max)} = 16 \text{ mA}$ and $I_{IL(\max)} = 1.6 \text{ mA}$ are typical currents.

$$\text{Therefore, fan-out} = \frac{16 \text{ mA}}{1.6 \text{ mA}} = 10$$

The fan-out in both the cases is 10. However, in practice, it is the smaller value, that is taken into account.

Fan-in: Fan-in normally refers to the number of inputs of a gate. A gate can have one input as in an inverter. In this case the fan-in is 1. An OR gate may have two inputs. Then, the fan-in is 2 and another AND gate may have four inputs for which the fan-in is 4. In general, the smaller is the fan-in the faster is the gate.

Propagation delay: In logic gates, diodes and transistors are used as switches. Proper fabrication techniques can help reduce the influence of stray capacitances to a minimum. However, it is practically impossible to eliminate the influence of these stray capacitances. These stray capacitances influence the switching speed of a device, as a consequence of which the output does not respond to an input instantaneously and may have a rise time though the input to the gate is a pulse with zero rise time. If the output of the first gate is the input to another gate, there is further distortion in the amplitude of the signal and this effect becomes cumulative when the signal passes through several gates. Thus, when the signal passes through several gate combinations, it is subjected to time delay and (possibly) appreciable distortion, which limits the utility of the gate. Hence,

while using a gate for a specific application, we need to know the propagation delay. The time interval from the instant the input pulse is applied to the gate to the time of occurrence of the resultant output pulse is called the propagation delay of the gate. Propagation delay specifies the switching speed of the gate. Alternatively, propagation delay can also be defined as the time required for the gate to switch from a low-output state to a high-output state and vice versa. Consider the gate shown in Fig. 10.19(a).

The following method is used for measuring the propagation delay. Consider a simple inverter gate with a finite propagation delay, where the output is shifted in the phase by 180° , as shown in Fig. 10.19(b).

On the other hand, if the output of the gate is in the same phase as the input with only a propagation delay as shown in Fig. 10.19(c):

t_{PLH} = Time for the output to go from low to high

t_{PHL} = Time for the output to go from high to low.

These times are measured between the 50 per cent levels of the input and output. Normally, $t_{PLH} \neq t_{PHL}$. In some cases, propagation delay, t_p is taken to be the larger of these two values, i.e., propagation delay, $t_p = \max(t_{PLH}, t_{PHL})$. More realistically, it is taken as the average of these two values i.e.,

$$\text{Propagation delay} = t_p = \frac{t_{PLH} + t_{PHL}}{2}$$

Noise immunity: In a logic gate, both the input and the output are either 0 level or 1 level, representative of dc voltages or pulse amplitudes. We already know that each gate has a maximum low-input voltage, $V_{IL(\max)}$, which is the highest voltage acceptable as a 0 input and a minimum high-input voltage, $V_{IH(\min)}$, acceptable as a 1 level at the input. Noise (unwanted signals at the input) sometimes may change the voltage at the input of a gate that may lead to unpredictable operation of a gate.

Noise immunity is the ability of the logic gates to tolerate changes at the input due to noise but still deliver the predictable output. Consider the input and output voltage levels of a logic gate as shown in Fig. 10.20.

Low-state noise margin, $V_{NL} = V_{IL(\max)} - V_{OL(\max)}$

High-state noise margin, $V_{NH} = V_{IH(\min)} - V_{OH(\min)}$

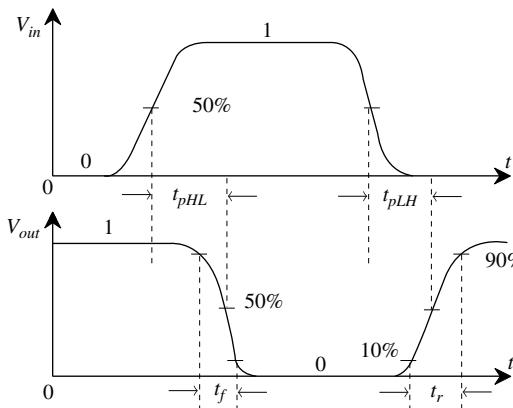


FIGURE 10.19(b) The inverter propagation delay

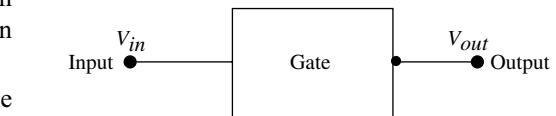


FIGURE 10.19(a) A basic gate

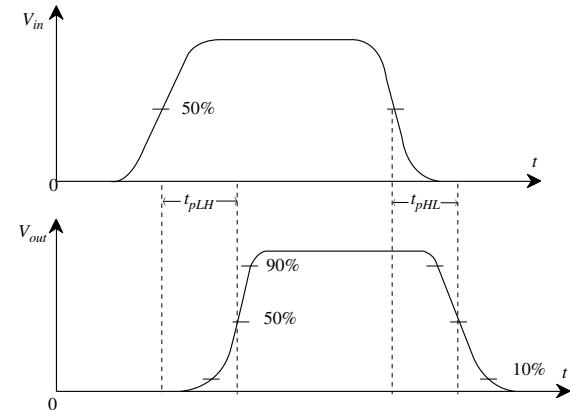


FIGURE 10.19(c) The non-inverter propagation delay

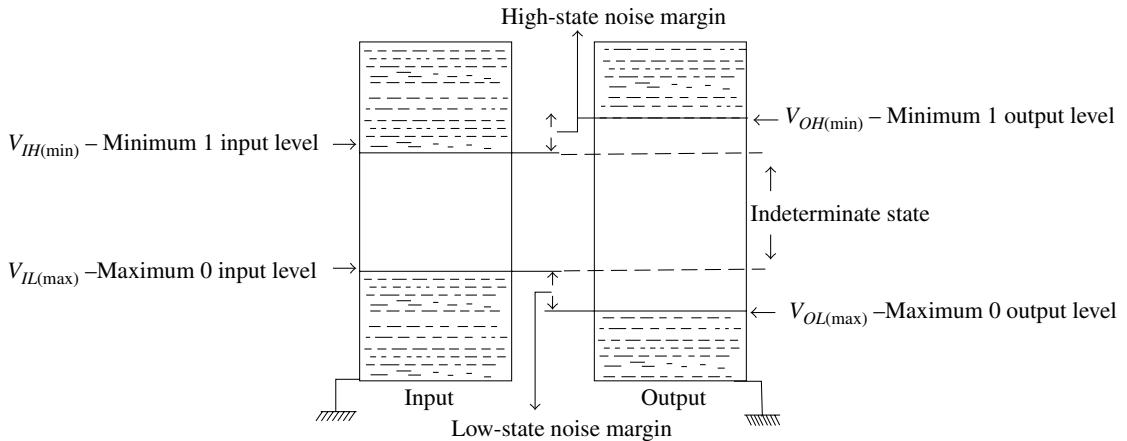


FIGURE 10.20 The input and output voltage levels of a logic gate and its noise immunity

Noise spikes greater than the noise margins specified may drive the gate into an intermediate range. This gives rise to ambiguity. Data sheets normally specify noise immunity for a gate as poor, fair, good or excellent.

Power dissipation: When batteries supply power to logic gates, the drain on the battery should be minimum. For this to happen we must use gates with the lowest dissipation possible. Typically power dissipation varies from 10 nW to 25 μ W per gate, depending on the circuitry. Power dissipation is generally large in a gate that switches fast (TTL gate) because, for faster switching, the transistor is held in the active region. Generally, a circuit employing many gates may generate more heat. Obviously, in such cases, the gates that have the least power dissipation are desirable. Hence, in applications where power dissipation is the major consideration in the choice of a gate, CMOS gates are preferred over TTL gates.

Figure of merit: The figure of merit of a logic gate is the product of propagation delay and the average power dissipation. The smaller the figure of merit the better is the performance of the gate. The figure of merit is also called the speed-power product.

Figure of merit = Propagation delay (seconds) \times average power dissipation (Watts) = Joules/s

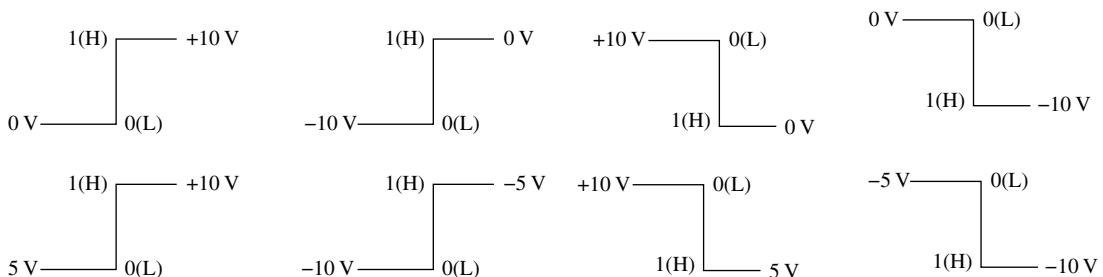


FIGURE 10.21(a) The positive logic

FIGURE 10.21(b) The negative logic

10.4 POSITIVE LOGIC, NEGATIVE LOGIC AND LOGIC CIRCUIT CONVERSION

Positive logic: If the signal that activates the logic gate has for its high (1) level a voltage more positive than for its low (0) level then the polarity of the logic is called positive logic, as shown in Fig. 10.21(a).

Negative logic: If the signal that activates the logic gate has for its high (1) level a voltage more negative than for its low (0) level then the polarity of the logic is called negative logic, as shown in Fig. 10.21(b).

Logic circuit conversion: A circuit using a positive (negative) logic can be converted into a circuit performing the same logic function but with a negative (positive) logic by following the procedure listed below.

Step 1. Reverse the polarities of all supply voltages.

Step 2. Reverse the polarity of the driving signals (input voltages).

Step 3. The polarities of all diodes are reversed and all transistors are changed from $p-n-p$ to $n-p-n$ and vice versa. Consider Example 10.5 to verify this procedure.

E X A M P L E

Example 10.5: Consider the NOR gate with a positive logic shown in Fig. 10.21(c). In the positive logic a '0' level is 0 V and '1' level is V . In this example $V = 10$ V. Obtain the truth table for a positive logic and verify with the negative logic.

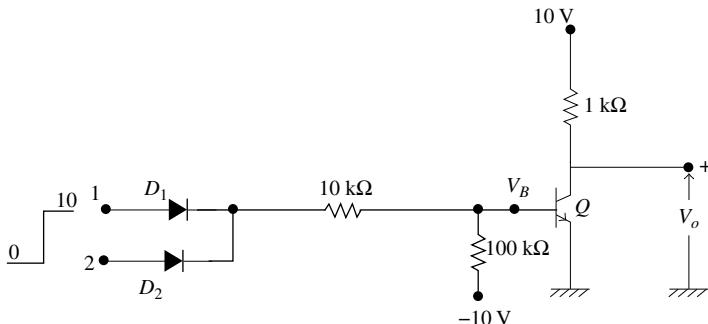


FIGURE 10.21(c) The DTL NOR gate with a positive logic

Solution:

For the circuit shown in Fig. 10.21(c), if both the inputs are of 0 V, diodes D_1 and D_2 conduct. Then, the voltage at P is 0 V. The voltage at the base of Q , V_B , is calculated using the circuit shown in Fig. 10.21(d).

$$V_B = \frac{-10 \times 10}{110} = -0.91 \text{ V}$$

Hence, Q is OFF. Therefore, $V_o = 10 \text{ V}$ (1 level).

If the input 1 is 10 V and the input 2 is 0 V, then D_1 is ON and the voltage at P is 10 V. This reverse-biases the diode D_2 and it is OFF. The corresponding circuit is shown in Fig. 10.21(e).

The voltage at the base of Q , V_B now is:

$$V_B = \frac{10 \times 100}{110} + (-10) \times \frac{10}{110} = 8.19 \text{ V}$$

Hence, Q is in saturation and $V_o \approx 0 \text{ V}$. The conditions are tabulated in the truth table given in Table 10.5. Hence, the circuit is a positive NOR.

To convert the positive NOR into a negative NOR, follow the given steps:

- 1 Let the driving input now have 1 level as -10 V and 0 level as 0 V (negative logic).
- 2 Reverse the polarity of the supply voltages.
- 3 Reverse the polarities of the diodes.
- 4 Replace the $n-p-n$ transistor by a $p-n-p$ transistor. Then, the circuit is still a NOR gate, but now with a negative logic, as shown in Fig. 10.21(f).

When both the inputs are -10 V (1 level), $V_B = -8.18\text{ V}$, Q is ON and $V_o = 0\text{ V}$ (0 level). When both the inputs are at 0 level (0 V), $V_B = 0.91\text{ V}$, Q is OFF and $V_o = -10\text{ V}$ (1 level). Thus, this circuit is also a NOR gate but with a negative logic.

Let us consider a logic gate and let a voltage V_1 be added to all the supply voltages, to all leads that are grounded and to both the binary levels (0 and 1). Then it can be verified that the logic function performed by the circuit to which these voltages are added is again the same as that of the original circuit.

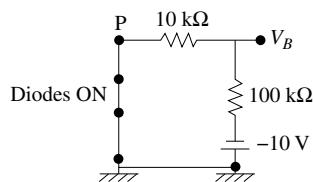


FIGURE 10.21(d) The circuit to calculate the output, when both the inputs are '0'

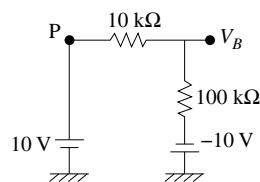


FIGURE 10.21(e) The circuit to calculate V_B , when input 1 is 10 V and input 2 is 0 V

TABLE 10.5 The truth table for a positive logic

V_1	V_2	V_o
0	0	1
0	1	0
1	0	0
1	1	0

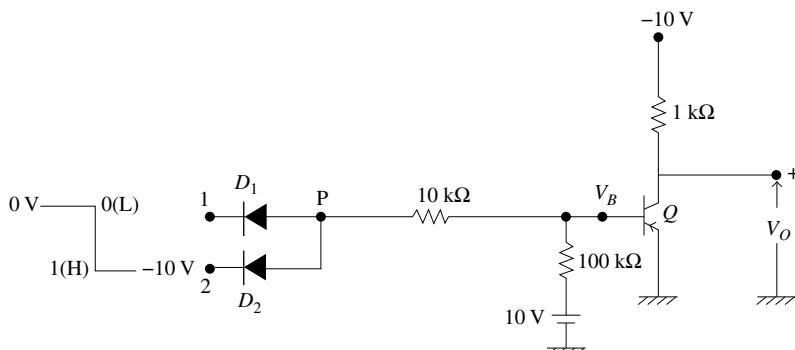
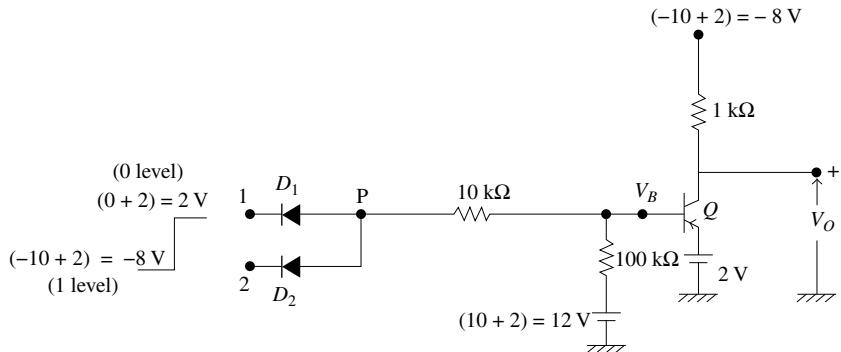


FIGURE 10.21(f) The DTL NOR gate with a negative logic (1 level is -10 V and 0 level is 0 V)

FIGURE 10.21(g) The equivalent circuit of 10.21(f) when $V_1 = 2$ V is added

To illustrate this consider the circuit shown in Fig. 10.21(f). If $V_1 = 2$ V is added, then the circuit is redrawn as shown in Fig. 10.21(g). This circuit performs the same logic operation as the circuit shown in Fig. 10.21(f).

10.4.1 Transistor–Transistor Logic Gates

In transistor–transistor logic (TTL) gates, the inputs are directly connected to the input terminals of the transistors. In this logic family, bipolar junction transistors are used as the basic building blocks. Let us consider two types of TTL gates, a TTL NAND gate and a TTL NOR gate.

TTL NAND Gates. Firstly consider the basic TTL NOT gate, shown in Fig. 10.22(a). When the input to the gate $V_i = 0$ (i.e., emitter is grounded), the base–emitter diode of Q_1 is forward-biased by a large voltage which drives the transistor into saturation. Therefore, the voltage between the collector and emitter (grounded) terminals is $V_{CE(\text{sat})}$ which is typically 0.2 V and cannot drive Q_2 ON. Hence, Q_2 is OFF and its output is $V_o = V_{CC}(1 \text{ level})$. Thus, when the input is 0, the output is 1 as shown in Fig. 10.22(b).

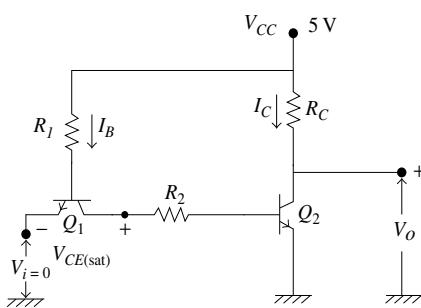


FIGURE 10.22(a) A TTL NOT gate

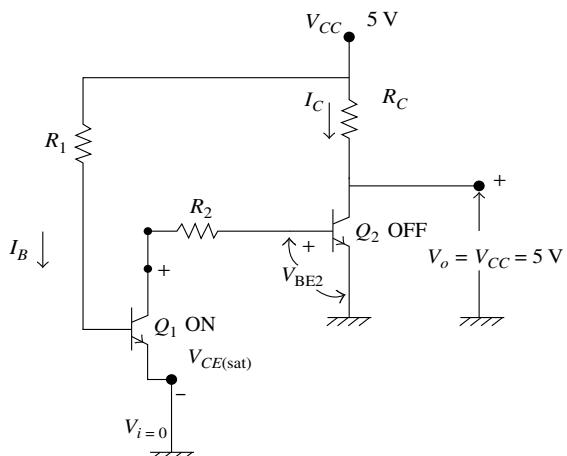


FIGURE 10.22(b) The circuit of Fig. 10.22(a) when the input is low

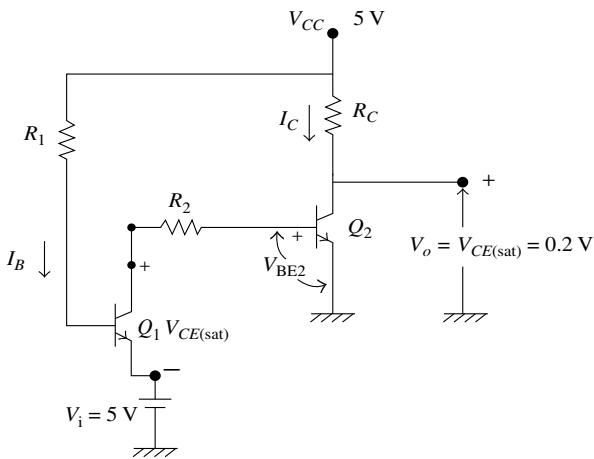


FIGURE 10.22(c) The circuit of Fig. 10.22(a) when the input is high

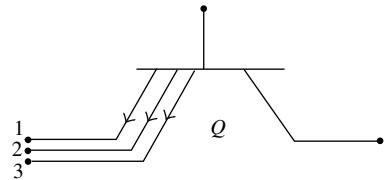


FIGURE 10.22(d) A multi-emitter transistor

Now, if a high input is applied ($V_i = 5\text{ V}$), the base-emitter diode of Q_1 is reverse-biased. As Q_1 cannot go into the OFF state immediately, $V_{CE(\text{sat})}$ still exists between the collector and emitter terminals of Q_1 . Hence, the net voltage at the collector of Q_1 is $V_i + V_{CE(\text{sat})}$. This voltage at the base of Q_2 drives it into saturation. As a result, its output $V_o = V_{CE(\text{sat})} = 0.2\text{ V}$ (0 level), as shown in Fig. 10.22(c). Thus, if the input is 1, the output is 0 and viceversa. Hence, this is a TTL NOT gate.

To ensure that more number of inputs can be connected to the gate, Q_1 can be a transistor with more number of emitters. A three-emitter transistor is shown in Fig. 10.22(d).

A two-input TTL NAND gate is shown in Fig. 10.22(e). When all the inputs are at 1 level, Q_2 is ON and in saturation. Therefore, the output V_o is a 0 level. When any or both the inputs are at 0 level (grounded), Q_2 is OFF and the output V_o is at 1 level. Hence, it is a NAND gate. Standard TTL gates are usually referred to as 74 or 7400 series and 54 or 5400 series. A 54 series gate operates over a wider temperature range (-55°C to $+125^\circ\text{C}$) and can tolerate variations of the supply voltage by $\pm 0.5\text{ V}$ (i.e., the supply voltage variation can be from 4.5 V to 5.5 V). A 74 series operates in the temperature range of 0 to 70°C and the supply voltage variation can only be $\pm 0.25\text{ V}$ (i.e., the supply voltage can vary from 4.75 V to 5.25 V). A two-input 74 series TTL NAND gate is shown in Fig. 10.22(f).

Diodes D_1 and D_2 are included in the gate circuit shown in Fig. 10.22(f). If, for any reason, the input has negative spikes, then diodes D_1 and D_2 conduct to limit the amplitude of these spikes. Apart from this, these diodes have no other specific role in the operation of the gate. To understand the operation of the gate, for all practical purposes diodes D_1 and D_2 can be disconnected. The gate circuit thus obtained is shown in Fig. 10.22(g).

When both the inputs are at 1, Q_1 is OFF and the voltage at the base of Q_2 is large. As such, Q_2 goes ON and into saturation. Hence, Q_3 is OFF and Q_4 is ON (saturation). As a result, the output V_o is pulled down and is at 0 level. With these inputs, drawing the output circuit only results in the circuit shown in Fig. 10.22(h).

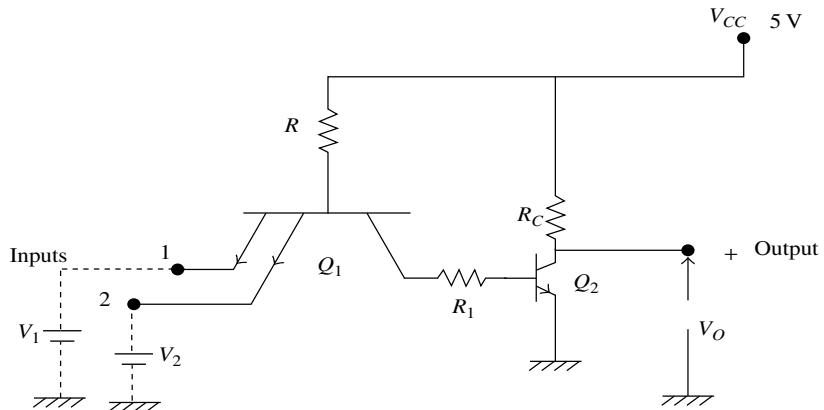


FIGURE 10.22(e) The two-input TTL NAND gate

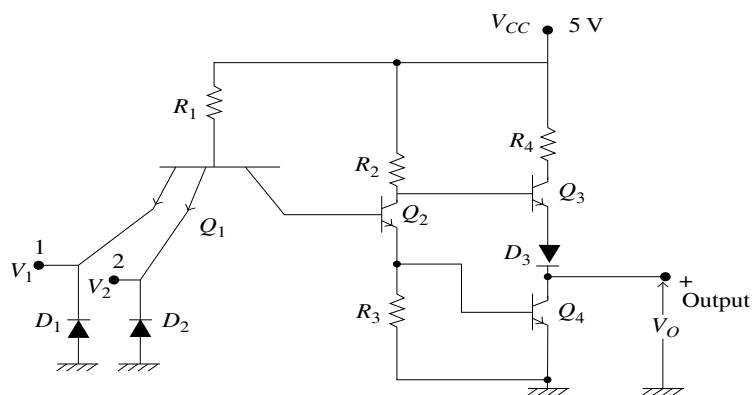


FIGURE 10.22(f) A 74 series two-input TTL NAND gate

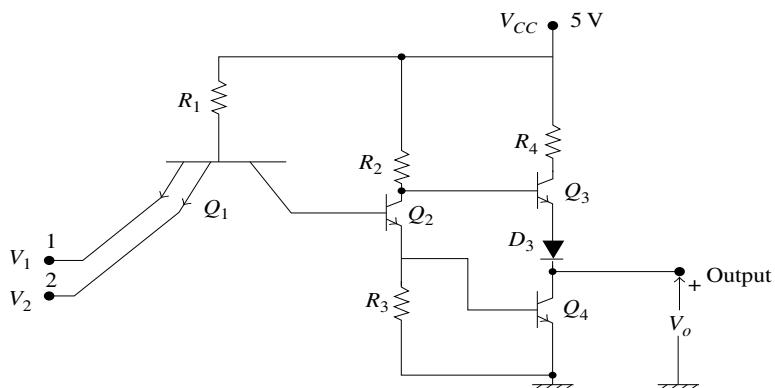


FIGURE 10.22(g) The practical TTL NAND gate

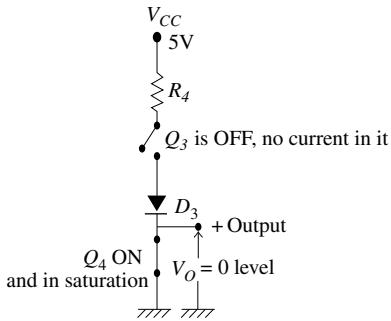


FIGURE 10.22(h) The circuit when both the inputs are at 1 (Q_3 is OFF and Q_4 is ON)

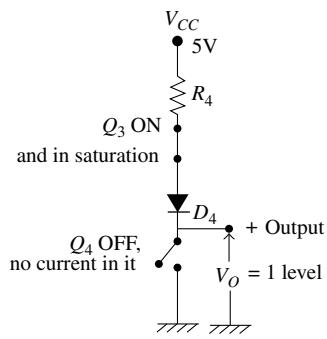


FIGURE 10.22(i) The circuit when any one input is at 0 (Q_3 is ON and Q_4 is OFF)

If any one of the inputs is at 0, Q_1 is in saturation and the voltage at the base of Q_2 is $V_{CE}(\text{sat})$, which is small. Therefore, Q_2 is OFF. Hence, Q_3 is ON and Q_4 is OFF. The output circuit is drawn as shown in Fig. 10.22(i).

The output is now at 1 level. Q_3 provides an active pull-up, that is, the output now at 1 level.

We have seen that when both the inputs are high (1 level = 5 V), the base-emitter junctions of Q_1 are reverse-biased and Q_1 is OFF. Hence, the voltage at the base of Q_2 is large. As a result, Q_2 is driven into saturation and consequently, Q_4 goes into saturation. Therefore, $V_o = 0.2$ V (0 level). Now if suddenly, one of the inputs goes low, the output is expected to jump to 1 level abruptly. This is possible because just prior to the instant that one input has become 0, as the voltage at the base of Q_1 is approximately 0.7 V and as Q_2 and Q_4 are in saturation, the voltage at the collector of Q_1 is $(V_{\sigma 2} + V_{\sigma 4}) = 1.4$ V.

Hence, the collector of Q_1 is positive than its base by 0.7 V, which means that its base-collector diode is reverse-biased. Hence, Q_1 is in the active region. This results in a large collector current in Q_1 due to the normal transistor amplification. This current flows out of the base of Q_2 and removes the stored charges quickly, thereby turning OFF Q_2 and Q_4 rapidly. As a result, the output goes to 1 level quickly, which accounts for the faster switching speed of the TTL gate. Q_2 also switches ON faster when all the inputs go high. Therefore, TTL gate is considered as the fastest logic gate.

In Fig. 10.22(g), in place of the collector load R_L for Q_4 , transistor Q_3 and diode D_3 are used as load (pull-up resistor, R_L). This arrangement, where at the output of TTL gate one transistor is stacked on top of the other and their operation is complementary, i.e., when one transistor is ON (say Q_3) the other is OFF (Q_4) and vice-versa, is called a totem-pole arrangement. The advantage of totem-pole output circuits is that there is always one totem-pole transistor that is cut-off; except for a short time during the transition from one output state to the other. As a result, although the pull-up resistor is required, it can be much smaller than in the simple passive pull-up circuit. This reduces the time required to charge the input capacitance of gates connected to a totem-pole output due to the reduced time constant.

Totem-poles are the monumental sculptures carved from the great trees by native Americans. Standard (74/54 series) TTL has a fan-out of 10, propagation delay of 10 ns, power dissipation of 10 mW/gate and good noise immunity. The standard TTL logic gate with totem-pole output has a disadvantage in that the outputs of two gates can not be connected together to function as an AND gate. Consider the outputs of two such gates, shown in Fig. 10.23.

The two outputs are connected at A. Q_{4B} acts as load for Q_{3A} and in fact Q_{4B} is a low-resistance load, hence, it draws a large load current I_{Load} . This may cause overheating of Q_{3A} .

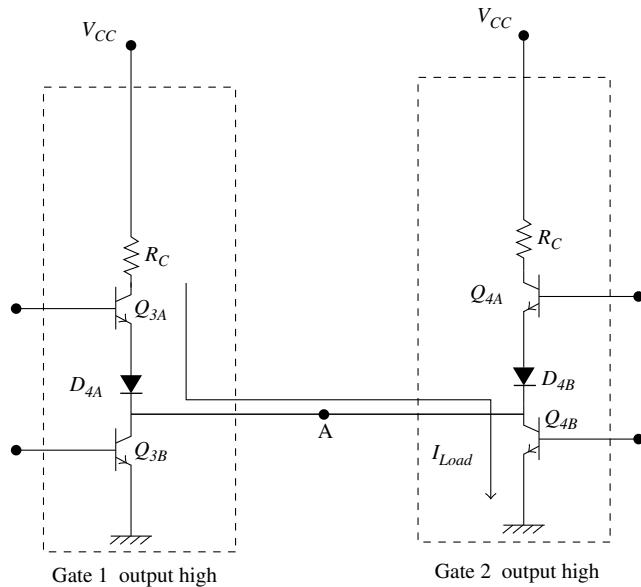


FIGURE 10.23 The TTL NAND gates with totem-pole output ANDed at A

TTL NOR Gates with Totem-pole Output. A TTL NOR gate with a totem-pole output is shown in Fig. 10.24. When both the inputs are V_1 and V_2 low, Q_{1A} and Q_{1B} are ON and Q_{2A} and Q_{2B} are OFF. Q_3 is ON and Q_4 is OFF. Hence, the output is 1. When both or any one of the inputs is 1, the output is low (0 level).

Open-Collector TTL Gates. The limitation in a standard TTL gate with totem-pole output is that the outputs can not be tied together. This can be overcome in an open-collector TTL gate. R_4 , D_3 and Q_3 that are there in a totem-pole circuit, as shown in Fig. 10.22 (g), are eliminated and Q_4 has open-circuited the collector.

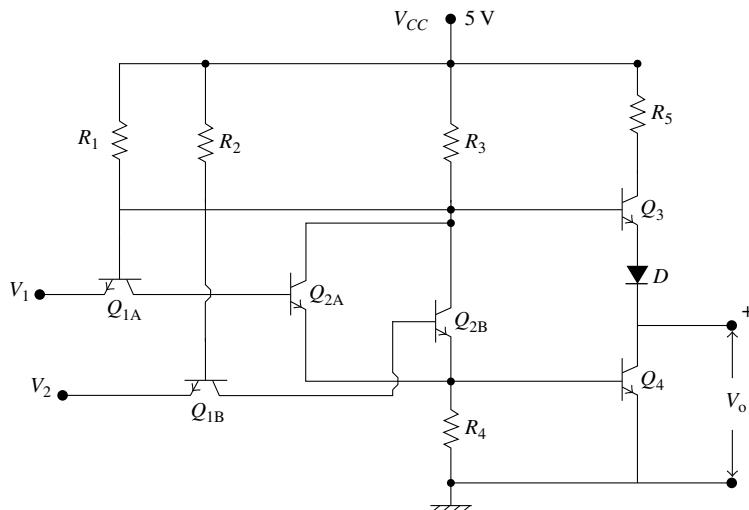


FIGURE 10.24 The TTL NOR gate totem-pole output

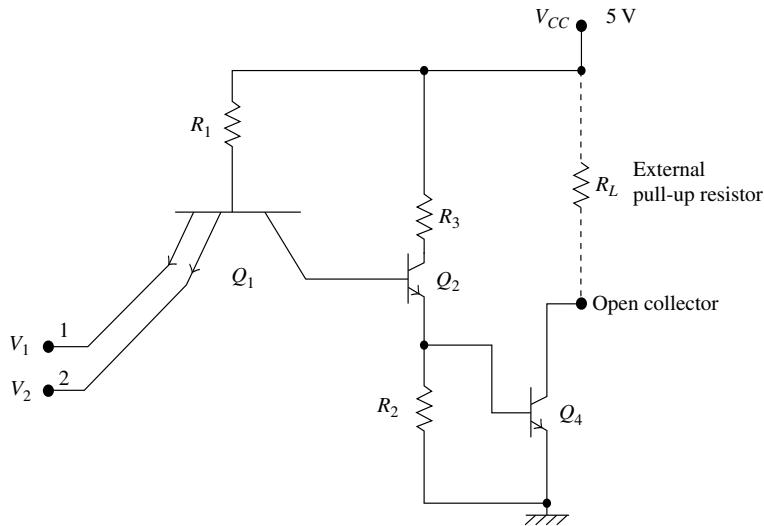


FIGURE 10.25 An open-collector TTL NAND gate

For this gate to work, an external pull-up resistor is connected from the collector of Q_4 to V_{CC} , as shown in Fig. 10.25.

The outputs of open-collector TTL gates can be connected together and the resultant arrangement is called a wired AND, as shown in Fig. 10.26. $Q_{4,1}$, $Q_{4,2}$ and $Q_{4,3}$ are the output transistors of gates 1, 2 and 3.

When all the transistors are OFF, the output is 1. If anyone of the inputs is 0, the output is 0 (AND operation). This gate, however, has a lower switching speed.

Tri-state Logic Gates. In the logic gates seen till now the output is either high or low. The output has only two states. But in tri-state logic, in addition to the high and low states at the output, the gate circuit offers high output impedance. A tri-state (TSL) NAND gate with totem-pole output is shown in Fig. 10.27. This circuit

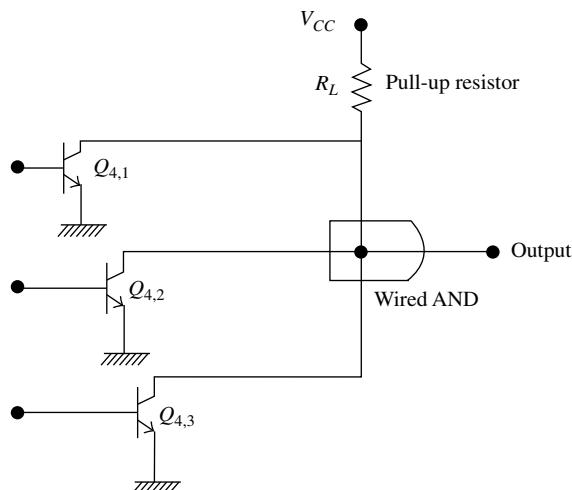


FIGURE 10.26 The wired AND gate

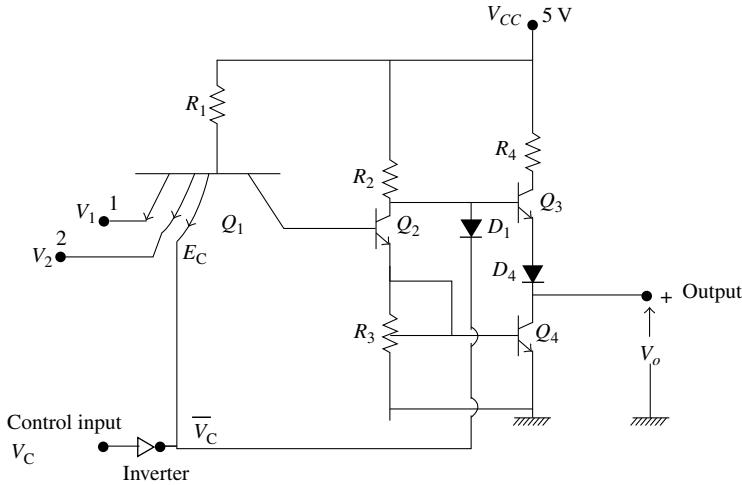


FIGURE 10.27 The TSL NAND gate

is similar to the circuit shown in Fig. 10.22(g), except for the fact that a control input is connected through an inverter to one of the emitters (E_C) of Q_1 and through a diode D_1 , to the base of Q_3 .

Let the control input be low (0 V). The output of the inverter is high (5 V). Hence, D_1 is reverse-biased and is an open circuit. The same high level (5 V) is connected to one emitter of Q_1 (E_C) which reverse-biases its base-emitter diode. Now, if both the inputs V_1 and V_2 are high, Q_1 is OFF. Hence, Q_2 is ON. Consequently Q_3 is OFF and Q_4 is ON. Thus, when all the inputs are high, the output is low.

When any or both the inputs are low, Q_1 is ON and Q_2 is OFF. Hence, Q_3 is ON and Q_4 is OFF. Hence, the output is at 1 level. We see that essentially the circuit behaves as a conventional TTL NAND gate when the control input is low.

If, on the other-hand, the control input is high, the output of the inverter is low. As a result, D_1 is ON and a low level (0 V) is connected to the base of Q_3 . Hence, Q_3 is OFF. At the same time, as a low level from the inverter is connected to E_C , Q_1 is ON, whatever may be the inputs to the gate terminals (V_1 and V_2). Therefore, Q_2 is OFF and its output is high. Hence, Q_3 should be ON and Q_4 is OFF. However, Q_3 is also OFF as a low level is connected to its base. Thus, both Q_3 and Q_4 are OFF when the control input is at 1 level. The output of this gate thus, offers a high impedance to all the circuits connected to it, when the control input to the inverter is high. This is the third state of the TSL gate. The TSL gate allows the output to be high, low or offers high output impedance. Hence, the name tri-state logic gates.

Emitter-coupled Logic (ECL). The TTL gates considered till now have one major limitation—the ON device is driven into saturation resulting in a longer storage time. As a result, the switching speed is reduced. However, in emitter-coupled logic (ECL), also known as current mode logic (CML), the ON device is prevented from going into saturation, which ensures lesser storage time and faster switching speed. A typical OR/NOR gate is shown in Fig. 10.28.

A suitable voltage V_{BB} is considered (This can be derived by using a potential divider network and also temperature compensation can be provided by using compensating diodes) such that there is a current $I_E (\approx I_{C3})$ in R_1 . This current can be adjusted so that Q_3 is ON and in the active region.

When both the inputs V_1 and V_2 are low (0 V), Q_1 and Q_2 are OFF. The voltage at the collectors of Q_1 and Q_2 is V_{CC} and is at 1 level (5 V), which is connected to the base of Q_4 . As Q_4 is used as an emitter follower, this 1 level is transmitted to the output. The output of this emitter follower corresponds to the output of the

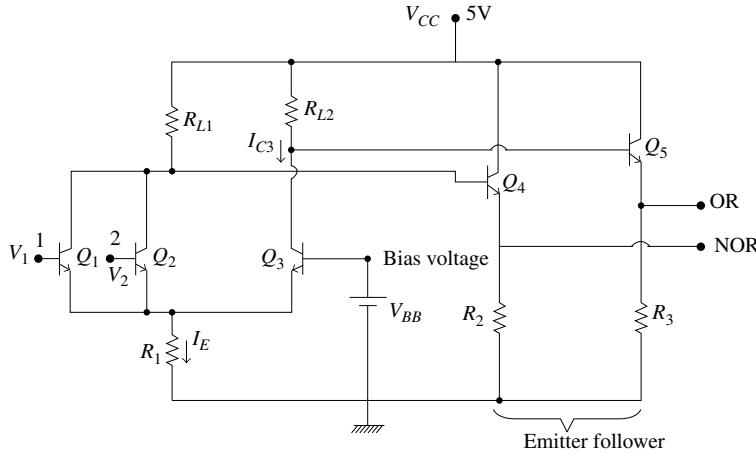


FIGURE 10.28 An emitter-coupled OR / NOR gate

NOR gate. At the same time Q_3 is ON, the voltage at the base of Q_5 is low and hence, the output of this emitter follower (OR) is low.

When a high level (5 V), is connected to any one of the inputs (say, V_1), then Q_1 is ON. As a result, the voltage connected to the base of Q_4 is low and the output of this emitter follower is low (NOR).

When Q_1 is ON, there is larger current in R_1 and a larger voltage drop in it. This reverse-biases the base-emitter diode of Q_3 , hence, Q_3 is OFF. The voltage at the base of Q_5 is high and the output of this emitter follower is high. Thus, if the output is taken at the emitter of Q_4 , this circuit is a NOR gate. And if the output is taken from the emitter of Q_5 , this circuit is an OR gate.

The major advantage of ECL gates is the smaller propagation delay as the devices are not allowed to saturate. However, at the same time, the resulting disadvantage is that the dissipation is larger as the ON device is held in the active region.

Integrated Injection Logic (I^2L). Faster switching speed and low power dissipation are the two major factors that weigh favorably while choosing a logic gate. Apart from these, physical size and manufacturing costs could also be of concern as these gates are manufactured as integrated circuits. In an integrated circuit, transistors occupy ten times less space than the resistors. Thus, if transistors can replace resistors, then an appreciable reduction in the gate area can be achieved. Further, if the transistors Q_1 and Q_2 share common regions of n -type and p -type material, it is possible to achieve a greater circuit density.

The I^2L gates eliminate the resistors. As n and p regions can be merged (alternately, transistors are merged), these logic gates are also called merged transistor logic (MTL) gates. Let us consider an RTL inverter, shown in Fig. 10.29.

In MTL logic, we want that R_1 and R_2 should be replaced by two $p-n-p$ transistors (as per the requirement of the current directions in Fig. 10.29) Q_1 and Q_3 . Then the inverter circuit with transistors replacing resistors is redrawn as in Fig. 10.30

If Q_1 and Q_3 supply the same currents I_1 and I_2 , then R_1 and R_2 can be replaced by Q_1 and Q_3 . The currents I_1 and I_2 are injected into the transistor emitters. Hence the name integrated injection logic.

When the output of one inverter is connected as input to the next inverter, the transistor that supplies the base current to second inverter can become the collector load of the first inverter. As such, each inverter consists of only two transistors, as shown in Fig. 10.31. Here, we see that the base current for Q_2 is supplied by Q_1 (R_1 shown in Fig. 10.29) and its collector current by Q_3 (R_2 shown in Fig. 10.29). Further Q_3 also supplies the base current for Q_4 .

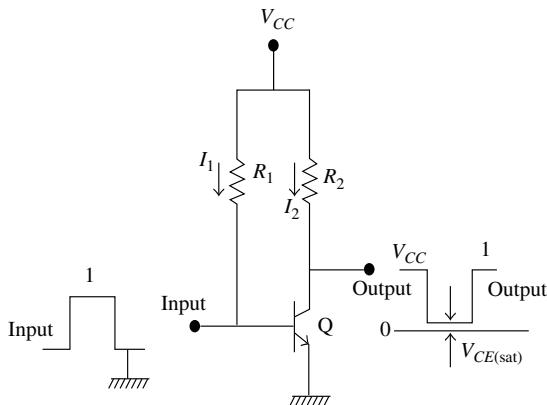


FIGURE 10.29 RTL inverter

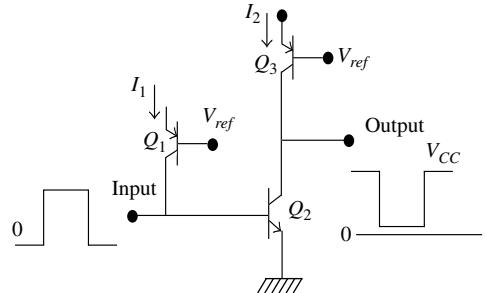


FIGURE 10.30 Inverter with transistors

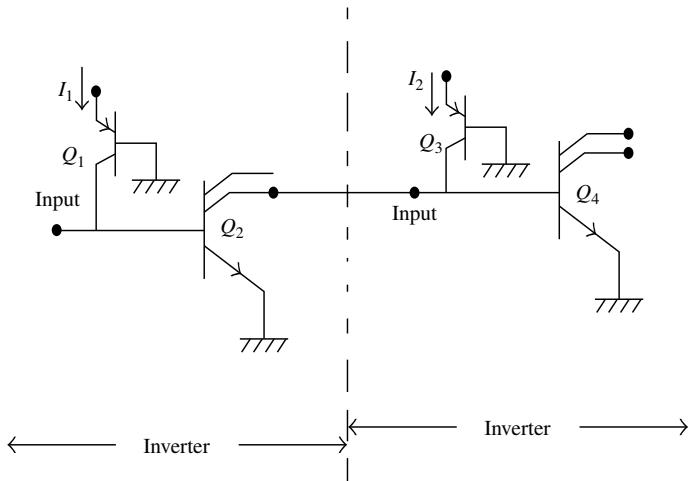
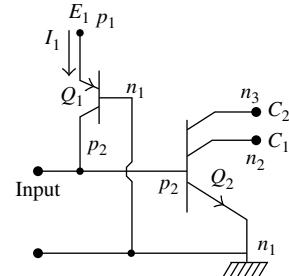


FIGURE 10.31 The two inverters connected in cascade

FIGURE 10.32 p and n regions are common for Q_1 and Q_2

In the manufacture of IC, if Q_1 and Q_2 share the common regions of p -type and n -type materials then these two transistors are said to be merged, as shown in Fig. 10.32.

As the base Q_1 and the emitter of Q_2 are n -type materials, a merged n -region (n_1) is used for both. Similarly, the collector of Q_1 and the base of Q_2 are p -type materials, a merged p -region (p_2) is used for both. The cross section of the above transistor gate is shown in Fig. 10.33.

By providing smaller currents I_1 and I_2 , the power dissipation can be minimized. However, this accounts for a slower switching speed.

10.4.2 PMOS and NMOS Logic Gates

The major advantages of MOSFET devices are their very large input resistance, negligible power dissipation and a very small area for fabrication. Only FETs—no resistors, diodes or capacitors—are used. This is an example of direct coupled transistor logic (DCTL). We already know that an n -channel MOSFET is normally

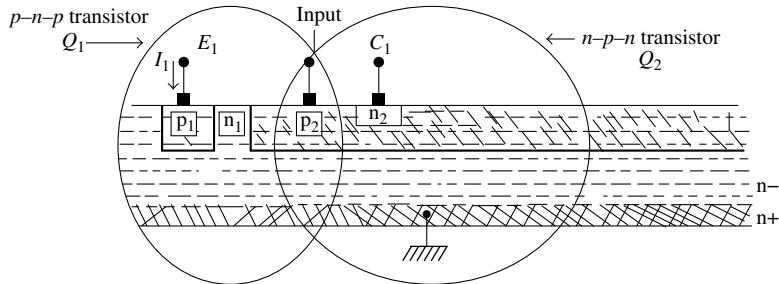


FIGURE 10.33 The cross-section of inverter where transistors replace resistors

OFF when $V_{GS} = 0$ and is ON when V_{GS} is positive. Similarly a *p*-channel MOSFET is OFF when $V_{GS} = 0$ and is ON when V_{GS} is negative.

p-channel MOSFETs are used in PMOS gates and *n*-channel MOSFETs are used in NMOS gates. These gates are similar except for the polarities of the supply voltages and direction of currents. However, NMOS gates are faster than PMOS gates because of the greater mobility of *n*-type charge carriers.

NMOS NAND Gates. NMOS NAND gate is shown in Fig. 10.34(a). The ON resistance, R_{on} of Q_1 is typically 100 k Ω and that of Q_2 and Q_3 is of the order by 1 k Ω .

When both the inputs V_1 and V_2 are high (Q_2 and Q_3 conduct when the voltages at their gates are positive) Q_2 and Q_3 are ON. Q_1 is also ON because its gate is tied to V_{DD} . The resultant circuit is as shown in Fig. 10.34(b).

Hence, V_o is low. Consider the following cases:

1. When V_1 is low and V_2 is high, Q_2 is OFF, Q_3 is ON and hence, V_o is high.
 2. When V_1 is high and V_2 is low, Q_3 is OFF, Q_2 is ON and hence, V_o is high.
 3. When V_1 is low and V_2 is low, Q_2 is OFF, Q_3 is OFF and hence, V_o is high.

Hence, the NMOS circuit as shown in Fig. 10.34(a) is a NAND gate Fig. 10.34(b). The circuit shown in Fig. 10.34(c) is an NMOS NOR gate.

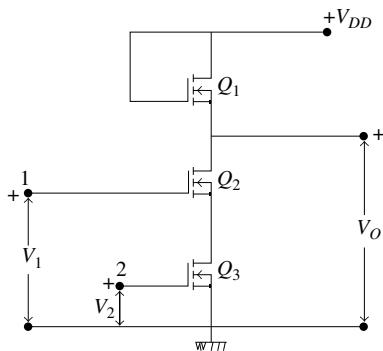


FIGURE 10.34(a) An NMOS NAND gate

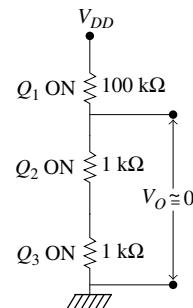


FIGURE 10.34(b) The resultant circuit when O_1 , O_2 and O_3 are ON

When both the inputs V_1 and V_2 are low, Q_2 and Q_3 are OFF. Hence, the output is high. When both the inputs V_1 and V_2 are high, Q_2 and Q_3 are ON and the output is low but, when V_1 or V_2 is high, Q_2 or Q_3 is ON and the output is low.

PMOS NAND and NOR gates are exactly similar to the NMOS counterparts except for the fact that the supply voltage is negative and the p -channel devices, which conduct when the gate voltage is negative, negative logic is employed.

PMOS NAND Gates. PMOS NAND gate is shown in Fig. 10.35(a). It is similar to its NMOS counterpart except for the fact that the supply voltage is negative. It employs negative logic.

Q_1 is ON as its gate is tied to -10V

- When both the inputs V_1 and V_2 are 1 ($= -10\text{ V}$), Q_2 and Q_3 are ON. $V_o = 0 (= 0\text{V})$.
- When both the inputs V_1 and V_2 are 0 ($= 0\text{ V}$), Q_2 and Q_3 are OFF. $V_o = 1 (= -10\text{ V})$.
- When $V_1 = 1 (= -10\text{ V})$ and $V_2 = 0 (= 0\text{ V})$, Q_2 is ON and Q_3 is OFF. $V_o = 1 (= -10\text{ V})$.
- When $V_1 = 0 (= 0\text{ V})$ and $V_2 = 1 (= -10\text{ V})$, Q_2 is OFF and Q_3 is ON. $V_o = 1 (= -10\text{ V})$.

The gate circuit in Fig. 10.35(a) is a NAND.

PMOS NOR Gates. PMOS NOR Gate is shown in Fig. 10.35(b). Q_1 is always ON as its gate is tied to -10V

- When both the inputs V_1 and V_2 are 1 ($= -10\text{ V}$), Q_2 and Q_3 are ON. $V_o = 0 (= 0\text{V})$.
- When both the inputs V_1 and V_2 are 0 ($= 0\text{ V}$), Q_2 and Q_3 are OFF. $V_o = 1 (= -10\text{ V})$.
- When $V_1 = 1 (= -10\text{ V})$ and $V_2 = 0 (= 0\text{ V})$, Q_2 is ON and Q_3 is OFF. $V_o = 0 (= 0\text{V})$.
- When $V_1 = 0 (= 0\text{ V})$ and $V_2 = 1 (= -10\text{ V})$, Q_2 is OFF and Q_3 is ON. $V_o = 1 (= 0\text{V})$.

The gate circuit in Fig. 10.35(b) is a NOR.

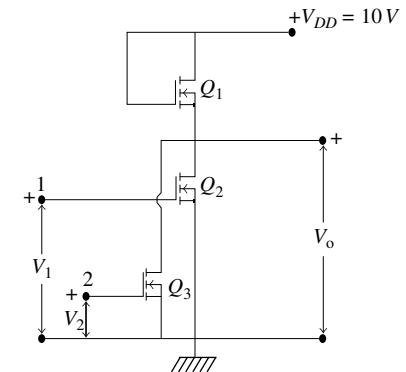


FIGURE 10.34(c) A NMOS NOR gate

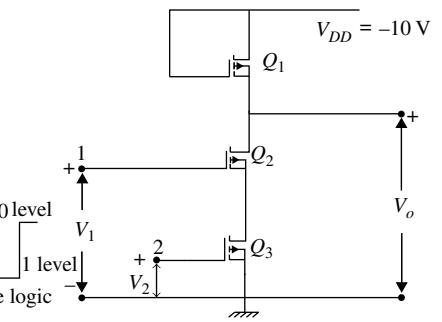


FIGURE 10.35(a) P-MOS NAND gate

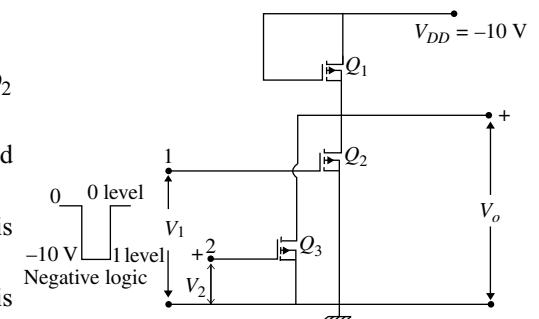


FIGURE 10.35(b) P-MOS NOR gate

10.4.3 Complementary MOSFET Logic Gates

When two devices are identical in every respect, except for the polarity of voltages and current directions, they are called complementary devices. Therefore, two MOSFETS, one of which is a p -channel device and the other

is an *n*-channel device, having identical parameters, are complementary devices. When these complementary devices are employed in a gate circuit the resulting gate is called a CMOS gate.

CMOS NAND Gates. Consider the CMOS NAND gate shown in Fig. 10.36(a). Here, Q_1 and Q_2 are PMOS devices and Q_3 and Q_4 are NMOS devices. Let us see the following conditions:

- (i) When V_1 and V_2 are low (grounded):

Here, the gates of Q_1 and Q_2 are negative with respect to the source terminals. Hence, Q_1 and Q_2 are ON as they are PMOS devices, whereas Q_3 and Q_4 are OFF as they are NMOS devices. Hence, the output is high, as shown in Fig. 10.36(b).

$$V_1 = V_2 = 0, \quad Q_1 \text{ and } Q_2 \text{ are ON, } Q_3 \text{ and } Q_4 \text{ are OFF, } V_o = 1.$$

- (ii) When V_2 is high and V_1 is low:

With V_2 high, Q_4 is ON and Q_2 is OFF. However, with V_1 low, Q_3 is OFF and Q_1 is ON. Therefore, the output is high, as shown in Fig. 10.36(c).

$$V_1 = 0, V_2 = 1, \quad Q_2, Q_3 \text{ are OFF and } Q_1, Q_4 \text{ is ON, } V_o = 1.$$

- (iii) When V_1 is high and V_2 is low:

With V_1 high, Q_3 is ON and Q_1 is OFF. However, when V_2 is low, Q_4 is OFF and Q_2 is ON. Therefore, the output once again is high, as shown in Fig. 10.36(d).

$$V_1 = 1, V_2 = 0, \quad Q_1 \text{ is OFF, } Q_2 \text{ and } Q_3 \text{ are ON and } Q_4 \text{ is also OFF, } V_o = 1.$$

- (iv) When the inputs V_1 and V_2 are high:

With V_2 high, Q_2 is OFF and Q_4 is ON. With V_1 high, Q_1 is OFF and Q_3 is ON. Hence, the output is low, as shown in Fig. 10.36(e).

$$V_1 = 1, V_2 = 1, \quad Q_1 \text{ and } Q_2 \text{ are OFF, } Q_3 \text{ and } Q_4 \text{ are ON, } V_o = 0$$

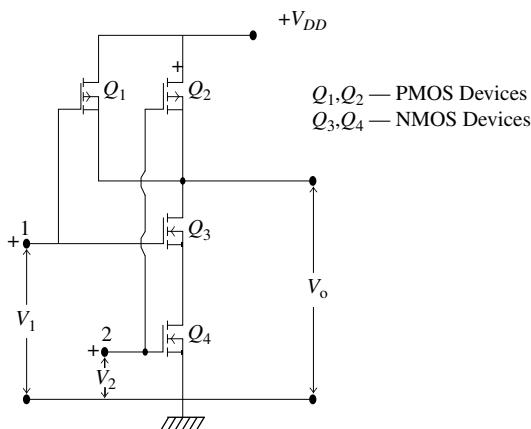


FIGURE 10.36(a) A CMOS NAND gate

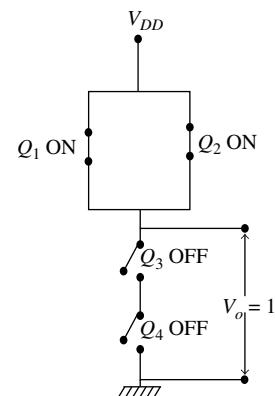


FIGURE 10.36(b) The equivalent circuit when V_1 and V_2 are low

CMOS NOR Gates.

(i) CMOS NOR gate is shown in Fig. 10.37(a). Q_1 and Q_2 are *p*-channel devices and Q_3 and Q_4 are *n*-channel devices. Consider the following conditions: When $V_1 = 0$ and $V_2 = 0$:

When $V_1 = 0$, Q_1 is ON and Q_3 is OFF and when $V_2 = 0$, Q_2 is ON and Q_4 is OFF then, $V_o = 1$, as shown in Fig. 10.37(b).

(ii) When $V_1 = 0$ and $V_2 = 1$:

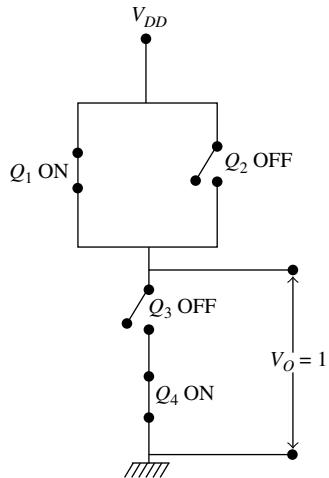


FIGURE 10.36(c) The equivalent circuit when V_1 is low and V_2 is high

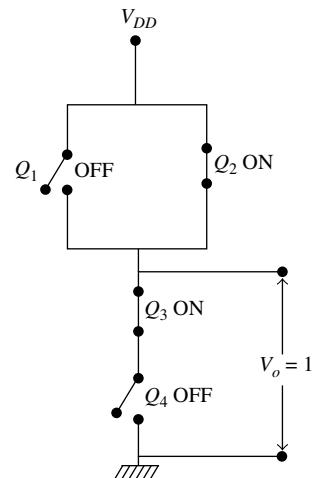


FIGURE 10.36(d) The equivalent circuit when V_1 is high and V_2 is low

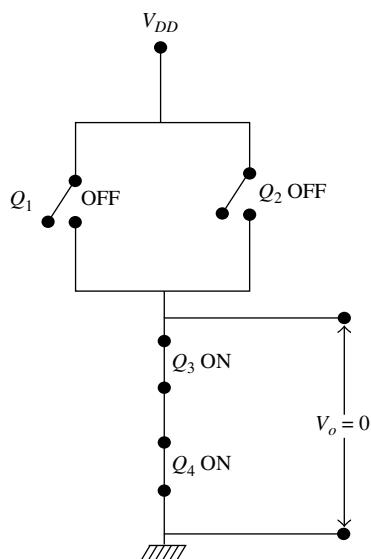


FIGURE 10.36(e) The equivalent circuit when V_1 and V_2 are high

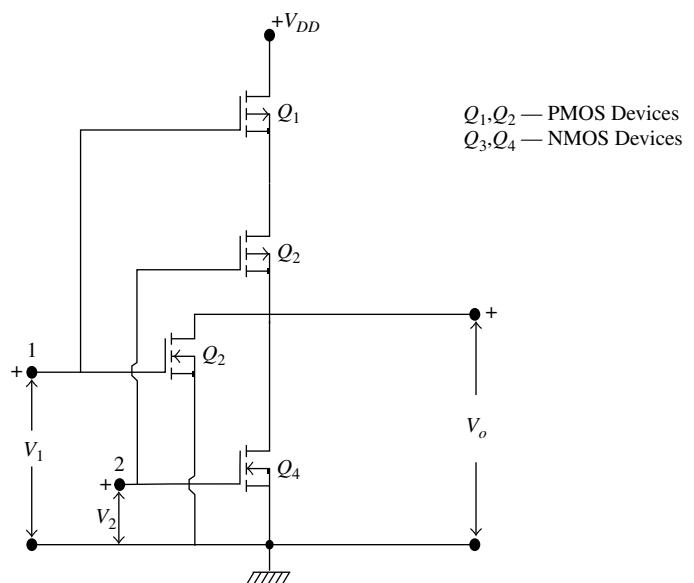


FIGURE 10.37(a) A CMOS NOR gate

When $V_1 = 0$, Q_1 is ON, Q_3 is OFF and when $V_2 = 1$, Q_2 is OFF and Q_4 is ON; then $V_o = 0$, as shown in Fig. 10.37(c).

(iii) When $V_1 = 1$ and $V_2 = 0$:

When $V_1 = 1$, Q_1 is OFF and Q_3 is ON and when $V_2 = 0$, Q_2 is ON and Q_4 is OFF; then $V_o = 0$, as shown in Fig. 10.37(d).

(iv) When $V_1 = 1$ and $V_2 = 1$:

When $V_1 = 1$, Q_1 is OFF and Q_3 is ON and when $V_2 = 1$, Q_2 is OFF and Q_4 is ON; then $V_o = 0$, as shown in Fig. 10.37(e).

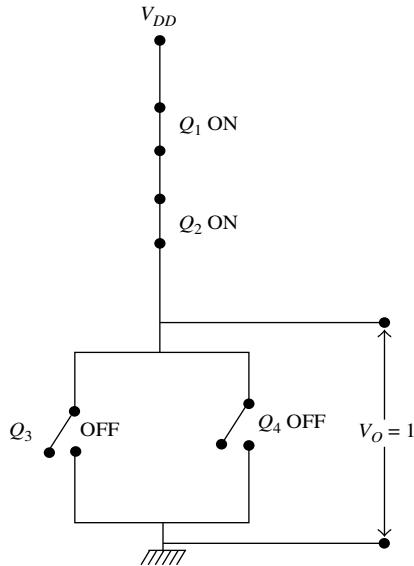


FIGURE 10.37(b) The equivalent circuit when V_1 and V_2 are low

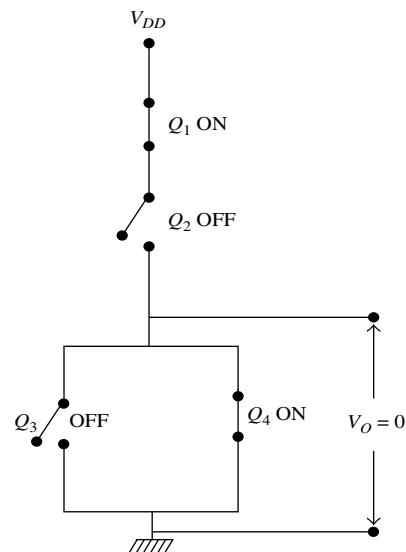


FIGURE 10.37(c) The equivalent circuit when V_1 is low and V_2 is high

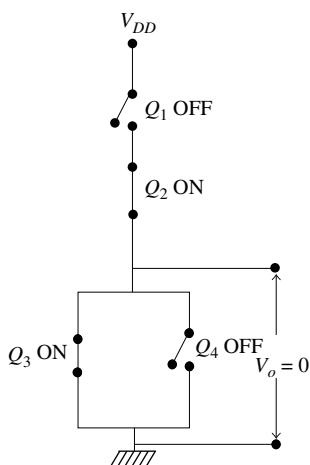


FIGURE 10.37(d) The equivalent circuit when V_1 is high and V_2 is low

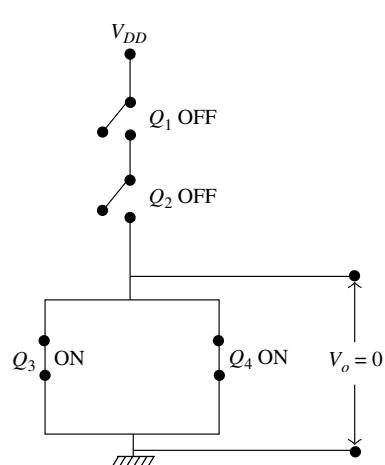


FIGURE 10.37(e) The equivalent circuit when V_1 and V_2 are high

CMOS devices must be handled properly as these can be destroyed by static electricity. The major advantage of CMOS is lesser power dissipation, larger fan-out and excellent noise immunity. The comparison of major IC logic families is shown in Table 10.6.

10.4.4 Interfacing of Logic Gates

When the output of a logic gate is required to drive another logic gate of a different family, then the logic 0 and 1 levels of the driving gate should be compatible with 0 and 1 levels of the driven gate, essentially because of the fact that the supply voltages of these two logic families could be different, also the currents could be different. This process of translation is called interfacing. Input and output voltage and current levels for standard TTL and CMOS logic gates are shown in Table 10.7.

When TTL Gate is Driving a CMOS Gate Operated with the same Supply Voltage. Supply voltage in both the cases is 5 V. Consider a TTL gate with totem-pole output driving a CMOS gate, as shown in Fig. 10.38(a). This is redrawn, representing the output of TTL gate driving the CMOS input shown in Fig. 10.38(b).

This is redrawn, representing the output of a TTL gate driving the CMOS input shown in Fig. 10.38(b).

We know that $V_{OL(max)}$ for TTL gate is 0.4 V and $V_{IL(max)}$ for a CMOS gate is 1.5 V. Hence, the logic 0 level is compatible. However, $V_{IH(min)}$ of CMOS gate (for 5 V supply) is 3.5 V i.e., $V_{OH(min)}$ of TTL is much smaller than $V_{IH(min)}$ of the CMOS gate. Hence, the TTL output must be raised to the acceptable level of CMOS and connecting a pull up resistor R_C does this. When Q_4 is OFF and $V_{OH(min)} \approx V_{CC} = 5$ V, $V_{IH(min)}$ being 3.5 V, this satisfies the input requirement.

TABLE 10.6 A comparision of the performance of logic families

Logic family	RTL	DTL	74 (TTL)	ECL	NMOS and PMOS	CMOS	I^2L
Characteristic							
Propagation delay (ns)	12	30	10	2	50 – 100	25	≈ 10 –250, depends on injection current
Power dissipation per gate (mW)	15	15	10	25	0.25	10^{-6}	≈ 6 nW– 70μ W, depends on injection current
Noise margin (V)	0.7	1.4	0.4	0.25	2	$0.3 V_{DD}$	0.25
Noise immunity rating	Poor	Good	Good	Fair	Excellent	Excellent	Fair
Fan-out	5	8	10	25	>50	>50	Depends on injection current

TABLE 10.7 The input and output voltages and current levels for standard TTL and CMOS logic gates

	$V_{IH(min)}$	$V_{IL(max)}$	$V_{OH(min)}$	$V_{OL(max)}$	$I_{IH(max)}$	$I_{IL(max)}$	$I_{OH(max)}$	$I_{OL(max)}$
Standard TTL	2 V	0.8 V	2.4 V	0.4 V	40 μ A	1.6 μ A	400 μ A	16 mA
CMOS (5 V)	3.5	1.5	5	0	0	0	-	-
CMOS (15 V)	11	4.5	15	0	0	0	-	-

TTL Driving a CMOS Gate with 15 V Supply. From the Table 10.7, $V_{IH(min)}$ of CMOS 15 V gate is 11 V and $V_{OH(min)}$ of CMOS is 15 V. As the TTL output cannot be pulled to 15 V, an open collector buffer is used to interface the output of the TTL gate with a totem-pole output and a CMOS gate operating at 15 V as shown in Fig. 10.39.

Alternately, a dc-level translator can be used to interface the output of a TTL gate with the input of the CMOS gate operated at a higher voltage, as represented in Fig. 10.40.

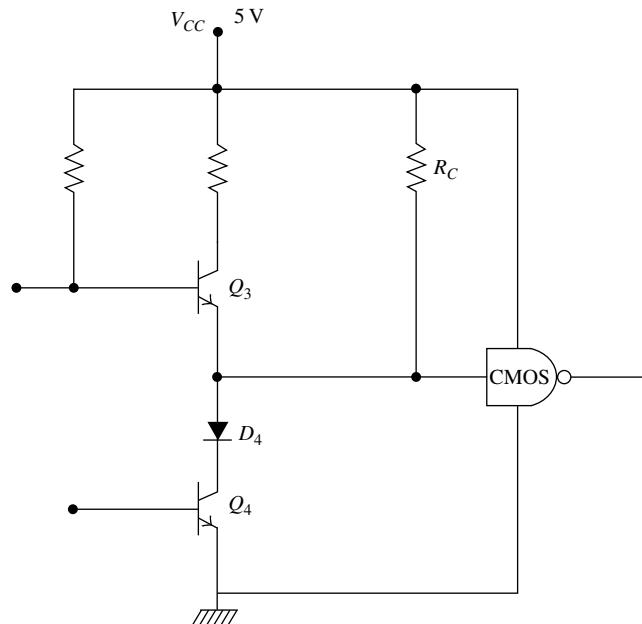


FIGURE 10.38(a) A TTL gate driving a CMOS gate

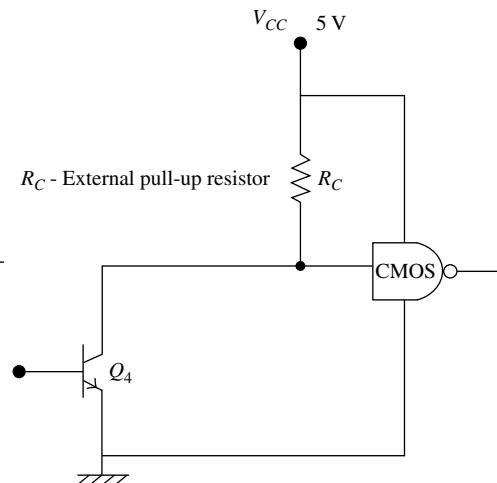


FIGURE 10.38(b) A modified TTL gate driving CMOS gate

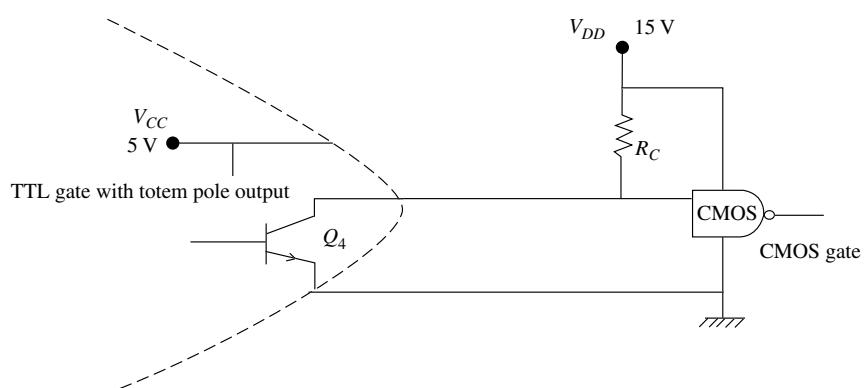


FIGURE 10.39 The logic gate interfacing the output of a TTL gate with a 15 V CMOS input

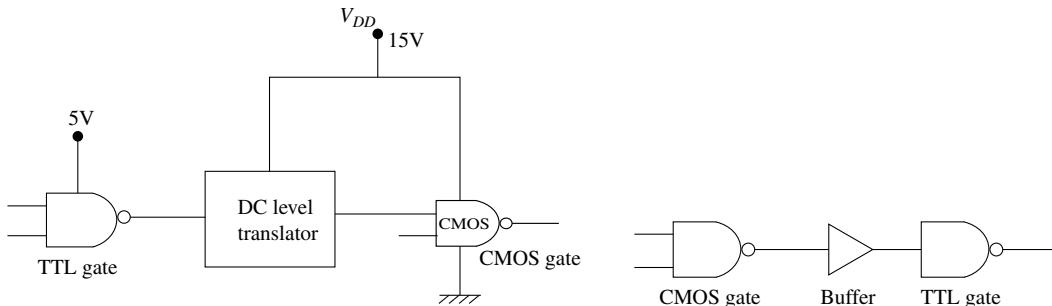


FIGURE 10.40 A TTL gate interfacing using a level translator

FIGURE 10.41 A CMOS gate driving a TTL gate

CMOS Gate Driving a TTL Gate. V_{OL} of CMOS satisfies the V_{IL} of a TTL gate. As the TTL input current is high and the CMOS output current is low, this may not be sufficient to drive the TTL gate. In such a case a buffer is used as an interface that can deliver the required TTL current as shown in Fig. 10.41.

S O L V E D P R O B L E M S

Example 10.6: Estimate suitable maximum logic 0 and minimum logic 1 input levels for the RTL gate in Fig. 10.42 with $V_{CC} = 5\text{ V}$, $R_C = 1\text{k}\Omega$, $R_B = 2\text{k}\Omega$ and $h_{FE} = 20$.

Solution: From Fig. 10.42

$$I_C = \frac{V_{CC} - V_{CE(\text{sat})}}{R_C} = \frac{5 - 0.2}{1\text{k}\Omega} = 4.8 \text{ mA} \quad I_B = I_{IH(\text{min})} = \frac{I_C(\text{sat})}{h_{FE}} = \frac{4.8}{20} = 0.24 \text{ mA}$$

$$V_{IH(\text{min})} = V_{BE} + I_{IH(\text{min})}R_B \quad V_{IH(\text{min})} = 0.7 + 0.24 \times 10^{-3} \times 2 \times 10^3 = 1.18 \text{ V}$$

$$V_{IL(\text{max})} = 0.2\text{V}$$

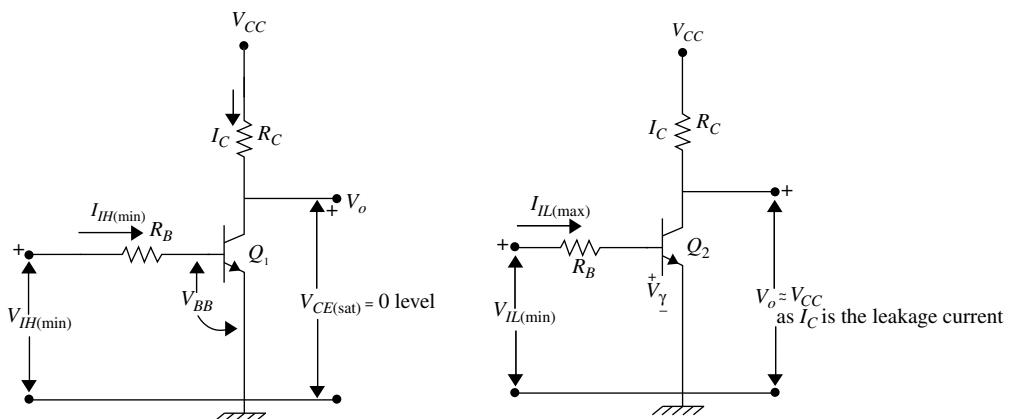


FIGURE 10.42 RTL gate with minimum high input and max low input voltages

Example 10.7: Determine the loading factor for the DTL gate in Fig.10.43 with $h_{FE} = 25$ Assume that Germanium transistors and diodes are used.

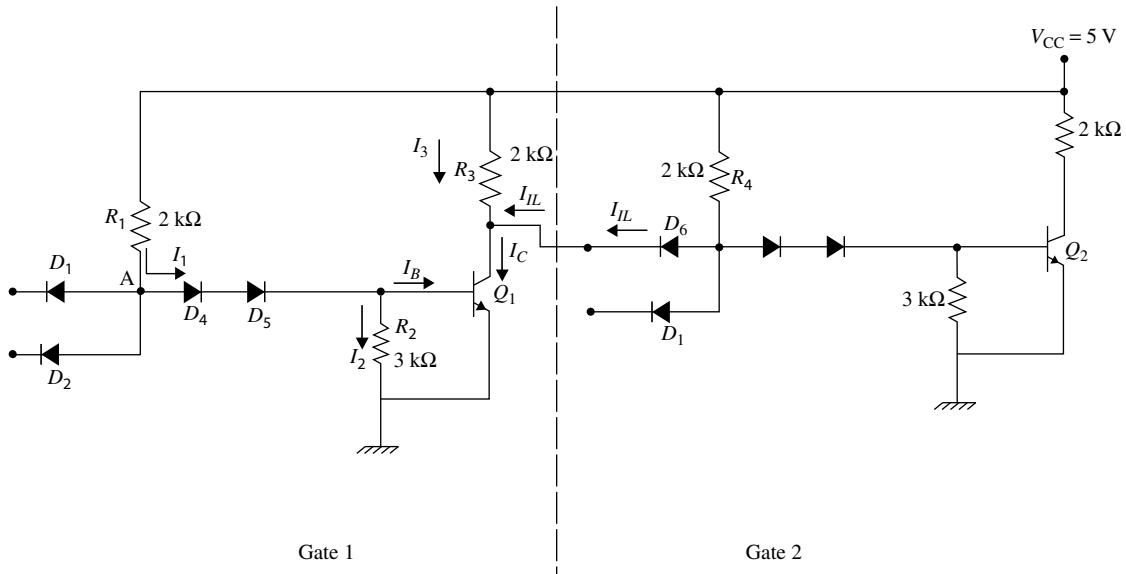


FIGURE 10.43 DTL NAND gate output is connected to the one inputs of another gate

Solution: From the Fig.10.43

$$I_2 = \frac{V_{BE1}}{R_2} = \frac{0.3}{3 \text{ k}\Omega} = 0.1 \text{ mA}$$

$$V_A = V_{F4} + V_{F5} + V_{BE1} = 0.3 + 0.3 + 0.3 = 0.9 \text{ V}$$

$$I_1 = \frac{V_{CC} - V_A}{R_1} = \frac{5 - 0.9}{2 \text{ k}\Omega} = 2.05 \text{ mA}$$

$$I_B = I_1 - I_2 = 2.05 - 0.1 = 1.95 \text{ mA}$$

$$I_{C1} = h_{FE} I_B = 25 \times 1.95 \times 10^{-3} = 48.75 \text{ mA}$$

$$I_3 = \frac{V_{CC} - V_{CE(\text{sat})}}{R_3} = \frac{5 - 0.1}{2 \text{ k}\Omega} = 2.45 \text{ mA}$$

The maximum low level output current $I_{OL} = I_{C1} - I_3 = 48.75 - 2.45 = 46.3 \text{ mA}$

When Q_2 OFF, signal load current $I_{IL} = \frac{V_{CC} - V_{F6}}{R_4} = \frac{5 - 0.3}{2 \text{ k}\Omega} = 2.35 \text{ mA}$

$$\text{Fan-out=Loading factor} = \frac{I_{OL}}{I_{IL}} = \frac{46.3}{2.35} = 19.70 \approx 19$$

Example 10.8: The wired AND gate is required to drive the inputs of three standard TTL gates, shown in Fig. 10.44, which have $V_{cc} = 5V$, $I_{IL(max)} = 1.6\text{ mA}$ and $I_{OL(max)} = 16\text{ mA}$ and $V_{OL(max)} = 0.4V$. Determine a suitable pull-up resistance.

Solution: Total load current for three gates $I_L = 3 \times I_{L(\max)} = 3 \times 1.6 \text{ mA} = 4.8 \text{ mA}$ Let us assume only one wired AND gate is ON

$$I_{RL} = I_{OL(\max)} - I_L = 16 - 4.8 = 11.2 \text{ mA}$$

$$V_{RL} = V_{CC} - V_{OL(\max)} = 6 - 0.4 = 5.6 \text{ V}$$

$$R_L = \frac{V_{RL}}{I_{RL}} = \frac{5.6}{11.2 \times 10^{-3}} = 500 \Omega$$

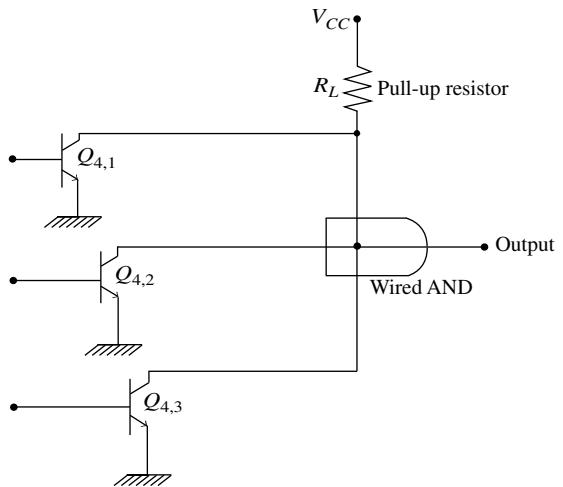


FIGURE 10.44 Wired AND gate

Example 10.9: Design a suitable interface circuit for CMOS, shown in Fig.10.45 with $C_{DD} = 5$ V, driving two standard TTL gates with $V_{CC} = 5$ V, $h_{FE(\min)}$ of $Q_1 = 30$ and $R_D(\text{ON}) = 1\text{ k}\Omega$. Given $V_{IH(\min)} = 2$ V, $I_{IL(\max)} = 1.6$ mA and $I_{IH(\max)} = 40$ μ A.

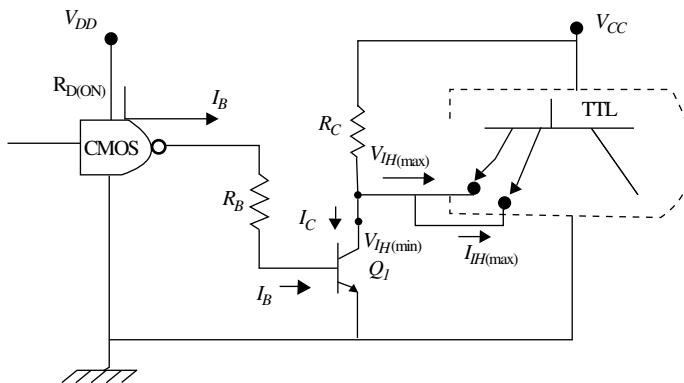


FIGURE 10.45 Interface circuit for CMOS to drive two standard TTL gates

$$Solution: R_C = \frac{V_{CC}V_{IH(\min)}}{2I_{IH(\max)}} = \frac{5 - 2}{2 \times 40 \times 10^{-6}} = 37.5 \text{ k}\Omega$$

The standard value is 33 k Ω

$$I_{C(\max)} = \frac{V_{CC} - V_{CE(\text{sat})}}{R_C} + 2I_{IL(\max)} = \frac{5 - 0.2}{33 \times 10^3} + 2 \times 1.6 \times 10^{-3} = 3.34 \text{ mA}$$

$$I_B = \frac{I_{C(\max)}}{h_{FE(\min)}} = \frac{3.34}{30} = 0.111 \text{ mA}$$

$$R_D(ON) + R_B = \frac{V_{DD} - V_{BE}}{I_B} = \frac{5 - 0.7}{0.111 \times 10^{-3}} = 38.7 \text{ k}\Omega$$

$$R_B = 38.7 - 1 = 37.7 \text{ k}\Omega \approx 33 \text{ k}\Omega \text{ (standard value)}$$

SUMMARY

- TTL gates operate with a supply voltage of 5 V whereas a CMOS gates operate with supply voltages ranging from 1 to 30 V.
- $V_{IH(\min)}$ of a gate is the minimum high-input voltage that represents a logic 1 level at the input.
- $V_{IL(\max)}$ of a gate is the maximum low-input voltage that represents a logic 0 level at the input.
- $I_{IH(\min)}$ of a gate is the minimum high-input current sufficient enough to drive the transistor into saturation.
- $I_{IL(\max)}$ is the maximum current that flows into an input when $V_{IL(\max)}$ is applied as an input.
- $I_{OH(\max)}$ is the maximum high-level output current through the load and $V_{OH(\min)}$ is the minimum output voltage for a logic 1 level.
- $I_{OL(\min)}$ is the minimum low-level output current through the load and $V_{OL(\max)}$ is the maximum output voltage for a logic 0 level.
- Fan-out of a gate is the number of inputs of the identical gates that a gate can drive.
- Fan-in is the number of inputs of a gate.
- Propagation delay is the time required for a gate to switch from a low-output state to a high-output state and vice-versa.
- Noise immunity is the ability of the logic gate to tolerate changes at the input due to the noise but be still able to deliver the predictable output.
- Power dissipation is the amount of power that is lost in heating the gate.
- The figure of merit of a gate is the product of propagation delay and average power dissipation.
- A tri-state logic gate allows the output to be low, high or offer high output impedance.
- I^2L or merged transistor logic (MTL) can provide larger circuit density as common regions of p -type and n -type are merged in fabricating the IC.
- When the output of one logic gate is required to drive the input of another logic gate, the 0 and 1 levels of the driving gate should be compatible with the 0 and 1 levels of the driven gate. This process of translation is called interfacing of logic gates.

MULTIPLE CHOICE QUESTIONS

- (1) The maximum number of inputs of many similar logic gates that any one gate output can drive is called:
 - Fan-in
 - Fan-out
 - Noise immunity
 - Noise margin
- (2) The maximum number of inputs a logic gate has is called:
 - Fan-out
- (b) Fan-in
- (c) Figure of merit
- (d) Totem-pole output
- (3) The time required for a logic gate to switch from a low output state to a high output state and vice-versa is called as:
 - Propagation delay
 - Rise time
 - Transition time
 - Turn-on time

- 4) Noise immunity is normally specified as:
 (a) Excellent or good or fair or poor
 (b) 100 per cent
 (c) 1/10 of the total noise
 (d) None of the above
- 5) NAND and NOR gates are called:
 (a) Bidirectional gates
 (b) Unilateral gates
 (c) Universal gates
 (d) High level logic gates
- 6) A logic gate that allows the output to be 0, 1 or offers high impedance is called a:
 (a) Tri-state logic gate
 (b) NAND gate
 (c) NOR gate
 (d) DTL gate
- 7) In an ECL gate, as the ON device is not driven into saturation, the advantage is:
 (a) Lesser power dissipation
 (b) Lower propagation delay
 (c) Better noise immunity
 (d) None of the above
- 8) In I^2L logic gates, as the transistors are merged, the major resultant advantage of this family is:
- 9) CMOS gates are preferred because of their:
 (a) Greater circuit density
 (b) Better noise immunity
 (c) Poor propagation delay
 (d) Greater power dissipation
- 9) CMOS gates are preferred because of their:
 (a) Lesser power dissipation
 (b) Faster switching speed
 (c) Manufacturing process is simple
 (d) Weight is less
- 10) TTL gates are preferred because of their:
 (a) Lesser power dissipation
 (b) Faster switching speed
 (c) Manufacturing process is simple
 (d) Weight is less
- 11) If the output of one family of logic gate is required to drive the input of another family of logic gate, 0 and 1 levels of the driving and the driven gate should be made compatible by a process of translation called:
 (a) Interfacing
 (b) Coupling
 (c) Amplification
 (d) Rectification

SHORT ANSWER QUESTIONS

1. Explain how to calculate the propagation delay of a logic gate.
2. What do you understand by the term noise immunity of a logic gate?
3. Explain the terms high state noise margin and low state noise margin.
4. What is meant by the figure of merit of a logic gate?
5. Draw the circuit of a DTL NOR gate and explain its working.
6. Draw the circuit of a DTL NAND gate and explain its working.
7. What is meant by tri-state logic?
8. What is the major advantage of an ECL gate?
9. What is the major advantage of an I^2L gate?
10. Explain, in what respect, CMOS gates are preferred over TTL gates.
11. Explain the process of interfacing the logic gates of different families.

LONG ANSWER QUESTIONS

1. Draw the circuit of a TTL NAND gate with totem-pole output and explain its working. What is its main disadvantage?
2. Draw the circuit of a TSL NAND gate and explain its working.
3. Draw the circuit of an ECL OR / NOR gate. Verify its truth table.
4. What is I^2L logic? Explain how merging of transistors takes place in the manufacturing of this type of gate.
5. Draw the circuits of PMOS NAND and NMOS NOR gates and verify their truth tables.
6. Draw the circuits of CMOS NAND and NOR gates and explain their working with the help of the truth tables.
7. Compare the performance of different logic families.

8. What is meant by interfacing of logic gates? Suggest interfacing methods when:
- A TTL gate drives a CMOS gate with an operating voltage of 15 V.

- A CMOS gate with an operating voltage of 30 V drives a TTL gate.

UNSOLVED PROBLEMS

- (1) Verify that the RLT gate in Fig.10p.1 is a NOR gate

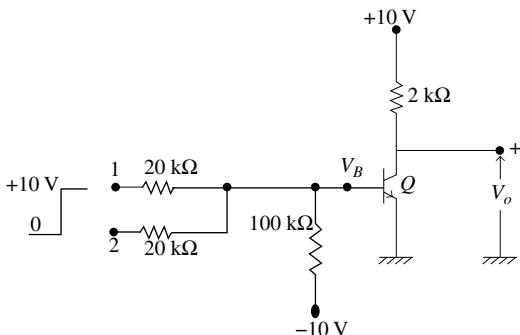


FIGURE 10P.1 RTL NOR gate

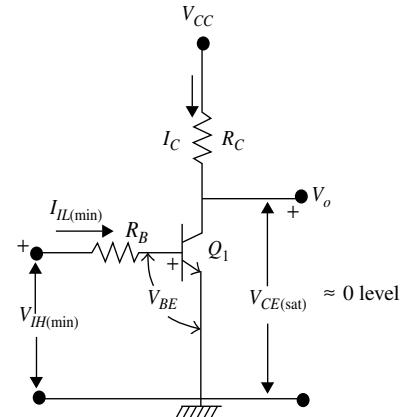


FIGURE 10P.3 RTL gate

- (2) (a) Verify that the circuit in Fig.10p.2 is a DTL positive NAND gate. Given $V_{CC} = V = 10$ V, $V_{BB} = 10$ V, $R_C = 2$ kΩ, $R_1 = 100$ kΩ and $h_{FE} = 30$; the input varies between 0 and 10V. Neglect the junction voltages (b) Also determine the loading factor.

- (4) (a) Verify that the circuit in Fig.10p.4 is a DTL positive NOR gate. Given $V_{CC} = 10$ V, $V_{BB} = 10$ V, $R_C = 2$ kΩ, $R_1 = 100$ kΩ, $R_2 = 200$ kΩ and $h_{FE} = 20$ and the input between 0 and 10 V. Neglect junction voltages. (b) Determine I_{OL} , I_{IL} and the loading factor.

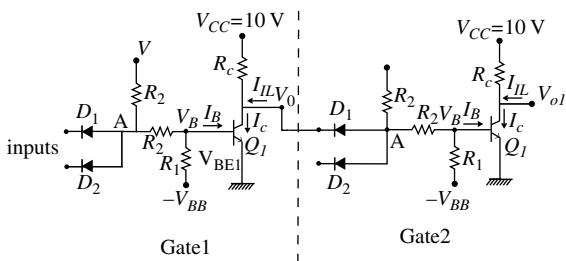


FIGURE 10P.2 DTL Positive NAND gate

- (3) The RTL gate shown in Fig.10p.3 has $V_{CC} = 9$ V, $V_{IL(\max)} = 0.2$ V, $V_{IH(\min)} = 2$ V, $I_{C(\max)} = 2$ mA and $h_{FE} = 40$. Calculate suitable resistance values for R_B and R_C .

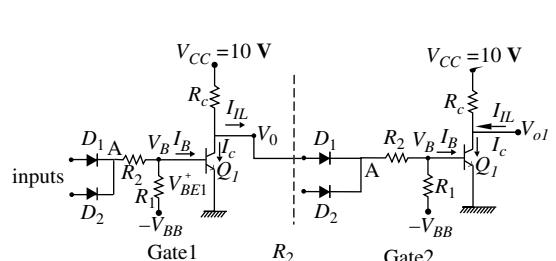


FIGURE 10P.4 RTL gate

- (5) Determine I_{OL} , I_{IL} and the loading factor for the DTL gate in Fig.10p.5. Assume that silicon transistors and diodes are used. The transistors have $h_{FE} = 20$.

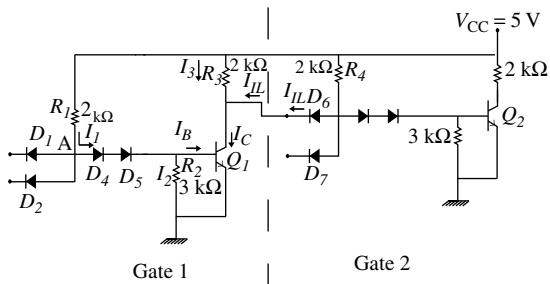


FIGURE 10P.5 RTL gate

- (6) Design a suitable interface circuit for CMOS (see Fig. 10p.6) with $V_{DD} = 15$ V, driving three standard TTL gates with $V_{CC} = 10$ V, $h_{FE(\min)}$ of $Q_1 = 30$ and

$R_{D(ON)} = 1 \text{ k}\Omega$. Given $V_{IH(\min)} = 2 \text{ V}$, $I_{IL(\max)} = 1.6 \text{ mA}$ and $I_{IH(\max)} = 40 \mu\text{A}$.

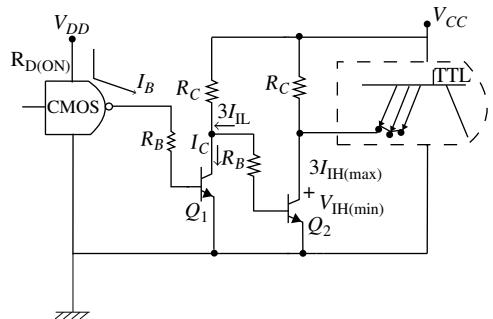


FIGURE 10P.6 RTL gate

Sampling Gates

LEARNING OBJECTIVES

After reading this chapter you will be able to:

- Understand the working of unidirectional and bidirectional sampling gates and their variations
- Describe the output by adjusting the levels of the control signal
- Derive a chopper stabilized amplifier using sampling gates
- Realize the application of sampling gates in sampling scope

11.1 INTRODUCTION

A sampling gate is a transmission circuit that faithfully transmits an input signal to the output for a finite time duration which is decided by an external signal, called a gating signal (normally rectangular in shape), as shown in Fig. 11.1.

The input appears without a distortion at the output, but is available for a time duration T and afterwards the signal is zero. They can transmit more number of signals. The main applications of the sampling gates are: (i) multiplexers; (ii) choppers; (iii) D/A converter; (iv) sample and hold circuits, etc.

Sampling gates can be of two types:

1. Unidirectional gates: These gates transmit the signals of only one polarity.
2. Bidirectional gates: These gates transmit bidirectional signals (i.e., positive and negative signals).

Earlier, we had seen logic gates in which the output, depending on the input conditions, is either a 1 level or a 0 level. That is, the inputs and outputs are discrete in nature. In a sampling gate, however, the output is a faithful replica of the input. Hence, sampling gates are also called linear gates, transmission gates or time selection circuits. Linear gates can use either a series switch, as shown in Fig. 11.2(a) or a shunt switch, as shown in Fig. 11.2(b). In Fig. 11.2(a), only when the switch closes, the input signal is transmitted to the output. In Fig. 11.2(b), only when the switch is open the input is transmitted to the output.

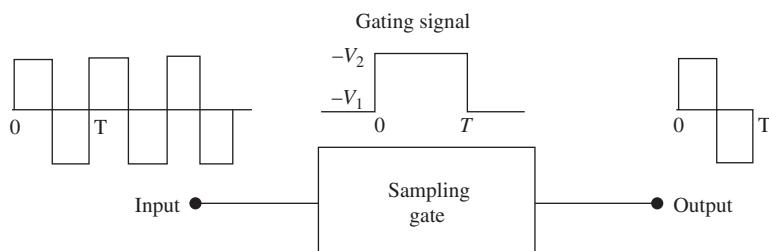


FIGURE 11.1 A sampling gate

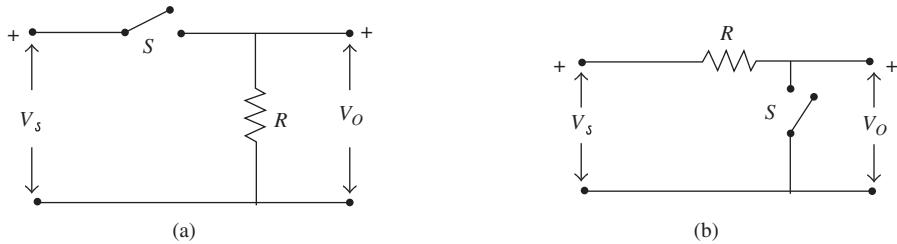


FIGURE 11.2 A linear gate (a) using a series switch; and (b) using a shunt switch

11.2 UNIDIRECTIONAL DIODE GATES

A unidirectional gate can transmit either positive or negative pulses (or signals) to the output. It means that this gate transmits pulses of only one polarity to the output. The signal to be transmitted to the output is the input signal. This input signal is transmitted to the output only when the control signal enables the gate circuit. Therefore, we discuss two types of unidirectional diode gates, namely, unidirectional diode gates that transmit positive pulses and unidirectional diode gates that transmit negative pulses.

11.2.1 Unidirectional Diode Gates to Transmit Positive Pulses

In order to transmit positive pulses, the unidirectional gate shown in Fig. 11.3 can be used. The gating signal is also known as a control pulse, selector pulse or an enabling pulse. It is a negative signal, whose magnitude changes abruptly between $-V_2$ and $-V_1$.

Consider the instant at which the gating signal is $-V_1$, which is a reasonably large negative voltage. As a result, D is OFF. Even if a positive input pulse is present when the gating signal with value $-V_1$ is present, the diode D remains OFF since the input may not be sufficiently large to forward-bias it. Hence, the output is zero.

Now consider the duration when the gate signal has a value $-V_2$ (smaller negative value) and when the input is also present (coincidence occurs). Assume that the control signal has peak-to-peak swing of 25 V and the signal has peak-to-peak swing of 15 V.

- (i) Let, for example, $-V_1 = -40$ V, $-V_2 = -15$ V and the signal amplitude be 15 V, as shown in Fig. 11.4(a). The net voltage at the anode of the diode, when the input is present for the duration of the gating signal, is 0. The diode is OFF and the output in this case is zero.

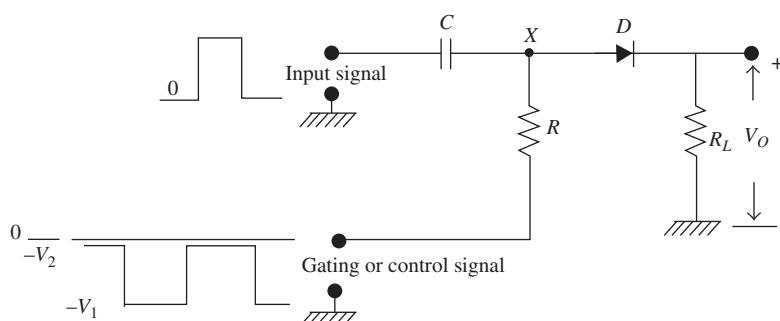


FIGURE 11.3 The unidirectional gate to transmit positive pulses

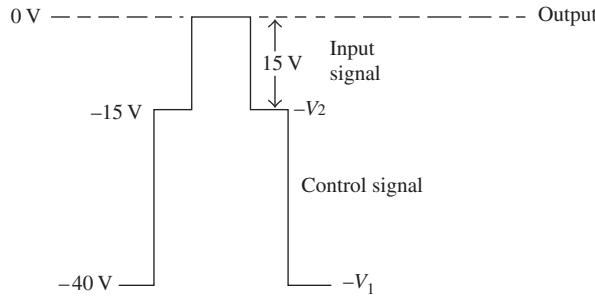


FIGURE 11.4(a) The control signal with $-V_1 = -40\text{ V}$, $-V_2 = -15\text{ V}$ and the input amplitude 15 V

- (ii) Now, change the levels to $-V_1 = -35\text{ V}$, $-V_2 = -10\text{ V}$ and the signal amplitude remains constant at 15 V , as shown in Fig. 11.4(b). Only when the input forward-biases the diode, there is an output. The output in this case is a pulse of amplitude 5 V (assuming an ideal diode). The duration of the output is the same as the duration of the input signal.
- (iii) Now let $-V_1 = -30\text{ V}$, $-V_2 = -5\text{ V}$ and the signal amplitude be 15 V , as shown in Fig. 11.4(c). As the signal above the zero level is 10 V , the output is a pulse of amplitude 10 V and has the same duration as the input.
- (iv) Let $-V_1 = -25\text{ V}$, $-V_2 = 0\text{ V}$ and the signal amplitude be 15 V , as shown in Fig. 11.4(d). The output in this case is 15 V and has the same duration as the input.
- (v) Let $-V_2 = +5\text{ V}$ and $-V_1 = -20\text{ V}$, as shown in Fig. 11.4(e). In this case, the output not only contains the input but also a portion of the control signal. The desired signal at the output is seen to be riding

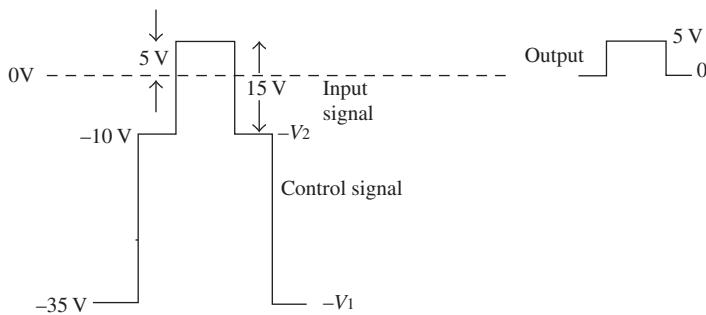


FIGURE 11.4(b) The control signal with $V_1 = -35\text{ V}$, $-V_2 = -10\text{ V}$ and the input amplitude 15 V

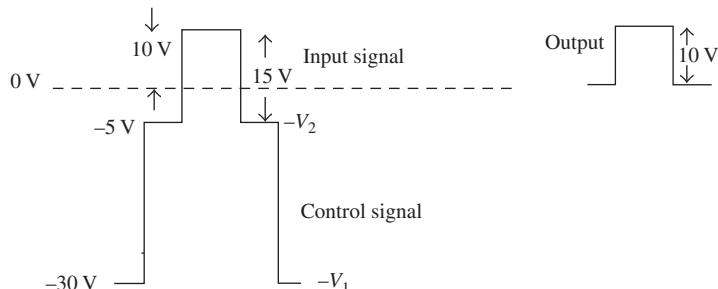
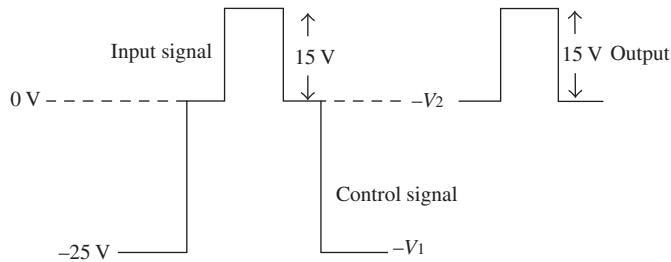
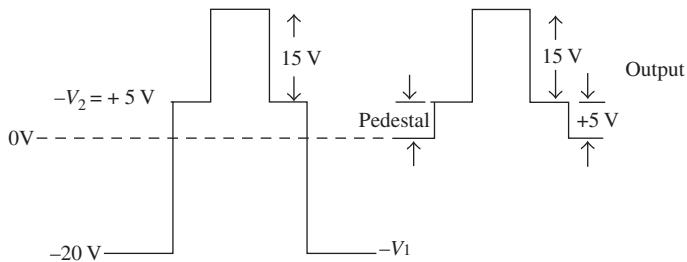


FIGURE 11.4(c) The control signal with $V_1 = -30\text{ V}$, $-V_2 = -5\text{ V}$ and the input amplitude 15 V

FIGURE 11.4(d) The control signal with $V_1 = -25$ V, $-V_2 = 0$ V and the input amplitude 15 VFIGURE 11.4(e) The control signal with $V_1 = -20$ V, $-V_2 = 5$ V and the input amplitude 15 V

over a pedestal. We see that the output of the gate changes by adjusting $-V_2$ and in the last case it is seen that the output is superimposed on a pedestal of 5 V. Thus, the output is influenced by the control signal.

For a gating signal, the RC network behaves as an integrator. Hence, the gate signal is not necessarily a rectangular pulse but rises and falls with a time constant RC . As a result, there is a distortion in the gate signal. However, if the duration of the input signal (a pulse) is much smaller than the duration of the gate, this distortion associated with the gating signal is not necessarily transmitted to the output; and the output is a sharp pulse as desired, provided the pedestal is eliminated, as shown in Fig. 11.4(f). On the contrary, if there is a pedestal, there is a corresponding distortion in the output, as shown in Fig. 11.4(g).

The advantages of unidirectional diode gates are: (i) they are simple to implement; (ii) have a negligible transmission delay; (iii) the gate draws no current in the quiescent condition; and (iv) by the proper modification of the circuit, more than one input signal can be transmitted through the gate circuit. However, there are two disadvantages of this arrangement. As the control signal and the input signal are directly connected at X

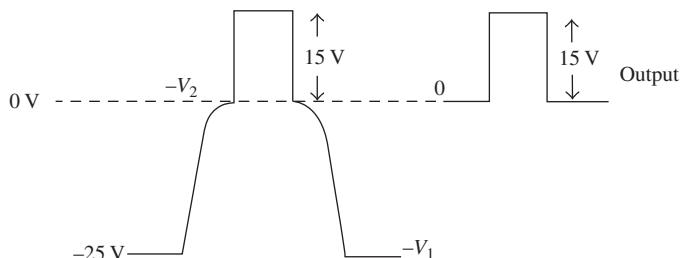


FIGURE 11.4(f) There is no distortion in the output though the control signal is distorted

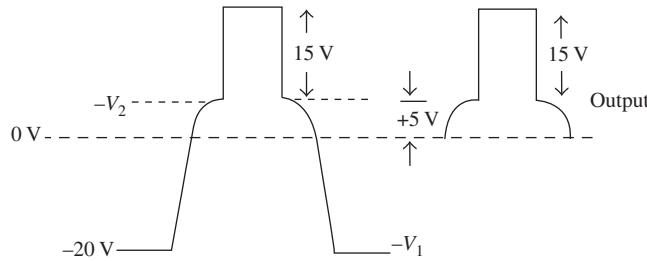


FIGURE 11.4(g) The distorted gate signal giving rise to a distorted pedestal

(see Fig. 11.3), there could be an interaction between these two sources. The time constant RC , if properly not chosen, can cause the distortion of the gate signal. A two-input unidirectional diode gate is shown in Fig. 11.5(a).

Let V_{s1} and V_{s2} be the pulses of amplitude 5 V. When both these signals appear at the input simultaneously, having the same duration, the output is shown in Fig. 11.5(b), when $-V_1 = -25$ V and $-V_2 = 0$.

When the control signal is at $-V_2 (= 0$ V), and if both the inputs are 0 the output is zero. When the inputs are above 0, the output is 5 V. However, when the control input is at $-V_1$ (-25 V), no output is available. This

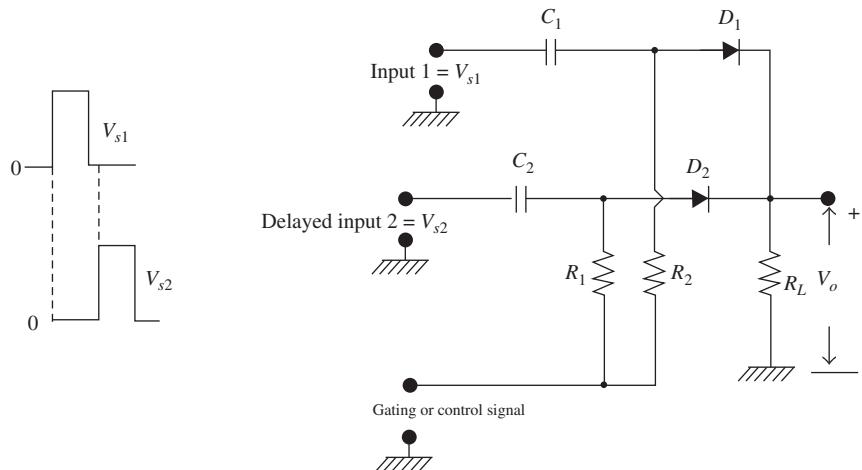


FIGURE 11.5(a) A unidirectional two-input diode gate

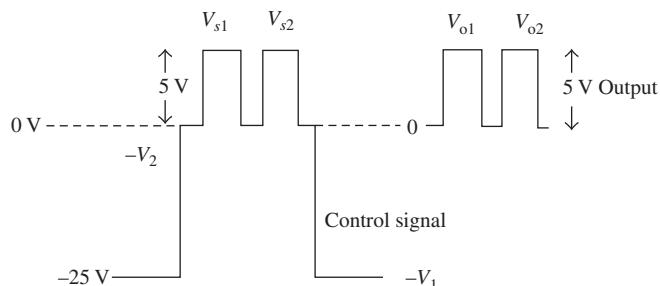


FIGURE 11.5(b) The waveforms of a two-input unidirectional gate

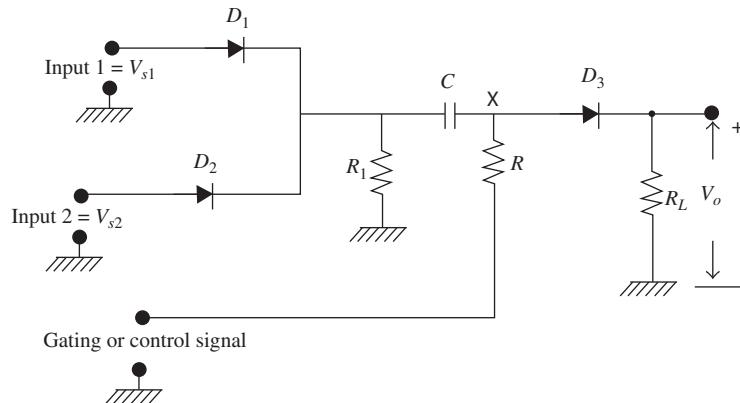


FIGURE 11.6 A two-input diode gate that avoids loading on the control signal

negative control signal inhibits the gate. Hence, this circuit is a two-input OR gate with $-V_1$ (-25 V) and inhibiting the gate operation. The waveforms shown in Fig. 11.5(b) suggest that time division multiplexing can be employed to simultaneously transmit a number of signals. The limitation of this arrangement is that signal sources may load the control input. To overcome this disadvantage, an arrangement in which the signal sources avoid loading the control input is suggested in Fig. 11.6. Here, the input signals are connected to point X through diodes D_1 and D_2 whereas the control source is connected at X directly to avoid interference and loading.

11.2.2 Unidirectional Diode Gates

- (i) **A unidirectional diode coincidence gate (AND gate):** In certain applications, it may become necessary that the input be transmitted to the output only when a set of conditions are simultaneously satisfied. In such cases, a coincidence gate is employed. A unidirectional diode coincidence (AND) gate is shown in Fig. 11.7(a).

When any of the control voltages is at $-V_1$ (-25 V), point X is at a larger negative voltage, even if the input pulse V_s (15 V) is present. D_0 is reverse-biased. Hence, there is no signal at the output.

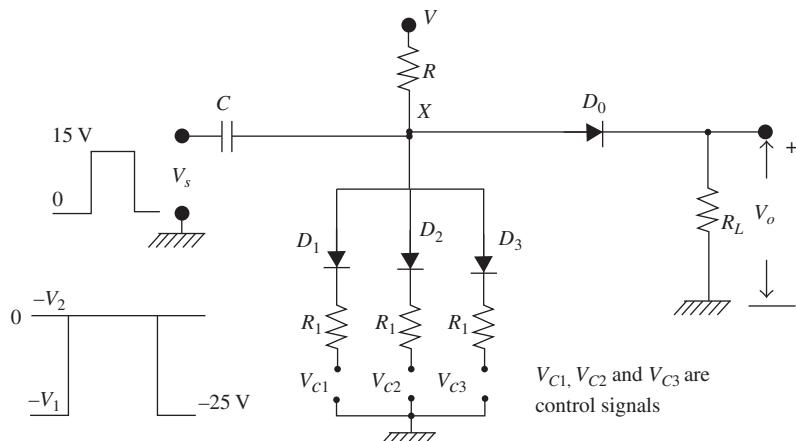


FIGURE 11.7(a) A unidirectional diode AND gate with multiple control signals

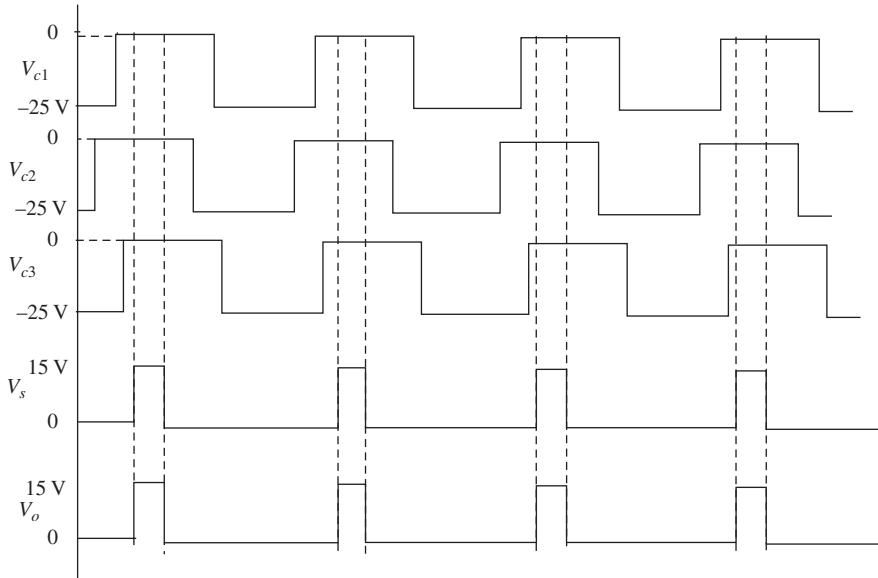


FIGURE 11.7(b) The waveforms of the coincidence (AND) gate

When all the control voltages, on the other hand, are at $-V_2$ (0 V), if an input signal V_s (15 V) is present, D_0 is forward-biased and the output is a pulse of 15 V. Thus, only when all the control signals are at 0 V (1 level) and if an input signal is present, then it is transmitted to the output. Hence, this circuit is a coincidence circuit or AND circuit, as shown in Fig. 11.7(b).

- (ii) **A unidirectional diode OR gate:** Consider the gate circuit shown in Fig. 11.8(a). Let the control voltages vary from -50 V to 0 V. If any control signal V_C (say V_{C1}) is at 0 V, D_1 conducts and behaves as a short circuit. Then the resultant circuit is shown in Fig. 11.8(b). If R_s is $1\text{ k}\Omega$ and if I is specified as 1 mA then $R = 149\text{ k}\Omega$. The voltage at X is now at -1 V . Hence, D_0 is reverse-biased and is an open circuit; and so the output is zero. Now, if a pulse V_s ($= 10$ V) is applied at the input, D_0 is forward-biased and D_1 and D_2 are reverse-biased. The output is 10 V .

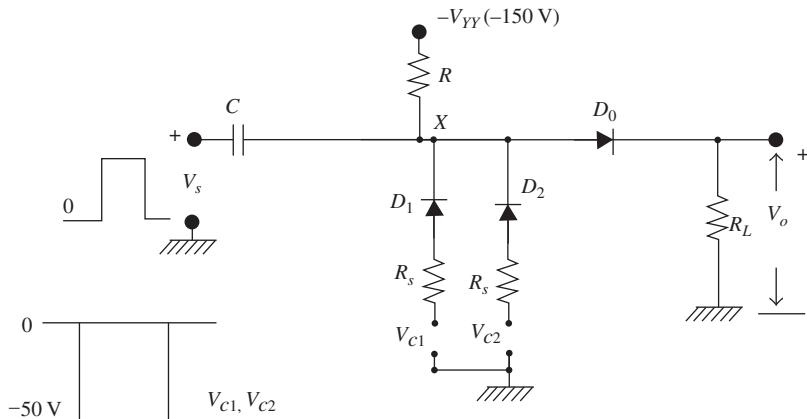


FIGURE 11.8(a) An OR sampling gate

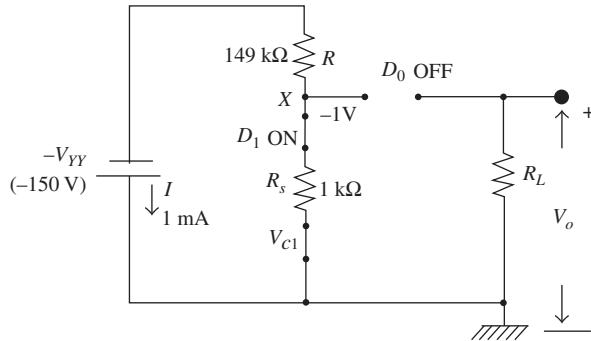


FIGURE 11.8(b) The circuit of Fig. 11.8(a) when any of the control signals and inputs is zero

Thus, the circuit shown in Fig. 11.8(a) is a gate that transmits the input signals to the output when any one of the control inputs is 0 V (1 level). This circuit is an OR circuit. The waveforms are shown in Fig. 11.8(c). The truth table, given in Table. 11.1 with control signals as logical inputs, verifies the OR operation. We see from the waveforms shown in Fig. 11.8(c) and Table.11.1 that the output is 0 V (0 level) for input pulses 4 and 8, for which both the control signals are -50 V (0 level).

(iii) **Unidirectional diode gate that eliminates pedestal:** In the unidirectional gates discussed till now, if the upper level of the gating signal ($-V_2$) is exactly zero volts, the gate is enabled and an input is faithfully transmitted to the gate output terminals. The output can also be derived if $-V_2$ is a positive voltage (say 5 V). In this case, the output will have a pedestal and the signal is superimposed on it. To ensure that the output is a faithful replica of the input even if the upper level of the control signal is positive (i.e., to eliminate pedestal), the circuit shown in Fig. 11.9(a) is employed.

(a) If the input V_s is zero and if the enabling control signal is not present, D_1 conducts and the negative voltage at X reverse-biases D_0 and $V_o = 0$, shown in Fig. 11.9(b).

TABLE 11.1 The truth table of the OR gate with control signals as logical inputs

Input pulse number	State of V_{C1}	State of V_{C2}	Output V_o
1	0 V (1 level)	0 V (1 level)	10 V (1 level)
2	-50 V (0)	0 V (1)	10 V (1)
3	0 V (1)	-50 V (0)	10 V (1)
4	-50 V (0)	-50 V (0)	0 V (0)
5	0 V (1)	0 V (1)	10 V (1)
6	-50 V (0)	0 V (1)	10 V (1)
7	0 V (1)	-50 V (0)	10 V (1)
8	-50 V (0)	-50 V (0)	0 V (0)
9	0 V (1)	0 V (1)	10 V (1)
10	-50 V (0)	0 V (1)	10 V (1)
11	0 V (1)	-50 V (0)	10 V (1)

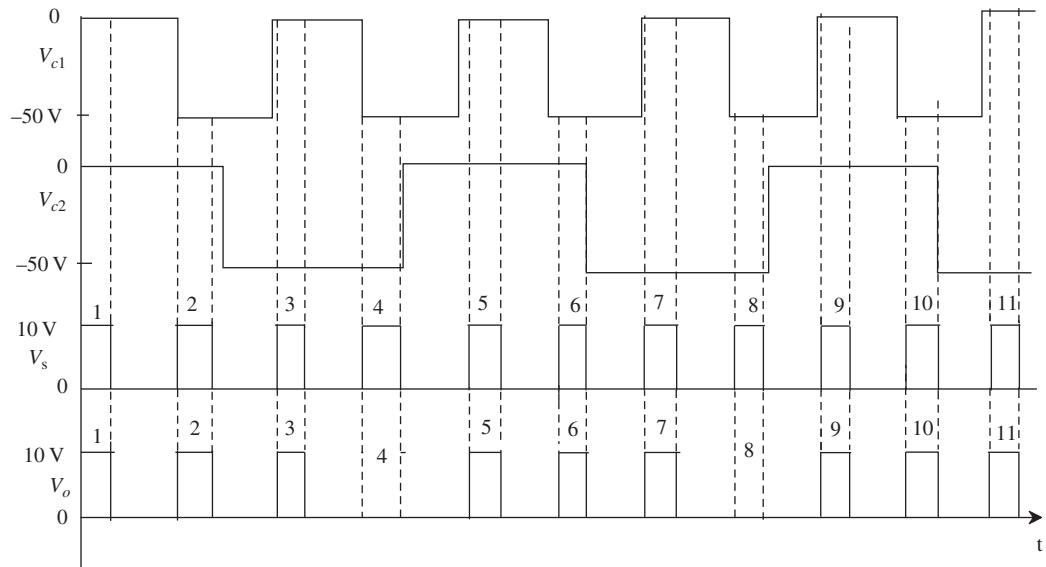


FIGURE 11.8(c) The waveforms of the OR gate shown in Fig. 11.8(a).

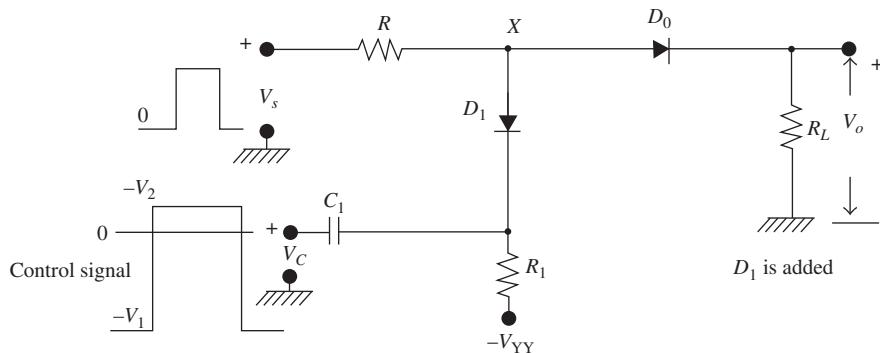


FIGURE 11.9(a) A sampling gate that is insensitive to the upper level ($-V_2$) of the control signal

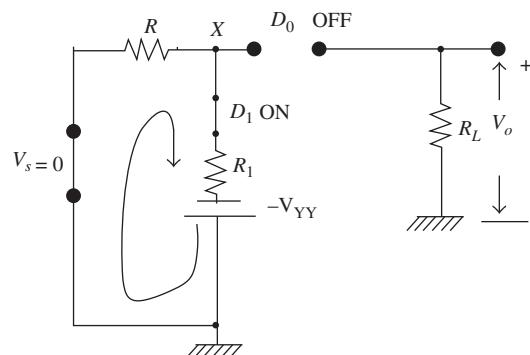


FIGURE 11.9(b) The circuit of Fig. 11.9(a) when $V_s = 0$ and the control signal is absent

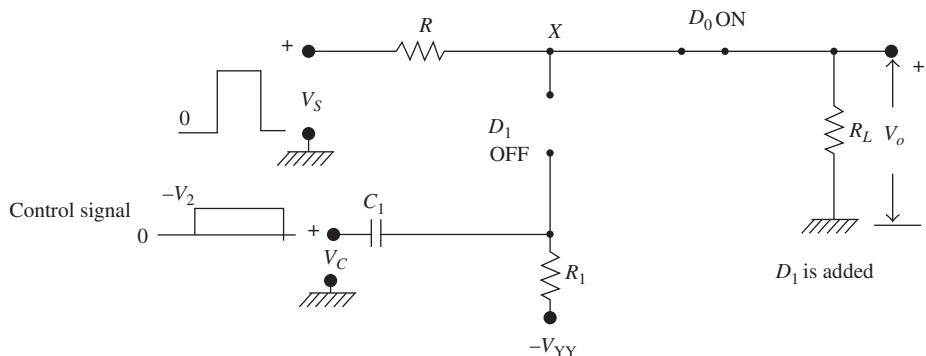


FIGURE 11.9(c) The circuit when the control signal is positive and the input is present

- (b) If the control voltage is now positive, D_1 is reverse-biased and is OFF, as shown in Fig. 11.9(c). An input signal V_s (a positive pulse) ensures conduction of D_0 and hence, the input signal is present at the output for the duration of the control signal. There is no pedestal in the output even though the control signal has a positive voltage as its upper level.

11.2.3 A Unidirectional Diode Gate to Transmit Negative Pulses

A unidirectional diode gate is shown in Fig. 11.3, to transmit the positive pulses when the gating signal is present. Similarly, a unidirectional diode gate to transmit negative pulses can be constructed as shown in Fig. 11.10. The difference between these two gates is that the input signals are negative pulses and the gating signal varies between V_1 and V_2 as shown in Fig. 11.10 and the diode is connected in the opposite direction.

When the gating signal is at V_1 , the voltage at X is a large positive voltage as a result D is reverse-biased. If an input signal is now present until the magnitude of the input is more negative than the positive voltage at X , the diode will not conduct, i.e., for the diode to conduct and thus transmit the signal to the output, the input is required to have a large negative value. Even if the diode conducts only the peak of the input will be transmitted to the output, but not the entire input signal. On the other hand, when the amplitude of the gating signal is V_2 , a small positive voltage, if a negative pulse is present at the input it can make the diode conduct. As such the output is present when the gating signal is at V_2 .

11.3 BIDIRECTIONAL SAMPLING GATES

Till now we have considered gates that pass only unidirectional signals. Bidirectional sampling gates transmit both positive and negative signals. These gates can be derived using diodes, BJTs, FETs, etc. We are going to consider some variations of the bidirectional gates.

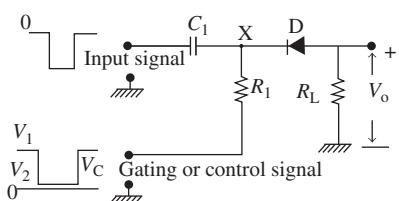


FIGURE 11.10 The unidirectional diode gate to transmit negative pulses

11.3.1 Single-transistor Bidirectional Sampling Gates

A bidirectional sampling gate using a single transistor is shown in Fig. 11.11. The control signal and the input are applied to the base of Q . The control signal is a pulse whose amplitude varies between V_1 and V_2 and has a duration t_p sufficient enough for a signal transmission. As long as V_C is at the lower level V_1 , Q is OFF and at the output we only have a dc voltage V_{CC} . However, when V_C is at its upper level V_2 , Q is ON for the duration t_p and if the input signal is present during this period, it is amplified and transmitted to the output with

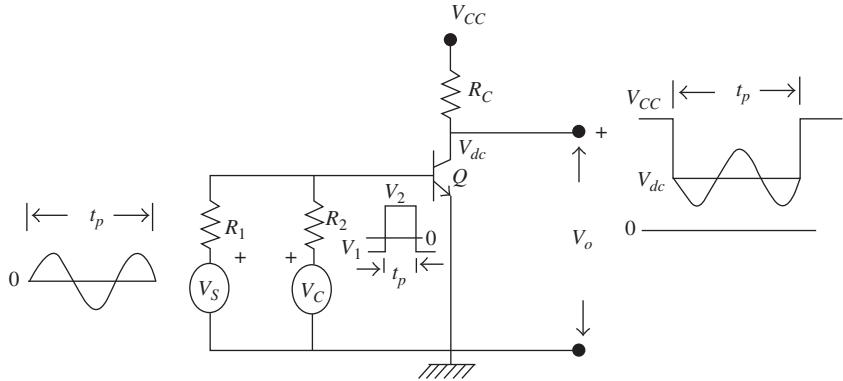


FIGURE 11.11 A bidirectional transistor gate

phase inversion but referenced to a dc voltage V_{dc} . At the end of t_p , Q is again OFF and the dc voltage at its collector jumps to V_{CC} . Thus, the signal is transmitted when the gating signal is at V_2 . However, the output contains a pedestal.

11.3.2 Two-transistor Bidirectional Sampling Gates

The Fig. 11.12(a) shows another bidirectional transistor gate where two devices Q_1 and Q_2 are used and the control signal and the input signal are connected to the two separate bases.

There is no external dc voltage connected to the base of Q_1 , only the gating signal V_C is connected. Let the control voltage be at its upper level, V_2 . Then, Q_1 is ON and there is sufficient emitter current I_{E1} which results in V_{EN1} across R_E . Q_2 is biased to operate in the active region using R_1 and R_2 . The voltage at the base of Q_2 with respect to its emitter (V_{BE2}) is $(V_{BN2} - V_{EN1})$. If this voltage is sufficient enough to reverse-bias the base-emitter diode of Q_2 , then Q_2 is OFF. There is no output signal, but only a dc voltage V_{CC} is available. However, when the gating signal is at its lower level V_1 , Q_1 is OFF and Q_2 operates in the active region and can also operate as an amplifier. If an input signal is present, there is an amplified output V_o . The presence of R_E increases the input resistance R_i and thus, the signal source is not loaded.

From the waveforms shown in Fig. 11.12(b) it is seen that the output is V_{CC} when Q_2 is OFF. When the gating signal drives Q_1 OFF and Q_2 ON, the dc voltage at the collector of Q_2 falls to V_{dc} (a voltage much smaller

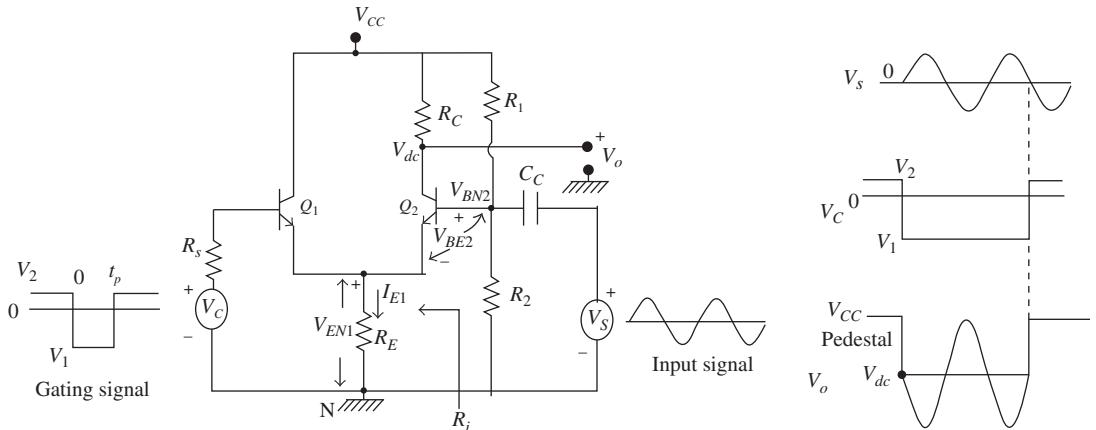


FIGURE 11.12(a) A bidirectional transistor gate

FIGURE 11.12(b) The waveforms

than V_{CC}). During the period of the gating signal, the input signal is amplified and phase inverted by Q_2 and is available at the output. Again at the end of the gating signal Q_2 goes OFF and V_o jumps to V_{CC} . Hence, the signal is superimposed on a pedestal.

11.3.3 A Two-transistor Bidirectional Sampling Gate that Reduces the Pedestal

A circuit arrangement that reduces the pedestal is shown in Fig. 11.13. The control signals applied to the bases of Q_1 and Q_2 may have the same amplitude but are of opposite polarity. When the gating signal is connected to Q_1 at $T = 0-$, it is negative (at level V_1). The net voltage at the base of Q_1 is $-(V_{BB1} + V_1)$. Therefore, Q_1 is OFF. At the same time the gating signal connected to Q_2 is positive and is V'_2 . The net voltage at the base of Q_2 is $(V'_2 - V_{BB2})$ and is positive and therefore, drives Q_2 ON. Q_2 draws a collector current I_C . As a result, there is a dc voltage V_{dc} at its collector and $V_o = V_{dc}$. However, when the gating voltage at the base of Q_1 drives Q_1 ON and into the active region, at $t = 0+$, Q_2 goes OFF as the gating signal is V'_1 . During this period when Q_1 is ON, if the input signal is present, it is amplified and is available at the output, with phase inversion. The bias voltages V_{BB1} and V_{BB2} are adjusted such that the quiescent current in Q_1 and Q_2 when ON is the same ($= I_C$) and consequently the quiescent dc voltage at the output is V_{dc} . Therefore, the dc reference level practically is V_{dc} . At the end of the time period t_p , Q_1 once again goes into the OFF state and Q_2 into the ON state and the dc voltage at the output is V_{dc} . As such the pedestal can be eliminated. However, our assumption is that the gating signals are ideal pulses (with zero rise time). In this case, the instant Q_1 switches ON, Q_2 switches OFF, as shown in Fig. 11.14(a). However, in practice the gating signals may not be ideal pulses but have a finite rise time and fall time; these may then give rise to spikes in the output shown in Fig. 11.14(b).

Let V_{BE} be the voltage between the base and emitter terminals of a transistor when the device is in the active region. If the gating pulse is at its lower level (V'_1 , negative), the net voltage as we have seen at the base of Q_2 is far below the cut-off. As a result, Q_2 goes OFF at $t = t_2$. At the same instant, Q_1 is required to go into the ON state, as the gating signal at its base is positive. However, because of the finite rise time associated with the gating signal at the base of Q_1 , it may not necessarily go into the ON state at the instant Q_2 has gone into the OFF state (t_2) and may go into the ON state at $t = t_1$. The result is that the output is nearly V_{CC} during the interval t_2 to t_1 . This voltage, however, falls to V_{dc} when eventually Q_1 is ON. A spike

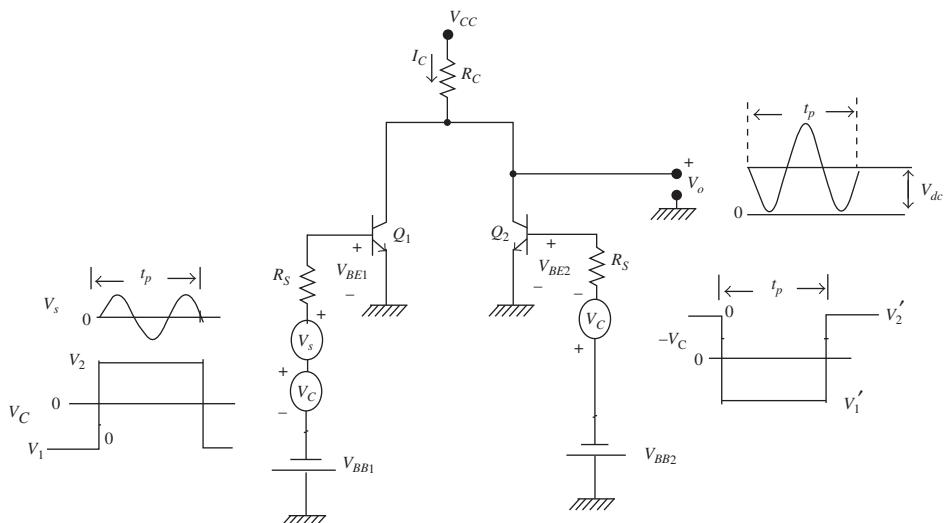


FIGURE 11.13 Circuit that reduces the pedestal

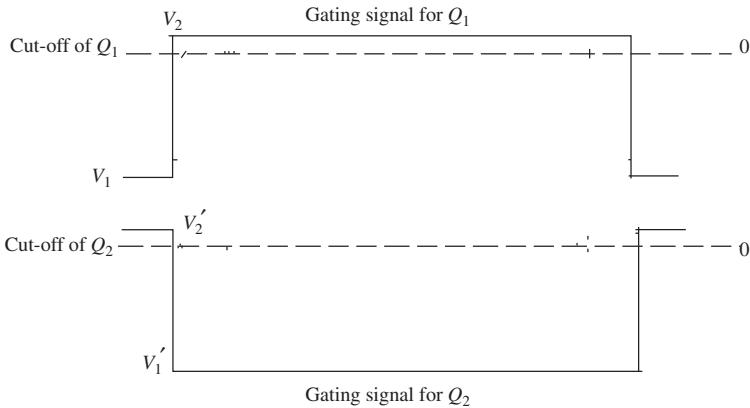


FIGURE 11.14(a) There are no spikes in the output when the gating signals are ideal

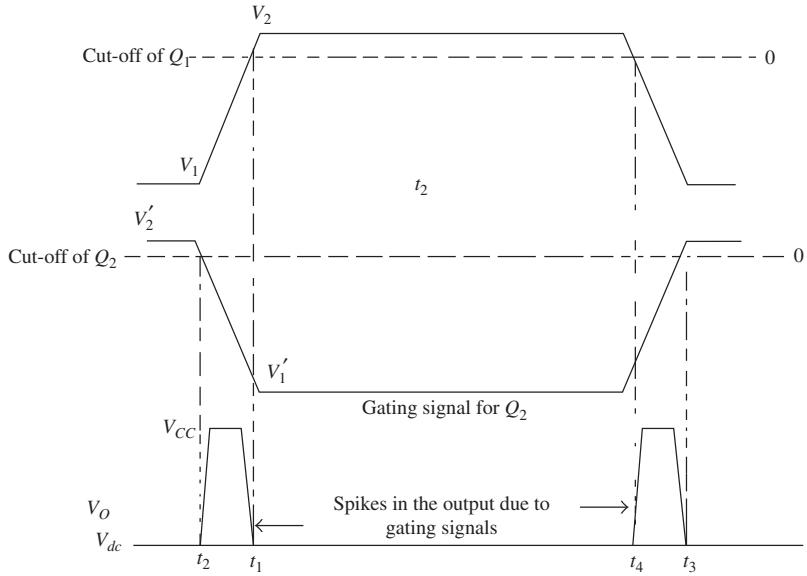


FIGURE 11.14(b) The spikes of a longer duration if the rise time of the gating signal is large

is developed at the output. Similarly, at the end of the gating signal Q_1 goes OFF (at $t = t_4$) before Q_2 goes ON (at $t = t_3$). Another spike develops at the output. It is seen that the gating signals themselves give rise to spikes in the output. If the rise time of the gating signal is large, these spikes are of larger duration as shown in Fig. 11.14(b), where as if the rise time of the gating signal is small, these output spikes are of smaller duration as shown in Fig. 11.15. If the rise time of the gating signal is small when compared to the duration of the gating signal, even though the spikes may occur in the output, as the duration of the signal is smaller than the spacing between the spikes, these spikes will not cause any distortion of the signal and hence, are not objectionable, as shown in Fig. 11.15.

11.3.4 A Two-diode Bridge Type Bidirectional Sampling Gate that Eliminates the Pedestal

A bidirectional diode gate that eliminates the pedestal is shown in Fig. 11.16(a). R_1 , R_2 , D_1 and D_2 form the four arms of the bridge. When the control signals are at V_1 , D_1 and D_2 are OFF and no input signal is

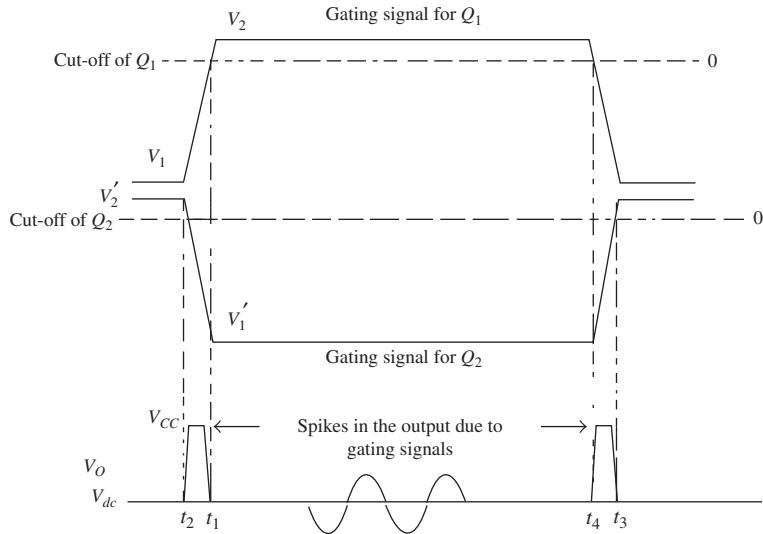


FIGURE 11.15 The spikes of relatively smaller duration when the rise time of the gating signals is small

transmitted to the output. However, when the control signals are at V_2 , diode D_1 conducts if the input ($= V_s$) are positive pulses and diode D_2 conducts if the input are negative pulses. Hence, these bidirectional inputs are transmitted to the output. This arrangement because of the circuit symmetry eliminates a pedestal. Consider one half of the circuit that transmits the positive pulses to the output when D_1 conducts (because of symmetry), as shown in Fig. 11.16(b).

Thévenizing the circuit shown in Fig. 11.16(b) at node A , the Thévenin voltage source magnitude due to V_s (shorting V_C source, considering one source at a time) and its internal resistance are calculated using the circuit shown in Fig. 11.16(c).

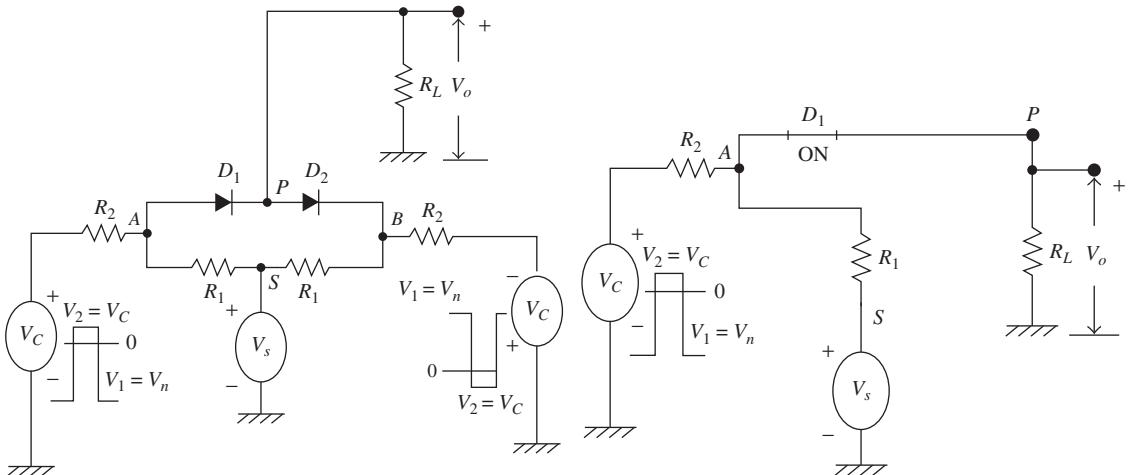


FIGURE 11.16(a) A bidirectional gate in the form of a bridge circuit

FIGURE 11.16(b) The circuit that transmits the positive pulses to the output

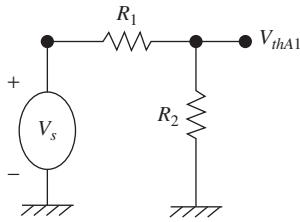


FIGURE 11.16(c) The equivalent circuit to calculate voltage at node A due to V_s source

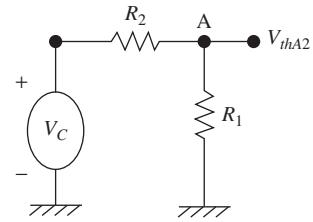


FIGURE 11.16(d) The equivalent circuit to calculate voltage at node A due to V_C source

$$V_{thA1} = \frac{R_2}{R_1 + R_2} V_s = \alpha V_s$$

$$\text{where } \alpha = \frac{R_2}{R_1 + R_2} \quad \text{and} \quad R_{th1} = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

Similarly, Thevenizing the circuit shown in Fig. 11.16(b) at node A , the Thévenin source due to V_C is (shorting V_s), shown in Fig. 11.16(d).

$$V_{thA2} = \frac{R_1}{R_1 + R_2} V_C \quad R_{th2} = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

$$V_{thA2} = \frac{R_1}{R_1 + R_2} V_C = (1 - \frac{R_2}{R_1 + R_2}) V_C = (1 - \alpha) V_C$$

We have $R_{th1} = R_{th2}$.

Redrawing the circuit shown in Fig. 11.16(b) and replacing the diode by its linear model (a battery of value V_γ in series with R_f , the forward resistance of the diode), results in the circuit shown in Fig. 11.16(e).

Similarly, considering the circuit when a negative signal is transmitted to the output when D_2 is ON and combining the equivalent circuits of the two halves, we finally have the circuit shown in Fig. 11.16(f).

$$R_3 = R + R_f, \text{ where } R = R_{th1} = R_{th2}$$

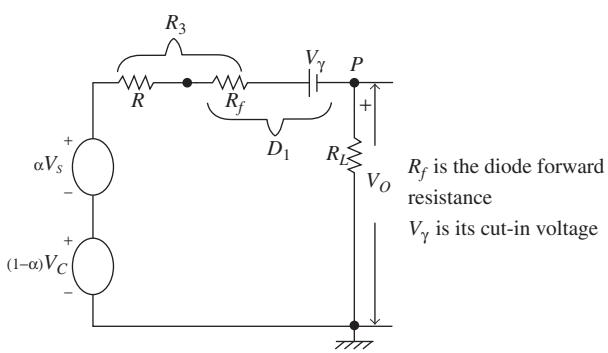


FIGURE 11.16(e) The equivalent circuit of the circuit shown in Fig. 11.16(b)

We shall now define the gain of the transmission gate A (strictly speaking this is attenuation) as the ratio of V_o/V_s during transmission period. The control and small diode voltages do not contribute to any current in R_L , the resultant simplified circuit is shown in Fig. 11.16(g). The open circuit voltage between P and the ground is αV_s and the Thévenin resistance is $R_3/2$, as shown in Fig. 11.16(h).

$$V_o = \alpha V_s \frac{R_L}{R_L + \frac{R_3}{2}} \quad A = \frac{V_o}{V_s} = \alpha \frac{R_L}{R_L + \frac{R_3}{2}}$$

But

$$\alpha = \frac{R_2}{R_1 + R_2}$$

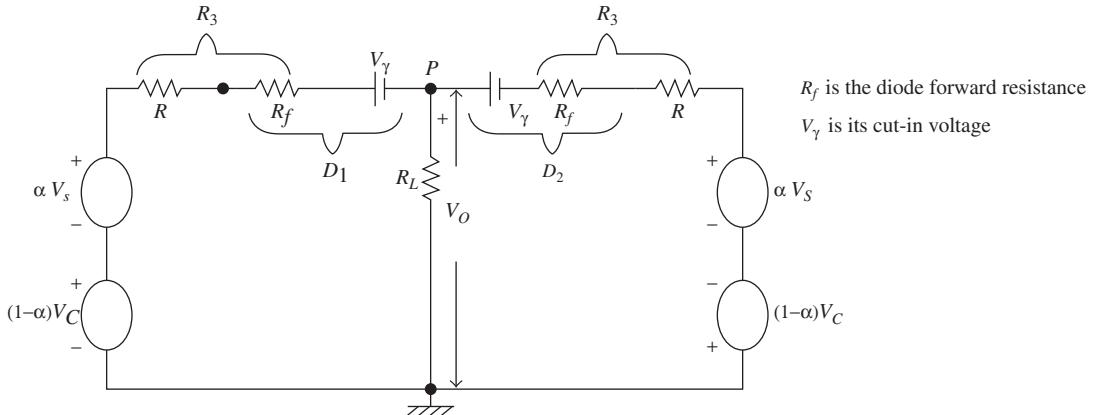


FIGURE 11.16(f) The equivalent circuit of Fig. 11.16(a)

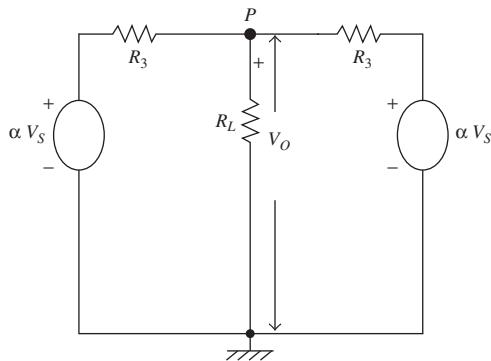
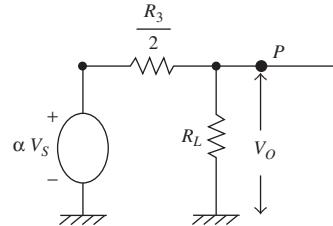


FIGURE 11.16(g) The simplified circuit of Fig. 11.16(f)

FIGURE 11.16(h) The circuit that enables the calculation of gain A

Therefore,

$$A = \frac{R_2}{R_1 + R_2} \times \frac{R_L}{R_L + \frac{R_3}{2}} \quad (11.1)$$

a) Minimum control voltage $V_C(\min)$ required to keep both the diodes D_1 and D_2 ON: Let only the gating signals be present. The amplitude and polarity of the gating signals are such that both the diodes D_1 and D_2 conduct, and equal currents flow in these two diodes. When these equal and opposite currents flow in R_L , the net voltage drop is zero and there is no pedestal.

Let V_s be a positive signal. As the amplitude of the signal goes on increasing, the current in D_1 goes on increasing and that in D_2 goes on decreasing. As V_s increases further, the current in D_2 becomes zero (i.e., D_2 is OFF). Thus, there is a minimum control voltage V_C that will keep both the diodes ON. To calculate this $V_{C(\min)}$, let it be assumed that D_2 has just stopped conducting i.e., the diode current has become zero; the drop across R_3 is zero. Therefore, the output voltage across R_L is the open circuit voltage, as shown in Fig. 11.17(a).

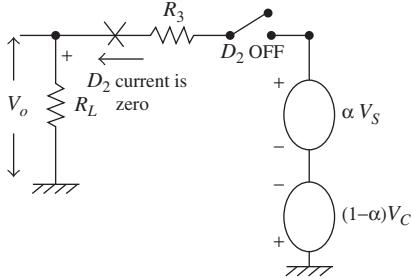


FIGURE 11.17(a) The voltage V_o when D_2 is OFF

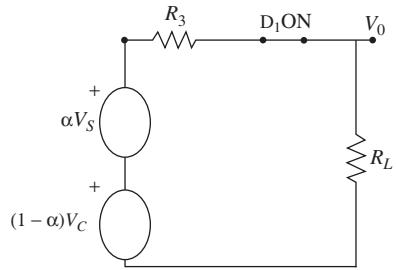


FIGURE 11.17(b) The voltage V_o when D_1 is ON

$$V_o = [\alpha V_s - (1 - \alpha) V_C] \quad (11.2)$$

Now, calculating the output due to the left hand side signal source V_s and control signal $(1 - \alpha) V_C$, with the assumption that $V_\gamma \ll V_s$ (i.e., $V_r \approx 0$), as shown Fig. 11.17(b).

$$V_o = [\alpha V_s + (1 - \alpha) V_C] \frac{R_L}{R_L + R_3} \quad (11.3)$$

Eqs. (11.2) and (11.3) represent V_o hence,

$$[\alpha V_s + (1 - \alpha) V_C] \frac{R_L}{R_L + R_3} = \alpha V_s - (1 - \alpha) V_C$$

$$\alpha V_s \left(1 - \frac{R_L}{R_L + R_3}\right) = (1 - \alpha) V_C \left(\frac{R_L}{R_L + R_3} + 1\right) \quad \alpha V_s \left(\frac{R_3}{R_L + R_3}\right) = (1 - \alpha) V_C \left(\frac{R_3 + 2R_L}{R_L + R_3}\right)$$

$$\alpha V_s R_3 = (1 - \alpha) V_C (R_3 + 2R_L)$$

$$\alpha = \frac{R_2}{R_1 + R_2} \text{ and } 1 - \alpha = 1 - \frac{R_2}{R_1 + R_2} = \frac{R_1}{R_1 + R_2}$$

$$\frac{R_2 R_3}{R_1 + R_2} V_s = \frac{R_1}{R_1 + R_2} (R_3 + 2R_L) V_C$$

$$V_{C(\min)} = \frac{R_2}{R_1} \times \frac{R_3}{R_3 + 2R_L} V_s \quad (11.4)$$

$V_{C(\min)}$ decreases with increasing R_L .

b) **Minimum control voltage $V_{n(\min)}$ to ensure that D_1 and D_2 are reverse-biased:** We have calculated the minimum control voltage $V_{C(\min)}$ i.e., needed to keep both the diodes, D_1 and D_2 ON. Similarly we calculate the minimum control voltage $V_{n(\min)}$ i.e., required to keep D_1 and D_2 OFF when no transmission takes place. If both the diodes are reverse-biased, the output voltage at point P is zero and P is at the ground potential, shown in Fig. 11.18(a). As D_1 is reverse-biased, it behaves as an open circuit. As a result, the input appears at the output.

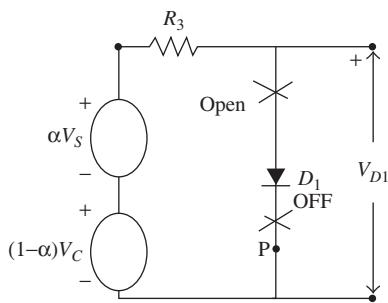
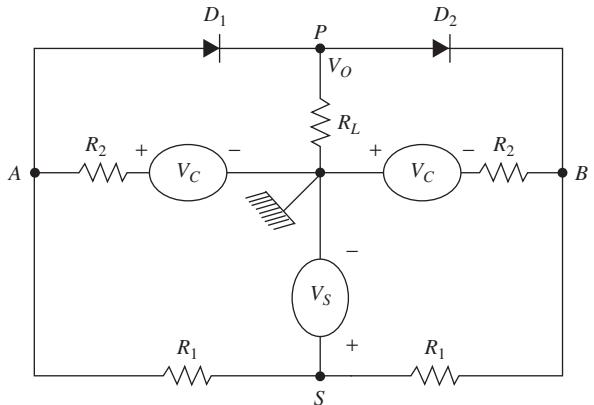
FIGURE 11.18(a) The gate circuit when D_1 and D_2 are reverse-biased

FIGURE 11.19(a) The bidirectional gate redrawn in the form of a bridge

$$V_{D1} = \text{Voltage across } D_1 = [\alpha V_s + (1 - \alpha) V_c]$$

If V_n is the magnitude of V_c at the lower level,

$$V_{D1} = [\alpha V_s + (1 - \alpha) V_n]$$

For D_1 to be OFF, V_{D1} must be either zero or negative. If V_{D1} is zero,

$$[\alpha V_s + (1 - \alpha) V_n] = 0 \quad V_n = V_{n(\min)} = \frac{-\alpha V_s}{1 - \alpha} \quad \frac{\alpha}{1 - \alpha} = \frac{R_2}{R_1}$$

Therefore,

$$V_{n(\min)} = \frac{-R_2}{R_1} V_s \quad (11.5)$$

In practice $V_{C(\min)}$ and $V_{n(\min)}$ are larger by 25 per cent. The bidirectional diode gate shown in Fig. 11.16(a) is redrawn as shown in Fig. 11.19(a). If the two control voltages are equal in magnitude but opposite in polarity the pedestal is not present in the output.

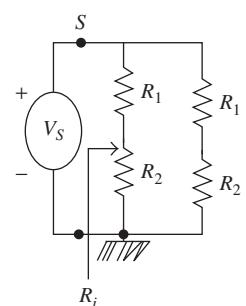
c) **Input resistance:** The purpose of the control signal is to enable the gate and the current drawn from the signal source does not depend on the control voltage. This current depends on the state of the diodes, whether they are ON or OFF. Here we assume that D_1 and D_2 as ideal diodes.

When the diodes D_1 and D_2 are OFF from Fig. 11.19(a) the equivalent circuit is as shown in Fig. 11.19(b) (obtained by open circuiting the diodes D_1 and D_2 and short circuiting V_C sources). The input resistance is calculated using the circuit shown in Fig. 11.19(b).

(i) When D_1 and D_2 are OFF

$$R_i = (R_1 + R_2) \parallel (R_1 + R_2) \quad (11.6)$$

$$R_i = \frac{(R_1 + R_2)}{2}$$

FIGURE 11.19(b) The circuit of Fig. 11.19(a) when D_1 and D_2 are OFF

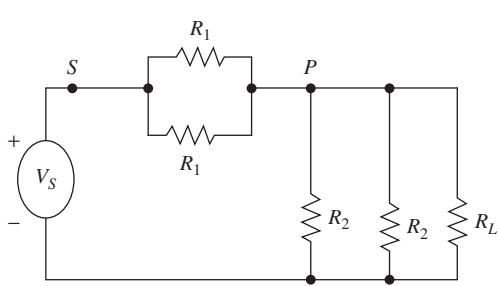


FIGURE 11.19(c) The circuit of Fig. 11.19(a) when D_1 and D_2 are ON

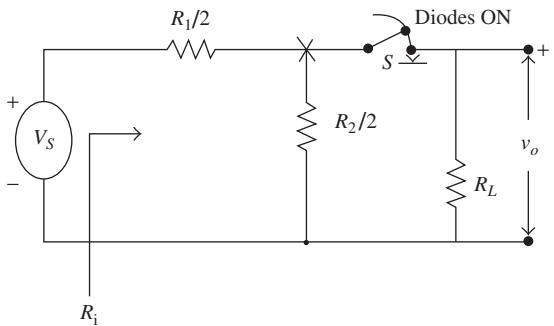


FIGURE 11.19(d) The simplified circuit of Fig. 11.19(c)

When the diodes are ON, the equivalent circuit is as shown in Fig. 11.19(c). The circuit of Fig. 11.19(c) after simplification is redrawn as shown in Fig. 11.19(d).

From the circuit in Fig. 11.19(d), input resistance R_i when the diodes are conducting is,

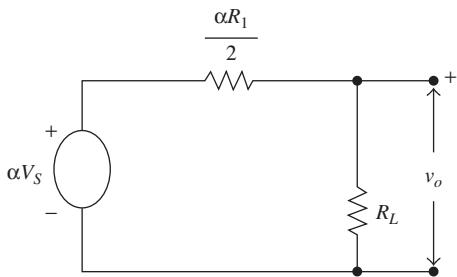
$$R_i = \frac{R_1}{2} + \frac{\frac{R_2}{2}R_L}{\frac{R_2}{2} + R_L}$$

$$R_i^{-1} = \frac{R_1}{2} + \frac{R_2R_L}{R_2 + 2R_L} \quad (11.7)$$

Now to calculate the gain of the transmission gate, A , let us calculate the Thévenin voltage source magnitude and its internal resistance. The circuit in Fig. 11.19(d) now reduces to that shown in Fig. 11.19(e).

$$V_{th} = V_s \times \frac{\frac{R_2}{2}}{\frac{R_1}{2} + \frac{R_2}{2}} = V_s \times \frac{R_2}{(R_1 + R_2)} = \alpha V_s$$

$$R_{th} = \frac{R_1}{2} \parallel \frac{R_2}{2} = \frac{R_1 R_2}{2(R_1 + R_2)} = \alpha \frac{R_1}{2}$$



$$V_o = \frac{\alpha V_s R_L}{R_L + \alpha \frac{R_1}{2}}$$

$$A = \frac{V_o}{V_s} = \frac{\alpha R_L}{R_L + \alpha \frac{R_1}{2}} = \frac{\alpha}{1 + \alpha \frac{R_1}{2R_L}} \quad (11.8)$$

FIGURE 11.19(e) The simplified circuit of Fig. 11.19(d)

Eq. (11.8) gives the expression for the transmission gain.

E X A M P L E

Example 11.1: In the circuit shown in Fig. 11.16(a), $R_L = R_1 = 100 \text{ k}\Omega$, $R_2 = 50 \text{ k}\Omega$ and the signal has a peak value of 20 V.

Find (a) A (b) $V_{C(\min)}$ (c) $V_{n(\min)}$ (d) R_i when the diodes are ON

Solution:

(a)

$$A = \frac{\alpha}{1 + \alpha \frac{R_1}{2R_L}} \quad \alpha = \frac{R_2}{R_1 + R_2} = \frac{50}{100 + 50} = \frac{50}{150} = \frac{1}{3}$$

$$\frac{R_1}{2R_L} = \frac{100}{2 \times 100} = \frac{1}{2}$$

Therefore,

$$A = \frac{\frac{1}{3}}{1 + \left(\frac{1}{3} \times \frac{1}{2}\right)} = \frac{\frac{1}{3}}{\frac{7}{6}} = \frac{2}{7} = 0.285$$

(b)

$$V_{C(\min)} = \frac{R_2}{R_1} \times \frac{R_3}{R_3 + 2R_L} V_s$$

$$R = \frac{R_2 R_1}{R_2 + R_1} = \frac{100 \times 50}{150} = \frac{100}{3} = \frac{100}{3} \text{ k}\Omega$$

$$R_3 = R + R_f \approx R = 33.3 \text{ k}\Omega$$

$$V_{C(\min)} = \frac{50}{100} \times \frac{33.3}{33.3 + 2 \times 100} \times 20 = \frac{333}{233.3} = 1.43 \text{ V}$$

(c)

$$V_{n(\min)} = \frac{-R_2}{R_1} \times V_s = \frac{-50}{100} \times 20 = -10 \text{ V}$$

(d) When the diodes are ON

$$R_i = \frac{R_L R_2}{R_2 + 2R_L} + \frac{R_1}{2}$$

$$= \frac{100 \times 50}{50 + 200} + \frac{100}{2}$$

$$= 20 + 50 = 70 \text{ k}\Omega$$

11.3.5 Four-diode Gates

The main disadvantages with two-diode gates are (i) although A is called the gain, the circuit actually offers a large attenuation to the signal since A is small (much less than 1); (ii) the two control voltages V_C and $-V_C$ should be equal in magnitude and opposite in polarity, failing which, there could be a pedestal in the output and (iii) $V_{n(\min)}$ can be appreciably large, as seen in Example 11.1. These limitations can be overcome in a four diode gate shown in Fig. 11.20(a). The differences seen in the four diode gate as compared to a two diode gate shown in Fig. 11.16(a) are (i) instead of connecting control signals at points A and B, sources $+V$ and $-V$ are connected at these points and (ii) the control signals are connected through the two additional diodes D_3 and D_4 to points P_1 and P_2 .

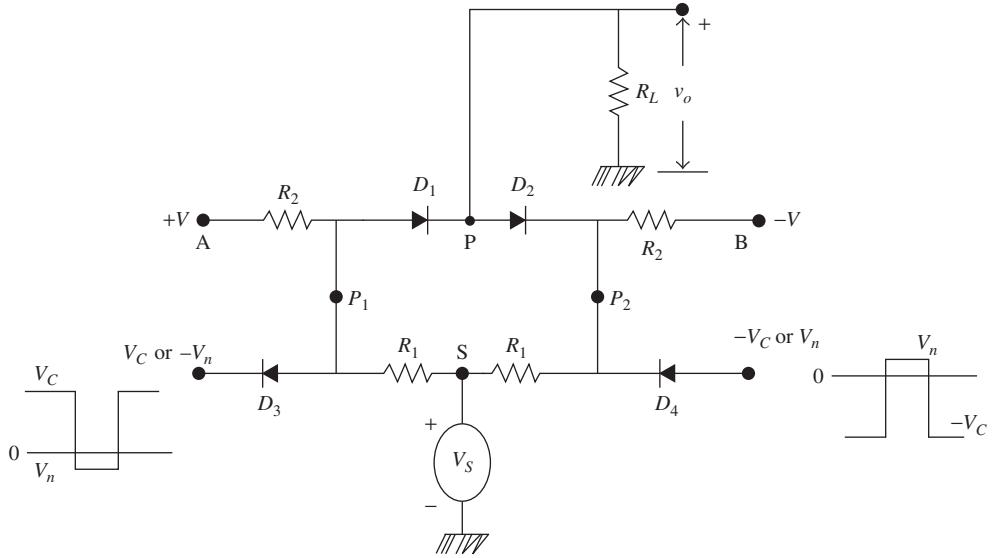


FIGURE 11.20(a) A four-diode gate

When the control voltages are V_C and $-V_C$, D_3 and D_4 are reverse-biased and are OFF. However, D_1 and D_2 are ON because of $+V$ and $-V$. The signal is connected to the load through R_1 and the conducting diodes, as shown in Fig. 11.20(b).

When the signal is transmitted, as D_3 and D_4 are OFF, even if there is a slight imbalance in the two control voltages $+V_C$ and $-V_C$, there is no pedestal at the output. Alternately, if the control voltages are at $-V_n$ and V_n respectively, D_3 and D_4 conduct. As a result, D_1 and D_2 are OFF and now the output is zero. When D_3 and D_4 are OFF, the circuit is similar to a two diode gate and A is the same as given in Eq. (11.1) except for the fact that V_C and $-V_C$ are replaced by V and $-V$. Also, the minimum value of voltage $V_{(\min)}$ is the same as $V_{C(\min)}$ in Eq. (11.4).

Therefore,

$$V_{\min} = \frac{R_2}{R_1} \times \frac{R_3}{R_3 + 2R_L} \times V_s \quad (11.9)$$

Let us now compute $V_{C(\min)}$. If $R_f \ll R_L$, for a positive V_s the voltage at P_1 is AV_s . If D_3 is to be OFF, V_C must at least be equal to AV_s .

$$\text{ie., } V_{C(\min)} \approx AV_s \quad (11.10)$$

$V_{n(\min)}$ is calculated to satisfy the condition that D_2 is OFF and D_4 is ON. Then we calculate the voltage at the cathode of D_4 (K_2) due to sources $-V$ and V_s using the superposition theorem, as shown in Fig. 11.20(c). The minimum voltage $V_{n(\min)}$ should at least be equal to V_{K2} .

Therefore,

$$V_{n(\min)} = V_s \times \frac{R_2}{R_1 + R_2} - V \times \frac{R_1}{R_1 + R_2} \quad (11.11)$$

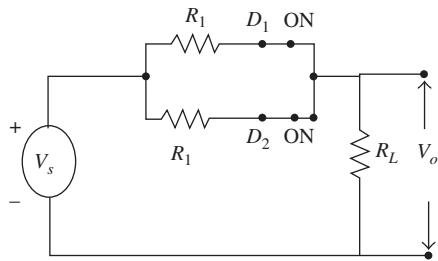


FIGURE 11.20(b) The circuit of Fig. 11.20(a) when D_1 and D_2 are ON and D_3 and D_4 are OFF

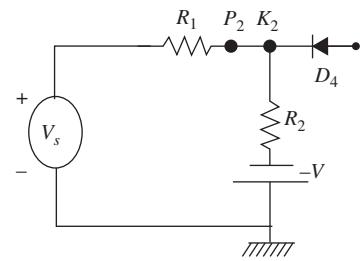


FIGURE 11.20(c) The circuit to calculate the voltage at the cathode of D_4

EXAMPLE

Example 11.2: For the four-diode gate shown in Fig. 11.20(a), $R_L = R_2 = 100 \text{ k}\Omega$ and $R_1 = 1 \text{ k}\Omega$, $R_f = 25 \Omega$, $V_s = 20 \text{ V}$. Calculate (a) A (b) $V_{(\min)}$ (c) $V_{C(\min)}$ (d) $V_{n(\min)}$ for $V = V_{(\min)}$

Solution:

(a) We have:

$$R = \frac{R_1 R_2}{R_1 + R_2}, \quad R_3 = R + R_f$$

$$R = \frac{100 \times 1}{101} = 990 \Omega$$

$$R_3 = 990 + 25 = 1015 \Omega$$

and

$$\begin{aligned} A &= \frac{R_2}{R_1 + R_2} \times \frac{R_L}{R_L + (R_3/2)} = \frac{100}{100 + 1} \times \frac{100}{100 + (1.015/2)} \\ &= 0.99 \times \frac{100}{100 + (1.015/2)} = 0.99 \times \frac{100}{100 + 0.507} \\ &A = 0.985 \end{aligned}$$

(b)

$$\begin{aligned} V_{\min} &= \frac{R_2}{R_1} \times \frac{R_3}{R_3 + 2R_L} \times V_s \\ &= \frac{100}{1} \times \frac{1.015 \times 20}{(1.015 + 200)} = \frac{101.5 \times 20}{201.015} = 10.1 \text{ V} \end{aligned}$$

(c)

$$V_{C(\min)} = AV_s = 0.985 \times 20 = 19.7 \text{ V}$$

(d)

$$V_{n(\min)} = V_s \times \frac{R_2}{R_1 + R_2} - V \times \frac{R_1}{R_1 + R_2}$$

Here $V = V_{(\min)} = 10.1 \text{ V}$ Therefore,

$$V_{n(\min)} = 20 \times \frac{100}{100 + 1} - 10.1 \times \frac{1}{100 + 1} = 19.80 - 0.1 = 19.70 \text{ V}$$

From Example 11.2 it is evident that the additional diodes D_3 and D_4 improve A . Further during the transmission of the signal, D_3 and D_4 are OFF, thereby eliminating the pedestal that could be present in the output due to the possible imbalance in the two control voltages V_C and $-V_C$.

An alternate form of four diode gate is shown in Fig. 11.21(a). The differences between the gate circuit shown in Fig. 11.21(a) and that shown in Fig. 11.20(a) are (i) in the four diode gate shown in Fig. 11.21(a), the load R_L is connected through a parallel path when all the diodes are conducting and (ii) there is no need for the sources $+V$ and $-V$.

When the control signals are V_C and $-V_C$, D_1, D_2, D_3 and D_4 are ON. Considering only V_C and $-V_C$ sources ($V_s = 0$), the resulting circuit can be redrawn as shown in Fig. 11.21(b). Redrawing the circuit shown in Fig. 11.21(b) the circuit that results is shown in Fig. 11.21(c). In this arrangement, V_C/R_C is the total current and $V_C/2R_C$ is the current in each arm. Now, considering only the signal source V_s ($V_C = 0$), the resultant circuit is shown in Fig. 11.21(d).

The voltages V_C and $-V_C$ depend on the amplitude of V_s of the signal, which satisfies the condition that all the diodes are conducting i.e., the current flows in the forward direction. The net current in the diodes is due to the sources V_C and V_s . The current in each diode due to the V_C sources is $V_C/2R_c$ and is a forward current. On the other hand, the current due to the V_s source flows in the reverse direction in D_3 and D_2 . The reverse current in D_3 is $V_s/2R_c + V_s/2R_L$ and that in D_2 is $V_s/2R_L$. Thus, the reverse current in D_3 is larger than the reverse current in D_2 .

For the diode D_3 to be conducting, the forward current should be greater than the reverse current. We can, therefore, arrive at the minimum value of $V_C(V_{C(\min)})$, when the forward current is equal to the reverse current.

$$\frac{V_C}{2R_C} = \frac{V_s}{R_C} + \frac{V_s}{2R_L}$$

$$V_{C(\min)} = 2V_s + \frac{R_C}{R_L} \times V_s = V_s \left(2 + \frac{R_C}{R_L} \right) \quad (11.12)$$

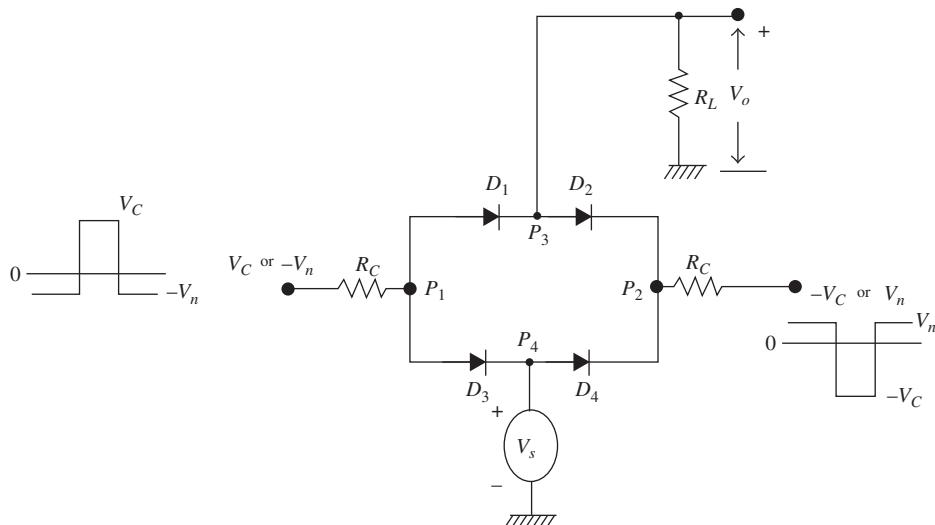


FIGURE 11.21(a) Another form of the four-diode gate

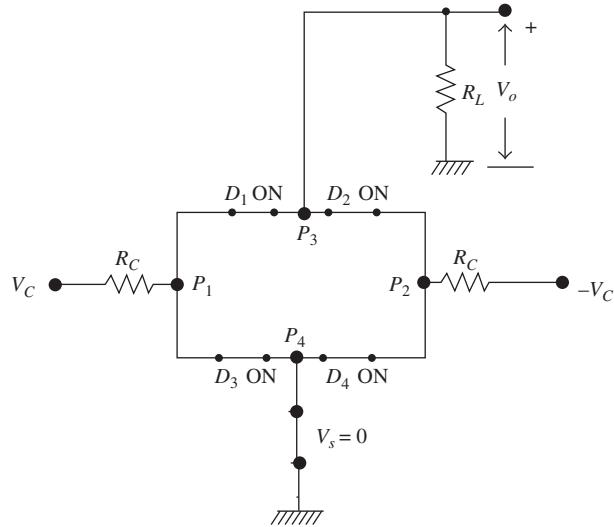


FIGURE 11.21(b) The circuit when all the diodes are ON

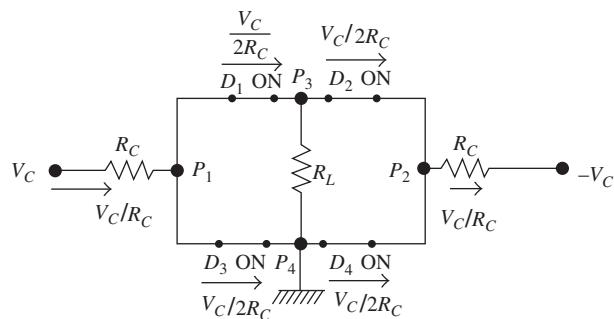


FIGURE 11.21(c) The redrawn circuit of Fig. 11.21(b)

A balancing resistance R (divided symmetrically as $R/2$ and $R/2$) is included between D_3 and D_4 to give zero output for zero input. Then the sampling gate is as shown in Fig. 11.21(e).

If R_f and R are much smaller than R_C or R_L , then P_1 , P_2 , P_3 and P_4 are all at the ground potential, with $V_s = 0$, as shown in Fig. 11.21(f). If P_1 is approximately at the ground potential,

$$I_1 = \frac{V_C}{R_C} \quad (11.13)$$

$$I = I_1 \times \frac{R_f + (R/2)}{R_f + R_f + (R/2)} = \frac{V_C}{R_C} \times \frac{R_f + (R/2)}{2R_f + (R/2)}$$

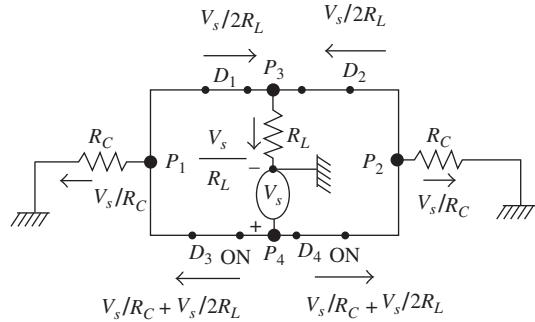
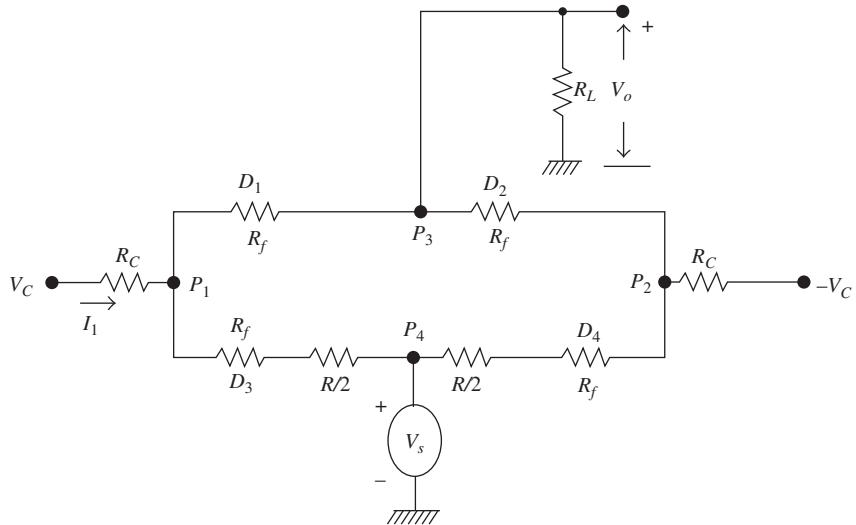
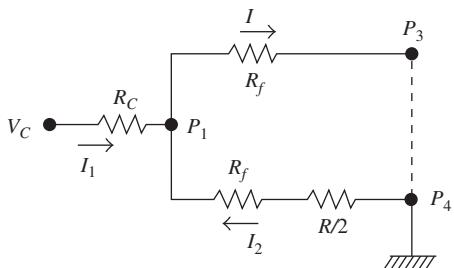
FIGURE 11.21(d) The circuit shown in Fig. 11.21(c) with $V_C = 0$ 

FIGURE 11.21(e) The four-diode gate with balancing resistance

FIGURE 11.21(f) The circuit of Fig. 11.21(e) when $V_s = 0$

$$I = \frac{V_C}{R_C} \times \frac{2(2R_f + R)}{2(4R_f + R)} = \frac{V_C}{2R_C} \left(\frac{4R_f + 2R}{4R_f + R} \right)$$

Dividing by $4R_f$

$$I = \frac{V_C}{2R_C} \left(\frac{1 + \frac{R}{2R_f}}{1 + \frac{R}{4R_f}} \right)$$

Since $R_f \ll R$

$$I \approx \frac{V_C}{2R_C} \left(\frac{1}{1 + \frac{R}{4R_f}} \right) \quad (11.14)$$

The larger reverse current in D_3 (I_2) is due to V_s (when $V_C = 0$).

$$I_2 = \frac{V_s}{R_C} + \frac{V_s}{2R_L}$$

For V_C to be $V_{C(\min)}$, the forward current due to V_C , i.e., I and the reverse current due to V_s , then I_2 must just be equal.

$$\frac{V_s}{R_C} + \frac{V_s}{2R_L} = \frac{V_C}{2R_C} \left(\frac{1}{1 + \frac{R}{4R_f}} \right) \quad \frac{V_{C(\min)}}{2R_C} = \left(\frac{V_s}{R_C} + \frac{V_s}{2R_L} \right) \left(1 + \frac{R}{4R_f} \right)$$

$$V_{C(\min)} = \left(2V_s + V_s \times \frac{R_C}{R_L} \right) \left(1 + \frac{R}{4R_f} \right)$$

Therefore,

$$V_{C(\min)} = V_s \left(2 + \frac{R_C}{R_L} \right) \left(1 + \frac{R}{4R_f} \right) \approx V_s \left(2 + \frac{R_C}{R_L} \right) \quad (11.15)$$

If $R \gg R_f$, $V_{C(\min)}$ becomes large and to calculate this value Eq. (11.15) may be used. If R_f and R are small as compared with R_C and R_L , the four diode gate during the transmission, can be represented as shown in Fig. 11.21(g). R_S is the internal resistance of the signal source, V_s .

Considering the effective resistances of the parallel combinations the circuit shown in Fig. 11.21(g) reduces to that shown in Fig 11.21(h). So,

$$I = \frac{V_s}{R_S + (R_f/2) + (R/4) + \left\{ \frac{R_C/2}{(R_C/2) + (R_f/2) + R_L} \left[(R_f/2) + R_L \right] \right\}}$$

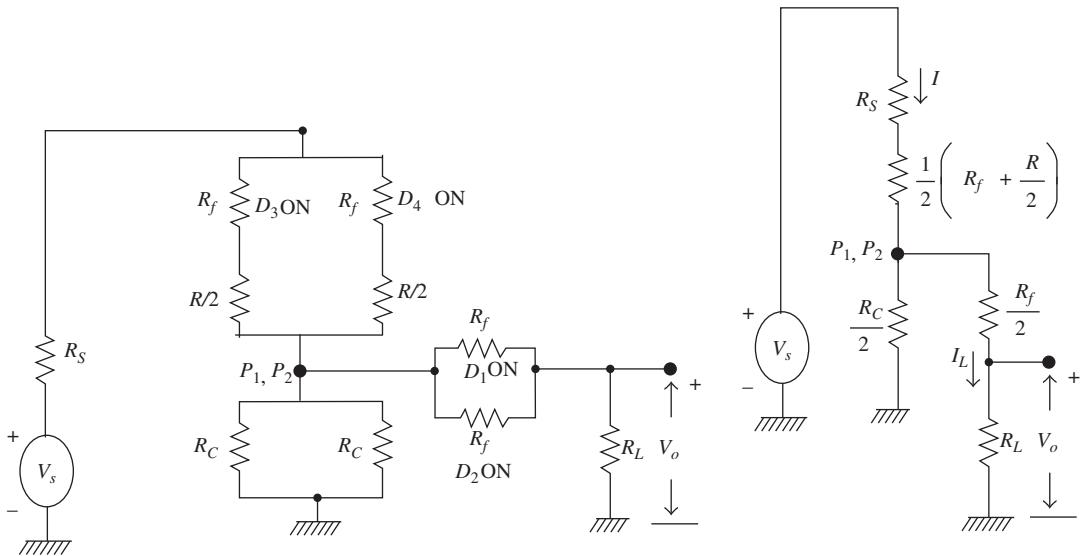


FIGURE 11.21(g) The four-diode gate during transmission

FIGURE 11.21(h) The simplified circuit of Fig. 11.21(g)

$$\begin{aligned}
&= \frac{V_s \left(\frac{R_C}{2} + \frac{R_f}{2} + R_L \right)}{\frac{R_S R_C}{2} + \frac{R_S R_f}{2} + R_S R_L + \frac{R_C R_f}{4} + \frac{R_f^2}{4} + \frac{R_L R_f}{2} + \frac{R R_C}{8} + \frac{R R_f}{8} + \frac{R_L R}{4} + \frac{R_C R_f}{4} + \frac{R_L R_C}{2}} \\
&= \frac{V_s (R_C + R_f + 2R_L)}{R_S R_C + R_S R_f + 2R_S R_L + \frac{R_C R_f}{2} + \frac{R_f^2}{2} + R_L R_f + \frac{R R_C}{4} + \frac{R R_f}{4} + \frac{R_L R}{2} + \frac{R_C R_f}{2} + R_L R_C} \\
&= \frac{V_s (R_C + R_f + 2R_L)}{R_S R_C + R_S R_f + 2R_S R_L + R_C R_f + \frac{R_f^2}{2} + R_L R_f + \frac{R R_C}{4} + \frac{R R_f}{4} + \frac{R_L R}{2} + R_L R_C} \\
I_L &= \frac{I \times \frac{R_C}{2}}{\frac{R_C}{2} + \frac{R_f}{2} + R_L} = I \times \frac{R_C}{R_C + R_f + 2R_L} \\
I_L &= \frac{V_s R_C}{R_S R_C + R_S R_f + 2R_S R_L + R_C R_f + \frac{R_f^2}{2} + R_L R_f + \frac{R R_C}{4} + \frac{R R_f}{4} + \frac{R_L R}{2} + R_L R_C} \\
V_o &= I_L R_L
\end{aligned}$$

$$A = \frac{V_o}{V_s} = \frac{R_C R_L}{R_S R_C + R_S R_f + 2R_S R_L + R_C R_f + \frac{R_f^2}{2} + R_L R_f + \frac{R R_C}{4} + \frac{R R_f}{4} + \frac{R_L R}{2} + R_L R_C}$$

Multiplying both the numerator and the denominator by 4 we get,

$$A = \frac{4R_C R_L}{4R_S R_C + 4R_S R_f + 8R_S R_L + 4R_C R_f + 2R_f^2 + 4R_L R_f + R R_C + R R_f + 2R_L R + 4R_L R_C}$$

Dividing the numerator and the denominator by $4R_C R_L$ we get,

$$\begin{aligned}
A &= \frac{1}{1 + \frac{R_S}{R_L} + \frac{R_S R_f}{R_L R_C} + \frac{2R_S}{R_C} + \frac{R_f}{R_L} + \frac{R_f^2}{2R_L R_C} + \frac{R_f}{R_C} + \frac{R}{4R_L} + \frac{R R_f}{4R_L R_C} + \frac{R}{2R_C}} \\
&= \frac{1}{1 + \frac{1}{R_L} \left(R_S + R_f + \frac{R}{4} \right) + \frac{1}{R_C} \left(2R_S + R_f + \frac{R}{2} \right) + \frac{R_f}{2R_L R_C} \left(R_f + 2R_S + \frac{R}{2} \right)} \\
A &= \frac{1}{1 + \frac{1}{R_L} \left(R_S + R_f + \frac{R}{4} \right) + \frac{1}{R_C} \left(2R_S + R_f + \frac{R}{2} \right) \left(1 + \frac{R_f}{2R_L} \right)}. \tag{11.16}
\end{aligned}$$

If the diodes shown in Fig. 11.21(g) are to be OFF when the control voltages are V_n and $-V_n$, then,

$$V_{n(\min)} = V_s \tag{11.17}$$

E X A M P L E

Example 11.3: For the four diode gate shown in Fig. 11.21(a), $V_s = 20$ V, $R_L = 200$ k Ω , $R_C = 100$ k Ω , $R_f = 0.5$ k Ω , $R = R_s = 1$ k Ω . Find $V_{n(\min)}$, A and $V_{C(\min)}$.

Solution:

(i) From Eq. (11.17), $V_{n(\min)} = V_s = 20$ V

(ii) From Eq. (11.15),

$$\begin{aligned} V_{C(\min)} &= V_s \left(2 + \frac{R_C}{R_L} \right) \left(1 + \frac{R}{4R_f} \right) \\ &= 20 \left(2 + \frac{100}{200} \right) \left(1 + \frac{1}{2} \right) = 20 \times 2.5 \times 1.5 = 75 \text{ V} \end{aligned}$$

(iii) From Eq. (11.16),

$$\begin{aligned} A &= \frac{1}{1 + \frac{1 + 0.5 + 0.25}{200} + \left(\frac{2 + 0.5 + 0.5}{100} \right) \left(1 + \frac{0.5}{400} \right)} \\ &= \frac{1}{1 + 0.00875 + 0.03} = 0.963 \end{aligned}$$

$$A = 0.963$$

From Examples 11.2 and 11.3 it is evident that the gain of the transmission gate is higher in a four-diode gate when compared to a two-diode gate.

11.3.6 Six-diode Gates

For the four-diode gate shown in Fig. 11.20(a), the voltages $+V$ and $-V$ need to be large and have to be balanced to avoid pedestal. This gate circuit is insensitive to slight variations in the control voltages. Also, for the four diode gate [see Fig. 11.21(a)], the control voltages tend to become large and further there is a need for balanced control voltages, which is difficult. However, in the former case it is easy to choose large desired values for $+V$ and $-V$ and also easy to balance these two voltages as these are dc sources. For the circuit shown in Fig. 11.21(a), R_L is connected through a parallel path with the result the current is shared by these two parallel branches. The transmission gain A in both the cases, however, is approximately unity. A six diode gate is shown in Fig. 11.22, and it combines the features of the gate circuits shown in Figs. 11.20(a) and 11.21(a).

When no signal is transmitted, D_5 and D_6 conduct while D_1 to D_4 remain OFF. During the transmission, D_5 and D_6 are OFF and this six diode gate is equivalent to the four diode gate seen in Fig. 11.21(a), earlier. If the diodes D_5 and D_6 remain OFF for the signal amplitude V_s , then,

$$V_{C(\min)} = V_s \quad (11.18)$$

The minimum required value of V_n is $V_{n(\min)}$ and is equal to V_s since the transmission diodes D_1 to D_4 will not conduct unless V_s exceeds V_n .

Hence,

$$V_{n(\min)} = V_s \quad (11.19)$$

The expression for A is given by Eq. (11.16).

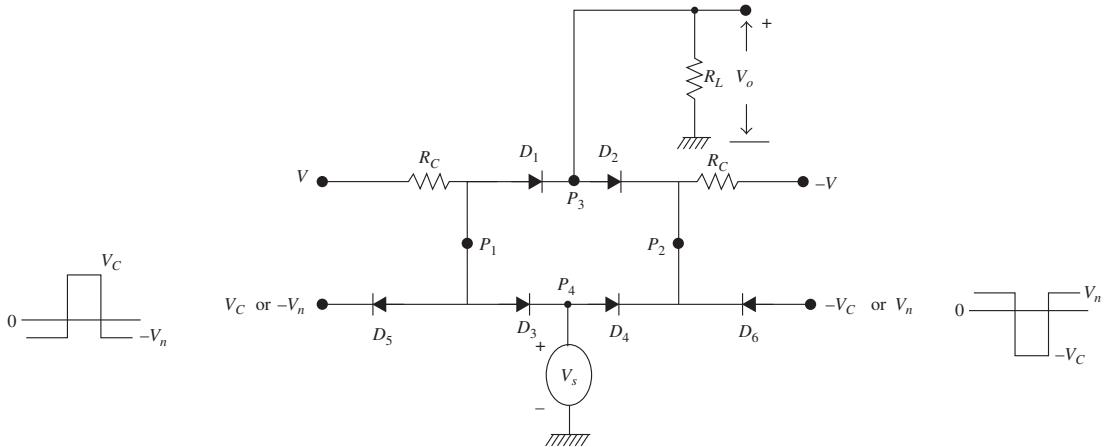


FIGURE 11.22 A six-diode gate

11.4 FET SAMPLING GATES

FET sampling gates can again be of two types: (i) a series gate and (ii) a shunt gate. The FET is simply used as a switch. In a series gate the FET switch is used as series element. Whereas in a shunt gate the FET switch is used as a shunt element. The advantage with FET and Op-amp sampling gates is that the input resistance is large and hence, the problem of loading is avoided.

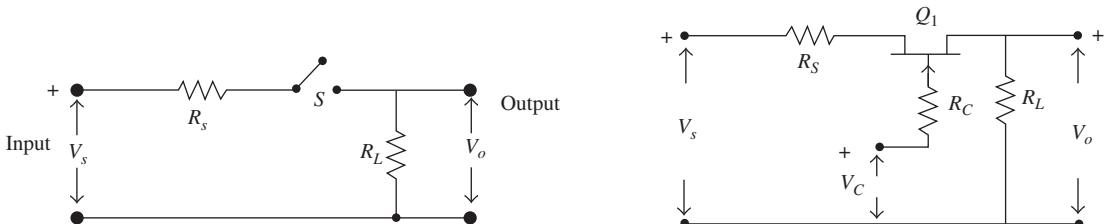
11.4.1 FET Series Gates

The Fig. 11.23(a) shows a sampling gate where the switch is used as a series element. The practical switch can be an *n*-channel FET. FET series gate is essentially a voltage switch. [see Fig. 11.23(b)]

The input V_s , control signal V_C and the output waveforms are shown in Fig. 11.23(c). The input V_s is a triangular wave, the control signal varies between V_1 and $-V_2$, and the output is either zero or varies as the input, depending on whether the FET is OFF or ON. The FET is ON (closed switch) when V_C is V_1 and is OFF (open switch) when V_C is $-V_2$.

A sampling gate is required to faithfully transmit the input signal to the output. For this to happen, the ON resistance of the FET, $R_{D(ON)}$ should ideally be zero and the drain current is kept at the minimum. Further R_s , the source resistance, should be very small when compared to R_L , as shown in Fig. 11.24(a).

$$V_o = V_s - I_D R_S - I_D R_{D(ON)} \quad (11.20)$$

FIGURE 11.23(a) The FET series gate with (a) S as an ideal switch; (b) with FET as a switch

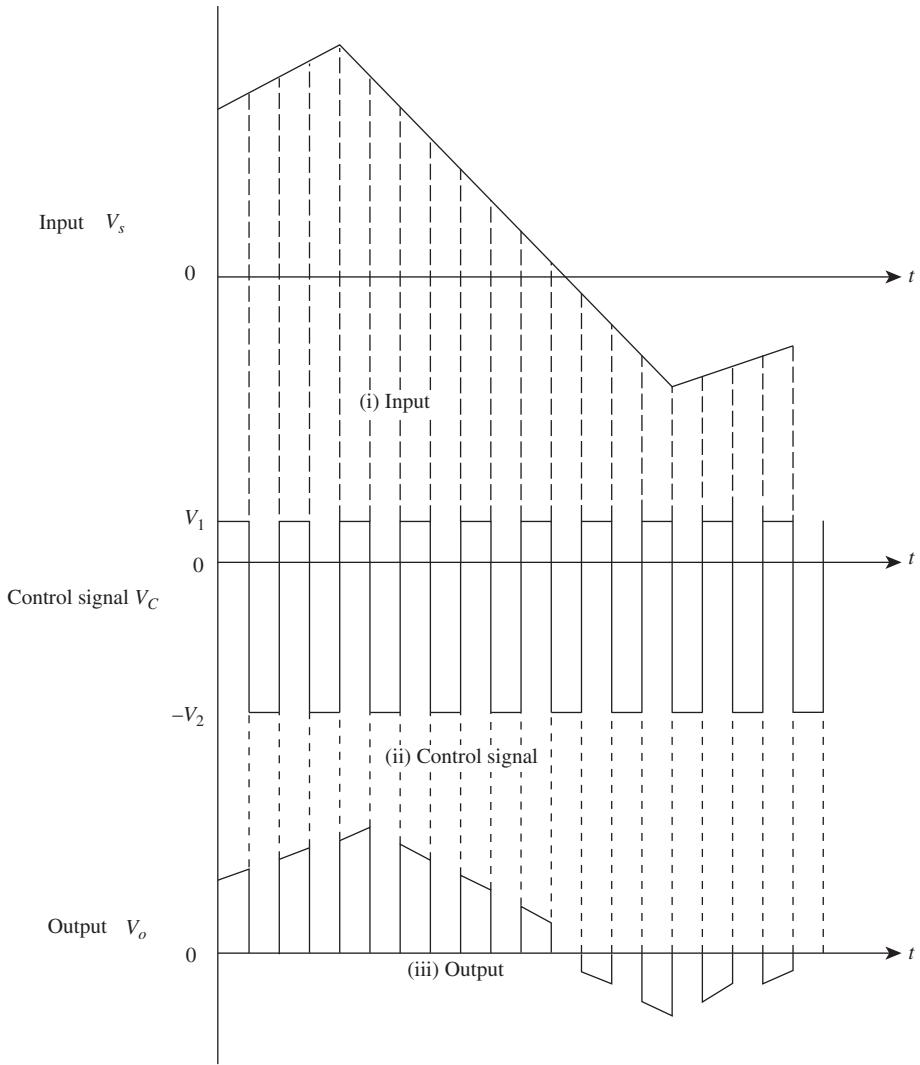


FIGURE 11.23(c) The waveforms of the series FET gate

If $R_s \ll R_L$ and $R_{D(ON)} \ll R_L$

$$V_o \approx V_s \quad (11.21)$$

On the other hand, if the FET is OFF, the gate to source leakage current I_{GSS} should be negligibly small. R_C is normally large, typically of the order $1 \text{ M}\Omega$, to make sure that I_{GSS} is negligible, as shown in Fig. 11.24(b).

For the switch Q_1 to be ON, the FET gate voltage V_C should be equal V_1 . Then as the FET is ON,

$$V_o = V_s \text{ and } V_C = V_1 = V_{s(\text{peak})}.$$

Alternately for the switch Q_1 to be OFF, the gate should be reverse-biased by approximately 1 V greater than the maximum $V_{GS(\text{OFF})}$. Further, $V_o = -V_s$, the FET source terminal goes to negative peak of V_s . Therefore, to make sure that Q_1 is OFF

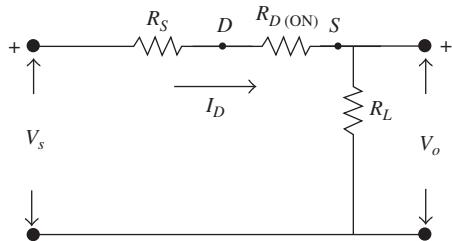


FIGURE 11.24(a) The FET switch when ON

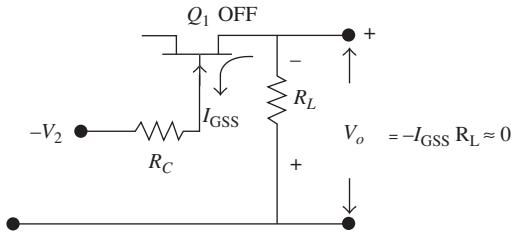


FIGURE 11.24(b) The FET switch when OFF

$$-V_2 = -(V_{s(\text{peak})} + V_{GS(\text{OFF})\text{max}} + 1\text{V})$$

To understand the procedure to calculate the voltages needed to keep the switch ON and OFF let us consider an example.

EXAMPLE

Example 11.4: Consider the following situation in the FET series gate, $V_s = \pm 2\text{ V}$, $R_s = 100\text{ }\Omega$, $R_L = 10\text{ k}\Omega$. The FET has the following parameters:

$$V_{GS(\text{OFF})\text{max}} = -10\text{ V} \text{ and } R_{D(\text{ON})} = 20\text{ }\Omega.$$

Calculate the voltage levels of the control signal, I_D , error due to R_s and error due to $R_{D(\text{ON})}$.

Solution:

The control signal should have a value V_1 for Q_1 to be ON.

Therefore, $V_1 = V_{s(\text{peak})} = 2\text{ V}$

For Q_1 to be OFF, the control signal should be $-V_2$:

$$-V_2 = -(V_{s(\text{peak})} + V_{GS(\text{OFF})\text{max}} + 1\text{V})$$

$$-V_2 = -(2 + 10 + 1) = -13\text{ V}$$

$$I_D = \frac{V_s}{R_s + R_{D(\text{ON})} + R_L} = \frac{2\text{ V}}{100 + 20 + 10000} = 197.4\text{ }\mu\text{A}$$

$$I_D R_s = 197 \times 10^{-6} \times 0.1 \times 10^3 = 19.74\text{ mV}$$

$$\text{Error due to } R_s = \frac{19.74\text{ mV}}{2\text{V}} \times 100\% = 0.987\%$$

$$I_D R_{D(\text{ON})} = 197.4\text{ }\mu\text{A} \times 20\text{ }\Omega = 3.948\text{ mV}$$

$$\text{Error due to } R_{D(\text{ON})} = \frac{3.948\text{ mV}}{2} \times 100\% = 0.197\%$$

11.4.2 FET Shunt Gates

When the source resistance R_S is significantly smaller than R_L then FET series gate is suitable. If R_S is large, the condition that $R_S \gg R_L$ can not be satisfied, in such a case, FET shunt gate is more suitable. A shunt sampling gate is shown in Fig. 11.25(a) and a shunt gate with an FET as a switch is shown in Fig. 11.25(b). The waveforms are shown in Fig. 11.25(c).

When Q_1 is OFF, there is a current I_L in the load and an output is present. When Q_1 is ON, the switch closes and the output is zero, as shown in Fig. 11.25(d).

Let us consider the situation when the FET switch is ON, as shown in Fig. 11.25(d).

$$I_L = \frac{I_D R_{D(ON)}}{R_L}$$

If $R_{D(ON)}$ is the ON resistance of the switch, then Fig. 11.25(d) is redrawn as shown in Fig. 11.25(e). Now, there is a small $V_o \approx I_D R_{D(ON)}$. Ideally V_o should be zero. Let us consider when the switch is open, as shown in Fig. 11.25(f).

$I_{D(OFF)}$ is the drain to source leakage current. Therefore,

$$I_L = I_S - I_{D(OFF)}$$

As $I_{D(OFF)}$ is negligible, I_L is expected to be I_S . Thus, errors could be present in this type of sampling gate also.

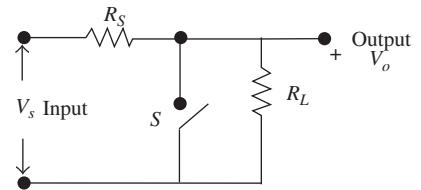


FIGURE 11.25(a) A shunt gate

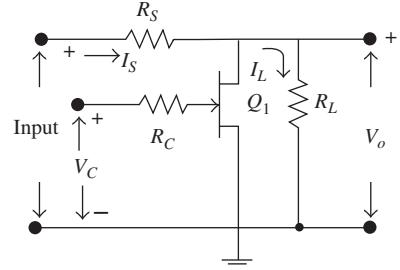


FIGURE 11.25(b) The FET shunt sampling gate

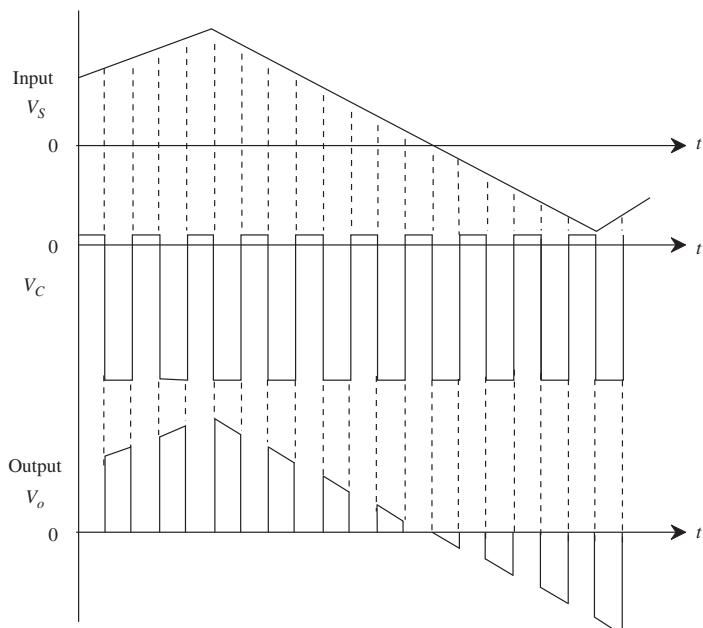
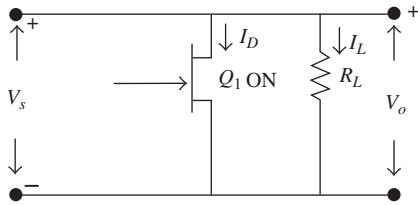
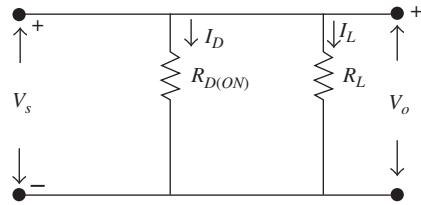


FIGURE 11.25(c) The waveforms of an FET shunt sampling gate

FIGURE 11.25(d) When Q_1 is ONFIGURE 11.25(e) The FET switch when ON is replaced by $R_{D(ON)}$

11.4.3 Op-amps as Sampling Gates

In the sampling gates seen till now, the signal is mostly attenuated during the transmission or some arrangements minimize attenuation. However, if the signal is to be amplified then an amplifier has to be provided. A FET controlled sampling gate employing an op-amp to amplify the signal is shown in Fig. 11.26(a).

The control signal V_C is a train of negative pulses and the input signal V_s is a sinusoidal signal. Op-amp is used as an inverting amplifier. The waveforms are shown in Fig. 11.26(b). The gain of the op-amp inverting amplifier is $A_V = -R_2/R_1$ when the FET Q_1 is OFF.

When the FET is ON, the effective resistance in the feedback path of the op-amp inverting amplifier is $R_2 \parallel R_{D(ON)}$ which is negligibly small. Therefore, the output when Q_1 is OFF is,

$$V_o = V_s \left(\frac{-R_2}{R_1} \right)$$

and the output when Q_1 is ON is,

$$V_o = V_s \left(\frac{-R_2 / R_{D(ON)}}{R_1} \right) \approx -V_s \left(\frac{R_{D(ON)}}{R_1} \right)$$

If $R_{D(ON)} \ll R_1$, $V_o \approx 0$.

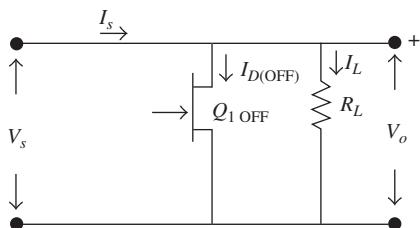


FIGURE 11.25(f) When the FET gate is OFF

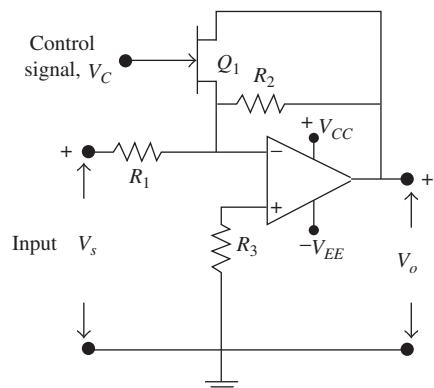


FIGURE 11.26(a) A FET controlled sampling gate using op-amp

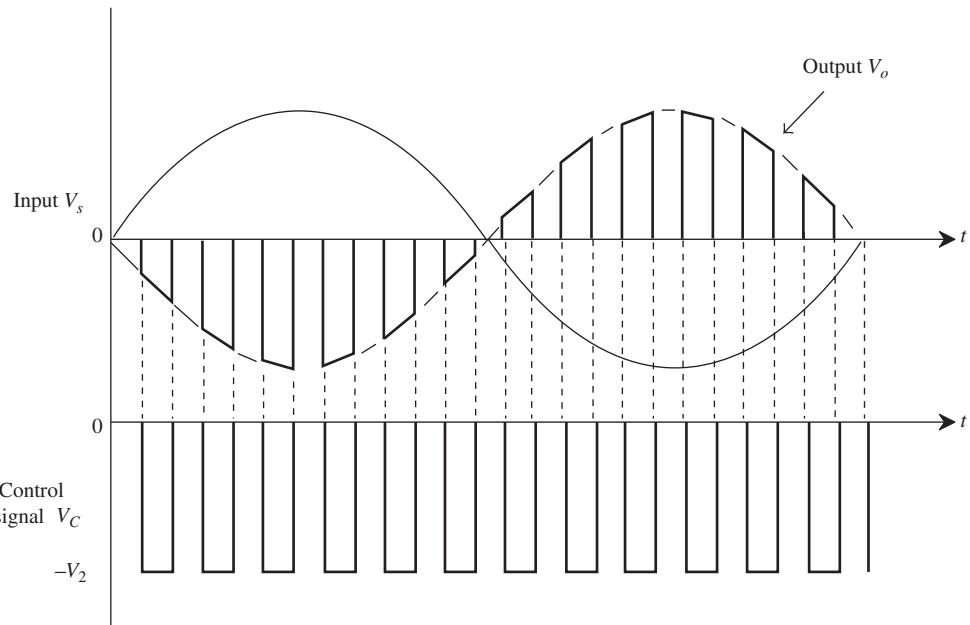


FIGURE 11.26(b) The waveform of a sampling gate in which FET is used as a switch and op-amp as an inverting amplifier

The advantage of this sampling gate is that the signal may be amplified to a desired level. The output resistance is very low and the input resistance is R_1 . As such R_1 can be appropriately chosen to have the desired input resistance.

11.5 APPLICATIONS OF SAMPLING GATES

Sampling gates find applications in many circuits. Sampling gates are used in multiplexers, D/A converters, chopper stabilized amplifiers, sampling scopes, etc. Here, the three specific applications of the sampling gates in: chopper stabilized amplifier; sampling scope and time division multiplexer are discussed.

11.5.1 Chopper Stabilized Amplifiers

Sometimes it becomes necessary to amplify a signal v that has a very small dv/dt and that the amplitude of the signal itself is very small, typically of the order of milli-volts. Neither, ac amplifiers using large coupling condensers nor dc amplifiers with the associated drift would be useful for such an application. A chopper stabilized amplifier employing sampling gates can be a useful option in such an application, as shown in Fig. 11.27(a).

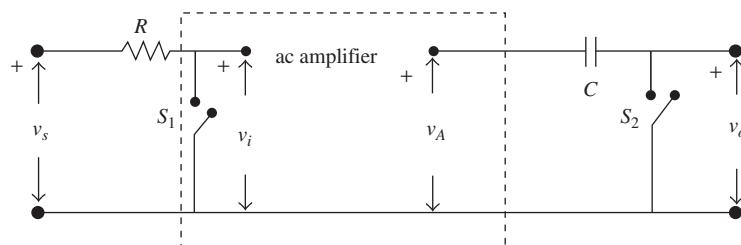


FIGURE 11.27(a) A chopper stabilized amplifier

Let the input v_s to the amplifier be a slowly varying sinusoidal signal. Switch S_1 and S_2 open and close synchronously at a fast rate i.e., the switching frequency is significantly larger than the signal frequency. When S_1 is open, v_i is the same as v_s . When S_1 is closed, $v_i = 0$. As the switching frequency is large, the samples are taken at smaller time intervals. With the result, the signal v_i contains pulses with almost flat tops and have the same amplitude of the input signal as is available at the instant of sampling. As a result, the input of the amplifier v_i is a chopped signal— R and S_1 constitute the chopper. Hence, v_i can be described as a square wave at the switching frequency (if dv/dt is small), i.e., amplitude modulated by the input signal and superimposed on a signal (dashed line) that is proportional to v_s . The waveform v_A at the amplifier output is an amplitude modulated square wave, as shown in Fig. 11.27(b). Hence, a chopper is also called a modulator.

Let S_1 and S_2 operate in synchronism. During $t = T_1$, the negative going component of v_A is zero and during $t = T_2$ the positive going component is zero. Also, because of the amplifier, v_o is greater than v_i in amplitude. Except for this change, v_A is similar to v_i , as shown in Fig. 11.27(c). This signal is passed through a low pass filter which eliminates the square wave and retrieves the original signal. If S_2 opens when S_1 is closed, the output is shifted in phase by 180° , as shown in Fig. 11.27(d). C and S_2 constitute a synchronous detector. The chopper eliminates the need for a dc stabilized amplifier. This amplifier is called a chopper stabilized amplifier.

11.5.2 Sampling Scopes

Another application of a sampling gate is in a sampling scope used to display very fast periodic waveforms, having a rise time of the order of nano-seconds. A general purpose CRO may be used for displaying such waveforms. However, a CRO needs a wideband amplifier. A sampling scope eliminates the use of the high gain wideband amplifier. The basic principle of a sampling scope is explained with the aid of a block diagram shown in Fig. 11.28(a) and the waveforms are shown in Fig. 11.28(b).

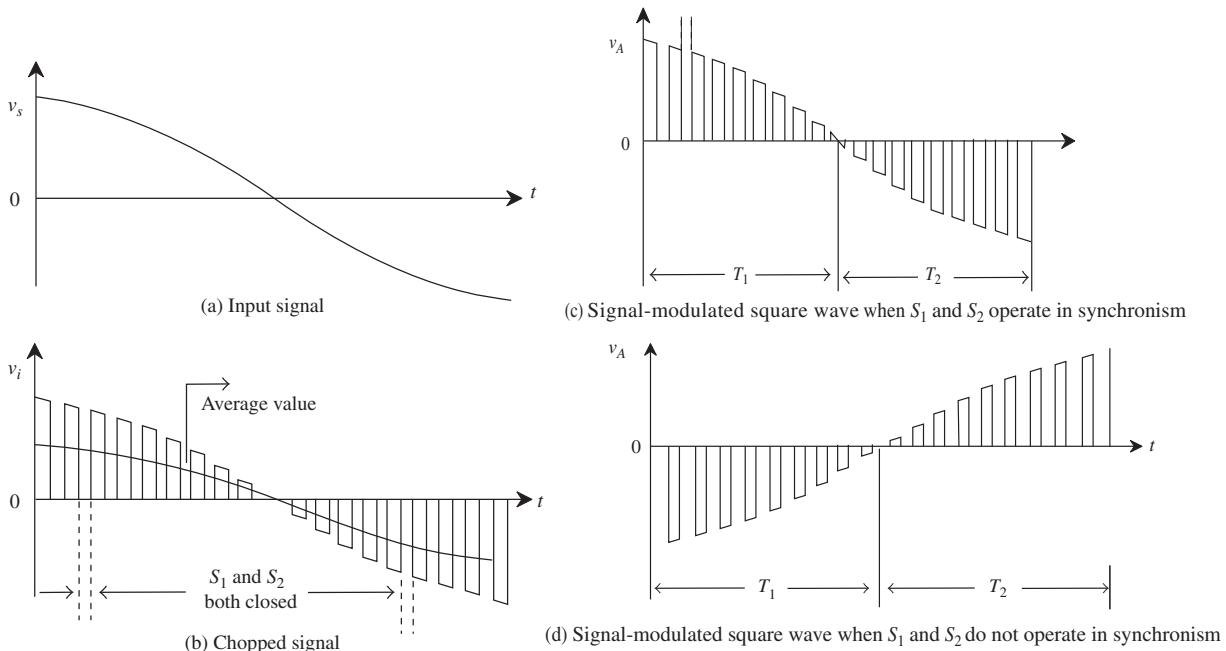


FIGURE 11.27(b) The waveforms of the chopper stabilized amplifier

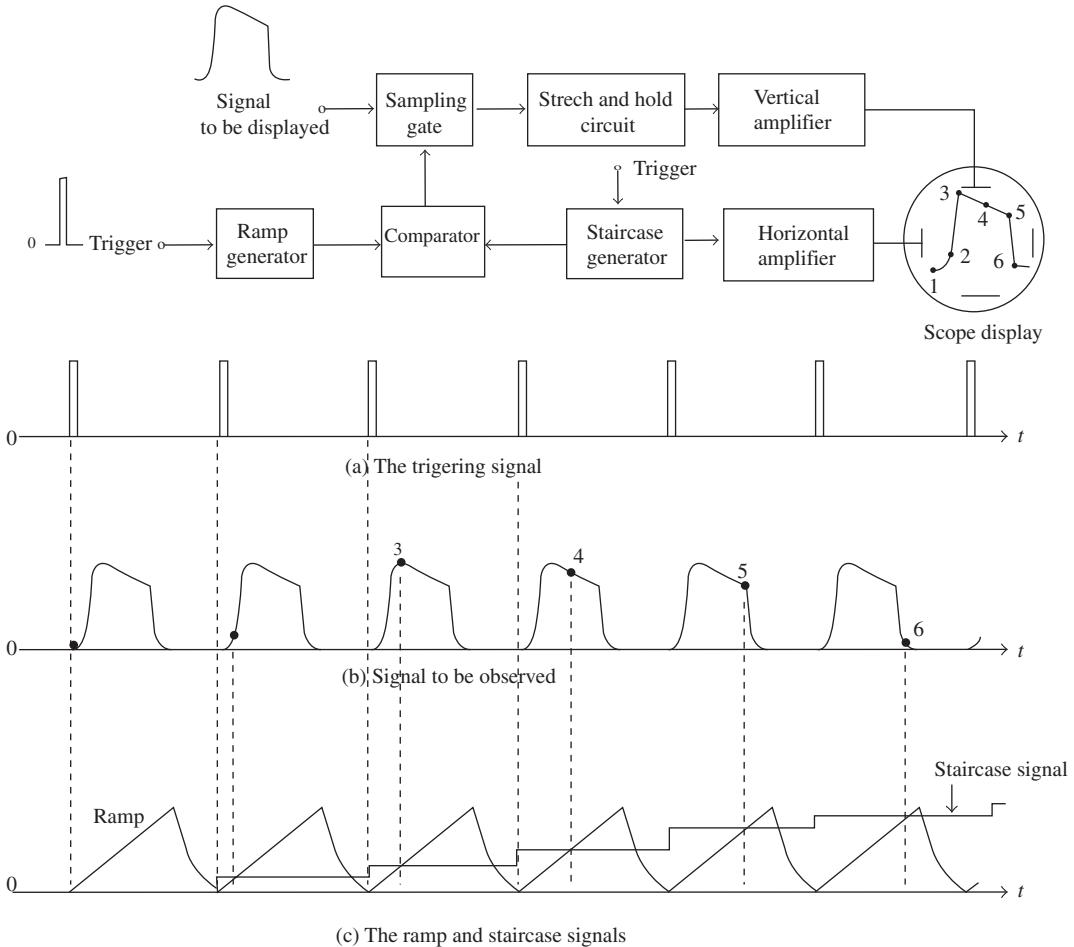


FIGURE 11.28(a) The waveforms that explain the principle of sampling-scope

Let the trigger signals shown in Fig. 11.28(a) occur slightly prior to the occurrence of the pulses that are to be displayed on the screen. These trigger signals trigger ramp and staircase generators. The staircase generator has constant amplitude between the triggers and its amplitude jumps to a higher level at the instant the trigger is present. The amplitude of the staircase generator remains the same till the presence of the next trigger. The inputs to the comparator are the staircase and ramp signals. The instant the ramp reaches the amplitude of the staircase signal; a pulse is produced at the output of the comparator. This pulsed output of the comparator is used as the control signal for the sampling gate. When a control signal is present, the gate transmits a sample of the signal to the vertical amplifier whose amplitude is the same as that of the signal at the instant of sampling and has the same duration as the control signal. Points 1, 2, ..., 6 are the instants at which the samples are taken. The output of the staircase generator is connected to the horizontal deflecting plates.

When one sample is taken, say at instant 1, to go to the next sample, i.e., sample 2, the amplitude of sample 1 should be held constant till the next trigger pulse arrives. Therefore, it becomes necessary to hold the amplitude of the input signal between successive triggers and hence, the need for a stretch and hold circuit. The staircase generator moves the spot horizontally across the screen in steps and at each step the spot is deflected vertically proportional to the signal amplitude. The CRT beam is blanked normally and is un-blanked only at the time of display of the sample. Thus, the signal is represented by a series of dots.

11.5.3 Multiplexers

An analog time division multiplexer using a sampling gate is shown in Fig. 11.29(a). In the FET Q_1 , Q_2 and Q_3 are ON when the control voltages V_{C1} , V_{C2} and V_{C3} are at 0 V. The voltage V is more negative than the pinch off voltage of the FET. As such the FET is OFF when the gate voltage is V . During the period 0 to T_1 , V_{C1} is such that Q_1 is ON. At the same time Q_2 and Q_3 are OFF. Hence, input V_{s1} , which is the sinusoidal signal is present at the output during this period. During the period T_1 to T_2 , Q_2 is ON and Q_1 and Q_3 are OFF. Hence, only V_{s2} is present at the output during this period. During the period T_2 to T_3 , Q_3 is only ON and hence, V_{s3} is present at the output. The output now contains all the input signals separated by a specific time interval, as shown in Fig. 11.29(b).

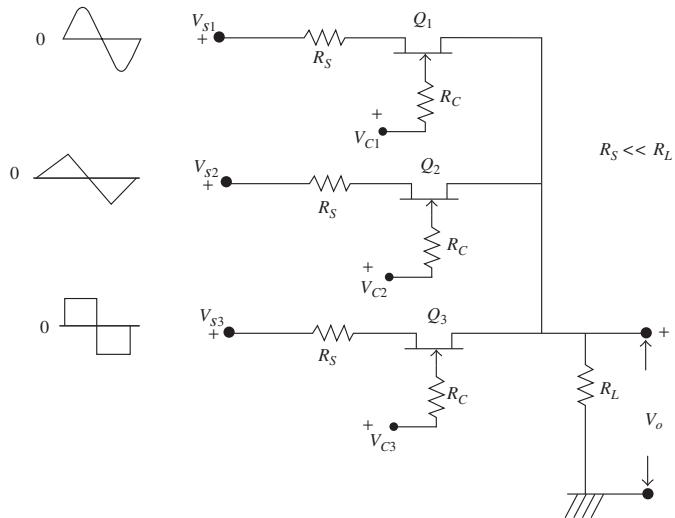


FIGURE 11.29(a) The sampling gate used for time division multiplexing

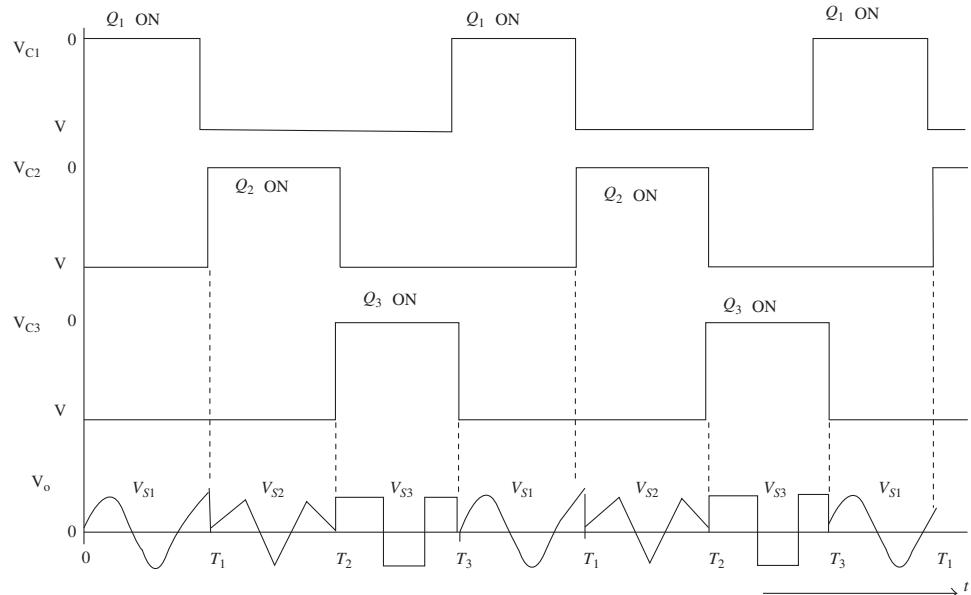


FIGURE 11.29(b) The control signals and the output of the multiplexer

S O L V E D P R O B L E M S

Example 11.5: In the circuit shown in Fig. 11.16(a), $R_L = R_1 = 200 \text{ k}\Omega$, $R_2 = 100 \text{ k}\Omega$ and the signal has a peak value of 10 V. Find (a) A (b) $V_{C(\min)}$ (c) $V_{n(\min)}$ (d) R_i

Solution:

(a)

$$A = \frac{\alpha}{1 + \alpha(R_1/2R_L)}$$

$$\alpha = \frac{R_2}{R_1 + R_2} = \frac{100}{200 + 100} = \frac{1}{3}$$

$$\frac{R_1}{2R_L} = \frac{200}{2 \times 200} = \frac{1}{2}$$

Therefore,

$$A = \frac{(1/3)}{1 + ((1/3) \times (1/2))} = \frac{(1/3)}{(7/6)} = \frac{1}{3} \times \frac{6}{7} = \frac{2}{7} = 0.285$$

(b)

$$V_{C(\min)} = \frac{R_2}{R_1} \times \frac{R_3}{R_3 + 2R_L} V_s$$

$$R = \frac{R_2 R_1}{R_2 + R_1} = \frac{100 \times 200}{300} = \frac{200}{3} \text{ k}\Omega$$

$$R_3 = R + R_f \approx R = 66.6 \text{ k}\Omega$$

$$V_{C(\min)} = \frac{100}{200} \times \frac{66.6}{66.6 + 2 \times 200} \times 10$$

$$V_{C(\min)} = 0.71 \text{ V}$$

(c)

$$V_{n(\min)} = \frac{-R_2}{R_1} \times V_s = \frac{-100}{200} \times 10 = -5 \text{ V}$$

(d) When the diodes are ON

$$\begin{aligned} R_i &= \frac{R_L R_2}{R_2 + 2R_L} + \frac{R_1}{2} \\ &= \frac{200 \times 100}{100 + 400} + \frac{200}{2} = \frac{200}{5} + 100 = 40 + 100 = 140 \text{ k}\Omega \end{aligned}$$

Example 11.6: For the four-diode gate shown in Fig 11.20(a), $R_L = R_2 = 50 \text{ k}\Omega$ and $R_1 = 1 \text{ k}\Omega$, $R_f = 25 \Omega$, $V_s = 10 \text{ V}$. Calculate (a) A (b) $V_{(\min)}$ (c) $V_{C(\min)}$ (d) for $V = V_{(\min)}$

Solution:

(a) We have

$$R = \frac{R_2 R_1}{R_2 + R_1}, \quad R_3 = R + R_f$$

$$\text{And } \alpha = \frac{R_2}{R_1 + R_2}$$

$$R = \frac{50 \times 1}{51} = 980 \Omega$$

$$\alpha = \frac{50}{51} = 0.98$$

$$R_3 = 980 + 25 = 1005 \Omega$$

and $A = \alpha \times \frac{R_L}{R_L + R_3/2}$. Therefore,

$$A = 0.98 \times \frac{50}{50 + (1.005/2)} = 0.98 \times \frac{50}{50 + 0.502}$$

$$A = 0.97$$

(b)

$$V_{\min} = \frac{R_2}{R_1} \times \frac{R_3}{R_3 + 2R_L} \times V_s$$

$$= \frac{50}{1} \times \frac{1.005 \times 10}{(1.005 + 100)} = \frac{502.5}{101.005} = 4.97 \text{ V}$$

(c)

$$V_{C(\min)} = A V_s = 0.97 \times 10 = 9.7 \text{ V}$$

(d)

$$V_{n(\min)} = V_s \times \frac{R_2}{R_1 + R_2} - V \times \frac{R_1}{R_1 + R_2}$$

Here, $V = V_{(\min)} = 4.97 \text{ V}$

Therefore,

$$V_{n(\min)} = 10 \times \frac{50}{50 + 1} - 4.97 \times \frac{1}{50 + 1} = 9.8 - 0.97 = 9.7 \text{ V}$$

Example 11.7: For the FET series gate shown in Fig. 11.30. $V_s = \pm 1 \text{ V}$, $R_s = 50 \Omega$, $R_L = 20 \text{ k}\Omega$. The FET has the following parameters, $V_{GS(\text{OFF})\max} = -10 \text{ V}$ and $R_{D(\text{ON})} = 20 \Omega$. Calculate the voltage levels of the control signal, I_D , error due to R_s and error due to $R_{D(\text{ON})}$.

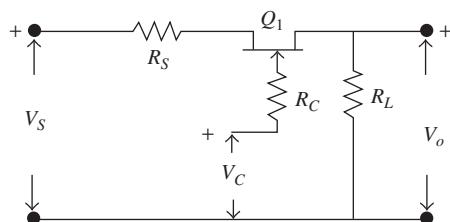


FIGURE 11.30 The FET series gate

Solution:

The control signal should have a value V_1 for Q_1 to be ON.

Therefore, $V_1 = V_{s(\text{peak})} = 1 \text{ V}$.

For Q_1 to be OFF, the control signal should be $-V_2$

$$-V_2 = -[V_{s(\text{peak})} + V_{GS(\text{OFF})\text{max}} + 1 \text{ V}]$$

$$-V_2 = -(1 + 10 + 1) = -12 \text{ V}$$

$$I_D = \frac{V_S}{R_S + R_{D(\text{ON})} + R_L} = \frac{1}{50 + 20 + 20000} = 49.8 \mu\text{A}$$

$$I_D R_S = 49.8 \times 10^{-6} \times 0.05 \times 10^3 = 2.49 \text{ mV}$$

$$\text{Error due to } R_S = \frac{2.49 \text{ mV}}{1 \text{ V}} \times 100\% = 0.249\%$$

$$I_D R_{D(\text{ON})} = 49.8 \mu\text{A} \times 20 \Omega = 0.996 \text{ mV}$$

$$\text{Error due to } R_{D(\text{ON})} = \frac{0.996 \text{ mV}}{1 \text{ V}} \times 100\% = 0.099\%$$

SUMMARY

- A sampling gate is used to transmit a signal faithfully from the input to the output terminals during a specified time interval. This time interval is decided by the external gating signal, also called the control signal.
- Sampling gates are of two types — unidirectional and bidirectional.
- A unidirectional sampling gate transmits a signal of only one polarity, either positive or negative.
- A bidirectional sampling gate transmits signals of both positive and negative polarities.
- Sometimes, in the output of a sampling gate, it is possible to get the signal superimposed on the control signal. Then the signal is said to be on a pedestal which is the part of the control signal available in the output. Pedestal is undesirable in the output.
- A sampling gate can be wired in such a fashion that it will transmit the signal only when a number of gating signals are present simultaneously. Such a sampling gate is called an AND circuit or coincidence circuit.
- It is possible to suppress the pedestal. However, if the gating signals have non-zero rise time and fall time, spikes may be generated at the output.
- A chopper amplifier employs a sampling gate. A chopper amplifier is used to amplify a small signal whose rate of change with time is small.
- A sampling gate is also employed in a sampling scope. A sampling scope is one in which the display consists of a sequence of samples of the input signal. These samples are taken at successively delayed time intervals with respect to a reference on the signal.
- The gain of a sampling gate— A —is defined as the ratio of the output signal to the input signal during the transmission.

MULTIPLE CHOICE QUESTIONS

- (1) A circuit that allows transmission faithfully during a fixed time interval is called a:
 - a) Logic gate
 - b) Flip-flop
 - c) Sampling gate
 - d) Schmitt trigger
- (2) The duration for which signal transmission takes place in a sampling gate is described by a:
 - a) Gating signal
 - b) Exponential signal
 - c) Sinusoidal signal
 - d) Ramp
- (3) A sampling gate that allows the transmission of a signal of only one polarity is called:
 - a) Bidirectional gate
 - b) Unidirectional gate
 - c) Logic gate
 - d) Flip-flop
- (4) A sampling gate that allows the transmission of signals of both positive and negative polarity is called:
 - a) Bidirectional gate
 - b) Unidirectional gate
 - c) Logic gate
 - d) Flip-flop
- (5) The dc voltage present in the output of a sampling gate along with the desired signal is termed as:
 - a) Pedestal
 - b) Noise
 - c) Gain
 - d) None of the above
- (6) A chopper amplifier is employed to amplify:
 - a) Small signals with small dV/dt
 - b) Large signals with large dV/dt
 - c) Small signals with large dV/dt
 - d) Large signals with small dV/dt
- (7) To display the shape of the waveform, some times a sequence of samples delayed in time with respect to a reference point are used in an instrument named as:
 - a) Sweep generator
 - b) Television
 - c) Sampling scope
 - d) None of the above

SHORT ANSWER QUESTIONS

- (1) What is a sampling gate? How does it differ from a logic gate?
- (2) What are unidirectional and bidirectional sampling gates?
- (3) Explain when a pedestal is seen in the output of a sampling gate.

- (4) What is a chopper amplifier? Name its applications.
- (5) Explain the basic principle employed in a sampling scope.

LONG ANSWER QUESTIONS

- (1) Explain with the help of a neat circuit diagram the working of a bidirectional transistor sampling gate. Suggest a circuit that minimizes or eliminates the pedestal.
- (2) Draw the circuit of a bidirectional sampling gate and derive the expression for its gain. Obtain the values of $V_{C(\min)}$ and $V_{n(\min)}$.

- (3) Draw the circuit of a four-diode sampling gate and explain its operation. Derive the expression for (i) $V_{C(\min)}$ and (ii) A .
- (4) Write short notes on
 - (i) Chopper stabilized amplifiers
 - (ii) Sampling scopes
 - (iii) Multiplexers

UNSOLVED PROBLEMS

- (1) In the circuit of Fig. 11.16(a), $R_L = R_1 = 50 \text{ k}\Omega$, $R_2 = 40 \text{ k}\Omega$ and the signal has a peak value of 5 V. Find (i) A (ii) $V_C(\text{min})$ (iii) $V_n(\text{min})$ (iv) R_i .
- (2) For the four-diode gate shown in Fig. 11.20(a), $R_L = R_2 = 150 \text{ k}\Omega$ and $R_1 = 2 \text{ k}\Omega$, $R_f = 25 \Omega$, $V_s = 20 \text{ V}$. Calculate (i) A (ii) $V_{(\text{min})}$ (iii) $V_C(\text{min})$ (iv) for $V = V_{(\text{min})}$ find $V_n(\text{min})$.
- (3) For the four-diode gate as shown in Fig. 11p.3, $V_s = 10 \text{ V}$, $R_f = 50 \Omega$, $R_L = R_C = 200 \text{ k}\Omega$, $R = R_s = 1 \text{ k}\Omega$. Find $V_n(\text{min})$, A and $V_C(\text{min})$.

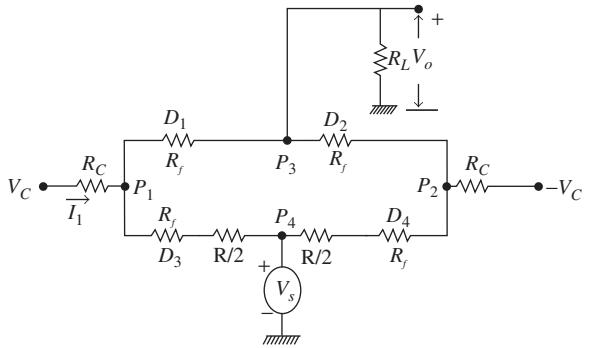


FIGURE 11p.3 The given four-diode gate with balancing resistance

CHAPTER 12

Voltage Sweep Generators

LEARNING OBJECTIVES

After reading this chapter, you will be able to:

- Derive expressions for errors that define deviation from linearity
 - Describe UJTs and transistor sweep generators
 - Describe the circuits that can improve the linearity of the voltage sweep such as Miller integrators and bootstrap sweep generators
 - Design sweep generators using UJT and Miller's and bootstrap sweep circuits
-

12.1 INTRODUCTION

When a time-varying signal, like a sinusoidal signal, is to be displayed on a CRT screen, the signal is applied to the Y -deflecting plates through an amplifier. However, when this time-varying signal is applied to the Y -deflecting plates, what we see on the CRT screen is only a vertical line, because the spot (electron beam) moves only vertically. Though this enables us to measure the peak-to-peak amplitude of the applied signal, this does not allow us to either see its shape or measure its frequency. Thus, to display a time-varying signal on the CRT screen, the spot needs to move linearly along the X -axis as a function of time. The sweep voltage (so called because it sweeps the spot linearly as a function of time along the X -axis) is applied between the pair of X -deflecting plates. The circuit that performs this task is called a sweep generator. A voltage sweep generator works on the principle of electrostatic deflection. The simplest sweep circuit is an exponential sweep generator in which a capacitor is allowed to charge to a supply voltage. However, the resultant sweep voltage is not necessarily linear; consequently, the spot does not always move linearly along the X -axis. To derive a linear sweep voltage, the capacitor needs to be charged with a constant current. The circuits that generate a linear sweep are Miller integrator and bootstrap sweep circuits. Miller integrator and bootstrap sweep circuits have negligible slope error and therefore, it can be said that these sweep generators generate a linear sweep voltage.

Let $X_1 - X_2$ be the horizontal deflecting plates of a CRO. When a voltage of the form shown in Fig. 12.1 is applied, the spot on the screen moves horizontally as the voltage varies linearly with time. As the sweep voltage falls to zero abruptly at t_1 , the spot also abruptly tries to come back to its initial position. Once again, as the voltage rises linearly, the spot also moves horizontally. This process is repeated. Due to persistence of vision, a continuous line is seen on the CRT screen. The applied voltage is called the sweep voltage.

Voltage sweep generators, which work on the principle of electrostatic deflection, are used in CROs, where a smaller deflection of the electron beam is sufficient because of the small screen. The sweep voltage so produced should vary linearly as a function of time. Only when the sweep voltage varies linearly as a function of time, the spot moves equal distances for equal increments in time along the x -axis. The goodness of the sweep is specified by the three errors that define deviation from linearity.

The three types of errors that define deviation from linearity are: (i) slope error or sweep speed error; (ii) displacement error and (iii) transmission error. The smaller these errors; more linear is the sweep voltage. Ideally these errors are zero for a linear sweep. Slope or sweep speed error, (e_s) is defined as the ratio of the difference between the initial and the final slopes to the initial slope, expressed as a percentage. Consider the sweep voltage as shown in Fig. 12.1(a).

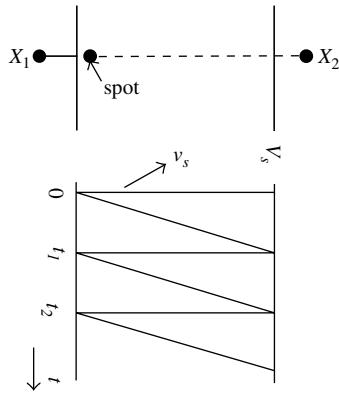


FIGURE 12.1 The sweep voltage applied to X-deflecting plates of a CRO

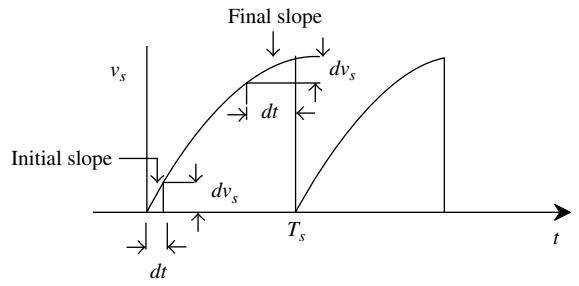


FIGURE 12.1(a) The waveform to calculate the slopes

$$\begin{aligned}
 e_s &= \frac{\text{initial slope} - \text{final slope}}{\text{initial slope}} \\
 &= \frac{\frac{dv_s}{dt} \Big|_{t=0} - \frac{dv_s}{dt} \Big|_{t=T_s}}{\frac{dv_s}{dt} \Big|_{t=0}}
 \end{aligned} \tag{12.1}$$

Displacement error (e_d) is the ratio of the maximum difference between the actual sweep voltage, v_s , and the linear sweep, v'_s , which passes through the initial and the end points of the sweep, to the sweep amplitude, shown in Fig.12.1(b).

$$e_d = \frac{(v'_s - v_s)_{\max}}{V_s} \tag{12.2}$$

Transmission error (e_t): If a ramp voltage is transmitted through a high-pass RC circuit, the output falls away from the input, as shown in Fig.12.1(c).

The transmission error e_t is given as:

$$e_t = \frac{(V'_s - V_s)}{V'_s} \tag{12.3}$$

where, V_s is the amplitude of the actual output; and V'_s is the amplitude of the linear input.

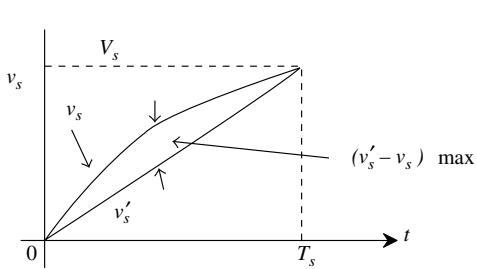


FIGURE 12.1(b) The waveforms to define displacement error

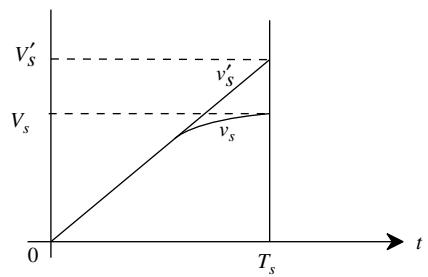


FIGURE 12.1(c) The ramp applied to high-pass circuit and the output

12.2 EXPONENTIAL SWEEP GENERATORS

In a simple voltage sweep generator, a capacitor (C) is allowed to charge to a voltage (V) through a resistance (R) with the time constant, RC , deciding the rate of charge of the condenser. However, as the capacitor charges exponentially, the resultant sweep voltage so generated may tend to be exponential or in other words, not necessarily linear. Thus, there is a need to make arrangements to linearize an exponential sweep. In such arrangements, a constant current is used to charge the capacitor.

The three types of voltage sweep generators considered in this chapter include exponential sweep generators, Miller's sweep generators, and bootstrap sweep generators.

A simple exponential sweep generator and its output are shown in Fig. 12.2(a) and (b), respectively. Initially, at $t = 0$, let the capacitor be uncharged. If now the switch S is open, then the capacitor tries to charge to the supply voltage V . At $t = T_s$ (sweep duration), when the voltage across the capacitor is V_s , if the switch is suddenly closed, the voltage across the capacitor, ideally, is expected to abruptly fall to zero.

However, if the resistance offered by the switch is ideally not zero, there is a finite time delay before the signal reaches its initial value. This time delay is called the fly-back time, restoration time or retrace time (T_r), as shown in Fig. 12.2(c).

Normally, $T_r \ll T_s$, so that $T \approx T_s$.

The voltage variation of the sweep voltage v_s is given as:

$$v_s = v_f - (v_f - v_i)e^{-t/\tau}$$

Here, $v_f = V$ and $v_i = 0$. Therefore, $v_s = V - (V - 0)e^{-t/\tau}$

$$v_s = V(1 - e^{-t/\tau}) \quad (12.4)$$

We assume that after an interval T_s , when $v_s = V_s$, the switch closes. Then the charge on the capacitor discharges with a negligible time constant and the voltage abruptly falls to zero at $t = T_S$. From Eq. (12.4), we have:

$$\frac{dv_s}{dt} = -Ve^{-t/\tau}(-\frac{1}{\tau}) = \frac{V}{\tau}e^{-t/\tau}$$

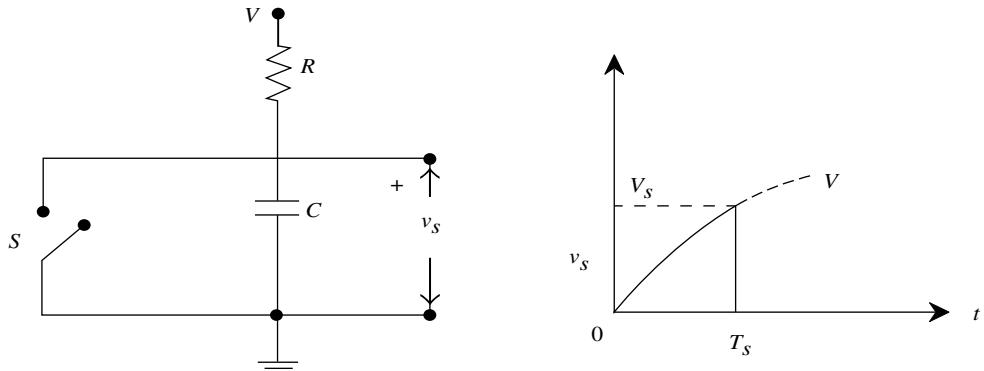


FIGURE 12.2(a) A simple exponential sweep generator; and (b) output of the sweep generator

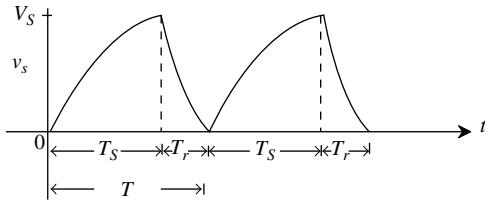


FIGURE 12.2(c) The waveform that depicts the sweep time and restoration time

The initial slope is:

$$\left. \frac{dv_s}{dt} \right|_{t=0} = \frac{V}{\tau}$$

The final slope is:

$$\left. \frac{dv_s}{dt} \right|_{t=T_S} = \frac{V}{\tau} e^{-T_S/\tau}$$

Therefore,

$$e_s = \frac{\frac{V}{\tau} - \frac{V}{\tau} e^{-T_S/\tau}}{\frac{V}{\tau}} = \left[1 - e^{-T_S/\tau} \right] \quad (12.5)$$

From Eq. (12.4), at $t = T_S$, $v_s = V_s$:

Hence,

$$V_s = V \left(1 - e^{-T_S/\tau} \right) \quad (12.6)$$

$$1 - e^{-T_S/\tau} = \frac{V_s}{V} \quad (12.7)$$

Substituting Eq. (12.7) in Eq. (12.5) we get:

$$e_s = \frac{V_s}{V} \quad (12.8)$$

From Eq. (12.8), it is evident that e_s is small when $V >> V_s$, i.e., linearity improves only if the supply voltage (V) is large when compared to V_s , the sweep amplitude. Therefore, the disadvantage of a simple exponential sweep is that a linear sweep is generated only when the sweep amplitude is much smaller than the applied supply voltage, V . For example if $V_s = 20$ V, $V = 100$ V

$$e_s = \frac{V_s}{V} = \frac{20}{100} \times 100\% = 20\%$$

And if $V_s = 20$ V, $V = 1000$ V

$$e_s = \frac{V_s}{V} = \frac{20}{1000} \times 100\% = 2\%$$

The above illustration explains that, for the same sweep amplitude, the smaller is the supply voltage the larger is the slope error. If the supply voltage is increased, the slope error decreases, which means linearity improves.

If $t/\tau \ll 1$

$$e^{-t/\tau} = 1 - \frac{t}{\tau} + \frac{t^2}{2\tau^2} - \frac{t^3}{6\tau^3} + \dots$$

We have from Eq.12.4:

$$\begin{aligned} v_s &= V(1 - e^{-t/\tau}) = V \left[1 - 1 + \frac{t}{\tau} - \frac{t^2}{2\tau^2} + \frac{t^3}{6\tau^3} \dots \right] \\ &= \frac{Vt}{\tau} \left[1 - \frac{t}{2\tau} + \frac{t^2}{6\tau^2} \right] \end{aligned} \quad (12.9)$$

Since $v_s = V'_s$ at $t = T_s$, for a linear sweep, then to the first approximation.

$$V'_s = \frac{VT_s}{\tau} \quad (12.10)$$

As this is a linear sweep:

$$e_s = \frac{V'_s}{V} = \frac{T_s}{\tau} \quad (12.11)$$

Hence, for e_s to be small, $\tau \gg T_s$, i.e., the time constant employed in the circuit should be much larger than the sweep duration. If the actual sweep is non-linear, consider the first two terms given in Eq. (12.9):

$$v_s = \frac{Vt}{\tau} \left(1 - \frac{t}{2\tau} \right) \quad (12.12)$$

Therefore, at: $t = T_s$:

$$V_s = \frac{VT_s}{\tau} \left(1 - \frac{T_s}{2\tau} \right) \quad (12.13)$$

This is a non-linear sweep. Hence, the transmission error e_t is:

$$e_t = \frac{V'_s - V_s}{V'_s}$$

Where V'_s is the amplitude of the linear sweep and V_s is the amplitude of the non-linear sweep.

$$\begin{aligned} \therefore e_t &= \frac{\frac{VT_s}{\tau} - \frac{VT_s}{\tau} \left(1 - \frac{T_s}{2\tau} \right)}{\frac{VT_s}{\tau}} \\ e_t &= \frac{T_s}{2\tau} \end{aligned} \quad (12.14)$$

From Eq. (12.11) we have:

$$e_s = \frac{T_s}{\tau}$$

If we relate e_s and e_t :

$$e_t = \frac{T_s}{2\tau} = \frac{e_s}{2} \quad (12.15)$$

Displacement error, e_d is:

$$e_d = \frac{(v'_s - v_s)_{\max}}{V_s}$$

From Eq. (12.12)

$$v_s = \frac{Vt}{\tau} \left(1 - \frac{t}{2\tau}\right) \quad v'_s = \frac{Vt}{\tau} \quad (v'_s - v_s) = \frac{Vt}{\tau} \times \frac{t}{2\tau}$$

The deviation is maximum at $t = (T_s/2)$

Therefore,

$$(v'_s - v_s)_{\max} = \frac{VT_s}{2\tau} \times \frac{T_s}{4\tau}$$

At

$$t = T_s \quad v'_s = V_s$$

Therefore,

$$V_s = \frac{VT_s}{\tau}$$

Therefore,

$$e_d = \frac{(v'_s - v_s)_{\max}}{V_s} = \frac{\frac{VT_s}{2\tau} \times \frac{T_s}{4\tau}}{\frac{VT_s}{\tau}} = \frac{T_s}{8\tau}$$

$$e_d = \frac{1}{8} e_s \quad (12.16)$$

From Eqs. (12.15) and (12.16), the interrelationship between the three types of errors is given as:

$$e_d = \frac{1}{8} e_s = \frac{1}{4} e_t \quad (12.17)$$

If we calculate one type of error, we can calculate the other types of errors also. If the capacitor is charged with a current I , the voltage across the capacitor C is $(I/C)t$. The rate of change of the voltage with time is called sweep speed. Therefore, sweep speed = I/C .

In the sweep generator described in Fig. 12.2(a), a switch S , which switches ON and OFF automatically at predetermined voltage levels, is used. The physical form of this switch could be a unijunction transistor (UJT).

12.2.1 A Voltage Sweep Generator Using a UJT

A UJT and its dc circuit are shown in Figs. 12.3(a) and (b), respectively. A UJT consists of an n -type semiconductor bar with leads B_1 and B_2 drawn. The emitter is composed of a heavily doped p -type material. Let a bias voltage, V_{BB} , be applied. R_{B1} is the resistance offered by the semiconductor bar from the emitter to base 1 and R_{B2} is the resistance offered by the semiconductor bar from the emitter to base 2.

From Fig. 12.3(b) we have:

$$V_1 = V_{BB} \frac{R_{B1}}{R_{B1} + R_{B2}}$$

$$= V_{BB} \frac{R_{B1}}{R_{BB}} = \eta V_{BB} \quad (12.18)$$

where $R_{BB} = (R_{B1} + R_{B2})$ and $\eta = (R_{B1}/R_{BB})$ is the intrinsic stand-off ratio (lies between 0.6 and 0.8).

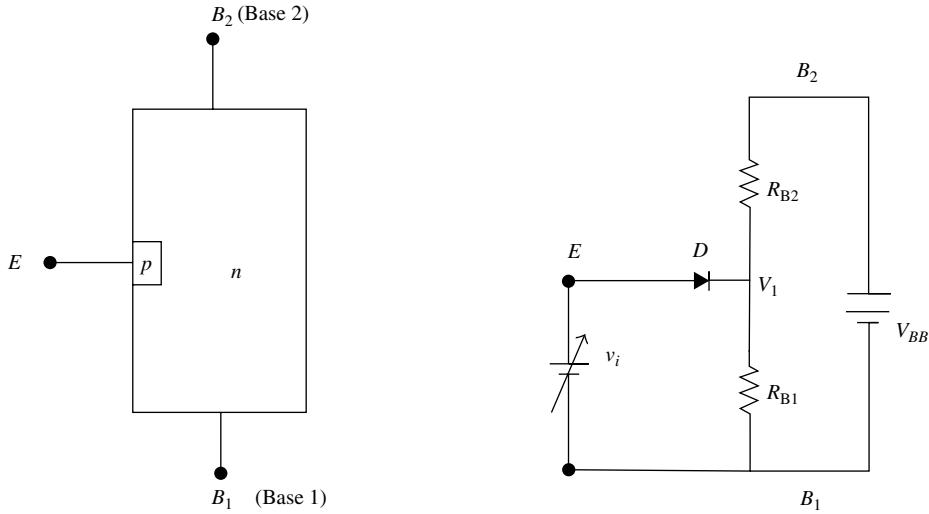


FIGURE 12.3(a) A unijunction transistor; and (b) its dc circuit

The *p*-type emitter and *n*-type semiconductor behave as a *p*–*n* junction diode, *D*. As long as $v_i < \eta V_{BB}$, *D* is OFF. When $v_i \geq \eta V_{BB}$, *D* is ON and a large number of charge carriers exist on the *n*-side, thus, reducing the resistance. The device conducts heavily and the switch *S* is said to be closed. The V–I characteristic of a UJT is shown in Fig. 12.3(c). From the characteristic shown in Fig. 12.3(c), it is seen that the UJT is ON when $v_i = V_P$, called the peak voltage, and is OFF when $v_i = V_V$, called the valley voltage. The device switches ON or OFF at predefined voltage levels. A practical UJT sweep generator is shown in Fig. 12.4(a) and its output is shown in Fig. 12.4(b). Initially, let the capacitor be uncharged. Once the power is ON, the voltage across the capacitor rises exponentially as:

$$v_s = V_{BB} (1 - e^{-t/\tau}) \quad (12.19)$$

At $t = T_s$, $v_s = \eta V_{BB}$

$$\eta V_{BB} = V_{BB} (1 - e^{-T_s/\tau}) \quad V_{BB} e^{-T_s/\tau} = V_{BB} (1 - \eta) \quad (12.20)$$

$$T_s = \tau \ln \frac{1}{(1 - \eta)}$$

Alternately,

$$v_s = v_f - (v_f - v_i) e^{-t/\tau}$$

We have, from Fig. 12.4(b), $v_i = V_V$ and $v_f = V_{BB}$

Therefore,

$$v_s = V_{BB} - (V_{BB} - V_V) e^{-t/\tau}$$

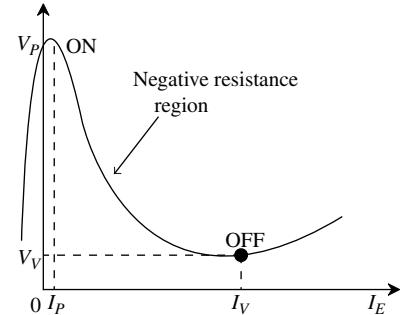


FIGURE 12.3(c) The V–I characteristic of a UJT

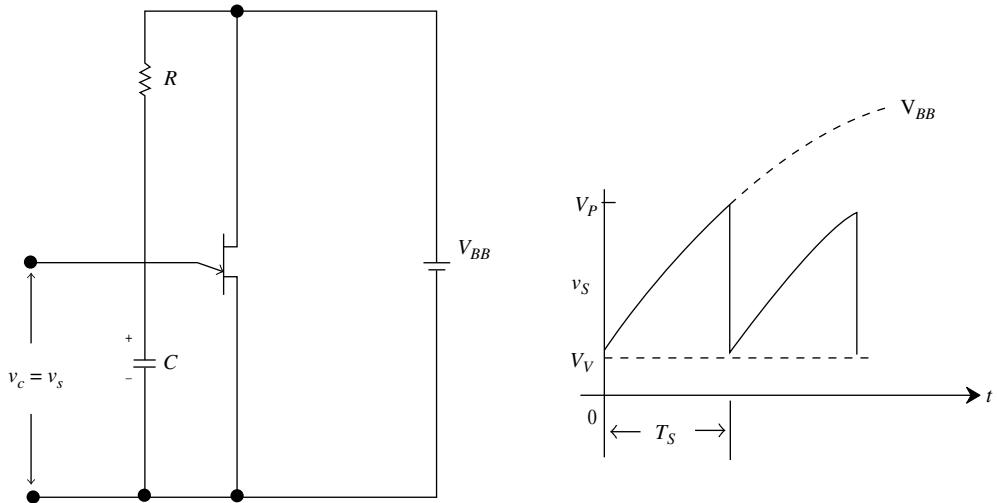
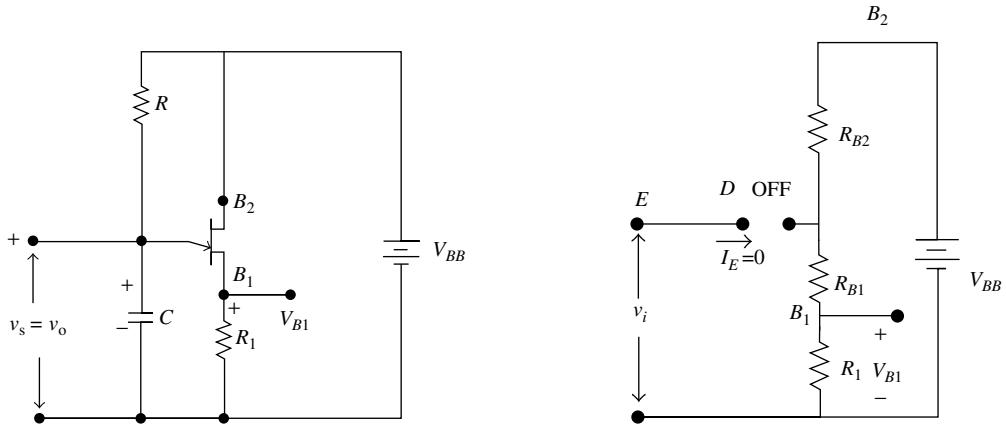


FIGURE 12.4(a) A practical UJT sweep generator; (b) its output

FIGURE 12.5(a) The resistance R_1 is added to generate positive spikesFIGURE 12.5(b) The circuit to calculate V_{B1} during the charging period

$$\text{At } t = T_s, v_s = V_P \quad V_P = V_{BB} - (V_{BB} - V_V)e^{-T_s/\tau}$$

$$T_s = \tau \ln \frac{(V_{BB} - V_V)}{(V_{BB} - V_P)} \quad (12.21)$$

Equations (12.20) and (12.21) give the sweep duration.

A small resistance (R_1), as shown in Fig. 12.5(a), can be now included to derive a positive spike at B_1 , which can then be used to trigger some other circuit. The circuit, when the UJT is OFF (during the charging period), from which V_{B1} is calculated is shown in Fig. 12.5(b).

From the circuit shown in Fig. 12.5(b), we have:

$$V_{B1} = V_{BB} \times \frac{R_1}{R_1 + R_{B1} + R_{B2}} = V_{BB} \times \frac{R_1}{R_1 + R_{B2}}$$

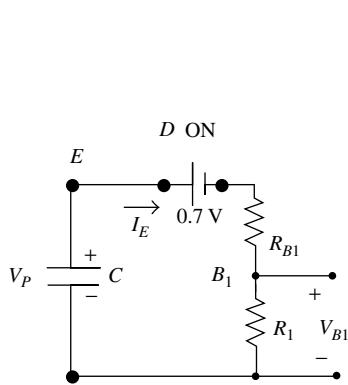


FIGURE 12.5(c) The circuit to calculate V_{B1} when the UJT is ON

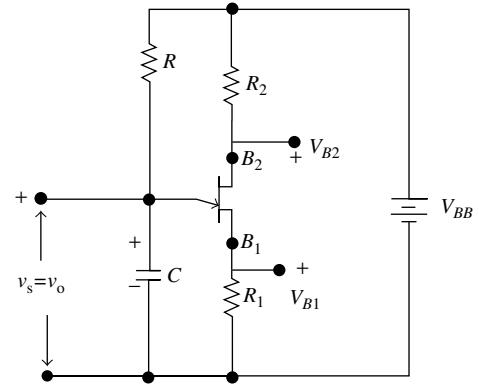


FIGURE 12.5(d) A UJT circuit to generate positive and negative spikes at B_1 and B_2

The circuit when the UJT is ON (during the discharge period), from which V_{B1} is calculated is shown in Fig. 12.5(c).

From the circuit shown in Fig. 12.5(c), V_{B1} is calculated as:

$$V_{B1} = (V_p - 0.7) \times \frac{R_1}{R_1 + R_{B1}}$$

If negative spikes are also to be generated, a resistance R_2 which is reasonably larger than R_1 is connected to B_2 , as shown in Fig. 12.5(d). The resultant waveforms are plotted as shown in Fig. 12.5(e).

In the waveform shown in Fig. 12.5(e), the output v_s is assumed to fall abruptly to V_V at T_s . In practice, however, there will be a finite retrace time, as an additional resistance R_1 is connected to B_1 . So, there is a need to calculate T_r to be able to calculate the time period (T) of the sweep ($= T_s + T_r$), as shown in Fig. 12.5(f). The output voltage for $t > T_s$ is given as:

$$v_s(t > T_s) = V_p e^{-t/(R_{B1}+R_1)C}$$

At $t = T_r$, $v_s = V_V$.

$$V_V = V_p e^{-T_r/(R_{B1}+R_1)C}$$

Therefore,

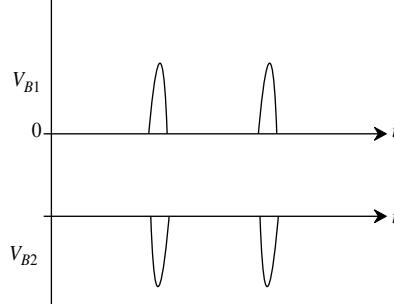
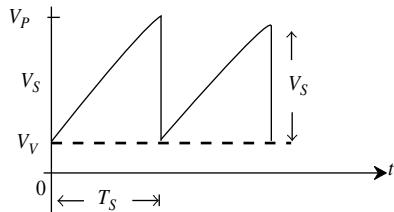
$$T_r = (R_{B1} + R_1) C \ln \frac{V_p}{V_V} \quad (12.22)$$

From Eq. (12.21), we have:

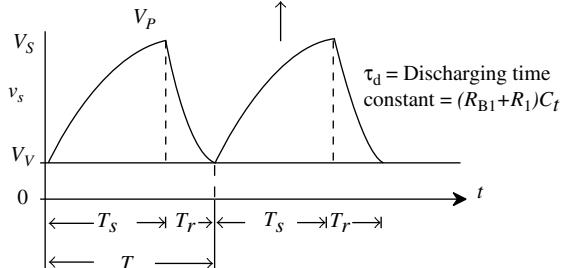
$$T_s = \tau_c \ln \frac{(V_{BB} - V_V)}{(V_{BB} - V_p)}$$

Combining Eqs. (12.21) and (12.22), we now have the total time period, $T = T_s + T_r$.

The design of an exponential sweep generator using UJT as the switch is illustrated in Example 12.1.

FIGURE 12.5(e) The voltages at B_1 and B_2 and V_o

$$\tau_C = \text{Charging time constant} = RC$$



$$\tau_d = \text{Discharging time constant} = (R_{B1} + R_1)C_t$$

EXAMPLE

Example 12.1: Design a relaxation oscillator using a UJT, with $V_V = 3$ V, $\eta = 0.68$ to 0.82 , $I_P = 2\mu\text{A}$, $I_V = 1$ mA, $V_{BB} = 20$ V, the output frequency is to be 5 kHz. Calculate the typical peak-to-peak output voltage.

Solution: The given UJT has the following parameters:

$$V_V = 3 \text{ V}, I_P = 2 \mu\text{A}, I_V = 1 \text{ mA}, \eta = 0.68 \text{ to } 0.82$$

$$\eta_{ave} = \frac{0.68 + 0.82}{2} = 0.75 \quad V_P = V_F + \eta V_{BB}$$

Therefore,

$$V_P = 0.7 + (0.75)(20) = 15.7 \text{ V}$$

$$R_{\max} = \frac{V_{BB} - V_P}{I_P} = \frac{20 - 15.7}{2 \mu\text{A}} = 2.15 \text{ M}\Omega \quad R_{\min} = \frac{V_{BB} - V_V}{I_V} = \frac{20 - 3}{1 \text{ mA}} = 17 \text{ k}\Omega$$

Thus, R must be in the range $17 \text{ k}\Omega$ to $2.15 \text{ M}\Omega$. If R is large, C must be very small. Therefore, choose R such that C is not very small.

Choosing $R = 22 \text{ k}\Omega$

$$T = \frac{1}{f} = \frac{1}{5 \times 10^3 \text{ Hz}} = 200 \mu\text{s} \quad T = RC \ln \frac{V_{BB} - V_V}{V_{BB} - V_P}$$

$$C = \frac{T}{R \ln \frac{20 - 3}{20 - 15.7}} = \frac{200 \mu\text{s}}{22 \times 10^3 \ln \frac{17}{4.3}} = 6600 \text{ pF}$$

Choose $C = 6800 \text{ pF}$ (a standard value)

Peak-to-peak sweep amplitude = $15.7 - 3 = 12.7 \text{ V}$.

12.2.2 Generation of Linear Sweep Using the CB Configuration

The sweep voltage generated by an exponential sweep generator is non-linear as the current in the capacitor varies exponentially. However, to generate a linear sweep, the capacitor is required to charge with a constant current. As discussed in the earlier chapters, the collector current in the CE configuration may not remain constant with the variation in V_{CE} . However, from the output characteristics of the CB configuration shown in Fig. 12.6, we see that for a constant value of I_E , I_C is independent of V_{CB} and the curves are parallel to the V_{CB} axis, except for a small range of values of V_{CB} .

As can be seen from Fig. 12.6, I_C remains practically constant with the variation in V_{CB} , except, at smaller values of V_{CB} . This suggests that if a capacitor is charged using the constant collector current of the CB configuration, the resultant sweep voltage must be a linear sweep voltage. Fig. 12.7(a) shows the circuit of a transistor constant current sweep generator using the CB configuration.

From Fig. 12.7(a), the current I_E in the base loop is:

$$I_E = \frac{V_{EE} - V_{EB}}{R_E}$$

Let the switch S be open at $t = 0$. The collector current is constant and is given by the relation: $I_C = h_{FB}I_E$. Hence, C charges with the constant I_C and the voltage across the capacitor varies linearly as a function of time. To determine the sweep voltage V_s , let us consider the small signal model of the transistor in the CB configuration as shown in Fig. 12.7(b).

Writing the KVL equation of the input loop:

$$V_i = I_e (R_E + h_{ib}) + h_{rb}v_s \quad (12.23)$$

Writing the KCL equation at the output node C :

$$I_c = h_{fb}I_e - h_{ob}v_s = C \frac{dv_s}{dt}$$

$$h_{fb}I_e - h_{ob}v_s = C \frac{dv_s}{dt} \quad (12.24)$$

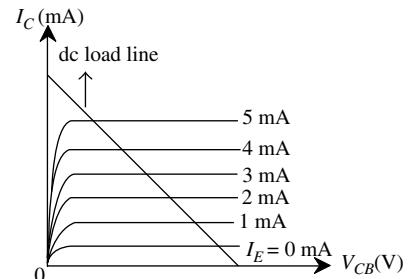


FIGURE 12.6 The output characteristics of the CB configuration

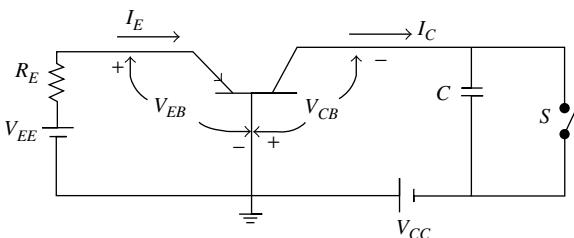


FIGURE 12.7(a) The CB constant current sweep generator

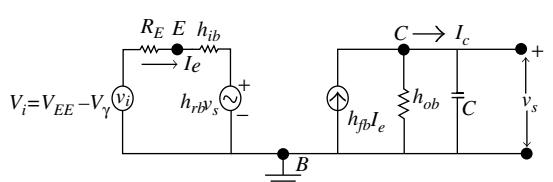


FIGURE 12.7(b) The equivalent circuit of Fig. 12.7(a)

From Eq. (12.23):

$$I_e = \frac{V_i - h_{rb}v_s}{R_E + h_{ib}}$$

Substituting this value of I_e in Eq.(12.24):

$$\frac{Cd v_s}{dt} = h_{fb} \left[\frac{V_i - h_{rb}v_s}{R_E + h_{ib}} \right] - h_{ob}v_s$$

Therefore,

$$\frac{dv_s}{dt} + \frac{1}{C} \left[h_{ob} + \frac{h_{fb}h_{rb}}{(R_E + h_{ib})} \right] v_s = \frac{h_{fb}V_i}{C(R_E + h_{ib})}$$

Let

$$\alpha = h_{fb} \quad \text{and} \quad \frac{1}{\tau} = \left(h_{ob} + \frac{\alpha h_{rb}}{R_E + h_{ib}} \right) \frac{1}{C} \quad (12.25)$$

$$\frac{dv_s}{dt} + \frac{1}{\tau} v_s = \frac{\alpha V_i}{C(R_E + h_{ib})}$$

Let

$$\frac{\alpha V_i}{C(R_E + h_{ib})} = K \quad \frac{dv_s}{dt} + \frac{1}{\tau} v_s = K$$

Applying Laplace transforms:

$$s v_s(s) + \frac{1}{\tau} v_s(s) = \frac{K}{s} \quad v_s(s) \left(s + \frac{1}{\tau} \right) = \frac{K}{s} \quad v_s(s) = \frac{K}{s \left(s + \frac{1}{\tau} \right)} = \frac{A}{s} + \frac{B}{\left(s + \frac{1}{\tau} \right)}$$

Put

$$s = 0$$

Therefore,

$$A = K\tau$$

Put

$$s = -\frac{1}{\tau} \quad B = -K\tau$$

Substituting the values of A and B :

$$v_s(s) = \frac{K\tau}{s} - \frac{K\tau}{\left(s + \frac{1}{\tau} \right)}$$

Taking inverse Laplace transform on both sides:

$$v_s(t) = K\tau \left(1 - e^{-t/\tau} \right)$$

Putting the value of K :

$$v_s(t) = \frac{\alpha\tau V_i}{C(R_E + h_{ib})} \left(1 - e^{-t/\tau} \right) \quad (12.26)$$

Expanding $e^{-t/\tau}$ as series and limiting only to the first two terms of the expansion:

$$v_s(t) = \frac{\alpha\tau V_i}{C(R_E + h_{ib})} \left[1 - \left(1 - \frac{t}{\tau} \right) \right] \quad (12.27)$$

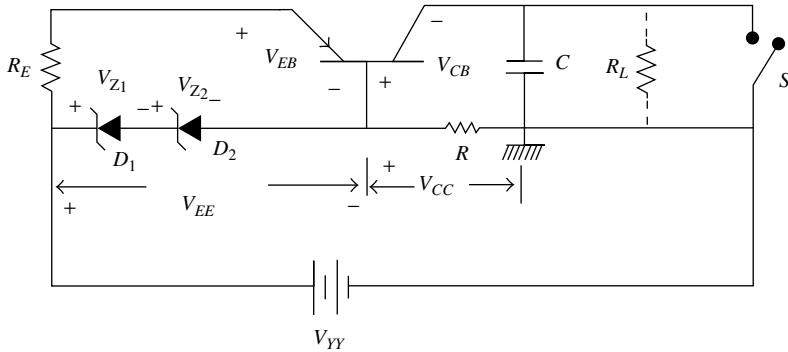


FIGURE 12.8 A constant current sweep with a single supply

Eq. (12.27) reduces to:

$$v_s = \frac{\alpha V_i t}{C (R_E + h_{ib})} \quad (12.28)$$

At $t = T_s$, $v_s = V_s$

Therefore,

$$V_s = \frac{\alpha V_i T_s}{(R_E + h_{ib}) C} \quad (12.29)$$

Therefore,

$$T_s = \frac{C V_s (R_E + h_{ib})}{\alpha V_i} \quad (12.30)$$

where T_s is the sweep duration and V_s the sweep amplitude.

From Eqs. (12.25) and (12.30), we get:

The slope error

$$e_s = \frac{T_s}{\tau} = \left(\frac{C V_s (R_E + h_{ib})}{\alpha V_i} \right) \left[\frac{1}{C} \left(h_{ob} + \frac{\alpha h_{rb}}{R_E + h_{ib}} \right) \right] = \frac{V_s (R_E + h_{ib}) h_{ob}}{\alpha V_i} + \frac{h_{rb} V_s}{V_i}$$

Therefore,

$$e_s = \frac{V_s}{V_i} \left[h_{rb} + \frac{h_{ob}}{\alpha} (R_E + h_{ib}) \right] \quad (12.31)$$

As the second term in the bracket tends to be small, e_s is small. The constant current sweep generator shown in Fig. 12.7(a) is modified such that a single source V_{YY} is used to derive V_{EE} and V_{CC} sources, as shown in Fig. 12.8.

In Fig. 12.8, D_1 and D_2 are Zener diodes. V_{EE} is derived from the V_{YY} source using these diodes such that $V_{EE} = (V_{Z1} + V_{Z2})$ where V_{Z1} and V_{Z2} are the breakdown voltages of D_1 and D_2 . Similarly, the V_{CC} source is also derived using the V_{YY} source (the Zener current through R derives V_{CC}). Hence, a single voltage source is used in the circuit shown in Fig. 12.8 when compared to the circuit shown in Fig. 12.7(a). R_L is the load connected. Example 12.2 highlights the procedure to calculate the slope error of this circuit.

EXAMPLE

Example 12.2: For the circuit shown in Fig. 12.8, it is given that: $V_{YY} = 20$ V, $V_{Z1} = 6.8$ V, $V_{Z2} = 3.8$ V, $h_{rb} = 3 \times 10^{-4}$, $h_{ib} = 20\Omega$, $h_{ob} = 0.5\mu\text{mhos}$, $\alpha = 0.98$ and $R_E = 1\text{k}\Omega$. Find the slope error: (a) when $R_L = \infty$ (b) when $R_L = 200\text{k}\Omega$ and (c) when $R_L = 50\text{k}\Omega$.

Solution:

$$V_{EE} = V_{Z1} + V_{Z2} = 6.8 + 3.8 = 10.6 \text{ V}$$

$$V_{CC} = V_{YY} - V_{EE} = 20 - 10.6 = 9.4 \text{ V}$$

Taking the junction voltages into account, the sweep voltage is:

$$V_s = V_{CC} - V_{BE} = 9.4 - 0.6 = 8.8 \text{ V.}$$

(a) The slope error of a transistor constant current sweep is:

$$e_s = \frac{V_s}{V_i} \left[h_{rb} + \frac{h_{ob}}{\alpha} (R_E + h_{ib}) \right]$$

$$V_i = V_{EE} - V_\gamma = 10.6 - 0.5 = 10.1 \text{ V} \quad \text{and} \quad V_s = 8.8 \text{ V}$$

$$e_s = \frac{8.8}{10.1} \left[3 \times 10^{-4} + \frac{0.5 \times 10^{-6}}{0.98} (1020) \right] \times 100 = \frac{8.8}{10.1} (0.081) = 0.07 \%$$

This error is small and hence, the sweep is linear.

(b) If R_L is connected as the load, then h_{ob} and R_L are in parallel. The effective admittance is :

$$= h_{ob} + \frac{1}{R_L}$$

If $R_L = 200 \text{ k}\Omega$, then the effective admittance:

$$= 0.5 \times 10^{-6} + 0.5 \times 10^{-5} = 5.5 \times 10^{-6} \text{ mhos}$$

$$e_s = \frac{8.8}{10.1} \left[3 \times 10^{-4} + \frac{5.5 \times 10^{-6}}{0.98} (1020) \right] \times 100 = \frac{8.8}{10.1} (0.60) = 0.52\%$$

In this case the slope error becomes large.

$$e_s \approx 0.52 \%$$

(c) $R_L = 50 \text{ k}\Omega$, then the effective admittance

$$= 0.5 \times 10^{-6} + 0.2 \times 10^{-4} = 20.5 \times 10^{-6} \text{ mhos}$$

$$\begin{aligned} e_s &= \frac{8.8}{10.1} \left[3 \times 10^{-4} + \frac{20.5 \times 10^{-6}}{0.98} (1020) \right] \times 100 \\ &= \frac{8.8}{10.1} (2.16) = 1.88\% \end{aligned}$$

In this case, the slope error becomes large.

$$e_s \approx 1.88\%$$

The slope error progressively becomes large as R_L decreases.

12.3 IMPROVING SWEEP LINEARITY

A simple exponential sweep generator shown in Fig. 12.9(a) essentially produces a non-linear sweep voltage, unless $\tau >> T_S$ or $V >> V_s$. In an exponential sweep generator, since the capacitor charges exponentially, the resultant sweep so generated is non-linear. To get a linear sweep, the capacitor is required to charge with a constant current. Let us consider the methods of linearizing an exponential sweep. Introduce an auxiliary generator, v , as shown in Fig. 12.9(b). If v is always kept equal to the voltage across C (i.e., $v = v_C$), as the polarities of v and v_C are opposite, the net voltage in the loop is V . Then $i = V/R$ which is a constant. That means, the capacitor charging current is constant and perfect linearity is achieved. Let us identify three nodes X , Y and Z . In a circuit one terminal is chosen as a reference terminal or the ground terminal. Ground in a circuit is nothing but an arbitrarily chosen reference terminal.

12.3.1 Miller Integrator Sweep Generators

Now let Z be the ground terminal. Then the circuit shown in Fig. 12.9(b) is redrawn as shown in Fig. 12.10(a). Again, redrawing the circuit shown in Fig. 12.10(a) with Z as the ground terminal results in the circuit shown in Fig. 12.10(b). Since v and v_C are equal in magnitude and opposite in polarity, $v_i = 0$. Hence, if the auxiliary generator is replaced by an amplifier with X and Z as the input terminals and Y and Z as output terminals, then the gain A of the amplifier should be infinity. Replacing the auxiliary generator by an amplifier with gain infinity, the circuit shown in Fig. 12.10(b) is redrawn as that shown in Fig. 12.10(c). The sweep generator shown in Fig. 12.10(c) is called the Miller integrator or Miller's sweep.

Slope Error in Miller's Sweep Generator. Consider the Miller's sweep circuit shown in Fig. 12.11(a), in which the auxiliary generator is replaced by an amplifier with gain infinity. Thévenizing the circuit at the input, the Thévenin voltage source and its internal resistance as V' and R' .

$$V' = V \frac{R_i}{R + R_i} = V \frac{1}{1 + \frac{R}{R_i}} \quad (12.32)$$

$$R' = \frac{R \times R_i}{R + R_i} \quad (12.33)$$

The circuit of Fig. 12.11(a) can be redrawn as shown in Fig. 12.11(b).

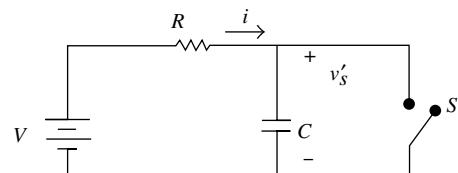


FIGURE 12.9(a) The exponential sweep generator

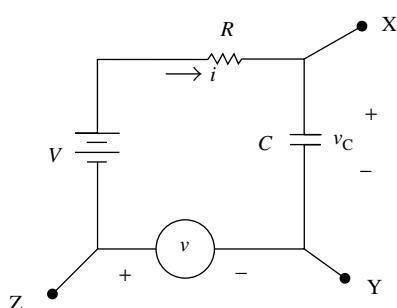


FIGURE 12.9(b) The circuit to derive constant charging current

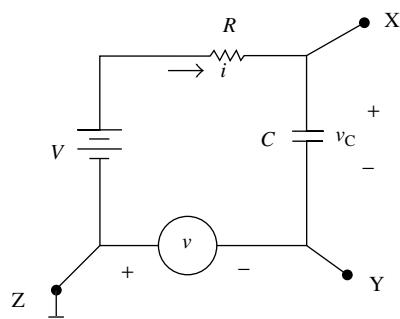


FIGURE 12.10(a) The circuit of Fig. 12.9(b) with Z as ground

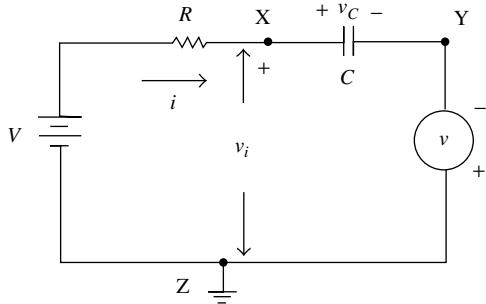


FIGURE 12.10(b) The sweep generator with Z as the ground terminal

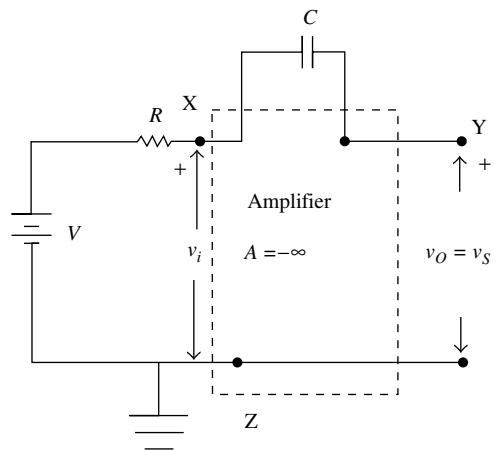


FIGURE 12.10(c) Miller's sweep generator

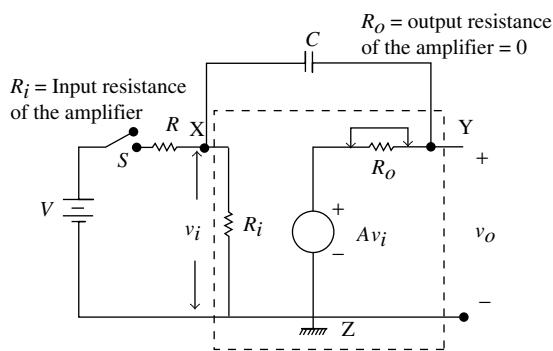


FIGURE 12.11(a) Miller's sweep circuit

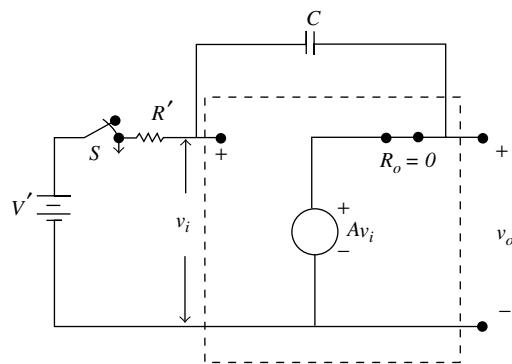


FIGURE 12.11(b) Miller's circuit with Thévenin source and its internal resistance at t = 0

Let $R_o = 0$ At $t = 0$ the voltage across the capacitor is zero. Therefore,

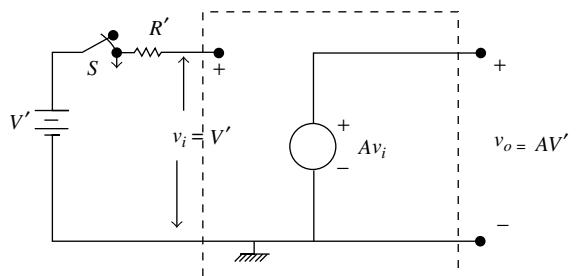
$$v_i - A v_i = 0$$

$$v_i(1 - A) = 0$$

$$v_i = 0$$

$$v_i = A v_i = v_o = 0$$

As $t \rightarrow \infty$, the capacitor is fully charged, hence, no current flows in it. Thus, to calculate the output voltage, the capacitor can be replaced by an open circuit. The resultant circuit is as shown in Fig. 12.11(c).

FIGURE 12.11(c) Miller's circuit as $t \rightarrow \infty$

At

$$t = \infty, v_i = V'$$

Hence,

$$v_o = AV'$$

We know that for an exponential sweep, $e_s = V_s/V$

where V_s is the sweep amplitude

V = total peak-to-peak excursion of the output swing.

In the case of Miller's sweep, the total peak-to-peak excursion of the output swing, $v_o = AV'$.

Hence,

$$e_{s\text{Miller}} = \frac{V_s}{|A|V'} = \frac{V_s}{|A|} \times \frac{1}{V'}$$

Substituting Eq. (12.32) in the equation:

$$\begin{aligned} e_{s\text{Miller}} &= \frac{V_s}{|A|} \times \frac{1 + R/R_i}{V} \\ &= \frac{V_s}{V} \times \frac{1 + R/R_i}{|A|} \end{aligned} \quad (12.34)$$

where, V_s/V is the slope error of the exponential sweep.

Therefore,

$$e_{s\text{Miller}} = e_s \times \frac{1 + R/R_i}{|A|} \quad (12.35)$$

Even if R_i is small, as A is large, the slope error of a Miller's sweep is very small. Hence, for all practical purposes this sweep generator produces a near-linear sweep.

Transistor Miller Sweep Generator. Let us consider the working of the triggered transistor Miller's sweep generator, as shown in Fig. 12.12(a).

- (i) In the quiescent state (before the application of the trigger): The circuit conditions are adjusted such that when the input is not present Q_1 is ON and in saturation. Therefore, the voltage at C_1 (collector of Q_1) is $V_{CE(\text{sat})} \approx 0$. Transistor Q_2 is OFF since $V_{BE2} \approx 0$. The voltage at C_2 (collector of Q_2) is V_{CC} , $v_o = V_{CC}$. The voltage across the capacitor C_s is V_{CC} .
- (ii) When trigger is applied at $t = 0$. When the input signal goes negative, Q_1 is OFF and the voltage at the collector of Q_1 rises; Q_2 is ON and the voltage at its collector is required to decrease abruptly to $V_{CE(\text{sat})}$. Due to the capacitor, the voltage falls almost linearly. The capacitor C_s charges through R_{C1} and the small resistance R_{CS} (saturation resistance) that exists between the collector and emitter terminals of Q_2 , which is driven into saturation as shown in Fig. 12.12(b). Hence, the output voltage decreases linearly from V_{CC} to $V_{CE(\text{sat})}$ in T_s and hence, is a negative-going ramp as shown in Fig. 12.12(d). Depending on the time constant employed, T_s may be less than or equal to T_g .
- (iii) At the end of the trigger: Again at the end of the input pulse, at $t = T_g$, Q_1 goes ON, Q_2 goes OFF and the capacitor discharges through R_{C2} and the output again reaches V_{CC} , as shown in Fig. 12.12(c). The waveforms are shown in Fig. 12.12(d).

(iv) Calculation of T_s :From Fig. 12.12(b), the charging current of C_s :

$$i_C \simeq \frac{V_{CC}}{R_{C1}} \quad v_o(t) = \frac{i_C}{C_s} t = \frac{V_{CC}}{R_{C1}} \times \frac{t}{C_s}$$

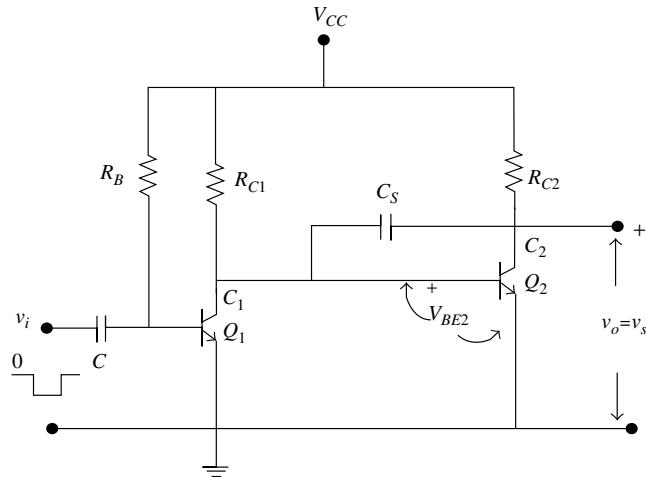
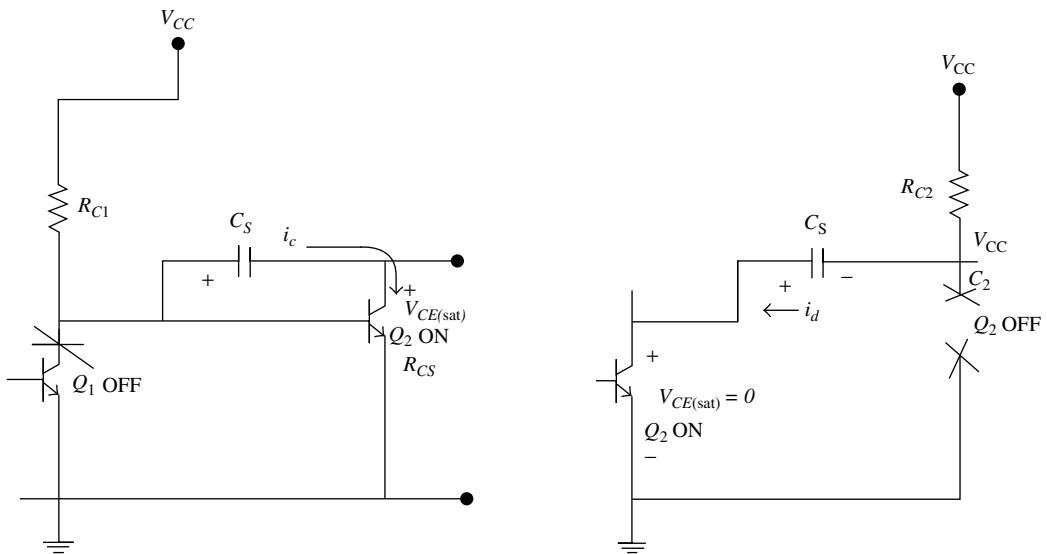


FIGURE 12.12(a) A transistor Miller sweep generator

FIGURE 12.12(b) The circuit of Fig. 12.12(a) when Q_1 is OFF and Q_2 is ONFIGURE 12.12(c) The discharge of C_s when Q_1 is ON and Q_2 is OFF

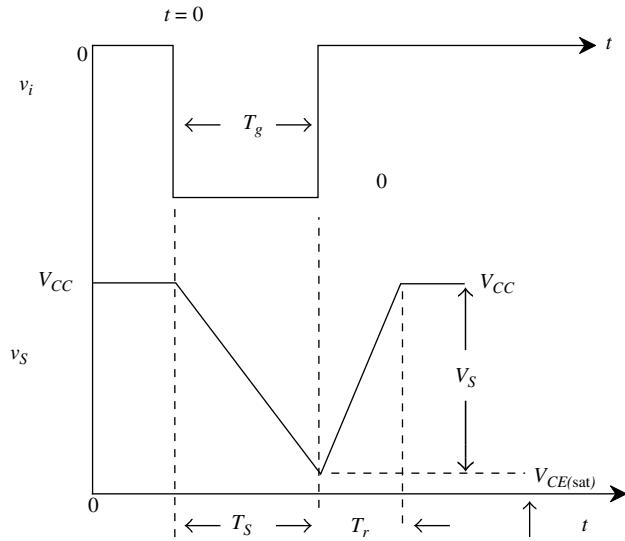
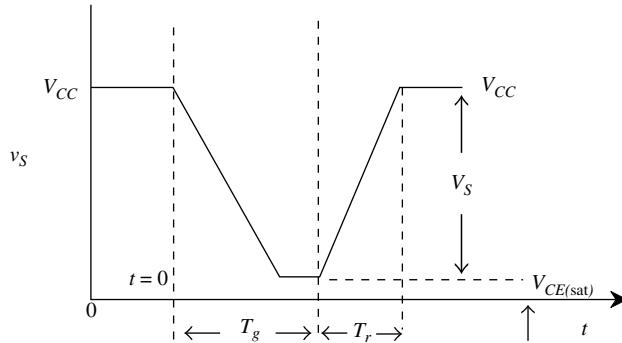
(i) When v_s reaches V_{CC} at T_g (ii) When v_s reaches V_{CC} before T_g

FIGURE 12.12(d) The waveforms of Miller's sweep transistor

At

$$t = T_s, v_o(t) = V_s$$

Therefore,

$$V_s = \frac{V_{CC} T_s}{R_{C1} C_s} \quad (12.36)$$

$$T_s = \frac{V_s}{V_{CC}} \times R_{C1} C_s$$

If

$$V_s = V_{CC}, T_s = R_{C1} C_s.$$

(v) Calculation of T_r :

From Fig. 12.12(c), the discharging current:

$$i_d = \frac{V_{CC}}{R_{C2}}$$

The change in voltage during T_r is once again V_s .

Therefore,

$$V_s = \frac{V_{CC} T_r}{R_{C2} C_s} \quad (12.37)$$

If $V_s = V_{CC}$, then, $T_r = R_{C2} C_s$,

(vi) Calculation of the slope error: The slope error of the Miller's sweep generator is given by the relation:

$$e_s = (V_s/V_{CC})[(1 + R/R_i) / |A|]$$

where, R is the resistance through which the capacitor charges when the switch is OFF. To calculate e_s , therefore, we have to calculate A and R_i of the common-emitter amplifier. The CE amplifier uses the h -parameter model as shown in Fig. 12.12(e):

We have from Fig. 12.12(e)

$$I_2 = h_{fe} I_1 + h_{oe} V_2 \quad (12.38)$$

and

$$V_2 = I_o R_C = -I_2 R_C$$

Putting

$$V_2 = -I_2 R_C$$

in Eq. (12.38):

$$I_2 = h_{fe} I_1 + h_{oe}(-I_2 R_C)$$

Dividing by I_1 :

$$\frac{I_2}{I_1} = h_{fe} - \left(\frac{I_2}{I_1}\right) h_{oe} R_C$$

Therefore,

$$\frac{I_2}{I_1} (1 + h_{oe} R_C) = h_{fe}$$

$$A_I = \frac{I_o}{I_1} = \frac{-I_2}{I_1} = \frac{-h_{fe}}{1 + h_{oe} R_C} \quad (12.39)$$

From Fig. 12.12(e), we also have the relation

$$V_1 = h_{ie} I_1 + h_{re} V_2 \quad (12.40)$$

Dividing by I_1 , we have:

$$R_i = \frac{V_1}{I_1} = h_{ie} + h_{re} \left(\frac{-I_2 R_C}{I_1} \right) = h_{ie} + h_{re} A_I R_C \quad (12.41)$$

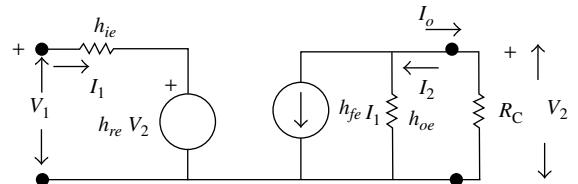


FIGURE 12.12(e) A CE amplifier

A , the voltage gain is given by:

$$A = \frac{V_2}{V_1} = \frac{-I_2 R_C}{I_1 R_i} = A_I \times \frac{R_C}{R_i} \quad (12.42)$$

R_i and A can be calculated using Eqs. (12.41) and (12.42) and hence, the value of e_s .

EXAMPLE

Example 12.3: For the Miller's sweep shown in Fig. 12.12(a), $V_{CC} = 25$ V, $R_{C2} = 5$ k Ω , $R_{C1} = 10$ k Ω . The duration of the sweep is 5 ms. The sweep amplitude is 25 V. Calculate (a) the value of C ; (b) the retrace time and (c) the slope error. The transistor has the following parameters: $h_{fe} = 80$, $h_{ie} = 1$ k Ω , $h_{oe} = 1/40$ k Ω and $h_{re} = 2.5 \times 10^{-4}$.

Solution: (a)

$$V_s = \frac{V_{CC}}{R_{C1} C_s} \times T_s$$

We have

$$V_s = V_{CC}$$

Therefore,

$$T_s = R_{C1} C_s \quad C_s = \frac{T_s}{R_{C1}} = \frac{5 \times 10^{-3}}{10 \times 10^3} = 0.5 \mu\text{F}$$

(b) Retrace time $T_r = R_{C2} \times C_s = 5 \times 10^3 \times 0.5 \times 10^{-6} = 2.5$ ms

(c)

$$A_I = \frac{-h_{fe}}{1 + h_{oe} R_{C2}} = \frac{-80}{1 + \frac{5}{40}} = -71.11$$

$$R_i = h_{ie} + h_{re} A_I R_{C2} = 1 + (2.5 \times 10^{-4})(-71.11)(5) = (1 - 0.0889) = 0.91 \text{ k}\Omega$$

$$A = A_I \frac{R_{C2}}{R_i} = -71.11 \times \frac{5}{0.91} = -390.71$$

$$e_s(\text{Miller}) = \frac{V_s}{V_{CC}} \times \frac{1}{|A|} \times \left(1 + \frac{R_{C1}}{R_i}\right) = \frac{25}{25} \times \frac{1}{390.71} \times \left(1 + \frac{10}{0.91}\right) = 0.0307 = 3.07 \text{ \%}.$$

12.3.2 Bootstrap Sweep Generators

Alternatively, in the circuit shown in Fig. 12.9(b) let Y be the ground terminal. The resultant circuit is shown in Fig. 12.13(a). Redrawing this circuit and replacing the auxiliary generator by an amplifier with X and Y as input terminals and Z and Y as the output terminals, the amplifier should have a gain of unity as $v = v_C$, as shown in Fig. 12.13(b).

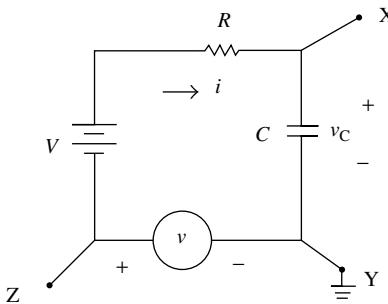


FIGURE 12.13(a) The sweep generator, with Y as the ground terminal

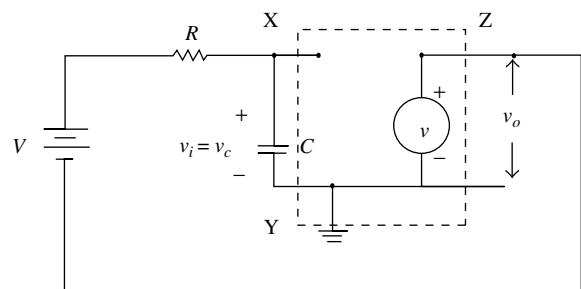


FIGURE 12.13(b) The redrawn circuit of Fig. 12.13(a)

Replacing the generator by an amplifier, the circuit shown in Fig. 12.13(b) is redrawn as shown in Fig. 12.13(c). The sweep generator represented in Fig. 12.13(c) is called a bootstrap sweep generator because the increasing input at X is accompanied by an identical rise in the output at Z , as the gain of the amplifier is unity.

Slope Error in Bootstrap Sweep Generators. Consider the bootstrap sweep generator shown in Fig. 12.14(a) in which the auxiliary generator is replaced by an amplifier with gain 1, which obviously is an emitter follower. If initially the capacitor is uncharged and if S is closed at $t = 0$, then the voltage across C and R_i , i.e., $v_i = 0$, R_i is replaced by a short circuit. As $v_i = 0$, $Av_i = 0$ and is also replaced by a short circuit. Hence, at $t = 0$, the circuit of Fig. 12.14(a) reduces to that in Fig. 12.14(b).

From Fig. 12.14 (b):

$$v_o = -V \times \frac{R_o}{R + R_o} \quad (12.43)$$

And as R_o of the emitter follower is very small: $v_o \approx 0$. As $t \rightarrow \infty$, C is fully charged and is open circuited and the resultant circuit is shown in Fig. 12.14(c).

From Fig. 12.14(c)

$$v_o(t \rightarrow \infty) = \frac{V(AR_i - R_0)}{R_o + R + R_i(1 - A)}$$

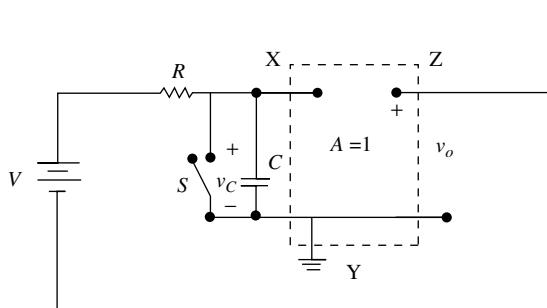


FIGURE 12.13(c) A bootstrap sweep generator

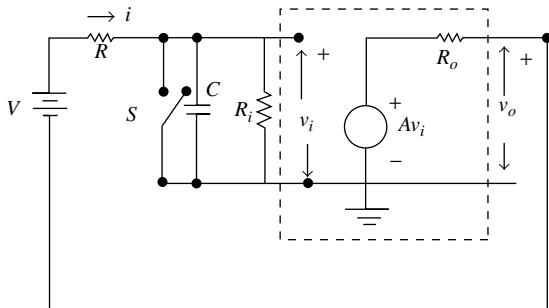


FIGURE 12.14(a) A bootstrap sweep generator with the auxiliary generator replaced by an amplifier

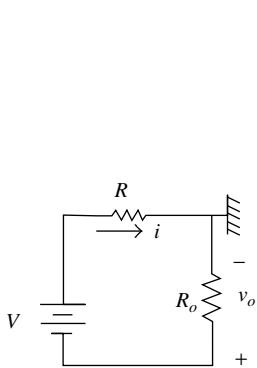


FIGURE 12.14(b) The circuit to calculate the output at $t = 0$

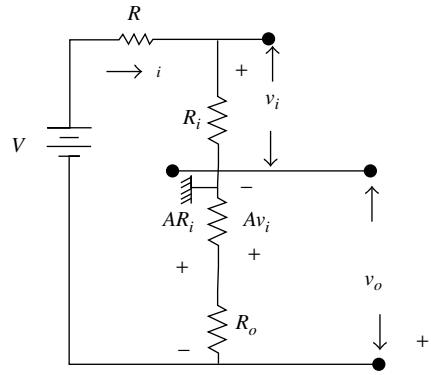


FIGURE 12.14(c) The circuit to calculate the output as $t \rightarrow \infty$

Dividing by R_i :

$$v_o(t \rightarrow \infty) = \frac{V(A - \frac{R_o}{R_i})}{(1 - A) + \frac{R}{R_i} + \frac{R_o}{R_i}}$$

Here, R_o is the output resistance of the emitter follower, which is small and R_i is its input resistance, which is large.

Therefore, R_o/R_i is negligible and $A \approx 1$

$$v_o(t \rightarrow \infty) = \frac{V}{(1 - A) + \frac{R}{R_i} + \frac{R_o}{R_i}} \approx \frac{V}{(1 - A) + R/R_i} \quad (12.44)$$

Eq. (12.44) gives the peak-to-peak excursion of the output swing.

Therefore,

$$e_{s(\text{Bootstrap})} = \frac{V_s \left[(1 - A) + \frac{R}{R_i} \right]}{V} \approx \frac{V_s}{V} \left(1 - A + \frac{R}{R_i} \right) \cong e_s \frac{R}{R_i} \quad (12.45)$$

since $A \approx 1$. If $R = R_i$, $e_{s(\text{Bootstrap})} = e_s$

This means that the bootstrap circuit will not provide any improvement in linearity if the input resistance of the amplifier is small. For the output of the sweep generator to be linear, $R_i \gg R$. As the emitter follower has a large input resistance, this requirement is normally satisfied. If not, a Darlington emitter follower may be used to derive a very large input resistance as shown in Fig. 12.15.

A Darlington pair is manufactured as a single transistor. In this transistor, the base current I_{B1} of Q_1 gives rise to its collector current $I_{C1} (= h_{FE1}I_{B1})$. I_{C1} becomes the base current I_{B2} for Q_2 and there results a current $I_{C2} (= h_{FE2}I_{B2} = h_{FE2} \times h_{FE1}I_{B1})$. Thus, we see that $h_{FE} = h_{FE2} \times h_{FE1}$, i.e., the current gain of the Darlington pair is the product of the current gains of the individual transistors. The input resistance of an emitter follower is given by: $R_i = h_{ie} + (1 + h_{fe})R_E$.

For a Darlington pair, as h_{FE} is very large, the input resistance of a Darlington emitter follower tends to be very large. However, the voltage gain $A \approx 1$. A practical bootstrap ramp generator is shown in Fig. 12.16(a). The ramp is generated across capacitor C_1 which is charged from the current through R_1 . The discharge transistor Q_1 , when ON, keeps V_1 at $V_{CE(sat)}$ until a negative input pulse is applied. Q_2 is an emitter follower with a low output resistance. Emitter resistance R_E is connected to a negative supply (V_{EE}) instead of referencing it to the ground to ensure that Q_2 remains conducting even when its base voltage V_1 is close to the ground. Capacitor C_3 , called the bootstrapping capacitance, has a much higher capacitance than C_1 . C_3 is meant to maintain a constant voltage across R_1 and thus, maintain a constant charging current. We now discuss the operation of the circuit.

(a) **Quiescent conditions:** The voltages under quiescent conditions (before the application of a trigger) are calculated as illustrated below, using Fig. 12.16(b).

When the input trigger signal is not present, Q_1 has sufficient base current. Therefore, Q_1 is driven into saturation and the voltage V_1 across the capacitor C_1 is $V_{CE(sat)}$. $V_1 = V_{CE(sat)}$ (point X), typically 0.2 V for Si, as shown in Fig. 12.16(b). Q_2 is an emitter follower for which input is V_1 and its output v_o is:

$$v_o = V_1 - V_{BE2} = V_{CE(sat)} - V_{BE2} \text{ (point Y)} \approx 0.2 - 0.6 = -0.4 \text{ V for Si}$$

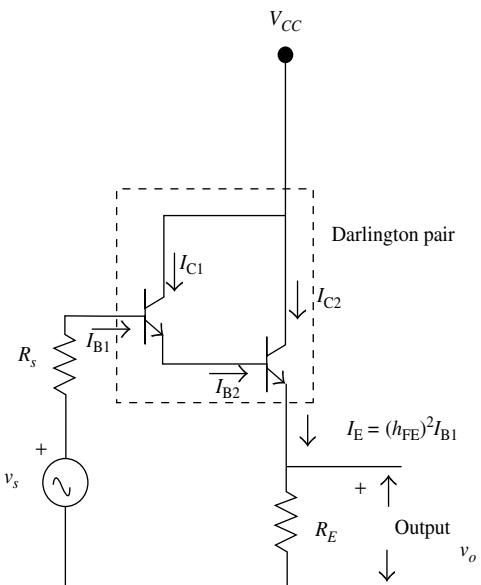


FIGURE 12.15 The Darlington emitter follower

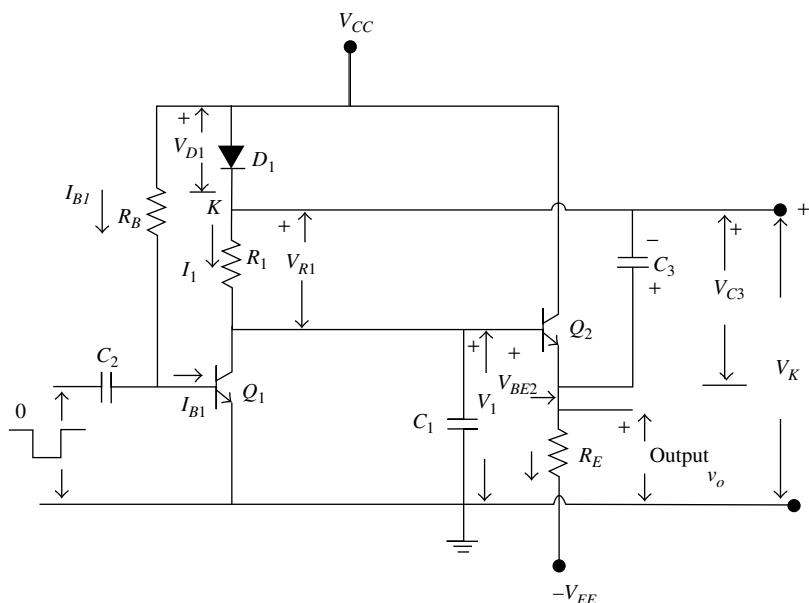


FIGURE 12.16(a) A practical bootstrap sweep generator

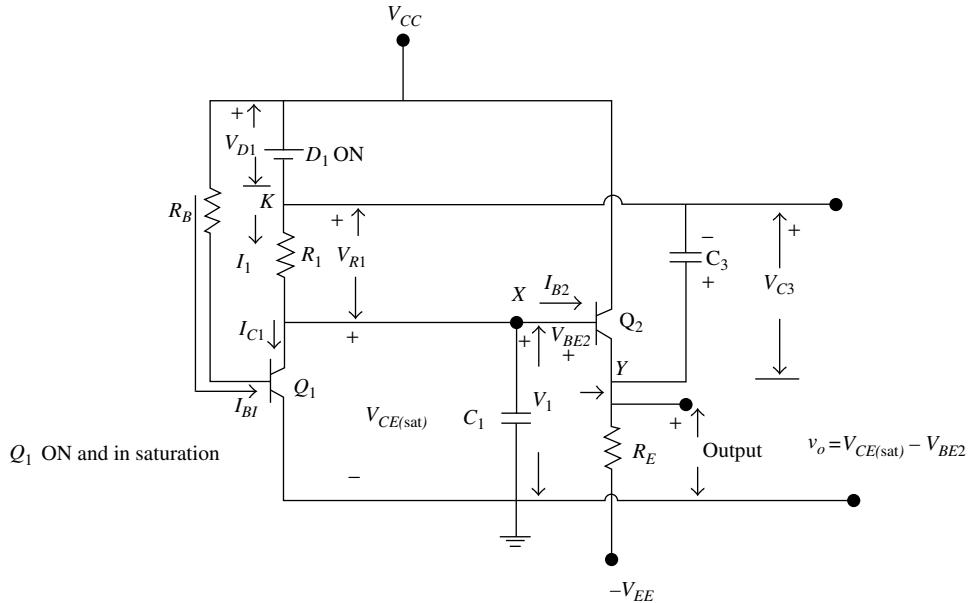


FIGURE 12.16(b) The circuit to calculate voltages under quiescent condition

As the voltage now at node K is $V_{CE(\text{sat})} \approx 0V$, D_1 is ON. The voltage across R_1 is,

$$V_{R1} = V_{CC} - V_{D1} - V_{CE(\text{sat})} \approx V_{CC}$$

where, V_{D1} is the diode voltage when ON. Hence, the current I_1 in R_1 is V_{CC}/R_1 and is constant. The base current I_{B2} of Q_2 is smaller than the collector current I_{C1} of Q_1 :

$$I_{C1} \approx I_1 = \frac{V_{CC}}{R_1} \quad \text{and} \quad I_{B1(\text{min})} = \frac{I_{C1}}{h_{FE}} = \frac{V_{CC}}{h_{FE}R_1}$$

$$I_{B1} = \frac{V_{CC}}{R_B}$$

For Q_1 to be in saturation:

$$I_{B1} > I_{B1(\text{min})}$$

Therefore,

$$\frac{V_{CC}}{R_B} > \frac{V_{CC}}{h_{FE}R_1} \quad \text{or} \quad R_B < h_{FE}R_1$$

For all practical purposes, when Q_1 is ON, both V_1 and V_o are zero.

(b) **Sweep generation:** At $t = 0$, as the trigger is applied, the voltage at the base of Q_1 goes negative, Q_1 is OFF, [see Fig. 12.16(c)]. The voltage at node K , $V_K = V_{CC} + V_1$ and D_1 is OFF and is an open circuit.

The voltage at node X is V_1 .

Therefore,

$$V_{R1} = V_K - V_1 = V_{CC} + V_1 - V_1 = V_{CC} \quad I_1 = \frac{V_{CC}}{R_1}$$

However, $I_1 = I_C + I_{B2}$, where I_C is the charging current of C_1 and I_{B2} is the base current of Q_2 . As Q_2 is an emitter follower with large input resistance, I_{B2} is small. As a result,

$$I_1 = \frac{V_{CC}}{R_1} = I_C$$

I_C , the charging current of C_1 , is constant. Hence, the resultant sweep is linear. When D_1 is OFF, the charging current I_1 to C_1 through R_1 is supplied by C_3 which is charged to V_{CC} .

There is no current into the collector lead of Q_1 and instead, this current flows through C_1 charging it. As the voltage across the capacitor C_1 varies as $(I_1/C)t$, so does the output.

$$v_o = \frac{V_{CC}}{R_1} \times \frac{t}{C_1} \quad (12.46)$$

From Fig. 12.16(d), it is seen that the output v_o varies linearly only when the duration of the gating signal (T_g) is small so that in this period v_o does not reach V_{CC} . However, if T_g is large, the output v_o may reach V_{CC} even before T_g . When $v_o = V_{CC}$, the voltage V_{CE2} of Q_2 is practically zero (saturation). Q_2 no longer behaves as an emitter follower. v_o and V_1 therefore remain at V_{CC} . The current V_{CC}/R_1 now flows through C_3 , R_1 and through the base-emitter diode of Q_2 ; thereby changing the voltage across C_3 by a small amount, ΔV_{C3} .

(i) If $T_s < T_g$ (i.e., v_o reaches V_{CC} before T_g) Then at

$$t = T_s$$

$$v_o = V_s = V_{CC}$$

From Eq. (12.46):

$$V_{CC} = \frac{V_{CC} T_s}{R_1 C_1}$$

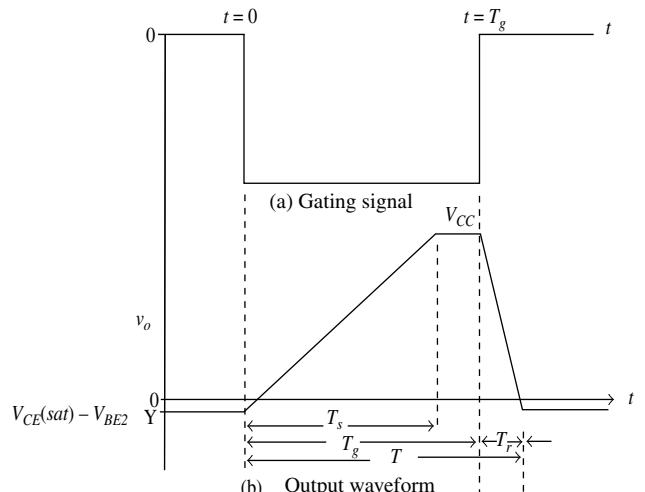
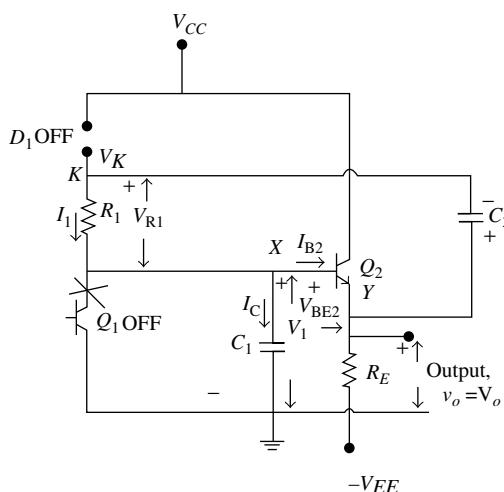
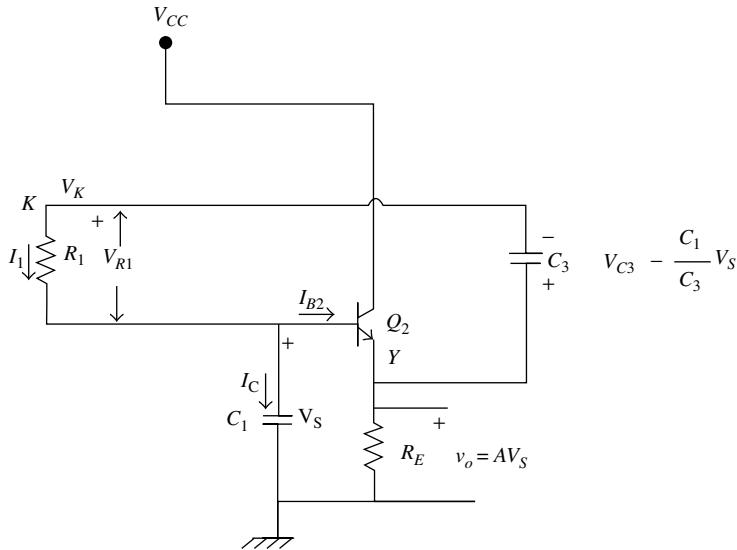


FIGURE 12.16(c) The circuit of Fig. 12.16(a) when Q_1 is OFF and C_1 charges

FIGURE 12.16(d) The output waveforms of the bootstrap sweep circuit

FIGURE 12.17 The calculation of I_1

or

$$T_s = R_1 C_1 \quad (12.47)$$

The amount of charge gained by C_1 is $Q_{C_1} = C_1 V_s$

The amount of charge lost by C_3 is $Q_{C_3} = C_3 \Delta V_{C_3}$

Assume that during T_s the current through capacitors C_1 and C_3 are same.

Therefore, the amount of charge gained by C_1 = the amount of charge lost by C_3 .

$$C_3 \Delta V_{C_3} = C_1 V_s$$

$$\Delta V_{C_3} = \frac{C_1}{C_3} V_s$$

Therefore, at $t = T_s$, the voltage across C_1 is V_s and the voltage across C_3 is $V_{C_3} - (C_1/C_3)V_s$ and the output voltage is $v_o = AVs$, as shown in Fig. 12.17.

$$I_C = I_1 - I_{B2}$$

and

$$I_{B2} = \frac{V_s}{R_i}$$

At

$$t = T_s$$

$$I_1 = \frac{AV_s + V_{C_3} - V_s \frac{C_1}{C_3} - V_s}{R_1}$$

At

$$t = T_s,$$

Therefore,

$$I_C = \left[\frac{\left(AV_s + V_{C3} - V_s \frac{C_1}{C_3} \right) - V_s}{R_1} \right] - \frac{V_s}{R_i} \quad (12.48)$$

At $t = 0$, $V_s = 0$. Hence, from Eq. (12.48), $I_C = V_{C3}/R_1$

$$\text{Sweep error, } e_s = \left(\frac{(I_C)_{t=0} - (I_C)_{t=T_s}}{(I_C)_{t=0}} \right) = \frac{\left[\frac{\left(V_{C3} - AV_s - V_{C3} + V_s \frac{C_1}{C_3} \right) + V_s}{R_1} \right] + \frac{V_s}{R_i}}{\frac{V_{C3}}{R_1}} \quad (12.49)$$

$$e_s = \frac{V_s}{V_{C3}} \left(1 - A + \frac{C_1}{C_3} + \frac{R_1}{R_i} \right)$$

Eq. (12.49) gives the expression for the slope error when the voltage V_{C3} changes during the sweep period.

(ii) On the other hand if $V_s < V_{CC}$, the maximum sweep voltage is:

$$V_s = \frac{V_{CC} T_g}{R_1 C_1} \quad (12.50)$$

(c) **Calculation of retrace time, T_r :** At the end of the gate signal, at $t = T_g$, a current $I_{B1} = (V_{CC}/R_B)$ again flows into the base terminal of Q_1 . Q_1 once again tries to go into saturation. However, till such time V_{CE} of Q_1 is $V_{CE(sat)}$ (Q_1 is in saturation), the collector current, i_{C1} remains constant at

$$i_{C1} = h_{FE} \times I_{B1} = h_{FE} \times \frac{V_{CC}}{R_B}$$

As shown in Fig. 12.18, the current i_{R1} through R_1 and the discharging current i_d of C_1 now constitutes i_{C1} , the collector current of Q_1 , neglecting the small base current I_{B2} of Q_2 ,

Writing the KCL equation at node C:

$$i_{C1} = i_{R1} + i_d \quad (12.51)$$

i_{R1} remains approximately at $V_{CC}/R_1 (= I_1)$ and the capacitor discharges with a constant current. The voltage across C_1 falls, and consequently v_o falls, since once again Q_2 behaves as an emitter follower. The discharge current i_d from Eq. (12.51) is:

$$i_d = i_{C1} - i_{R1}$$

$$i_d = \frac{h_{FE} V_{CC}}{R_B} - \frac{V_{CC}}{R_1} \quad (12.52)$$

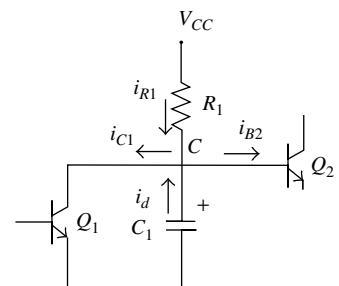


FIGURE 12.18 The circuit to calculate i_d

Therefore V_1 and v_o fall linearly to the initial value. The voltage variation during the retrace time T_r is:

$$v_s = V_s = \frac{i_d T_r}{C_1} \quad T_r = \frac{C_1 V_s}{i_d}$$

Using Eq. (12.52), we have,

$$T_r = \frac{C_1 V_s}{V_{CC} \left(\frac{h_{FE}}{R_B} - \frac{1}{R_1} \right)} = \frac{C_1 \frac{V_s}{V_{CC}}}{\left(\frac{h_{FE}}{R_B} - \frac{1}{R_1} \right)} \quad (12.53)$$

If the retrace time is large, it takes a longer time to initiate a new sweep cycle. From Eq. (12.53), it is seen that R_B will have to be small to reduce the retrace time. However, if R_B is too small, then the collector current of Q_1 becomes large as:

$$i_{C1} = h_{FE} \frac{V_{CC}}{R_B}$$

This results in greater dissipation in Q_1 . During the period, $T = T_g + T_r$, though C_3 is a large capacitor, it may still lose some charge. The circuit is said to have recovered completely only when the charge lost by C_3 is regained. The minimum recovery time T_1 for C_3 can be found out as follows:

Charge lost by C_3 in time $T = V_{CC} T / R_1$

The charging current of $C_3 = V_{EE} / R_E$

Therefore, the charge recovered in time $T_1 = (V_{EE} / R_E) T_1$

Charge lost = charge regained

$$\begin{aligned} \frac{V_{CC} T}{R_1} &= \frac{V_{EE}}{R_E} T_1 \\ T_1 &= \frac{V_{CC}}{V_{EE}} \times \frac{R_E}{R_1} T \end{aligned} \quad (12.54)$$

To reduce T_1 , V_{EE} may be increased. However, this increases the quiescent current in Q_2 and hence, the dissipation in it.

(d) Calculation of the slope error of a bootstrap sweep circuit: The slope error of the bootstrap, assuming that the charge on C_3 remains unaltered during the sweep duration, is given by the relation:

$$e_s = \frac{V_s}{V_{CC}} \left(1 - A + \frac{R}{R_i} \right) \quad (12.55)$$

To calculate e_s , we have to calculate A and R_i . For a common collector amplifier we have:

$$A_I = \frac{-h_{fc}}{1 + h_{oc} R_L} = \frac{1 + h_{fe}}{1 + h_{oe} R_L}$$

since

$$h_{fc} = -(1 + h_{fe}) \quad \text{and} \quad h_{oc} = h_{oe}$$

$$R_i = h_{ic} + h_{rc} A_I R_L = h_{ie} + A_I R_L \quad (12.56)$$

since

$$h_{rc} = 1 \quad \text{and} \quad h_{ic} = h_{ie}$$

From Eq. (12.56) dividing by R_i :

$$1 = \frac{h_{ie}}{R_i} + A_I \frac{R_L}{R_i} = \frac{h_{ie}}{R_i} + A$$

Therefore,

$$(1 - A) = \frac{h_{ie}}{R_i} \quad (12.57)$$

Using Eqs. (12.55), (12.56) and (12.57), it is possible to calculate e_s . To understand the procedure to analyse and also design a bootstrap sweep let us consider the following examples.

E X A M P L E

Example 12.4: The transistor bootstrap circuit in Fig. 12.16(a) has the following parameters, $V_{CC} = 15$ V, $V_{EE} = -10$ V, $R_B = 30$ k Ω , $R_1 = 10$ k Ω , $R_E = 5$ k Ω , $C_1 = 0.005$ μ F, $C_3 = 1.0$ μ F. The input trigger is negative and has an amplitude of 2 V and a width of 60 μ s. The transistor parameters are $h_{FE} = h_{fe} = 50$, $h_{ic} = 1$ k Ω , $1/h_{oe} = 40$ k Ω , $h_{rc} = 1$. Assume that the forward-biased junction voltages are negligible. The diode is ideal. Evaluate (a) the sweep speed and the sweep duration; (b) retrace time and recovery time and (c) the slope error; (d) plot the gate voltage, the output voltage V_o and the collector current of Q_1 .

Solution: Referring to the circuit in Fig. 12.16(a):

$$(a) \text{ Sweep speed} = \frac{I_1}{C_1} = \frac{V_{CC}}{R_1 C_1} = \frac{15}{10 \times 10^3 \times 0.005 \times 10^{-6}} = 3 \times 10^5 \text{ V/s}$$

$$V_{s(\max)} = V_{CC} = 15 \text{ V} = \text{Sweep speed} \times T_s$$

i.e.,

$$15 = (3 \times 10^5) T_s$$

Therefore, sweep time,

$$T_s = \frac{15}{3 \times 10^5} = 50 \mu\text{s}$$

(b) At the end of the input pulse, Q_1 once again goes into saturation.

$$i_{B1} = \frac{V_{CC}}{R_B} = \frac{15}{30 \times 10^3} = 0.5 \text{ mA} \quad i_{C1} = h_{FE} i_{B1} = 50 \times 0.5 = 25 \text{ mA}$$

The retrace time T_r is,

$$T_r = \frac{\frac{V_s}{V_{CC}} C_1}{\frac{h_{FE}}{R_B} - \frac{1}{R_1}} = \frac{\frac{15}{15} \times 5 \times 10^{-9}}{\frac{50}{30 \times 10^3} - \frac{1}{10 \times 10^3}} = 3.18 \mu\text{s}$$

$$T = T_g + T_r = (60 + 3.18) = 63.18 \mu\text{s}$$

$$\text{Recovery time } T_1 = \frac{V_{CC}}{V_{EE}} \times \frac{R_E}{R_1} \times T = \frac{15}{10} \times \frac{5}{10} \times 63.18 \times 10^{-6} = 47.385 \mu\text{s}$$

(c) To find the slope error:

The current gain of the emitter follower is given by:

Therefore,

$$A_I = \frac{1 + h_{fe}}{1 + h_{oe}R_E} = \frac{1 + 50}{1 + \frac{1}{40} \times 5} = \frac{51}{1.5} = 45.33$$

Input impedance of the emitter follower is given by:

$$R_i = h_{ie} + A_I R_E$$

Therefore,

$$1 - A = \frac{h_{ie}}{R_i}$$

A is the voltage gain of the emitter follower.

$$R_i = h_{ie} + A_I R_E = 1\text{k}\Omega + 45.33 \times 5\text{k}\Omega = 227.67\text{k}\Omega$$

$$1 - A = \frac{h_{ie}}{R_i} = \frac{1}{227.67} = 0.00439$$

The slope error,

$$e_s = \left(1 - A + \frac{R_1}{R_i}\right) \frac{V_s}{V_{CC}} = \left[0.00439 + \frac{10}{227.67}\right] \frac{15}{15} = 0.0483 = 4.83\%$$

(d) Using the above calculations, the waveforms can be sketched as shown in Fig. 12.19.

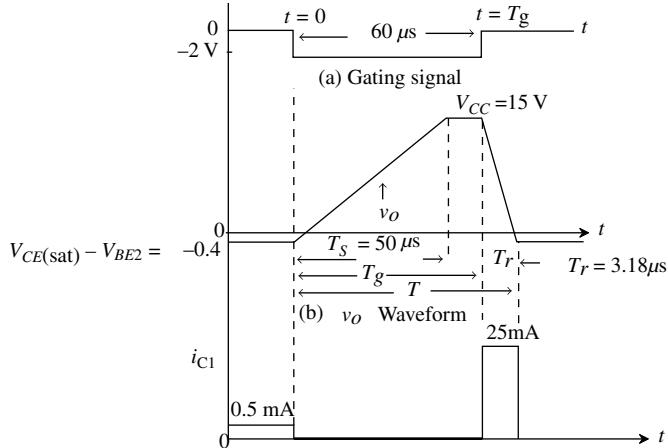


FIGURE 12.19 The waveforms of the bootstrap circuit

E X A M P L E

Example 12.5: Design a transistor bootstrap sweep generator to provide an output amplitude of 10 V over a time period of 1 ms. The ramp is to be triggered by a negative going pulse with an amplitude of 5 V, a pulse width of 1 ms and a time interval between the pulses is 0.1ms. The load resistance is 1 $\text{k}\Omega$ and the ramp is to be linear within 1 per cent. The supply voltage is 18 V, $h_{FE(\min)} = 100$.

Solution:

Refer to the bootstrap circuit shown in Fig. 12.16(a).

$$R_L = R_E = 1 \text{ k}\Omega$$

When $V_o = 0$,

$$I_{E2} = \frac{0 - (-V_{EE})}{R_E} = \frac{18 \text{ V}}{1 \text{ k}\Omega} = 18 \text{ mA}$$

When $V_o = V_s (= 10V)$,

$$I_{E2} = \frac{10 - (-V_{EE})}{R_E} = \frac{28 \text{ V}}{1 \text{ k}\Omega} = 28 \text{ mA}$$

At $V_o = 0$,

$$I_{B2} = \frac{I_{E2}}{h_{FE}} = \frac{18 \text{ mA}}{100} = 0.18 \text{ mA}$$

At $V_o = V_s$,

$$I_{B2} = \frac{I_{E2}}{h_{FE}} = \frac{28}{100} = 0.28 \text{ mA} \quad \Delta I_{B2} = 0.28 - 0.18 = 0.10 \text{ mA}$$

I_1 is much larger than I_{B2}

Let

$$I_1 = 100 \times \Delta I_{B2} = 100 \times 0.10 \text{ mA} = 10 \text{ mA} \quad C_1 = \frac{I_1 T_s}{V_s} = \frac{10 \times 10^{-3} \times 1 \times 10^{-3}}{10 \text{ V}} = 1 \mu\text{F}$$

$$V_{R1} = V_{CC} - V_{D1} - V_{CE}(\text{sat}) = 18 - 0.7 - 0.2 = 17.1 \text{ V} \quad R_1 = \frac{V_{R1}}{I_1} = \frac{17.1}{10 \times 10^{-3}} = 1.71 \text{ k}\Omega$$

For 1 per cent non-linearity due to discharge of C_3 :

$\Delta V_{C3} = 1$ per cent of the initial V_{CC} level

Initial

$$V_{C3} = V_{CC} = 18 \text{ V} \quad \Delta V_{C3} = \frac{18 \times 1}{100} = 0.18 \text{ V}$$

And C_3 discharge current I_1 is equal to 10 mA. Therefore,

$$C_3 = \frac{I_1 T_{(\text{spacing})}}{\Delta V_{C3}} = \frac{10 \times 10^{-3} \times 1 \times 10^{-3}}{0.18 \text{ V}} = 55 \mu\text{F}$$

The discharge time of C_1 is 0.1ms which is 1/10 th of the charging time. For Q_1 to discharge C_1 in 1/10 th of the charging time,

$$I_{C1} = 10 \times (\text{C}_1 \text{ charging current}) = 10 \times 10 \text{ mA} = 100 \text{ mA}$$

$$I_{B1} = \frac{I_{C1}}{h_{FE}} = \frac{100 \text{ mA}}{100} = 1 \text{ mA} \quad R_B = \frac{V_{CC} - V_{BE1}}{I_{B1}} = \frac{18 - 0.7}{1 \text{ mA}} = \frac{17.3 \text{ V}}{1 \text{ mA}} = 17.3 \text{ k}\Omega$$

Choose $R_B = 20 \text{ k}\Omega$, Q_1 is to be biased OFF at the end of the input pulse.

$$|\Delta V_B| = v_o - (\text{pulse amplitude}) = 0.7 - 5 \text{ V} = -4.3 \text{ V}$$

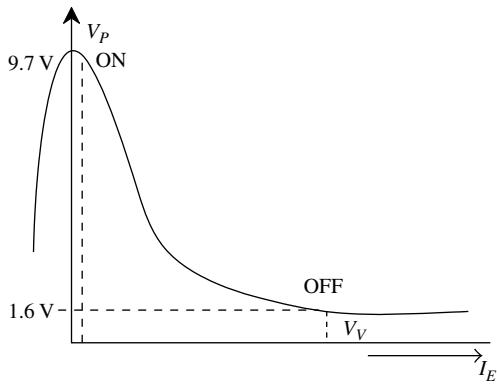
The charging current of C_2 is equal to the current through R_B when Q_1 is OFF.

$$I = \frac{V_{CC} - V_i}{R_B} = \frac{18 - (-5)}{20 \text{ k}\Omega} = \frac{23 \text{ V}}{20 \text{ k}\Omega} = 1.15 \text{ mA}$$

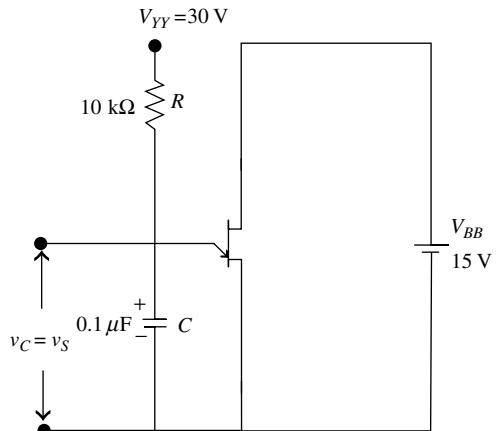
$$C_2 = \frac{I \times t}{\Delta V_B} = \frac{1.15 \text{ mA} \times 1 \text{ ms}}{4.3 \text{ V}} = 0.27 \mu\text{F}$$

S O L V E D P R O B L E M S

Example 12.6: A UJT has characteristic as shown in Fig. 12.20(a) and the UJT relaxation oscillator is shown in Fig. 12.20(b). Find the values of: (a) Sweep amplitude, (b) the slope and displacement errors, (c) the duration of the sweep. and (Assume $\eta = 0.6$ and $V_F = 0.7 \text{ V}$ for silicon.)



(a)



(b)

FIGURE 12.20(a) UJT characteristic; (b) UJT relaxation oscillator

Solution: The waveform of the sweep generator is shown in Fig. 12.20(c)

Given, $V_{BB} = 15 \text{ V}$, $V_{YY} = 30 \text{ V}$, $R = 10 \text{ k}\Omega$, $C = 0.1 \mu\text{F}$

We know that

$$V_P = \eta V_{BB} + V_F = 0.6 \times 15 + 0.7 = 9.7 \text{ V}.$$

From UJT characteristics, we have $V_V = 1.6 \text{ V}$

$$\begin{aligned} \text{(a) Amplitude of the sweep} &= V_s = V_P - V_V \\ &= 9.7 - 1.6 = 8.1 \text{ V.} \end{aligned}$$

(b) Sweep speed error,

$$e_s = \frac{V_s}{V} = \frac{V_s}{V_{YY} - V_V} = \frac{8}{30 - 1.6} = 0.28 = 28\%$$

$$\text{Displacement error, } e_d = \frac{1}{8} e_s = \frac{1}{8} (28) = 3.5\%$$

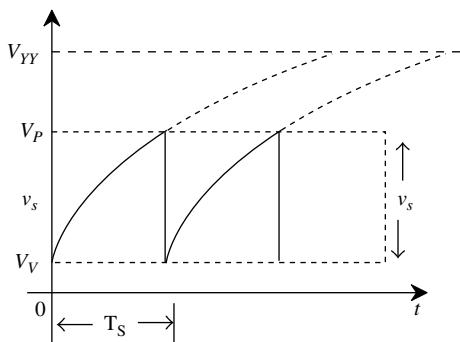


FIGURE 12.20(c) The waveform of the sweep generator

(c) Sweep time,

$$\begin{aligned}
 T_s &= RC \log_e \left(\frac{V_{YY} - V_V}{V_{YY} - V_P} \right) \\
 &= 10 \times 10^3 \times 0.1 \times 10^{-6} \times \log_e \left(\frac{30 - 1.6}{30 - 9.7} \right) \\
 &= 335.74 \mu\text{s}
 \end{aligned}$$

Example 12.7: Using the characteristic of UJT shown in Fig. 12.21 (a), calculate the values of R , C , R_1 and R_2 of the relaxation oscillator shown in Fig. 12.21; (b) to generate a sweep with a frequency of 10 kHz and amplitude of 10V, T_s is 0.5 % of T .

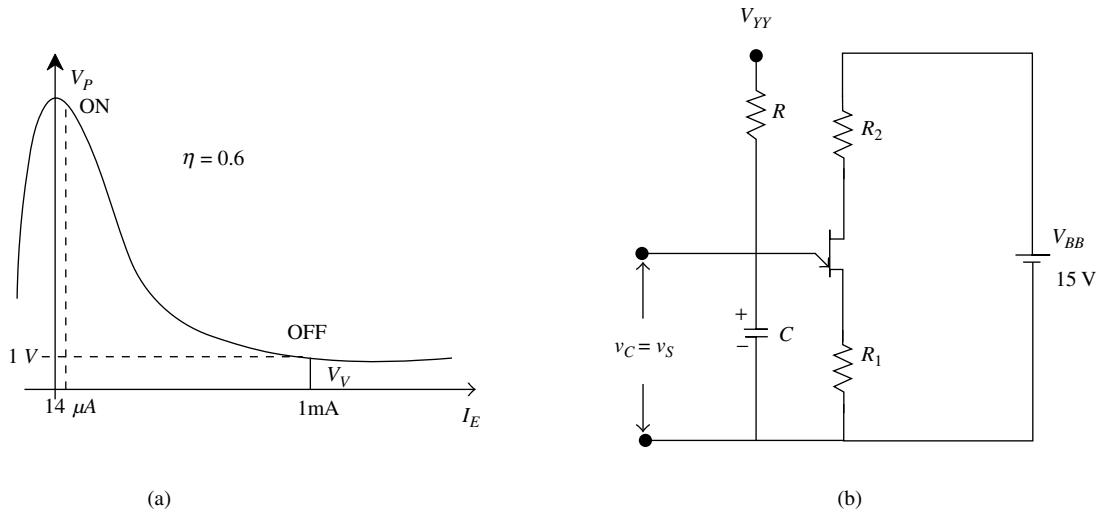


FIGURE 12.21(a) UJT characteristic; (b) UJT relaxation oscillator

Solution:

Given,

$$f = 10 \text{ kHz}, V_s = 10 \text{ V}, V_{BB} = 15 \text{ V}, V_V = 1 \text{ V}, I_P = 14 \mu\text{A}.$$

$$I_V = 1 \text{ mA}, \eta = 0.6$$

Therefore,

$$V_P = V_s + V_V = 10 + 1 = 11 \text{ V}$$

$$R_{(\max)} = \frac{V_{BB} - V_P}{I_P} = \frac{15 - 11}{14 \times 10^{-6}} = 285 \text{ k}\Omega$$

$$R_{(\min)} = \frac{V_{BB} - V_V}{I_V} = \frac{15 - 1}{1 \times 10^{-3}} = 14 \text{ k}\Omega$$

R should lie between $R_{(\max)}$ and $R_{(\min)}$.

Let $R = 150 \text{ k}\Omega$.

$$\text{Sweep time } T_s = RC \log_e \left(\frac{V_{BB} - V_V}{V_{BB} - V_P} \right) = RC \log_e \left(\frac{15 - 1}{15 - 11} \right)$$

$$T_s = 1.252RC \quad T = \frac{1}{f} = \frac{1}{10 \times 10^3} = 0.1 \text{ ms} = 100 \mu\text{s}$$

As $T_r = 0.5\% \text{ of } T$,

$$T_r = 0.5\mu\text{s}$$

$$\therefore T_s = T - T_r = 100 - 0.5 = 99.5\mu\text{s} \quad RC = \frac{T_s}{1.252} = \frac{99.5 \times 10^{-6}}{1.252} = 79.4728 \times 10^{-6}\text{s}$$

Therefore,

$$C = \frac{79.4728 \times 10^{-6}}{150 \times 10^3} = 0.53 \text{ nF}$$

Return time $T_r = R_1 C = 0.5\mu\text{s}$

Therefore,

$$R_1 = \frac{T_r}{C} = \frac{0.5 \times 10^{-6}}{0.53 \times 10^{-9}} = 943 \Omega$$

The value of R_2 is usually higher than R_1 . So, choose $R_2 = 3 \text{ k}\Omega$.

Example 12.8: For the UJT relaxation oscillator shown in Fig.12.21(c), $R_{BB} = 3 \text{ k}\Omega$, $R_1 = 0.1 \text{ k}\Omega$, $\eta = 0.7$, $V_V = 2\text{V}$, $I_V = 10 \text{ mA}$, $I_P = 0.01 \text{ mA}$. (a) Calculate R_{B1} and R_{B2} under quiescent condition (i.e., when $I_E = 0$). (b) Calculate the peak voltage, V_P . (c) Calculate the permissible value of R . (d) Calculate the frequency, assuming that the retrace time is negligible. Also calculate f using the value of η . (e) Calculate the frequency, considering the retrace time also. Assume $R_{B1} = 0.1 \text{ k}\Omega$ during the retrace time. (f) Calculate the voltage levels of V_{B1} . (g)Plot the waveforms of the output voltage and V_{B1} .

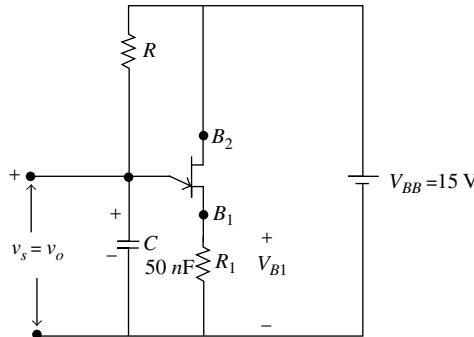


FIGURE 12.21(c) The UJT oscillator

Solution:

Given $R_{BB} = 3 \text{ k}\Omega$, $\eta = 0.7$.

(a)

$$\eta = \frac{R_{B1}}{R_{B1} + R_{B2}} = \frac{R_{B1}}{R_{BB}}$$

$$0.7 = \frac{R_{B1}}{3 \text{ k}\Omega}$$

$$R_{B1} = 0.7 \times 3 \text{ k}\Omega = 2.1 \text{ k}\Omega$$

We have

$$R_{BB} = R_{B1} + R_{B2}$$

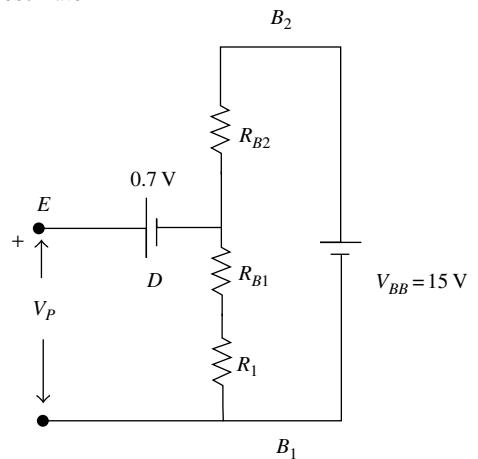


FIGURE 12.21(d) The circuit to calculate V_P

Therefore,

$$R_{B2} = R_{BB} - R_{B1} = 3 \text{ k}\Omega - 2.1 \text{ k}\Omega = 0.9 \text{ k}\Omega$$

(b) The circuit that enables the calculation of V_P is shown in Fig. 12.22(d). From Fig. 12.22(d):

$$V_P = 0.7 \text{ V} + V_{BB} \times \frac{R_{B1} + R_1}{R_{BB} + R_1} = 0.7 + 15 \times \frac{(2.1 + 0.1)}{(3 + 0.1)} = 11.34 \text{ V}$$

(c)

$$R_{(min)} = \frac{(V_{BB} - V_V)}{I_V} = \frac{(15 - 2)}{10 \times 10^{-3}} = 1.3 \text{ k}\Omega$$

$$R_{(max)} = \frac{(V_{BB} - V_P)}{I_P} = \frac{(15 - 11.34)}{0.01 \times 10^{-3}} = 366 \text{ k}\Omega$$

$$R_{(min)} < R < R_{(max)}$$

Choose

$$R = 100 \text{ k}\Omega$$

$$(d) T_s = RC \ln \frac{(V_{BB} - V_V)}{(V_{BB} - V_P)} = 100 \times 10^3 \times 50 \times 10^{-9} \times \ln \frac{(15 - 2)}{(15 - 11.34)} = 6.335 \text{ ms}$$

$$f = \frac{1000}{6.335} = 157.85 \text{ Hz}$$

T_s using the value of η is given as:

$$T_s = RC \ln \frac{1}{(1 - \eta)} = 100 \times 10^3 \times 50 \times 10^{-9} \ln \frac{1}{1 - 0.7} = 6.015 \text{ ms}$$

$$f = \frac{1000}{6.015} = 166.25 \text{ Hz.}$$

$$(e) T_r = (R_{B1} + R_1)C \times \ln \frac{V_P}{V_V} = (0.1 + 0.1)10^3 \times 50 \times 10^{-9} \times \ln \frac{11.34}{2} = 17.35 \mu\text{s}$$

$$T = T_s + T_r = 6.335 + 0.01735 = 6.352 \text{ ms}$$

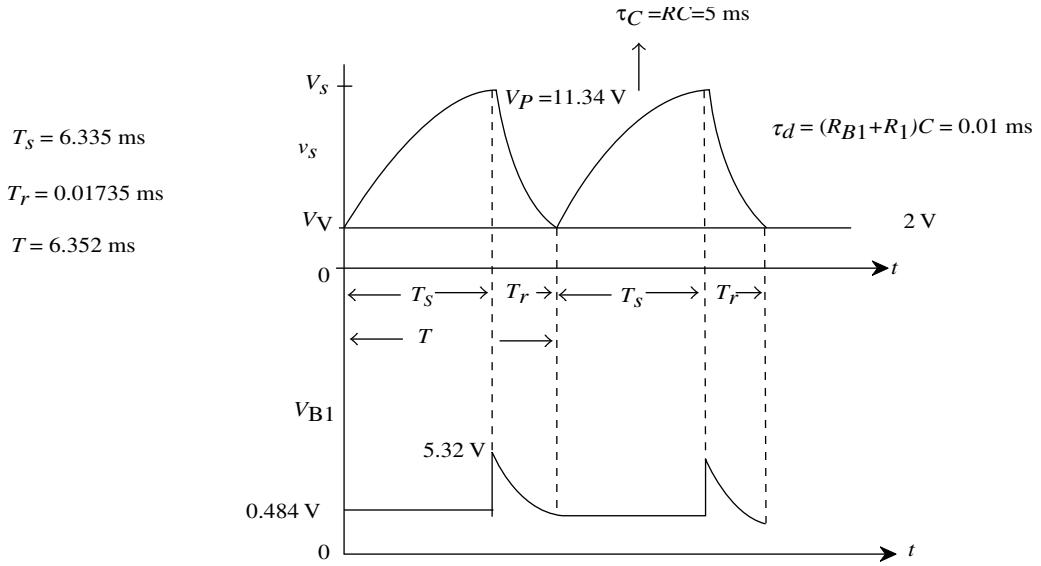
$$f = \frac{1000}{6.352} = 157.43 \text{ Hz}$$

(f) V_{B1} during charging of C is given as:

$$V_{B1} = V_{BB} \times \frac{R_1}{(R_1 + R_{BB})} = \frac{15 \times 0.1}{3 + 0.1} = 0.484 \text{ V}$$

V_{B1} during discharge of C is given by:

$$V_{B1} = (V_P - V_F) \times \frac{0.1}{0.1 + 0.1} = \frac{(11.34 - 0.7)}{2} = 5.32 \text{ V}$$

FIGURE 12.21(e) The waveforms of the output and V_{B1}

V_F is the diode voltage when ON, Fig. 12.21(d).

(g) Waveforms of the output and V_{B1} are shown in Fig. 12.21(e).

Example 12.9: The bootstrap sweep circuit is shown in Fig. 12.22. A square wave whose amplitude varies between 0 and -4 V and duration 0.5 ms is applied as a trigger. a) Calculate all the quiescent state currents and voltages. b) Determine the sweep amplitude, sweep time and sweep frequency. Assume $h_{FE}(\min) = 30$, $V_{CE(\text{sat})} = 0.3$ V, $V_{BE(\text{sat})} = 0.7$ V, $V_{BE(\text{active})} = V_D = 0.6$ V

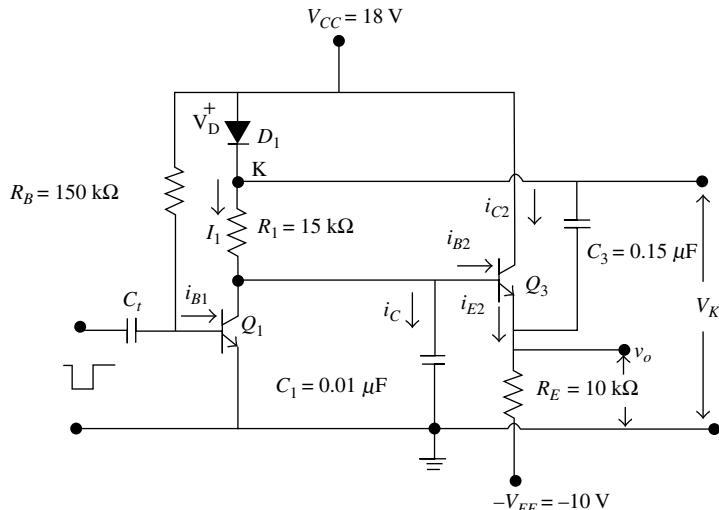


FIGURE 12.22 A bootstrap sweep generator

Solution:

(a) Current through R_1 is:

$$I_1 = \frac{V_{CC} - V_D - V_{CE}(\text{sat})}{R_1} = \frac{18 - 0.6 - 0.3}{15 \times 10^3} = 1.14 \text{ mA}$$

Base Current of Q_1 is:

$$i_{B1} = \frac{V_{CC} - V_{BE}(\text{sat})}{R_B} = \frac{18 - 0.7}{150 \text{ k}\Omega} = 116 \mu\text{A}$$

$$\text{Emitter current of } Q_2 = i_{E2} = \frac{v_o + V_{EE}}{R_E}$$

$$v_o = V_{C1} - V_{BE2}(\text{active})$$

$$v_o = V_{CE}(\text{sat}) - V_{BE2}(\text{active}) = 0.3 - 0.6 = -0.3 \text{ V}$$

Therefore,

$$i_{E2} = \frac{-0.3 + 10}{10 \times 10^3} = 0.97 \text{ mA}$$

$$i_{E2} = i_{B2} + i_{C2} = i_{C2} \left(1 + \frac{i_{B2}}{i_{C2}} \right) = i_{C2} \left(1 + \frac{1}{h_{FE}} \right)$$

Therefore,

$$i_{C2} = \frac{i_{E2}}{1 + \frac{1}{h_{FE}}} = \frac{0.97 \times 10^{-3}}{1 + \frac{1}{30}} = 0.938 \text{ mA}$$

$$i_{B2} = i_{E2} - i_{C2} = 0.97 \times 10^{-3} - 0.938 \times 10^{-3} = 0.032 \text{ mA}$$

$$i_C = I_1 - i_{B2} = 1.14 \times 10^{-3} - 0.032 \times 10^{-3} = 1.108 \text{ mA}$$

$$V_{CE2} = V_{CC} - v_o = 18 + 0.3 = 18.3 \text{ V}$$

(b) Sweep time $T_s = R_1 C_1 = 15 \times 10^3 \times 0.01 \times 10^{-6} = 0.15 \text{ ms}$

Therefore,

$$T_g = 0.5 \text{ ms}$$

Since

$$T_s < T_g \quad , \quad V_s = V_{CC} = 18 \text{ V}$$

$$\text{Return time, } T_r = \frac{\frac{C_1 V_s}{V_{CC}}}{\frac{h_{FE}}{R_B} - \frac{1}{R_1}} = \frac{\frac{0.01 \times 10^{-6} \times 18}{18}}{\frac{30}{150 \times 10^3} - \frac{1}{15 \times 10^3}} = 0.075 \text{ ms}$$

$$T = T_g + T_r = 0.5 + 0.075 = 0.575 \text{ ms}$$

$$f = \frac{1}{T} = \frac{1000}{0.575} = 1.74 \text{ kHz}$$

Example 12.10: Determine the values of R_1 , R_E , R_B , C_1 and C_3 of a bootstrap circuit shown in Fig. 12.23, if $I_{C1} = 1.5$ mA, $I_{E2} = 1.75$ mA, $h_{FE(\min)} = 30$, $V_{CE(\text{sat})} = 0.3$ V, $V_{BE(\text{sat})} = 0.7$ V and $V_{BE(\text{active})} = V_{D1} = 0.6$ V. Assume $T_s = 12$ ms.

Solution:

To calculate R_1 :

Applying KVL to collector loop of Q_1 , we have the collector voltage of Q_1 when it is ON:

$$V_{C1} = V_{CC} - V_{D1} - I_1 R_1$$

$$\begin{aligned} R_1 &= \frac{V_{CC} - V_{D1} - V_{C1}}{I_1} \\ &= \frac{20 - 0.6 - 0.3}{1.5 \times 10^{-3}} \\ &= 12.73 \text{ k}\Omega \end{aligned}$$

To calculate R_B :

Applying KVL to the base loop of Q_1 we have $V_{CC} - I_{B1} R_B - V_{BE(\text{sat})} = 0$

$$R_B = \frac{V_{CC} - V_{BE(\text{sat})}}{I_{B1}}$$

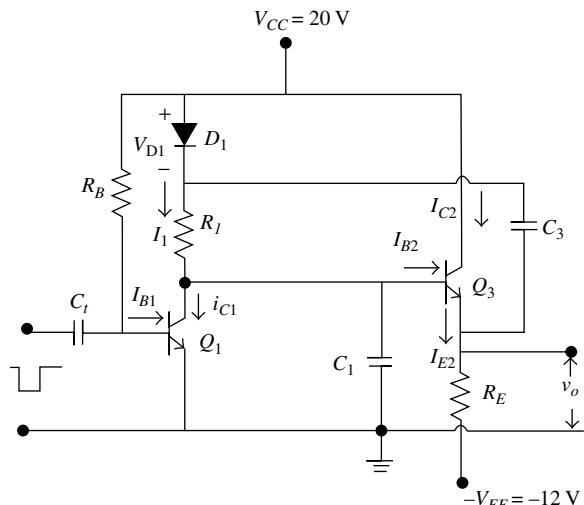


FIGURE 12.23 A bootstrap sweep generator

$$\text{Choose, } I_{B1} = 1.5I_{B1(\min)} = 1.5 \times \frac{I_{C1}}{h_{FE(\min)}} = 1.5 \times \frac{1.5 \times 10^{-3}}{30} 0.075 \text{ mA}$$

Therefore,

$$R_B = \frac{20 - 0.7}{0.075 \times 10^{-3}} = 257.3 \text{ k}\Omega$$

To calculate C_1 :

Sweep Time $T_s = R_1 C_1$

Therefore,

$$C_1 = \frac{T_s}{R_1}$$

Given

$$T_s = 12 \text{ ms}$$

$$C_1 = \frac{12 \times 10^{-3}}{12.73 \times 10^3} = 0.943 \mu\text{F}$$

The value of C_3 should be larger than C_1 , therefore, choose C_3 as 10 times of C_1 .

Therefore,

$$C_3 = 9.43 \mu\text{F}$$

To Calculate R_E :

The output voltage $v_o = V_{CE(\text{sat})} - V_{BE(\text{active})}$

Therefore,

$$v_o = 0.3 - 0.6 = -0.3$$

Applying KVL, to the input side of Q_2 we have:

$$v_o + V_{EE} - R_E i_{E2} = 0$$

Therefore,

$$R_E = \frac{v_o + V_{EE}}{I_{E2}} = \frac{-0.3 + 12}{1.75 \times 10^{-3}} = 6.68 \text{ k}\Omega$$

S U M M A R Y

- Voltage sweep generators are based on the principle of electrostatic deflection.
- In an ideal sweep generator (saw-tooth generator), the sweep voltage increases linearly till T_s (sweep duration) and abruptly falls to a small value.
- In a practical sweep generator, however, at the end of the sweep a small time may elapse before the sweep voltage reaches the initial value. This time interval is called the retrace time, restoration time or fly-back time.
- Slope error e_s is defined as the ratio of the difference between the initial slope and the final slope to the initial slope and is expressed as a percentage.
- Displacement error e_d is defined as the ratio of the maximum difference between the actual sweep voltage and the linear sweep voltage to the sweep amplitude and is expressed as a percentage.
- Transmission error e_t is defined as the ratio of the difference in amplitude between a linear sweep voltage and the practical voltage to the amplitude of the linear sweep and is expressed as a percentage.
- Slope error e_s is given by V_s/V where V_s is the sweep amplitude and V is the peak-to-peak excursion of the output swing. The larger the V , the smaller the deviation from linearity.
- Slope error e_s is also given as T_s/τ where T_s is the sweep duration and τ is the time constant of the sweep circuit. The larger the τ , the smaller the deviation from linearity.
- The interrelation between the three types of errors is given as: $e_d = (1/8)e_s = (1/4)e_t$.
- A UJT is a negative resistance device and is used as a switch.
- The sweep duration of a UJT sweep generator is given by $T_s = \tau \ln(1/(1 - \eta))$ where, η is the intrinsic stand-off ratio and typically lies between 0.6 to 0.8.
- An alternate expression for the sweep duration of an UJT sweep generator is given as $T_s = \tau \ln(V_{BB} - V_V)/(V_{BB} - V_P)$ where V_{BB} is supply voltage, V_V and V_P are the valley and peak voltages of the UJT.
- The auxiliary generator in a Miller sweep generator is replaced by an amplifier with a gain of infinity.
- The auxiliary generator in a bootstrap sweep generator is replaced by an amplifier with unity gain.
- The slope error of a Miller sweep generator is given as $e_{s(Miller)} = e_s \times 1 + (R/R_i)/|A|$ and this is small as $|A|$ is large.
- The slope error of a bootstrap sweep generator is $e_{s(Bootstrap)} \approx e_s(R/R_i)$ and is small only when R_i is large.

M U L T I P L E C H O I C E Q U E S T I O N S

- (1) The application of a voltage time base generator is in a measuring instrument like:
 - CRO
 - Frequency counters
 - Digital voltmeter
 - Multimeter
- (2) The deflection of the electron beam in a CRO employing a voltage sweep generator is based on the principle of:
 - Electromagnetic deflection
 - Electrostatic deflection
 - Frequency multiplication
 - Counting

- (3) Errors e_s , e_d and e_t define:
- Current gain
 - Voltage gain
 - Deviation from linearity
 - Bandwidth
- (4) If in a simple exponential sweep generator, the supply voltage is 200 V and the required sweep amplitude is 10 V, and then the slope error is:
- 5 %
 - 20 %
 - 200 %
 - 0.5 %
- (5) In a simple exponential sweep generator, the time constant of the circuit is 1000 μ s and the sweep duration is 100 μ s, then the slope error is:
- 5 %
 - 100 %
 - 20 %
 - 10 %
- (6) For the output of a voltage sweep generator to be linear, the capacitor must be charged with a:
- Constant current
 - Linearly varying current
 - Exponentially varying current
 - Zero current
- (7) A Miller sweep generator produces a:
- Positive-going sweep
 - Negative-going sweep
 - Constant sweep voltage
- (d) Infinite output voltage
- (8) A bootstrap generator produces a:
- Positive-going sweep voltage
 - Negative-going sweep voltage
 - Constant sweep voltage
 - Infinite sweep voltage
- (9) The slope error e_s and the displacement error e_d are related as:
- $e_s = 2e_d$
 - $8e_s = e_d$
 - $e_s = 4e_d$
 - $e_s = 8e_d$
- (10) The displacement error e_d and the transmission error e_t are related as:
- $e_t = 4e_d$
 - $e_t = 2e_d$
 - $4e_t = e_d$
 - $e_t = e_d$
- (11) The slope error e_s and the transmission error e_t are related as:
- $e_s = 2e_t$
 - $e_s = 0.5e_t$
 - $e_s = e_t$
 - $e_s = 4e_t$
- (12) The sweep duration of a UJT sweep generator is given as:
- 0.69τ
 - $\tau \ln\{(V_{BB} - V_P)/(V_{BB} - V_V)\}$
 - $\tau \ln\{(V_{BB} - V_V)/(V_{BB} - V_P)\}$
 - 1.4τ

SHORT ANSWER QUESTIONS

- Define the three errors that specify deviation from linearity.
- Draw the circuit of a UJT sweep generator and explain its operation.
- Derive the expression for the frequency of oscillations of a UJT sweep generator in terms of η , the intrinsic stand-off ratio.
- Derive the expression for the frequency of oscillations of a UJT sweep generator in terms of V_V and V_P .
- Explain the basic principle employed in a Miller sweep to linearize the non-linear sweep.
- Explain the basic principle employed in a bootstrap sweep to linearize a non-linear sweep.

LONG ANSWER QUESTIONS

- Draw the circuit of a UJT sweep generator and explain its operation. Derive the expression for e_s , e_d and e_t and obtain their inter-relationship.
- Explain the principle of working of a transistor constant current sweep generator with the help of a circuit diagram. Derive the expression for its slope error.
- Explain how a linearly varying sweep voltage is generated in a Miller sweep generator. Draw the circuit and explain its operation. Derive the expression for its slope error.
- Explain the basic principle of a bootstrap sweep generator. Draw the circuit and explain its operation. Derive the expression for its slope error.

UNSOLVED PROBLEMS

- (1) For the UJT relaxation oscillator shown in Fig. 12p.1, $R_{BB} = 4 \text{ k}\Omega$, $R_1 = 0.1 \text{ k}\Omega$, $\eta = 0.6$, $V_V = 3 \text{ V}$, $I_V = 10 \text{ mA}$, $I_P = 0.01 \text{ mA}$.
- Calculate R_{B1} and R_{B2} under quiescent condition (i.e., $I_E = 0$).
 - Calculate the peak voltage, V_P .
 - Calculate the permissible value of R .
 - Calculate the frequency assuming that the retrace time is negligible. Also calculate f using the value of η .
 - Calculate the frequency, also considering the retrace time. Assume $R_{B1} = 0.1 \text{ k}\Omega$ during the retrace time.
 - Calculate the voltage levels of V_{B1} .
 - Plot the waveforms of the output voltage and V_{B1} .

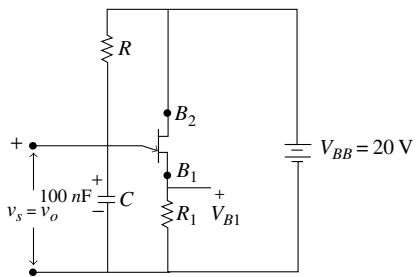


FIGURE 12p.1 The given UJT sweep circuit

- (2) The UJT relaxation oscillator is shown in Fig. 12p.2.

Find:

- The sweep amplitude.
- The slope and displacement errors.
- The duration of the sweep.

Given that $V_V = 3 \text{ V}$, $\eta = 0.6$.

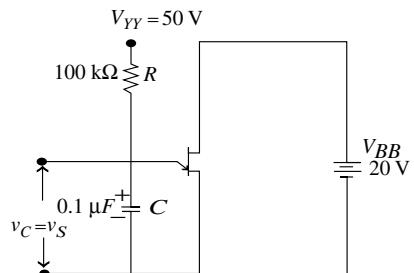


FIGURE 12p.2 The given UJT relaxation oscillator

- (3) (a) Design a UJT sweep circuit shown in Fig. 12p.3(b) to generate a sweep of 15 V amplitude and 3 ms duration, given that $\eta = 0.6$. (b) If the sweep error is 10% and $T_r = 1\%$ of T_s , calculate V_{BB} , V_{YY} , R , R_1 , R_2 and C . If the sweep duration is 300 μs, calculate the new value of C . The V-I characteristic of UJT is as shown in Fig. 12p.3(a).

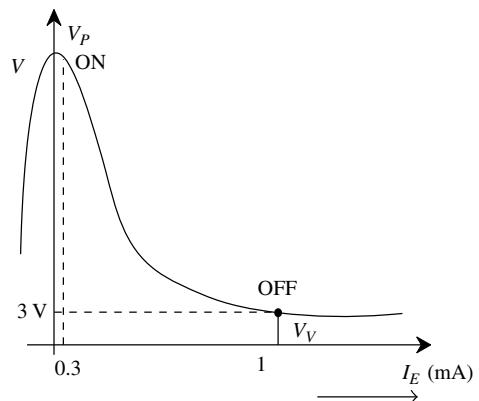


FIGURE 12p.3(a) V-I characteristic of a given UJT

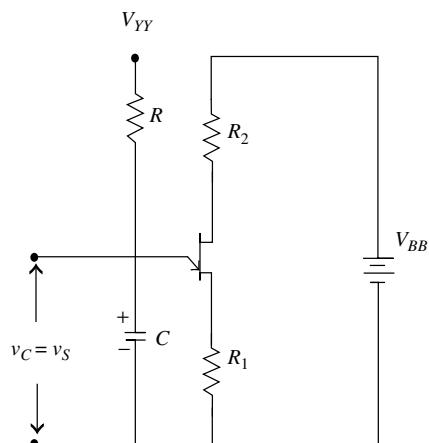


FIGURE 12p.3(b) UJT circuit

- (4) For the Miller's sweep shown in Fig. 12.12(a), $V_{CC} = 24 \text{ V}$, $R_{C2} = 2 \text{ k}\Omega$, $R_{C1} = 10 \text{ k}\Omega$ and $C = 1 \mu\text{F}$. The amplitude of the sweep is 18 V. (a) Calculate the sweep duration T_s ; (b) the retrace time T_r ; (c)

frequency of the sweep generator and (d) the slope error. The transistor has the following parameters:

$$h_{fe} = 100, h_{ie} = 1 \text{ k}\Omega, h_{oe} = 1/20 \text{ k}\Omega \text{ and } h_{re} = 2.5 \times 10^{-4}.$$

- (5) The transistor used in the bootstrap circuit shown in Fig. 12p.4 has the following h -parameter values: $h_{re} = 2.5 \times 10^{-4}$, $h_{ie} = 1.1 \text{ k}\Omega$, $h_{fe} = 60$, $1/h_{oe} = 40 \text{ k}\Omega$. Assume $V_{BE(\text{sat})} = V_{CE(\text{sat})} = 0$. If the applied input gating voltage is a symmetrical square wave of the frequency 9.5 KHz, determine the time-base amplitude, the retrace time and the recovery time.

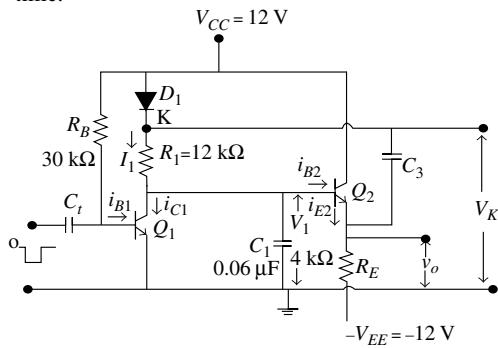


FIGURE 12p.4 The given bootstrap sweep circuit

- (6) Find (a) the sweep amplitude and (b) the slope error for the bootstrap sweep generator shown in Fig. 12p.5, when a 2 kHz symmetrical square wave is applied as an input to it. Plot to scale the input and output waveforms. The typical h -parameter values of transistor are, $h_{fe} = 90$, $1/h_{oe} = 35 \text{ k}\Omega$, $h_{ie} = 1 \text{ k}\Omega$

and $h_{rc} = 1$. Assume all forward-biased junction voltages are zero.

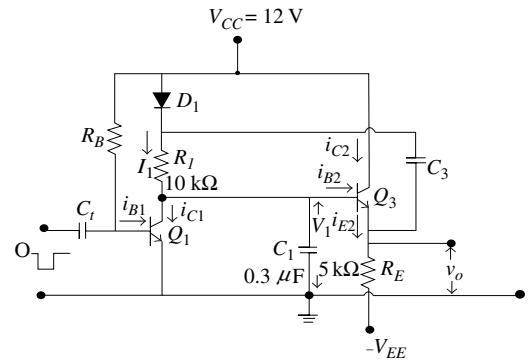


FIGURE 12p.5 A bootstrap sweep circuit

- (7) The transistor bootstrap has the following parameters:

$V_{CC} = 20 \text{ V}$, $V_{EE} = -20 \text{ V}$, $R_B = 15 \text{ k}\Omega$, $R_1 = 5 \text{ k}\Omega$, $R_E = 2.5 \text{ k}\Omega$, $C_1 = 0.001 \mu\text{F}$, $C_3 = 0.25 \mu\text{F}$. The input gate has the amplitude of 1 V and a width of 50 μs . The transistor parameters are $h_{fe} = 60$, $h_{ie} = 2 \text{ k}\Omega$, $1/h_{oe} = 10 \text{ k}\Omega$, $h_{re} = 10^{-4}$ and the forward-biased junction voltages are negligible. The diode is ideal.

(i) Evaluate (a) the sweep speed and the maximum amplitude of the sweep; (b) the retrace time; (c) the peak voltage change across C_3 and the recovery time and (d) the slope error. (ii) Plot the gate voltage, collector current i_{C1} , and the output voltage v_o .

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Current Sweep Generators

LEARNING OBJECTIVES

After reading this chapter, you will be able to:

- Understand the working of a simple current sweep generator
 - Describe the method to linearize the current sweep by adjusting the driving waveform
 - Realize the circuit to generate the trapezoidal driving waveform that achieves linearity correction
 - Understand the principle of working of a transistor television sweep
-

13.1 INTRODUCTION

We saw in Chapter 12 that voltage sweep generators are used where smaller deflections of the electron beam are required, such as in CROs with small screens mainly because of the requirement of supply voltages, as the deviation from linearity is negligible only when the supply voltage is significantly higher than the sweep amplitude. This condition implies that supply voltages could be prohibitively high if larger sweep amplitude is required to achieve larger deflections of the electron beam, as in the case of television and radar receivers. In such instances, voltage sweep generators will not meet the requirements and hence, the need for current sweep generators. The basic principle employed in current sweep generators is electromagnetic deflection. In these sweep generators, when a voltage is applied to a coil of inductance L , the current in the inductance increases linearly with time. Usually a coil or a set of coils—called the yoke—is mounted externally onto the gun structure of the tube and the current in the yoke produces a magnetic field that deflects the electron beam. However, in practice, the current sweep so generated may not necessarily be linear. In order to linearize the current sweep, the driving waveform needs to be adjusted. It will be shown that a trapezoidal driving waveform generates a linear current sweep. The application of a current sweep in a television receiver is considered in the chapter.

13.1.1 A Simple Current Sweep Generator

A simple current sweep generator is shown in Fig. 13.1(a). The circuit basically consists of a transistor used as a switch driven by a trigger signal. The current in the inductor rises exponentially during the period the switch is closed (the transistor is ON). At the end of the trigger signal, the device switches into the OFF state and the current in the inductor decays. If at a time $t = 0$, a voltage V is applied to a coil of inductance L in which the current is initially zero, then the inductor current i_L will increase linearly with time, $i_L = (V/L)t$ (in a capacitor, $V = (I/C)t$). A time-base circuit using this principle is shown in Fig. 13.1(a). The waveforms of this sweep circuit are shown in Fig. 13.1(b).

The trigger signal V_B operates between the two levels. The lower level (negative going period) keeps the transistor in the cut-off state, while the upper level (positive going period) drives the transistor into saturation.

As long as the input is negative, Q_1 is biased OFF and the inductor current is zero. At $t = 0+$, as the input goes positive, Q_1 is driven into saturation. The current i_L increases linearly with time $\{i_L = (V_{CC}/L)t\}$. The inductor current attains a maximum value of I_L , (see Fig. 13.2).

During the sweep period, Q_1 is ON and the voltage at its collector is $V_{CE(sat)}$ which is small. The diode D does not conduct since it is reverse-biased. The sweep terminates at $t = T_s$ when the trigger signal drives the transistor to cut-off. The current in the inductor at T_s is the peak current I_L . A spike of amplitude $I_L R_d$ appears across the inductance L . The net result is that the voltage at the collector of the transistor is $(V_{CC} + I_L R_d)$. The diode D is now forward-biased. The inductor current then continues to flow through the diode D and the resistance R_d till it decays to zero eventually. This decay is exponential with a time constant $\tau = L/R_d$ where, R_d is the sum of the damping resistance and the diode forward resistance:

$$[i_L(t > T_s) = I_L e^{-(R_d/L)t}].$$

At $t = 0-$, $V_{CE} = V_{CC}$. When the transistor is ON, $V_{CE} = V_{CE(sat)}$, which is very small. At $t = T_s$, Q_1 is turned OFF. The net voltage at the collector of the transistor is $(V_{CC} + I_L R_d)$, and must be limited to make sure that it would not exceed the break down voltage of the

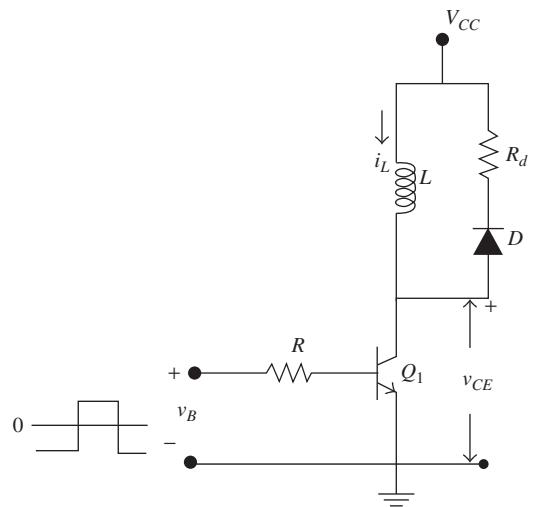


FIGURE 13.1(a) A current sweep generator

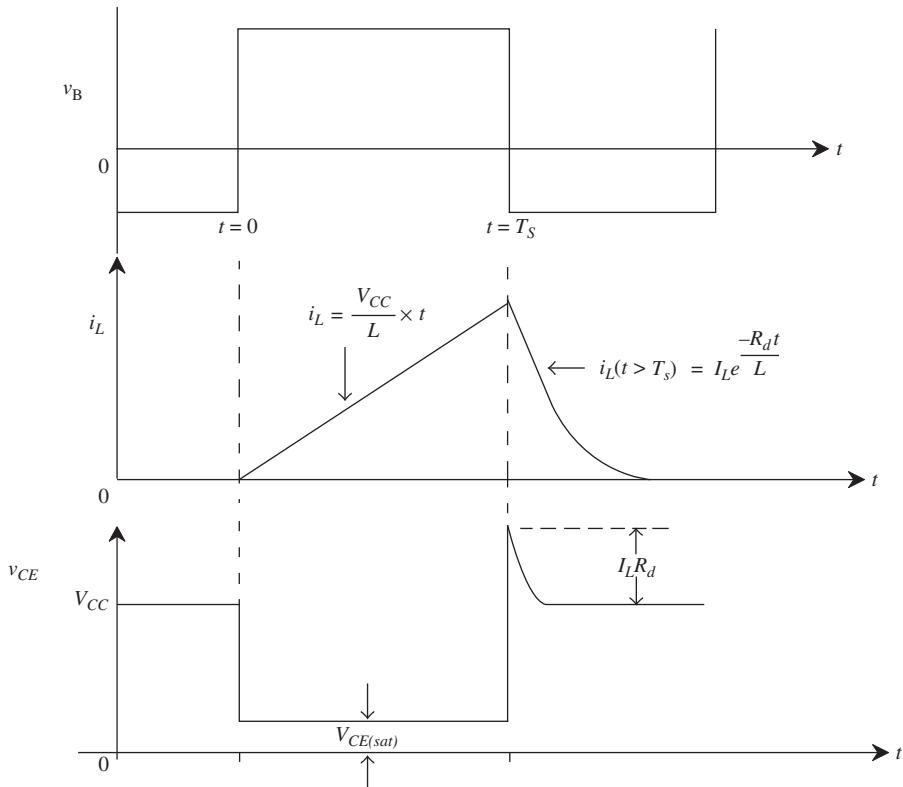


FIGURE 13.1(b) The waveforms of a current sweep circuit

collector base junction. The peak current I_L is chosen on deflection requirements, and as a result a spike of magnitude $I_L R_d$ is generated. There is an upper limit to the size of R_d to limit the magnitude of this spike to a safe value. The spike decays with the same time constant as the inductor current. Thus, we see that the spike duration depends on L , whereas the spike amplitude does not depend on L but instead depends on R_d . So far, the resistance of the inductor R_L and the collector saturation resistance of the transistor, R_{CS} are neglected. Taking R_L and R_{CS} into account, i_L is written as:

$$i_L = \frac{V_{CC}}{R_L + R_{CS}} \left(1 - e^{-(R_L + R_{CS})t/L} \right)$$

Expanding the exponential into series

$$\begin{aligned} i_L &\approx \frac{V_{CC}}{R_L + R_{CS}} \left[1 - 1 + \frac{(R_L + R_{CS})t}{L} - \frac{(R_L + R_{CS})^2 t^2}{2L^2} \right] \\ i_L &= \frac{V_{CC}}{L} t \left[1 - \frac{1}{2} \frac{(R_L + R_{CS})t}{L} \right] \end{aligned} \quad (13.1)$$

The peak-to-peak excursion of the sweep is $V_{CC}/(R_L + R_{CS})$ and the sweep amplitude is I_L .

The slope error is, therefore, given as:

$$e_s = \frac{I_L}{V_{CC}/(R_L + R_{CS})} = \frac{(R_L + R_{CS})I_L}{V_{CC}} \quad (13.2)$$

From Eq. (13.1) it is evident that the sweep is non-linear. The current sweep is linear if the slope error is small. Therefore, from Eq. (13.2), to ensure linearity the voltage $(R_L + R_{CS})I_L$ must be small when compared with the supply voltage, V_{CC} . To understand the procedure to plot the waveforms let us consider an example.

EXAMPLE

Example 13.1: In the circuit shown in Fig. 13.2(a) the resistance of the coil is 10Ω , collector saturation resistance of the transistor is 5Ω and the diode forward resistance is zero.

- For a $400 \mu\text{s}$ sweep, draw waveforms of i_L and v_{CE} indicating the voltage, current levels and time constants.
- Calculate the retrace time (time during which the inductor current falls to 10 per cent of its maximum value) if (i) $R_d = 150 \Omega$ and (ii) $R_d = 1000 \Omega$.
- Calculate the slope error of the sweep.

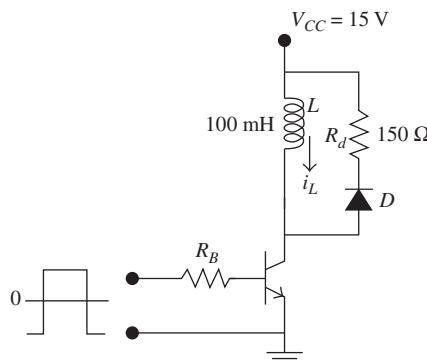


FIGURE 13.2(a) A current sweep generator

Solution:

(a)

$$i_L = \frac{V_{CC} t}{L} \left(1 - \frac{1}{2} \frac{(R_L + R_{CS}) t}{L} \right)$$

At

$$t = T_s, i_L = I_L$$

$$I_L = \frac{15 \times 400 \times 10^{-6}}{100 \times 10^{-3}} \left(1 - \frac{1}{2} \frac{(10 + 5)}{(100 \times 10^{-3})} \times 400 \times 10^{-6} \right) = 0.0582 \text{ A}$$

The waveforms of i_L and v_{CE} are shown in Fig. 13.2(b).

The amplitude of spike $= I_L R_d = 0.0582 \times 150 = 8.73 \text{ V}$

(b)

$$(i) R_d = 150 \Omega, \therefore \tau = \frac{L}{R_d} = \frac{100 \times 10^{-3}}{150} = 667 \times 10^{-6} \text{ s}$$

Let the current fall to 10 per cent of the maximum value at $t = T_r$ (retrace time).

We have

$$\frac{I_L}{i_L} = e^{t/\tau}.$$

At

$$t = T_r, i_L = \frac{I_L}{10}$$

Therefore,

$$e^{T_r/\tau} = 10$$

$$T_{r1} = \tau \ln 10 = 2.30 \tau = 2.3 \times 0.66 \times 10^{-3} = 1.53 \text{ ms}$$

(ii) Let

$$R_d = 1000 \Omega$$

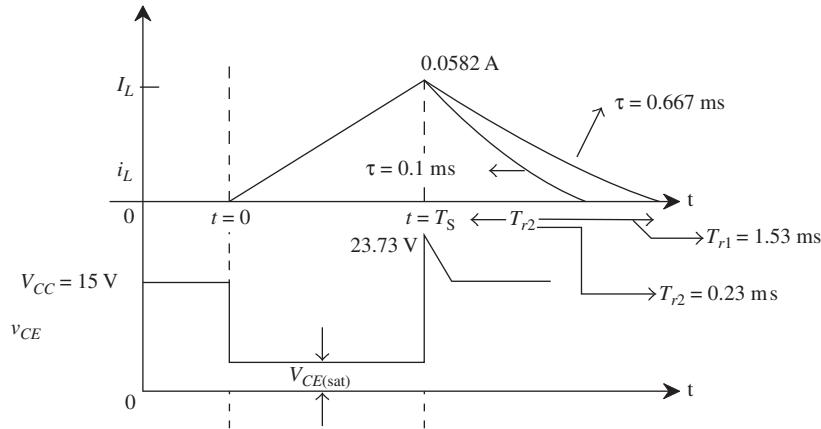
Then

$$\tau = \frac{L}{R_d} = \frac{100 \times 10^{-3}}{1000} = 0.1 \times 10^{-3} \text{ s},$$

$$T_{r2} = \tau \ln 10 = 0.1 \times 10^{-3} \times 2.30 = 0.23 \text{ ms}$$

(c)

$$e_s = \frac{(R_L + R_{CS}) I_L}{V_{CC}} = \frac{(10 + 5) \times 0.0582}{15} = 0.0582$$

FIGURE 13.2(b) The waveforms of i_L and v_{CE}

13.1.2 Linearity Correction through Adjustment of the Driving Waveform

The current sweep shown in Fig. 13.1(a) with pulse as the driving waveform may not necessarily generate a linear output. One simple method to produce a linear current sweep is by adjusting the driving waveform.

The non-linearity encountered in this circuit, as seen from Eq. (13.1), results from the fact that as the inductor (yoke) current increases, the current in the internal resistance of the source R_s also increases. Consequently the voltage across the inductor decreases, as shown in Fig. 13.3(a). So, $v_L = V_s - i_L R_s$ as v_s is constant at V_s .

If we can compensate for the voltage developed across the resistance R_s then the current sweep tends to be linear. This can be achieved as shown in Fig. 13.3(b). Let R_s be the internal resistance of the source v_s .

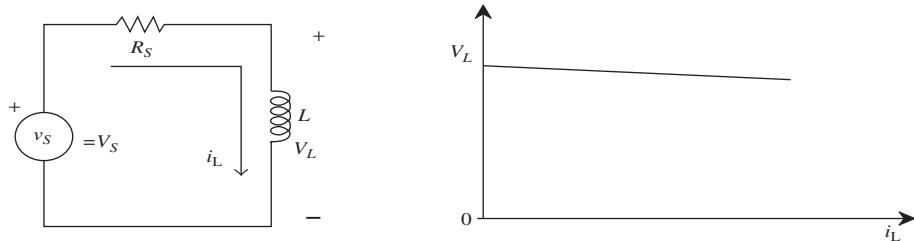


FIGURE 13.3(a) The inductor voltage decreases as the inductor current increases

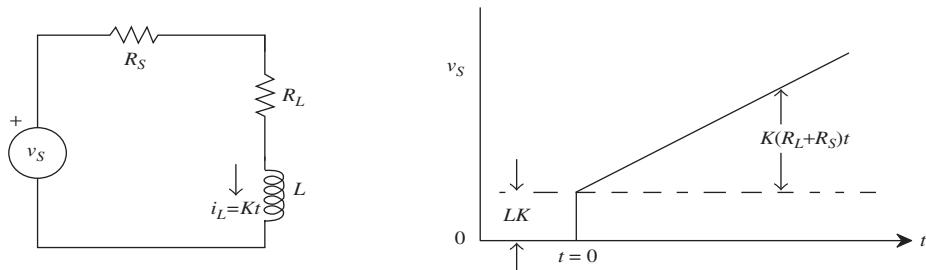


FIGURE 13.3(b) The driving waveform for generating a linear current sweep

The total circuit resistance is $(R_s + R_L)$. Now, if we want the inductor current to vary linearly, i.e., $i_L = Kt$ (where K is the constant of proportionality) then the source voltage v_s is,

$$v_s = L \frac{di_L}{dt} + (R_s + R_L)i_L$$

As,

$$i_L = Kt, \quad \frac{di_L}{dt} = K$$

Therefore,

$$v_s = LK + (R_s + R_L)Kt. \quad (13.3)$$

This waveform consists of a step followed by a ramp $(R_s + R_L)Kt$. Such a waveform is called a trapezoidal waveform. We can thus see that if the driving signal is trapezoidal as given by Eq. (13.3) then the current sweep is linear (i.e., $i_L = Kt$). The Norton representation of the driving source, using Eq.(13.3) is:

$$i_s = \frac{v_s}{R_s} = \frac{LK}{R_s} + \left(1 + \frac{R_L}{R_s}\right)Kt \quad (13.4)$$

The waveform of this current source is also a step followed by a ramp, as shown in Fig. 13.4. Thus, a trapezoidal driving waveform generates a linear current sweep. At the end of the sweep, the current once again will return to zero exponentially with a time constant $\tau = L/(R_s + R_L)$. Generally, $R_s \gg R_L$, hence, $\tau \approx L/R_s$.

The question now is, should R_s be small or should it be large? The resistance R_s is chosen based on two conflicting requirements. If R_s is small, the current will decay slowly and a long period will have to elapse before another sweep is possible, i.e., the fly-back time becomes unacceptably long. This could be construed as a disadvantage. However, the advantage is that the peak voltage developed across the inductor ($= I_L R_s$) may not be unduly large. As a result, the voltage at the collector of the transistor when the sweep terminates ($= V_{CC} + I_L R_s$), which reverse-biases the base-collector diode of the transistor may not be large enough to damage the device.

Alternately, if R_s is large, the current will decay rapidly. This means that the retrace time is negligible, which enables us to initiate the next sweep immediately after the sweep duration. On this count, R_s is required to be large. However, a large peak voltage will appear across the inductor and the voltage that now reverse-biases the base-emitter diode of the transistor may be excessively large and can damage the device.

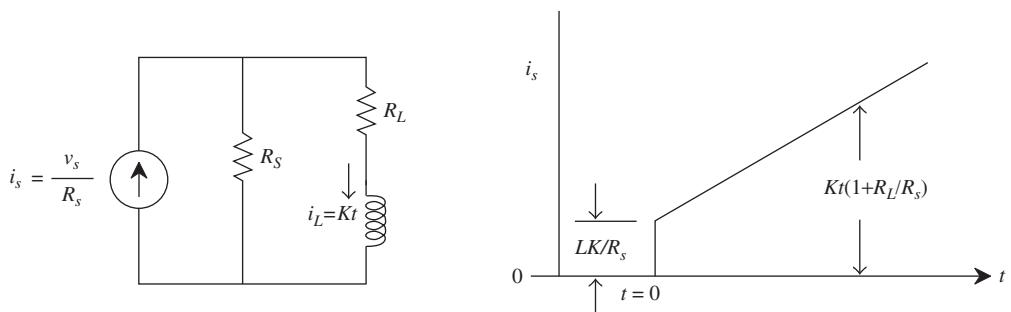


FIGURE 13.4 The trapezoidal current source and the wave form

Generally, a compromise has to be struck such that the spike amplitude is not appreciably large and also the inductor current decays in a smaller time interval. Normally, to achieve this, a damping resistance R_d is connected across the yoke to limit the peak voltage. Let R be the parallel combination of R_s and R_d . Then the retrace time constant is $\tau_r = L/R$. The trapezoidal waveform required to improve the linearity of the current sweep is generated using the circuit shown in Fig. 13.5 from the figure, we have:

$$v_o = V - \frac{R_2}{R_1 + R_2} V e^{-t/(R_1 + R_2)C_1} \quad (13.5)$$

Generally, $R_2 \gg R_1$:

$$v_o = \frac{V(R_1 + R_2) - R_2 V e^{-t/(R_1 + R_2)C_1}}{R_1 + R_2}$$

Dividing by R_2 :

$$v_o = \frac{V \left(1 + \frac{R_1}{R_2} \right) - V e^{-t/(R_1 + R_2)C_1}}{\frac{R_1}{R_2} + 1}$$

Generally $R_2 \gg 1$. Therefore,

$$\begin{aligned} v_o &\approx \frac{VR_1}{R_2} + V - V e^{-t/\{R_2 C_1 (1 + R_1/R_2)\}} \\ &= \frac{VR_1}{R_2} + V(1 - e^{-t/R_2 C_1}) \end{aligned}$$

Expanding the exponential as a series and limiting to the first few terms of the expansion, we have:

$$v_o = V \frac{R_1}{R_2} + \frac{Vt}{R_2 C_1} \left(1 - \frac{t}{2R_2 C_1} \right)$$

If

$$\frac{t}{2R_2 C_1} \ll 1$$

$$v_o = V \frac{R_1}{R_2} + \frac{Vt}{R_2 C_1} \quad (13.6)$$

Thus, the first term is a step and the second term represents a ramp. Therefore, v_o is a step followed by ramp (trapezoidal). A practical linear transistor current sweep is shown in Fig. 13.6.

Here, Q_1 acts as switch, it is ON when the input is zero and is OFF when the input goes negative. R_1 , R_2 and C_1 generate the trapezoidal driving waveform. Q_2 and Q_3 combination is a Darlington pair and R_E stabilizes i_L . The Darlington emitter follower provides a large input resistance and thus eliminates the loading on the driving source by its input. The current i_L varies linearly with time.

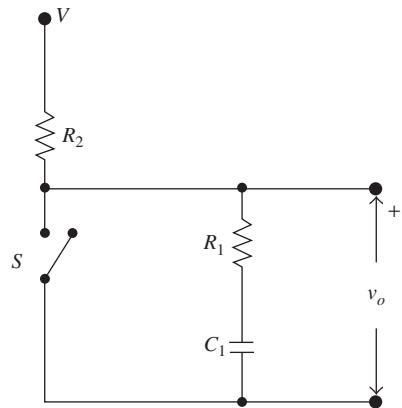


FIGURE 13.5 The generation of a trapezoidal waveform

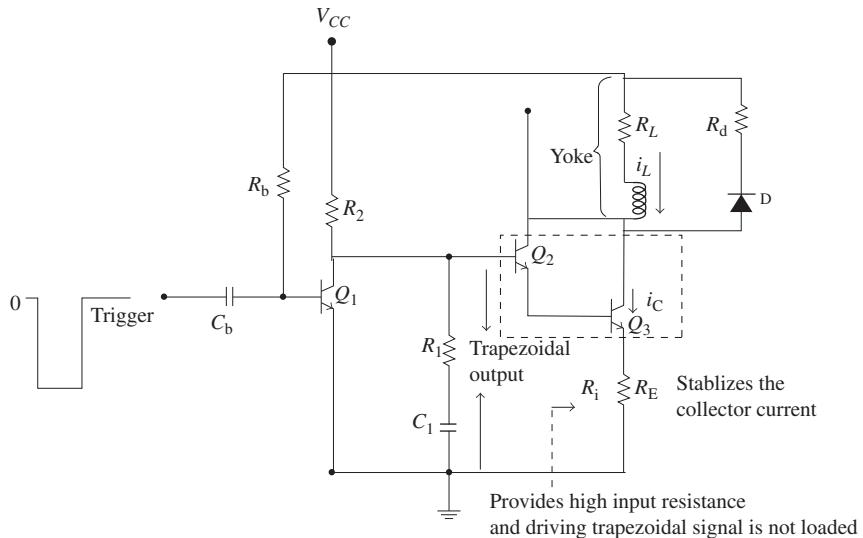


FIGURE 13.6 A practical linear current sweep generator

13.2 A TRANSISTOR TELEVISION SWEEP CIRCUIT

In television receivers, magnetic deflection is used due to higher deflection sensitivity. To produce the necessary magnetic deflection, we use current sweeps. For scanning a horizontal line, the frequency of the sweep circuit in a television receiver is 15.75 kHz, i.e., a total time of $63.5\mu\text{s}$ which is the sum of retrace time or fly-back time ($16\mu\text{s}$) and sweep time ($47.5\mu\text{s}$). During the sweep period the current must increase linearly with time. For the retracing action, current must reverse the direction to bring the spot for next scanning. The maximum energy stored in an inductor of value L is $1/2(LI_m^2)$, where I_m is the peak current. This energy, if dissipated in one cycle, represents the power lost in the yoke:

$$P = \frac{1}{2} \times L \times I_m^2 \times f_h$$

where, $f_h = 15.75$ kHz, the scanning frequency. If $L = 50$ mH, $I_m = 300$ mA, $f_h = 15.75$ kHz, then $P = 35$ W, which is large.

For a television sweep, it is desired that the overall power dissipation should be small. The basic television sweep circuit is shown in Fig. 13.7. Here, The inductor L and the capacitor C form the loss-less tuned circuit. V_{CC} is the supply voltage and it is assumed that the switch is ideal. The waveforms are shown in Fig. 13.8. The operation of the circuit is explained here.

(i) At $t = 0$:

Let us assume that initially the stored energy in a capacitor or an inductor is zero. When the transistor switches ON (closed), the device draws the current; and as the inductor opposes sudden changes in the current, it acts as an open circuit. The current in the inductor at $t = 0$ is, therefore, zero as shown in Fig. 13.8(b). The capacitor acts as a short circuit and charging current flows. The capacitor almost instantaneously charges to voltage V_{CC} and consequently the voltage across the inductor is V_{CC} .

(ii) During time $0 \leq t \leq t_1$:

For the time period $t > 0$ the voltage across the inductor remains at V_{CC} as shown in Fig. 13.8(c). Once the capacitor is fully charged, it behaves as an open circuit for dc. The inductor current increases linearly with time as shown in Fig. 13.8(b) and reaches a peak value I_m at $t = t_1 = T_s$.

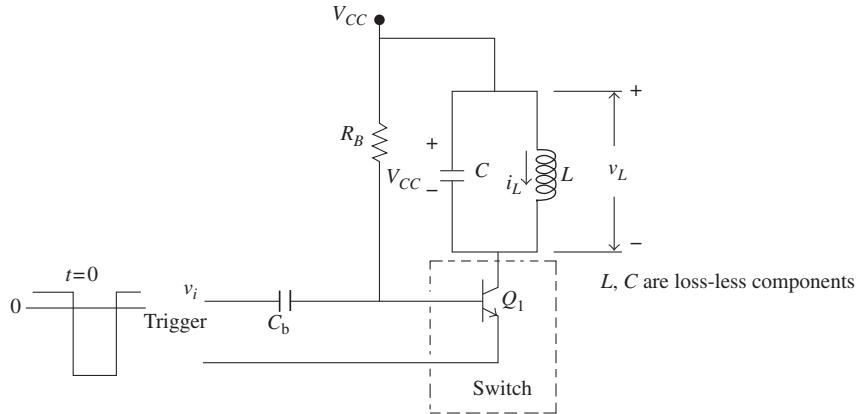


FIGURE 13.7 The basic television sweep circuit

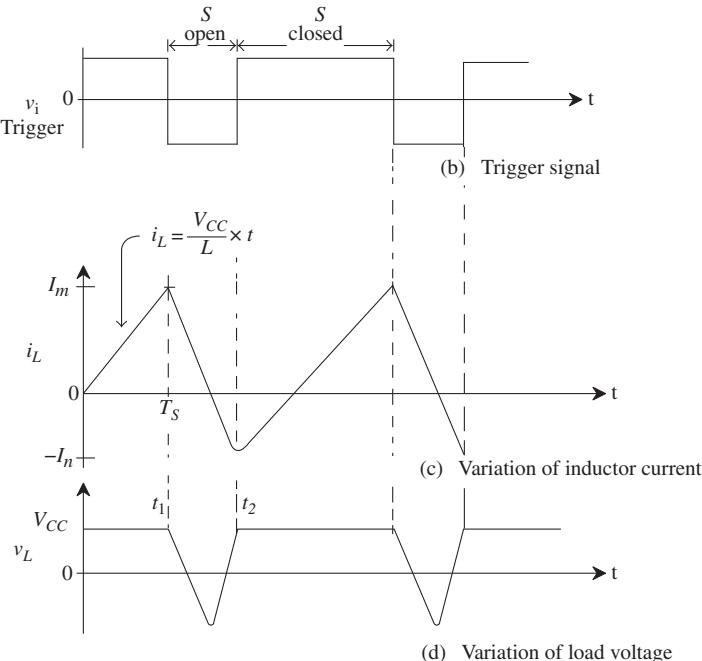


FIGURE 13.8 The waveforms of the television sweep

(iii) During time $t_1 \leq t \leq t_2$:

At time $t = t_1$, when the trigger is negative, the transistor is OFF (switch is open). In the time period $t > T_s$; the voltage across the capacitor, which earlier was V_{CC} , now begins to discharge through the inductor. The current in the inductor begins to decrease. Thus, the LC -tuned circuit oscillates. In this process, the current goes negative and reaches the negative peak. Hence, at $t = t_2$, the inductor current attains the negative peak value ($-I_n$). As the input trigger is once again positive, it drives the switch ON.

(iv) During time $t > t_2$:

We have seen that during the interval t_1 to t_2 , the inductor current is negative and it reaches a peak value of $-I_n$ at $t = t_2$. From this negative value, the current begins to rise linearly with time towards $+I_m$,

since the switch once again closes. Eventually, sometime beyond t_2 , the current in the inductor becomes positive. When the current reaches the peak value $+I_m$, the switch S is again open and the cycle repeats.

S O L V E D P R O B L E M S

Example 13.2: For the circuit shown in Fig. 13.9, at $t = 0$, the driving waveform is applied to the base of the transistor.

- Calculate the time required for the inductor current to reach the maximum value. Assume that the inductor is ideal, the saturation resistance of the transistor is zero and $h_{FE} = 20$.
- Calculate the time required for the inductor current to decay to 10 mA.
- If the sum of saturation resistance and inductive resistance is 20Ω , determine the time required for sweep, T_s , to reach its maximum value I_L .
- Calculate the collector-emitter voltage at the time when the transistor is reverse-biased.

Solution:

$$(a) \text{At } t = 0, \text{ the base current } i_B = I_B = \frac{v_B - V_{BE}}{R_B} = \frac{(10 - 0.7) \text{ V}}{10 \text{ k}\Omega} = 0.93 \text{ mA}$$

Therefore,

$$i_L = I_{L(\max)} = h_{FE} \times I_B = 20 \times 0.93 = 18.60 \text{ mA}$$

Since the transistor is in saturation, the voltage available across the inductor is:

$$v_L = V_{CC} - V_{CE(\text{sat})} = 10 - 0.3 = 9.7 \text{ V}$$

Therefore,

$$I_{L(\max)} = \frac{v_L}{L} T_s$$

$$T_s = \frac{L \times I_{L(\max)}}{v_L} = \frac{10 \times 10^{-3} \times 18.60 \times 10^{-3}}{9.7} = 19.1 \times 10^{-6} \text{ s}$$

- At $t = T_s$ the transistor is reverse-biased, current flowing through the inductor decays with a time constant

$$\tau = \frac{L}{R_d} = \frac{10 \times 10^{-3}}{10} = 1 \text{ ms}$$

The time duration in which the current in inductor decays to 10 mA can be found from the relation:

$$i_L = I_L e^{-t/\tau}$$

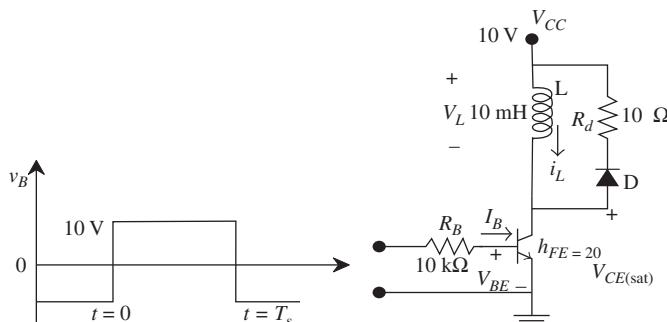


FIGURE 13.9 The given current sweep circuit and the input

We have to calculate t at which $i_L = 10$ mA.

$$10 \times 10^{-3} = 18.60 \times 10^{-3} e^{-t/1 \times 10^{-3}}$$

$$e^{t/10^{-3}} = 1.86$$

Therefore,

$$t = 0.62 \text{ ms}$$

c) If we consider inductor resistance R_L and transistor saturation resistance R_{CS} , the current flowing in the circuit is given by:

$$i_L = \frac{v_L}{R_L + R_{CS}} \left(1 - e^{-t(R_L + R_{CS})/L} \right)$$

At

$$t = T_s, i_L = I_L(\text{max}).$$

$$18.6 \times 10^{-3} = \frac{9.7}{20} \times \left(1 - e^{-20t/10 \times 10^{-3}} \right)$$

$$T_s = 19.1 \mu\text{s}$$

d) At the instant when the transistor is reverse-biased v_{CE} is:

$$v_{CE} = V_{CC} + I_L R_d = 10 + 18.6 \times 10^{-3} \times 10 = 10 + 0.186 = 10.186 \text{ V}$$

Example 13.3: For the triggered current sweep generator shown in Fig. 13.10(a):

- If the sum of the inductor resistance (R_L) and saturation resistance of the transistor (R_{CS}) is zero, calculate V_{CC} required to increase the current in the inductor from zero to 90 mA in 1 ms.
- Draw the waveforms of i_L and V_{CE} , indicating the time constants.
- Find the sweep speed error if $(R_L + R_{CS}) = 10 \Omega$.

Assume the diode to be ideal.

Solution:

Given that the inductor current increases from 0 to its maximum value of 90 mA in 1 ms, as shown in Fig. 13.10(b).

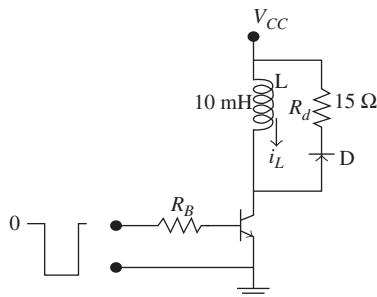


FIGURE 13.10(a) The given current sweep circuit

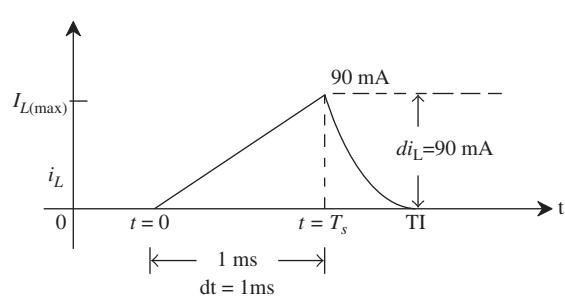


FIGURE 13.10(b) The calculation of the slope of the sweep circuit

(a)

$$V_{CC} = L \frac{di_L}{dt} = 100 \times 10^{-3} \times \left(\frac{90 - 0}{1 - 0} \right) = 9 \text{ V}$$

(b) Time constant

$$\tau = \frac{L}{R_d} = \frac{100 \times 10^{-3}}{15 \Omega} = 6.667 \text{ ms}$$

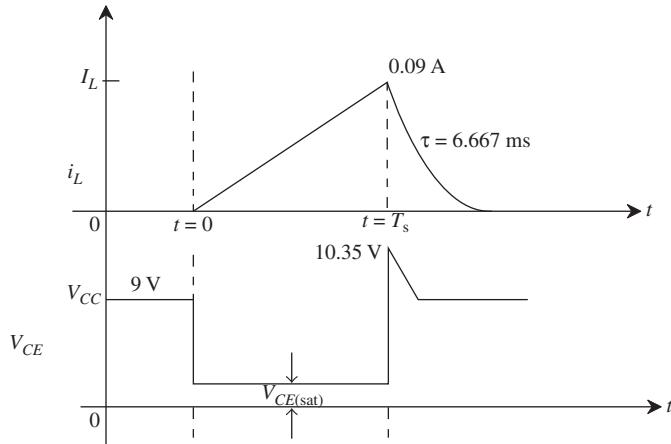
For

$$0 < t < T_s$$

$$i_L = \frac{V_{CC} t}{L} \left(1 - \frac{1}{2} \frac{(R_L + R_{CS}) t}{L} \right)$$

At $t = T_s = 1 \text{ ms}$

$$i_L = I_L = \frac{9 \times 1 \times 10^{-3}}{100 \times 10^{-3}} \left\{ 1 - \frac{1}{2} \left(\frac{0 + 0}{100 \times 10^{-3}} \right) 0.001 \right\} \quad I_L = 0.09 \text{ A}$$

For $t > T_s$, i_L decays with a time constant 6.667 ms.FIGURE 13.10(c) The waveforms of i_L and v_{CE} Spike amplitude $= I_L R_d = 0.09 \times 15 = 1.35 \text{ V}$. The waveforms of i_L and v_{CE} are shown in Fig. 13.10(c).

(c) Given

$$R_L + R_{CS} = 10 \Omega \quad i_L = \frac{V_{CC} t}{L} \left(1 - \frac{1}{2} \frac{(R_L + R_{CS}) t}{L} \right)$$

$$\text{at } t = T_s = 0.001 \text{ s} \quad i_L = I_L = \frac{9 \times 1 \times 10^{-3}}{100 \times 10^{-3}} \left(1 - \frac{1}{2} \times \frac{(10)}{100 \times 10^{-3}} \times 0.001 \right)$$

$$I_L = 0.0855 \text{ A}$$

$$e_s = \frac{(R_L + R_{CS}) I_L}{V_{CC}} = \frac{10 \times 0.0855}{9} \times 100 = 9.5\%$$

SUMMARY

- Current time base generators are used in the applications where large deflection of the electron beam is required like in television and radar receivers.
- Current time base generators work on the principle of electromagnetic deflection.
- A simple current sweep generator gives rise to a non-linear sweep.
- To linearize the current, a trapezoidal waveform is applied as a driving signal to a current sweep circuit.

MULTIPLE CHOICE QUESTIONS

- (1) Television and radar receivers employ the following circuit to derive a larger deflection of the electron beam:
 - Miller's sweep circuit
 - Bootstrap sweep circuit
 - Exponential voltage sweep
 - Current sweep circuit
- (2) The principle employed in a current sweep is:
 - Electrostatic deflection
 - Electromagnetic deflection
 - Frequency synchronization
 - Frequency division
- (3) The driving signal that linearizes a current sweep generator is:
 - Trapezoidal waveform
 - Saw-tooth waveform
 - Square wave
 - Ramp
- (4) A trapezoidal waveform is a:
 - Square wave followed by a ramp
 - Step followed by a ramp
 - Exponential followed by a ramp
 - Pulse
- (5) For the slope error to be negligible in a simple current sweep generator:
 - $V_{CC} >> (R_L + R_{CS}) I_L$
 - $V_{CC} << (R_L + R_{CS}) I_L$
 - $V_{CC} = (R_L + R_{CS}) I_L$
 - None of the above

SHORT ANSWER QUESTIONS

- (1) Explain the basic principle of a current sweep generator.
- (2) With the help of a simple circuit, explain the working of a current sweep generator.
- (3) Suggest a suitable method to improve the linearity of a simple current sweep generator.

LONG ANSWER QUESTIONS

- (1) Draw the circuit of a simple current sweep generator and explain its operation. Derive the expression for its slope error e_s .
- (2) (a) It is said that a trapezoidal driving signal improves the linearity of a current sweep generator. Justify.
 - Suggest a circuit arrangement which will generate a trapezoidal waveform.
 - Explain the working of a practical sweep generator that generates a linear current sweep.

UNSOLVED PROBLEMS

- (1) In the circuit shown in Fig. 13p.1, $L = 100 \text{ mH}$. It is required that the current in L increases from 0 to 50 mA in 1 ms. Find V_{CC} for $R_L = 0$ and $V_{CE(\text{sat})} = 0$. If R_d (damping resistance) is 10Ω , draw the waveforms of i_L and v_{CE} with voltage levels. If the transistor can withstand a collector to emitter voltage of 60 V, what is the maximum value of R_d that can be used?

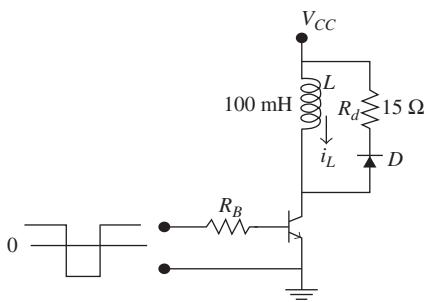


FIGURE 13p.1 The given current sweep generator

- (2) For the circuit shown in Fig. 13p.2, at $t = 0$, the input waveform is applied to the base of the transistor.

- (a) Calculate the time required for the inductor current to reach a maximum value of I_L . Assume that inductor is ideal and the saturation resistance of transistor is zero and $h_{FE} = 40$.
- (b) Calculate the time required for the inductor current to decay to 10 mA.
- (c) If the sum of saturation resistance and inductive resistance is 20Ω , determine the time required for sweep, T_s , to reach its maximum value I_L .
- (d) Calculate the collector-emitter voltage at T_s when the transistor is reverse-biased.

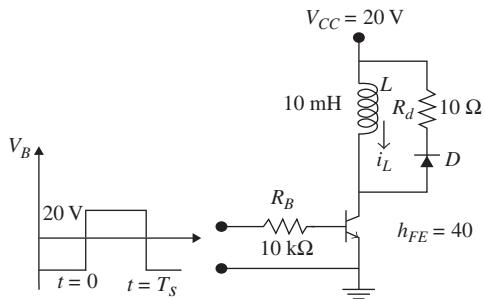


FIGURE 13p.2 The given current sweep and the input

Blocking Oscillators

LEARNING OBJECTIVES

After reading this chapter, you will be able to:

- Understand the principle of operation of regenerative circuits called blocking oscillators
 - Describe monostable blocking oscillators with base timing and emitter timing and derive the expressions for their pulse width
 - Describe RC -controlled and diode-controlled astable blocking oscillators and derive the expressions for the frequency of oscillations
 - Realize the influence of core saturation on the pulse width of the blocking oscillator
-

14.1 INTRODUCTION

A transformer is a device that transfers electrical energy from one winding to the other through inductive coupling. A changing current in the primary winding creates a changing magnetic field. This changing magnetic field induces a changing voltage in the secondary winding by mutual induction. Transformers work on Faraday's law of induction which says that the induced electromotive force or EMF in any closed circuit is equal to the time rate of change of the magnetic flux through the circuit. A pulse transformer is one which is optimized for transmitting rectangular electrical pulses, that is, pulses with negligible rise and fall times and a relatively constant amplitude. To minimize distortion of the pulse shape, a pulse transformer needs to have low values of leakage inductance and distributed capacitance, a high open-circuit inductance and a duty cycle of less than one. The energy stored in the coil during the pulse must be cleaned out before the next pulse. Pulse transformers are wide-band transformers, i.e., they pass a wide band of frequencies with minimum attenuation and no or minimum phase change. These pulse transformers can be used for many applications:

- The desired output pulse amplitude can be obtained by appropriately choosing the turns ratio of the windings in the transformer.
- A centre-tapped transformer can be used to derive positive and negative pulses.
- The pulse transformer can be used as an inter-stage coupling element in applications where there is a need to block the dc component.
- The pulse transformer winding has associated inductance. This, in conjunction with resistance R , can be used as a high-pass RL configuration that serves as a differentiator circuit to derive sharp pulses that can be used to trigger other circuits.

Blocking oscillators are pulse-shaping or pulse-generation circuits. Unlike multivibrators, these circuits use a single transistor to achieve regeneration, which is made possible by the use of a pulse transformer. The output can be fed back to the input in the same phase by properly choosing the winding polarities of the pulse transformer. A blocking oscillator is a single-transistor electronic circuit which can produce a free-running signal, requiring only a capacitor and broad-band (pulse) transformer. The circuit is called a blocking oscillator because the transistor is cut-off or blocked for most of the duty cycle, producing periodic pulses. If the device employed in the circuit is initially OFF, on the application of a trigger, the regenerative circuit quickly turns it ON. However, after a finite time interval, the device switches into the OFF state, ending the quasi-stable state.

This circuit is called a monostable blocking oscillator. This monostable circuit can be modified to generate oscillations and the resultant circuit is called an astable blocking oscillator. However, bistable operation is not possible in a blocking oscillator as a single transistor is used with a transformer as a coupling element for regeneration. In this chapter, we consider astable and monostable blocking oscillators. The influence of core saturation on the pulse width of a monostable circuit is also considered.

14.2 MONOSTABLE BLOCKING OSCILLATORS

A pulse transformer is used as a coupling element in a blocking oscillator to provide positive feedback. If the blocking oscillator generates a single pulse, the circuit is called a monostable circuit. Monostable blocking oscillators can be of two types: Monostable circuit with base timing and monostable circuit with emitter timing. In a monostable blocking oscillator using base timing, the timing resistance R (a component that controls the gate width) is used in the base circuit of the transistor. This circuit, however, does not ensure stable pulse width. Alternatively, the timing resistance R is shifted to the emitter circuit of the transistor in the emitter-timing monostable blocking oscillator. This in turn generates a stable pulse, independent of the temperature-dependent parameters of the transistor.

14.2.1 A Triggered Transistor Monostable Blocking Oscillator (Base Timing)

A monostable blocking oscillator circuit triggered by a pulse is shown in Fig. 14.1(a). The pulse transformer has a turns ratio of $n:1$ where the base circuit has n turns for every turn on the collector circuit. It is connected to provide polarity inversion (as indicated by the dots). A resistance R is included in series with the base of the transistor and this resistance controls the timing, i.e., the pulse duration (hence, the name base-timing). In the quiescent state (when the trigger is zero), the transistor is OFF. V_{BB} may be taken to be zero as the cut-in voltage is small. However, to ensure that the noise pulses do not trigger the circuit and drive it into free-running operation at higher temperatures, a small V_{BB} (few tenths of a volt) is provided. Since $V_{BB} \ll V_{CC}$, V_{BB} can be neglected in the analysis.

The voltage at the collector initially is V_{CC} as, with $V_{BE} \approx 0$, the device is OFF. A trigger (a negative pulse) is momentarily applied to the collector at $t = 0$. This pulse reduces the voltage at the collector. The winding polarities of the transformer (dot convention) are so chosen that when the voltage at the collector goes down, the voltage at the base rises. When $V_{BE} > V_\gamma$, the transistor draws a small base current. The collector current, therefore rises and the collector voltage decreases. This in turn raises the base voltage further. Hence, still some more base and collector currents flow, resulting in a further drop in the collector potential. If the ac loop gain exceeds unity, due to regenerative action, the transistor is driven into saturation quickly. To calculate the pulse width of the monostable multivibrator, we draw the equivalent circuit during pulse formation, as shown in Fig. 14.1(b). In the equivalent circuit, the pulse transformer is replaced by an ideal transformer. If the secondary winding of the transformer is disconnected then we only have the primary winding in the core, which behaves as an inductor.

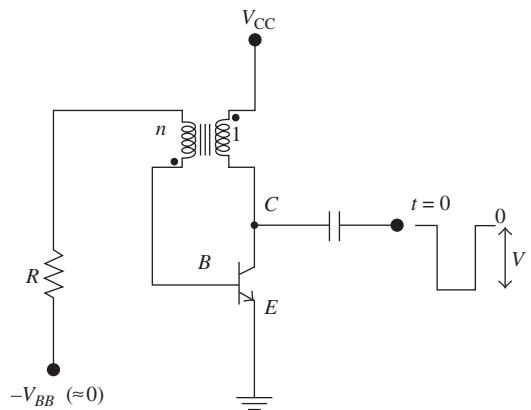


FIGURE 14.1(a) A monostable blocking oscillator with base timing

This inductor is called the magnetizing inductance L and refers to the primary winding. Using this equivalent circuit, it is possible to find the amplitude and the width of the pulse; and to predict its shape. Since $V_{BE} \cong V_{CE} \cong 0$, the base, emitter and collector terminals are at the ground potential, as shown in Fig. 14.1(b). We know that, for an ideal transformer, the sum of the ampere turns is constant and the induced voltages are proportional to the turns. In the quiescent state, as all currents are zero, the algebraic sum of the ampere turns within the dashed box must be zero. Let i be the current in the ideal transformer winding in the collector circuit. The ampere turns in the collector winding is ($i \times 1$) and that in the base winding is ($n \times i_B$). Taking the winding polarities into account:

$$i - ni_B = 0 \quad (14.1)$$

If V is the amplitude of the negative pulse across the collector winding, then nV is the corresponding voltage across the base winding, where n is the number of turns in the base winding. From the collector circuit shown in Fig. 14.1(b):

$$V = V_{CC} \quad (14.2)$$

From the base circuit,

$$i_B = \frac{nV}{R} = \frac{nV_{CC}}{R} \quad (14.3)$$

From Eq. (14.1), $i = ni_B$. Using Eq. (14.3):

$$i = \frac{n^2 V_{CC}}{R} \quad (14.4)$$

If i_m is the magnetizing current and since V is constant, then:

$$L \frac{di_m}{dt} = V$$

Or

$$i_m = \frac{V}{L} t = \frac{V_{CC}}{L} t \quad (14.5)$$

But

$$i_C = i + i_m$$

That is,

$$i_C = \frac{n^2 V_{CC}}{R} + \frac{V_{CC}}{L} t \quad (14.6)$$

From Eq. (14.6) it is seen that the collector current is trapezoidal [the sum of a step, $n^2 V_{CC}/R$ and ramp, $(V_{CC}/L)t$] in nature. Though the collector current is trapezoidal, from Eq. (14.3), it is evident that the base current is constant, as shown in Fig. 14.1(c).

From the output characteristics of the transistor, it is seen that when the device switches suddenly from the OFF state into saturation, the path of the collector current is along the saturation line from P to P' . The pulse ends at P' , at which instant the transistor comes out of saturation and goes into the active region, as shown in Fig. 14.2(a).

At $t = 0+$, the operating point on the collector characteristics is at point P as shown in Fig. 14.2(a).

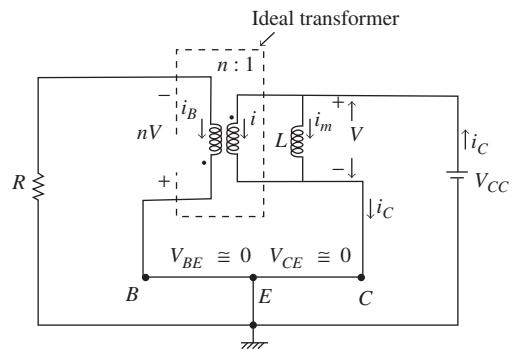


FIGURE 14.1(b) The equivalent circuit of Fig. 14.1(a) during pulse formation

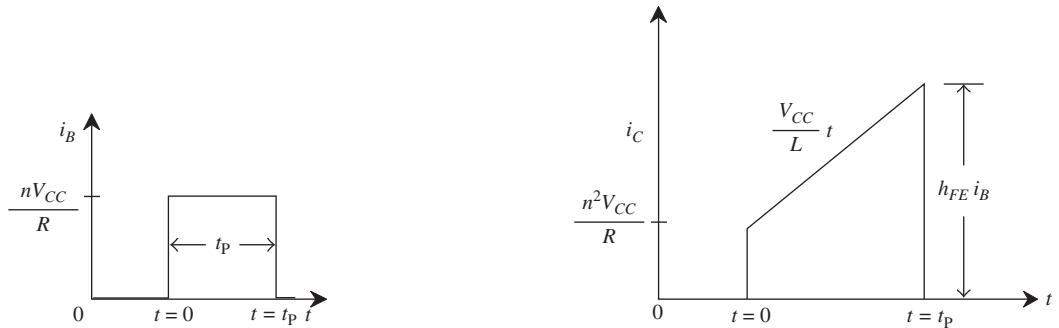


FIGURE 14.1(c) The base and collector current waveforms

From Eq. (14.6), at $t = 0+$:

$$i_C = \frac{n^2 V_{CC}}{R}$$

and from Eq. (14.3):

$$i_B = \frac{n V_{CC}}{R}$$

However, the transistor is said to be in saturation only when:

$$h_{FE} i_B > i_C$$

i.e.,

$$h_{FE} \frac{n V_{CC}}{R} > \frac{n^2 V_{CC}}{R}$$

Or

$$h_{FE} > n \quad (14.7)$$

This condition in Eq. (14.7) can be easily satisfied as the turns ratio n is usually close to one and h_{FE} is reasonably large. For $t > 0$, the collector current increases and the operating point moves up the curve (point P') corresponding to the constant base current:

$$i_B = \frac{n V_{CC}}{R} = I_B$$

as shown in Fig. 14.2(a).

When the point P' is reached, the voltage at the collector $V_C (= V_{CE})$ increases rapidly and, for the given winding polarities, the voltage at the base decreases, resulting in a decreased base current. At this point P' , the transistor comes out of saturation into the active region. In the active region, as the loop gain is greater than unity, the transistor is quickly driven into cut-off by regenerative action and the pulse is terminated. The pulse width t_p is determined by the condition:

$$i_C = h_{FE} i_B \quad (14.8)$$

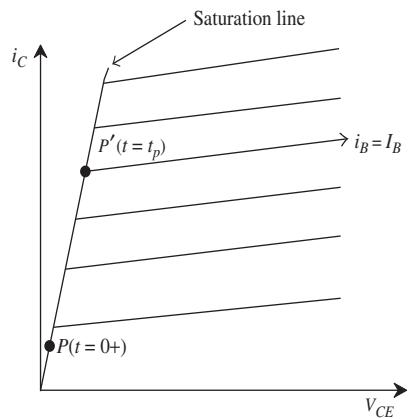


FIGURE 14.2(a) The output characteristics

From Eq. (14.3), we have:

$$i_B = \frac{nV_{CC}}{R}$$

$$i_C = h_{FE} \frac{nV_{CC}}{R} \quad (14.9)$$

From Eq. (14.6):

$$i_C = \frac{n^2 V_{CC}}{R} + \frac{V_{CC}}{L} t$$

Substituting these values in Eq. (14.6), at $t = t_p$:

$$\frac{n^2 V_{CC}}{R} + \frac{V_{CC}}{L} t_p = h_{FE} \frac{nV_{CC}}{R} \quad (14.10)$$

$$V_{CC} \frac{t_p}{L} = h_{FE} \frac{nV_{CC}}{R} - \frac{n^2 V_{CC}}{R} = \frac{nV_{CC}}{R} (h_{FE} - n)$$

Therefore,

$$t_p = \frac{nV_{CC}}{R} \times \frac{L}{V_{CC}} (h_{FE} - n) = \frac{nL}{R} (h_{FE} - n)$$

Therefore,

$$t_p \approx \frac{nL}{R} h_{FE} \quad (14.11)$$

since n is very small when compared to h_{FE} . Eq. (14.11) indicates that the pulse width t_p varies linearly with h_{FE} . However, h_{FE} is a temperature-dependent parameter that may vary with transistor replacement also. Hence, stable pulse width can not be maintained with base timing. Thus, the major limitation with the monostable blocking oscillator with base timing is that a stable pulse width cannot be maintained, as elucidated in these discussions and exemplified by Example 14.1.

One way to ensure that the pulse width of the blocking oscillator is independent of h_{FE} (hence, stable) is to remove the timing resistance R from the base loop and include it in the emitter loop.

EXAMPLE

Example 14.1: The monostable blocking oscillator shown in Fig. 14.1 (a), has the following parameters: $V_{CC} = 10$ V, $R = 0.5$ k Ω , $L = 5$ mH, $h_{FE} = 30$ and $n = 1.5$. (a) Calculate and plot the base current and collector current waveforms and calculate the pulse width. (b) if due to temperature variation, h_{FE} increases to 40, calculate the pulse width. (c) Due to the replacement of the transistor, if the new transistor has $h_{FE} = 25$, what is the new pulse width?

Solution:

(a) From Eq. (14.3) we have:

$$i_B = \frac{nV_{CC}}{R} = \frac{1.5 \times 10}{0.5 \times 10^3} = 30 \text{ mA}$$

From Eq. (14.6):

$$i_C = \frac{n^2 V_{CC}}{R} + \frac{V_{CC}}{L} t = \frac{(1.5)^2 \times 10}{0.5 \times 10^3} + \frac{10}{5 \times 10^{-3}} t = 45 \times 10^{-3} + 2 \times 10^3 t$$

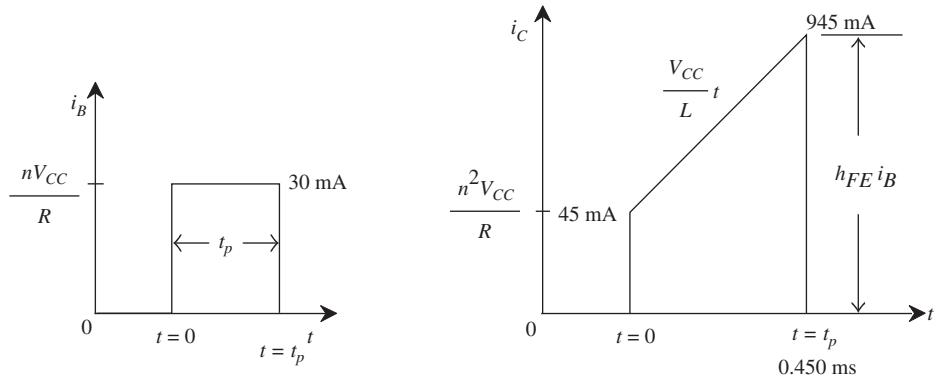


FIGURE 14.2(b) The waveforms for condition (a)

Therefore, from Eq. (14.11):

$$t_p \approx \frac{nL}{R} h_{FE} = \frac{1.5 \times 5 \times 10^{-3}}{0.5 \times 10^3} \times 30 = 0.450 \text{ ms}$$

i_C at $t = 0$ is, $i_C = 45 \text{ mA}$

i_C at $t = t_p$ is $i_C = 45 \times 10^{-3} + 2 \times 10^3 \times 0.450 \times 10^{-3} = 945 \text{ mA}$

(b) Pulse width when $h_{FE} = 40$

$$t_p \approx \frac{nL}{R} h_{FE} = \frac{1.5 \times 5 \times 10^{-3}}{0.5 \times 10^3} \times 40 = 0.6 \text{ ms}$$

(c) Pulse width when $h_{FE} = 25$

$$t_p \approx \frac{nL}{R} h_{FE} = \frac{1.5 \times 5 \times 10^{-3}}{0.5 \times 10^3} \times 25 = 0.375 \text{ ms}$$

The waveforms for the condition (a) are plotted in Fig. 14.2(b).

14.2.2 A Triggered Transistor Blocking Oscillator (Emitter Timing)

A triggered transistor blocking oscillator with emitter timing is shown in Fig. 14.3 (a). This blocking oscillator consists of a transistor with an emitter resistance and a three-winding pulse transformer. The turns ratio of the transformer in the base and collector windings is $n : 1$. Another winding, connected to load R_L (output winding), has n_1 turns in it. The polarities of the base and collector windings are so chosen that the signal appearing at the collector undergoes phase inversion when it appears at the base, as indicated by the dots on the transformer windings. The polarity of the third winding (output winding) of the transformer is chosen, in this specific case, to be similar to that of the collector winding so as to derive a positive pulse. One can derive a pulse of opposite polarity by choosing an opposite polarity for the output winding. The equivalent circuit during pulse formation is shown in Fig. 14.3(b).

Let a negative pulse of magnitude V be applied at the collector. Then the voltage in the base winding is nV and that in the third winding (output winding) is $n_1 V$. The base, emitter and collector terminals are at the same potential.

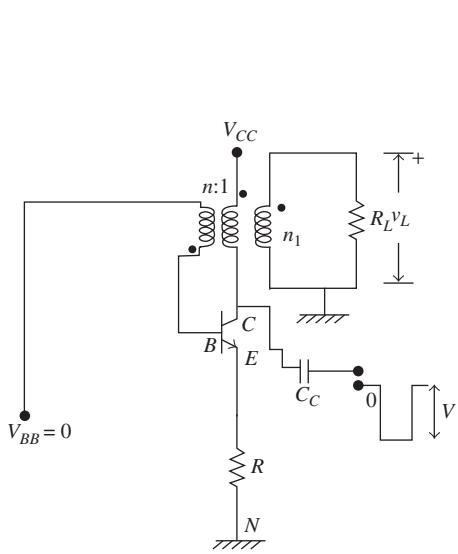


FIGURE 14.3(a) A monostable blocking oscillator with emitter timing

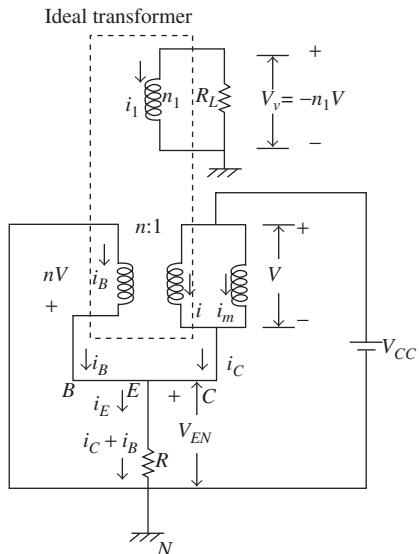


FIGURE 14.3(b) The equivalent circuit of Fig. 14.3(a) during pulse formation

Applying KVL to the outside loop, as shown in Fig. 14.3(c):

$$V_{CC} = V + nV \quad (14.12)$$

Therefore,

$$V_{CC} = V(n+1)$$

Hence,

$$V = \frac{V_{CC}}{n+1} \quad (14.13)$$

From the base circuit shown in Fig. 14.3(d), the drop across R is:

$$V_{EN} = nV = (i_C + i_B)R \quad (14.14)$$

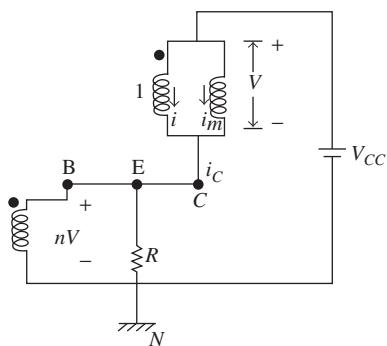


FIGURE 14.3(c) The outer loop of the oscillator circuit

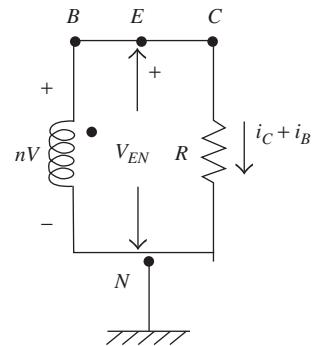


FIGURE 14.3(d) The base circuit of the transistor

From the given current direction:

$$i_C + i_B = i_E \quad (14.15)$$

For the given current directions, from Eq. (14.14) and (14.15):

$$i_E = i_C + i_B = \frac{nV}{R} \quad (14.16)$$

However, from Eq. (14.13):

$$V = \frac{V_{CC}}{n+1}$$

Therefore,

$$(i_C + i_B) = i_E = \frac{n}{n+1} \times \frac{V_{CC}}{R} \quad (14.17)$$

The emitter current as given by Eq. (14.17) is constant. To find i_C and i_B , we need to have another relation between i_C and i_B . The sum of the ampere turns in an ideal transformer is zero, as shown in Fig. 14.3(b):

$$i - ni_B + n_1 i_1 = 0 \quad (14.18)$$

where, $(i \times 1)$ is the ampere turns in the collector winding, $(n \times i_B)$ is the ampere turns in the base winding and $(n_1 \times i_1)$ is the ampere turns in the output winding.

From the load circuit:

$$i_1 = \frac{-n_1 V}{R_L} \quad (14.19)$$

From the equivalent circuit:

$$i = i_C - i_m \quad \text{and} \quad i_m = \frac{Vt}{L} \quad (14.20)$$

Therefore,

$$i = i_C - \frac{Vt}{L} \quad (14.21)$$

Substituting these values in Eq. (14.18):

$$i_C - \frac{Vt}{L} - ni_B - \frac{n_1^2 V}{R_L} = 0 \quad (14.22)$$

Equation 14.22 is the required second relation involving i_C and i_B . From Eq. (14.17):

$$\begin{aligned} i_C + i_B &= \frac{n}{n+1} \times \frac{V_{CC}}{R} \\ i_B &= -i_C + \frac{n}{n+1} \times \frac{V_{CC}}{R} \end{aligned} \quad (14.23)$$

Substituting Eq. (14.23) in Eq. (14.22):

$$i_C - \frac{Vt}{L} - n \left(-i_C + \frac{n}{n+1} \times \frac{V_{CC}}{R} \right) - \frac{n_1^2 V}{R_L} = 0 \quad i_C(n+1) = \frac{Vt}{L} + \frac{n_1^2 V}{R_L} + \frac{n^2}{n+1} \times \frac{V_{CC}}{R}$$

From Eq. (14.13):

$$V = \frac{V_{CC}}{n+1}$$

Therefore,

$$i_C(n+1) = \frac{V_{CC}}{n+1} \times \frac{t}{L} + \frac{n_1^2 V_{CC}}{(n+1) R_L} + \frac{n^2}{n+1} \times \frac{V_{CC}}{R} = \frac{V_{CC}}{n+1} \left(\frac{t}{L} + \frac{n_1^2}{R_L} + \frac{n^2}{R} \right)$$

Therefore,

$$i_C = \frac{V_{CC}}{(n+1)^2} \left(\frac{t}{L} + \frac{n_1^2}{R_L} + \frac{n^2}{R} \right) \quad (14.24)$$

From Eq. (14.23):

$$i_B = \frac{n}{n+1} \times \frac{V_{CC}}{R} - i_C$$

And from Eq. (14.24):

$$i_C = \frac{V_{CC}}{(n+1)^2} \left(\frac{t}{L} + \frac{n_1^2}{R_L} + \frac{n^2}{R} \right)$$

$$i_B = \frac{n}{n+1} \times \frac{V_{CC}}{R} - \frac{V_{CC}}{(n+1)^2} \left(\frac{t}{L} + \frac{n_1^2}{R_L} + \frac{n^2}{R} \right) = \frac{V_{CC}}{(n+1)^2} \left(\frac{n(n+1)}{R} - \frac{t}{L} - \frac{n_1^2}{R_L} - \frac{n^2}{R} \right)$$

$$= \frac{V_{CC}}{(n+1)^2} \left(\frac{n^2 + n - n^2}{R} - \frac{t}{L} - \frac{n_1^2}{R_L} \right)$$

$$i_B = \frac{V_{CC}}{(n+1)^2} \left(\frac{n}{R} - \frac{n_1^2}{R_L} - \frac{t}{L} \right) \quad (14.25)$$

The emitter current:

$$i_E = i_C + i_B = \frac{n}{n+1} \times \frac{V_{CC}}{R}$$

Again, using Eq. (14.13):

$$V = \frac{V_{CC}}{n+1}$$

Therefore,

$$i_E = \frac{nV}{R} \quad (14.26)$$

The waveforms of these three currents, i_C , i_E and i_B , are plotted in Fig. 14.3(e).

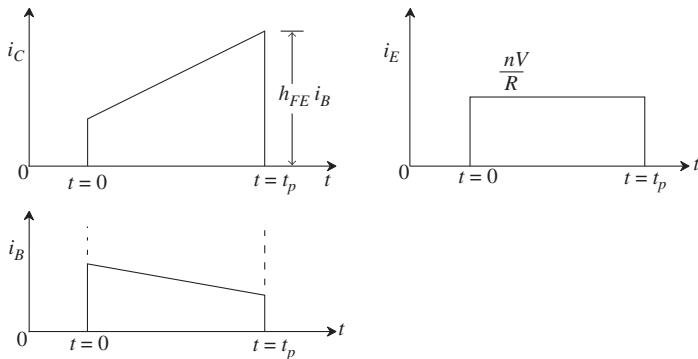


FIGURE 14.3(e) The waveforms of the currents

From the waveforms, it is seen that the collector current is trapezoidal (step followed by a positive ramp), as is the base current (step followed by a negative ramp). However the emitter current is constant during the pulse formation. The waveforms of the voltages are shown in Fig. 14.3(f).

From the waveforms shown in Fig. 14.3(f), it is seen that when a negative trigger of magnitude V is applied, the voltage at the collector, V_{CN} falls by V . At the end of the pulse, this voltage is once again required to return to V_{CC} . However, a spike appears and eventually decays as the inductor current does not immediately become zero when the transistor is switched into the OFF state. Because of the polarity inversion, the voltage at the base, V_{BN} is of positive polarity. The voltage in the output winding is typically the inverted version of V_{CN} , but is referenced to the zero level.

At $t = t_p$, due to regenerative action, the transistor turns OFF and terminates the pulse when $i_C = h_{FE}i_B$.

Substituting Eq. (14.24) and Eq. (14.25), at $t = t_p$ in $i_C = h_{FE}i_B$

$$\frac{V_{CC}}{(n+1)^2} \left(\frac{n^2}{R} + \frac{n_1^2}{R_L} + \frac{t_p}{L} \right) = h_{FE} \frac{V_{CC}}{(n+1)^2} \left(\frac{n}{R} - \frac{n_1^2}{R_L} - \frac{t_p}{L} \right)$$

$$\frac{n^2}{R} + \frac{n_1^2}{R_L} + \frac{t_p}{L} = h_{FE} \left(\frac{n}{R} - \frac{n_1^2}{R_L} - \frac{t_p}{L} \right)$$

$$\frac{t_p}{L} (1 + h_{FE}) = \frac{n}{R} (h_{FE} - n) - \frac{n_1^2}{R_L} (1 + h_{FE}) \quad \frac{t_p}{L} = \frac{n}{R} \times \frac{(h_{FE} - n)}{1 + h_{FE}} - \frac{n_1^2}{R_L}$$

Therefore,

$$t_p = \frac{nL}{R} \left(\frac{h_{FE} - n}{1 + h_{FE}} \right) - \frac{n_1^2 L}{R_L} \quad (14.27a)$$

Usually n is small and lies typically between 0.2 and 1. As $h_{FE} \gg n$ in Eq. (14.27a),

$$\left(\frac{h_{FE} - n}{1 + h_{FE}} \right) \approx 1$$

Therefore,

$$t_p = \frac{nL}{R} - \frac{n_1^2 L}{R_L} \quad (14.27b)$$

For t_p to be positive:

$$\frac{nL}{R} > \frac{n_1^2 L}{R_L}$$

Or

$$R_L > \frac{n_1^2 R}{n} \quad (14.28)$$

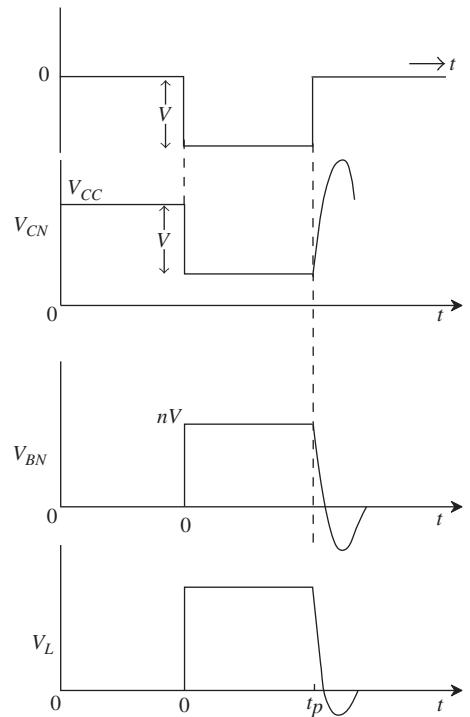


FIGURE 14.3(f) The voltage waveforms

This is the condition to be satisfied for pulse formation. Thus, the pulse width is independent of h_{FE} and this circuit generates a pulse of stable duration.

EXAMPLE

Example 14.2: The blocking oscillator with emitter timing shown in Fig. 14.3(a) has the following parameters: $n = 1$, $n_1 = 1$, $L = 5 \text{ mH}$, $R = 0.5 \text{ k}\Omega$, $h_{FE} = 25$ and $V_{CC} = 10 \text{ V}$. Calculate (a) the amplitude of the trigger; (b) the value of R_L that allows the pulse formation; (c) the pulse width with $h_{FE} = 25$ and also calculate t_p using the approximate relation; (d) the base, collector and emitter currents and (e) plot the current waveforms.

Solution:

(a) The Amplitude of the trigger pulse is:

$$V = \frac{V_{CC}}{n+1} = \frac{10}{1+1} = 5.0 \text{ V}$$

(b) The value of R_L that allows the pulse formation is given by the relation:

$$R_L > \frac{n_1^2 R}{n}$$

$$\frac{n_1^2 R}{n} = \frac{1 \times 0.5 \times 10^3}{1} = 500 \Omega$$

As R_L should be greater than 500Ω , choose, $R_L = 1000 \Omega$

(c) The pulse width is calculated using the relation:

$$t_p = \frac{nL}{R} \left[\frac{h_{FE} - n}{1 + h_{FE}} \right] - \frac{n_1^2 L}{R_L} = \frac{1 \times 5 \times 10^{-3}}{0.5 \times 10^3} \left(\frac{25 - 1}{1 + 25} \right) - \frac{1 \times 5 \times 10^{-3}}{1 \times 10^3} = 9.23 - 5 = 4.23 \mu\text{s}$$

The pulse width using the approximate relation is given by:

$$t_p = \frac{nL}{R} - \frac{n_1^2 L}{R_L} = \frac{1 \times 5 \times 10^{-3}}{0.5 \times 10^3} - \frac{1 \times 5 \times 10^{-3}}{1 \times 10^3} = 10 - 5 = 5 \mu\text{s}$$

(d) The base current is given by the relation:

$$i_B(t = t_p) = \frac{V_{CC}}{(n+1)^2} \left(\frac{n}{R} - \frac{n_1^2}{R_L} - \frac{t}{L} \right) = \frac{10}{(1+1)^2} \left(\frac{1}{0.5 \times 10^3} - \frac{1}{1 \times 10^3} - \frac{4.23 \times 10^{-6}}{5 \times 10^{-3}} \right) = 0.38 \text{ mA}$$

$$i_B(t = 0) = 2.5 \text{ mA}$$

Collector current i_C is given by:

$$i_C(t = t_p) = \frac{V_{CC}}{(n+1)^2} \left(\frac{t}{L} + \frac{n_1^2}{R_L} + \frac{n^2}{R} \right) = 2.5 \left(\frac{4.23 \times 10^{-6}}{5 \times 10^{-3}} + \frac{1}{1 \times 10^3} + \frac{1}{0.5 \times 10^3} \right) = 9.615 \text{ mA}$$

$$i_C(t = 0) = 7.5 \text{ mA}$$

The emitter current i_E is given as:

Therefore,

$$i_E = \frac{nV}{R} = \frac{5}{0.5 \times 10^3} = 10 \text{ mA}$$

(e) The current waveforms are shown in Fig. 14.3(g).

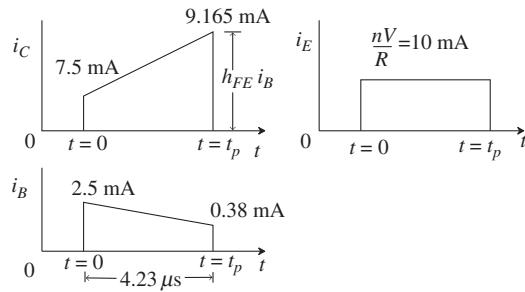


FIGURE 14.3(g) The waveforms of the currents

14.3 ASTABLE BLOCKING OSCILLATORS

Now let us consider astable operation. In an astable operation, the device switches state automatically. However, in astable blocking oscillators, a trigger is used to initiate regeneration after which the circuit oscillates on its own. Here, two types of astable blocking oscillators are considered: a diode-controlled astable blocking oscillator and an RC -controlled astable blocking oscillator. In a diode-controlled astable blocking oscillator, a diode circuit is used to trigger regeneration and the operation then switches to astable mode whereas in an RC -controlled astable blocking oscillator, an RC circuit is used for the astable operation.

14.3.1 Diode-controlled Astable Blocking Oscillators

A diode-controlled astable blocking oscillator is shown in Fig. 14.4(a). If a negative pulse is applied at the collector of Q , the base current starts to flow and regeneration takes place as discussed earlier (Section 14.2.2). The waveforms indicated in Fig. 14.3(e) and Fig. 14.3(f), for $0 \leq t \leq t_p$ are generated. When regeneration takes place, the diode combination (D_1 and D_2) is OFF and the circuit is essentially a monostable circuit. The amplitude and the duration of the pulse have the values previously calculated for the monostable circuit (for

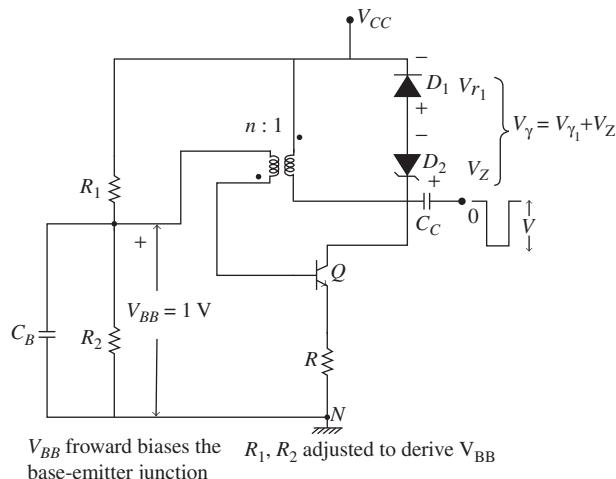


FIGURE 14.4(a) A diode-controlled astable blocking oscillator

$V_{BB} \ll V_{CC}$). At the end of the pulse, the magnetizing current is i_m .

$$L \frac{di_m}{dt} = V$$

Or

$$i_m = \frac{V}{L} t_p \quad \text{and} \quad V = \frac{V_{CC}}{n+1}$$

Therefore,

$$i_m = \frac{V_{CC}}{n+1} \times \frac{t_p}{L} = I_o \text{ (the peak magnetizing current)} \quad (14.29)$$

From Eq. (14.27 b), t_p is calculated as:

$$t_p = \frac{nL}{R} - \frac{n_1^2 L}{R_L} \quad (14.30)$$

With $R_L \rightarrow \infty$

$$t_p = \frac{nL}{R} \quad (14.31)$$

Substituting the Eq. (14.31) in Eq. (14.29):

$$I_o = \frac{V_{CC}}{n+1} \times \frac{nL}{R} \times \frac{1}{L} = \frac{V_{CC}}{R} \times \frac{n}{n+1} \quad (14.32)$$

which shows that the peak magnetizing current is independent of the inductance. At $t = t_p$, the transistor is cut-off; the diode combination conducts and the inductor current now flows through the winding capacitance of the transformer, as shown in Fig. 14.5(a).

If $R_f = 0$, V_γ appears directly across L and C . Hence, the collector voltage rises above V_{CC} by V_γ . Since, for $t > t_p$:

$$L \frac{di_m}{dt} = -V_\gamma$$

Then, shifting the time origin to the end of the pulse, we obtain:

$$i_m = \frac{-V_\gamma t}{L} + I_o \quad (14.33)$$

The magnetizing current i_m decreases linearly with time after the pulse ends. The diode current also falls to zero at a time t_f .

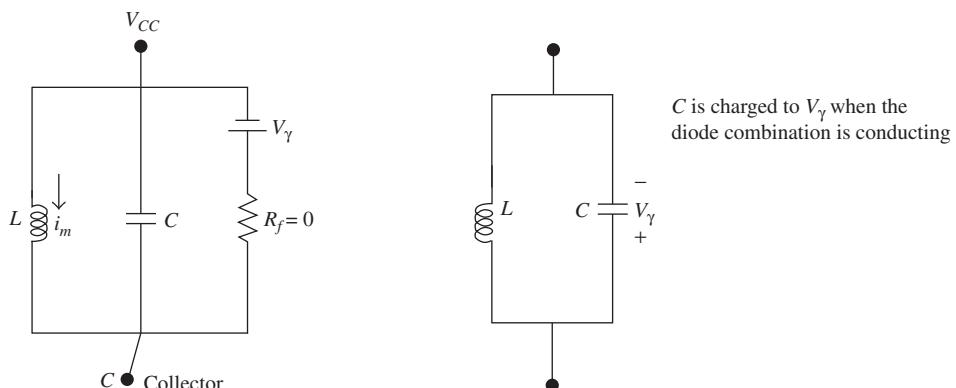


FIGURE 14.5(a) When Q_1 is OFF the diode combination is ON, transistor is cut-off; (b) the ringing circuit

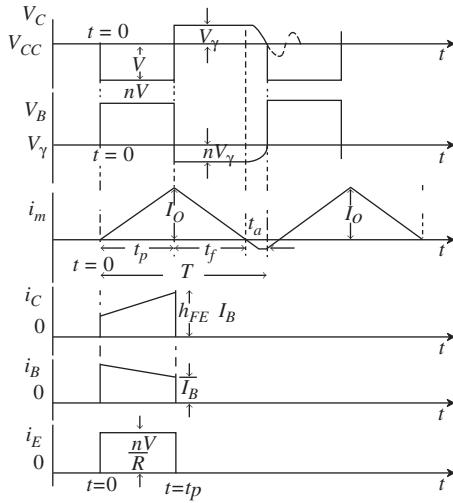


FIGURE 14.6 The waveforms of a diode-controlled astable blocking oscillator

At t_f , $i_m = 0$, from Eq. (14.33):

$$I_o = \frac{V_\gamma t_f}{L} \quad \text{or} \quad t_f = \frac{I_o L}{V_\gamma}$$

And from Eq. (14.32):

$$I_o = \frac{n}{n+1} \times \frac{V_{CC}}{R}$$

Therefore,

$$t_f = \frac{n}{n+1} \times \frac{V_{CC}}{V_r} \times \frac{L}{R} \quad (14.34)$$

After i_m is reduced to zero, the diode becomes an open circuit. This results in an under-damped ringing circuit shown in Fig. 14.5(b). Since the shunt capacitor is initially charged to V_r , a sinusoidal oscillation of amplitude V_r and time period $2\pi\sqrt{LC}$ begins (dashed curve). After one quarter of a cycle, that is, at the time $t_a = 2\pi\sqrt{LC}/4 = 1.57\sqrt{LC}$, V_C falls below V_{CC} . There results a negative swing at the collector and because of the polarity inversion, this appears as a positive swing at the base. When V_{BE} exceeds the cut-in voltage of the transistor Q , regeneration takes place again. Q again turns ON and the cycle repeats itself. Hence, without the need for any further external trigger, a new cycle starts. Thus, at the end of the pulse generated by the monostable circuit, the diode combination conducts and the capacitor charges to V_γ . Also, the LC (C is the distributed capacitance of the inductance, represented as a lumped capacitance) circuit oscillates when D is OFF, leading to the regeneration of the pulse and hence, sustained oscillations. As the diode combination causes the circuit to function in the astable mode, this astable multivibrator is called a diode-controlled circuit. The time period of oscillations is $T = t_p + t_f + t_a$. The collector and base voltages are nearly rectangular. The waveforms are plotted as shown in Fig. 14.6.

To understand the procedure to make the calculations and plot the waveforms let us consider Example 14.3.

E X A M P L E

Example 14.3: The astable blocking oscillator (diode-controlled) shown in Fig. 14.7 has the following parameters: $L = 5.2 \text{ mH}$, $C = 90 \text{ pF}$, $V_{CC} = 10 \text{ V}$, $R = 500 \Omega$, $V_r = 0.6 \text{ V}$, $n = 1$ and $V_{BB} = 0.5 \text{ V}$. Calculate (a) the period and the

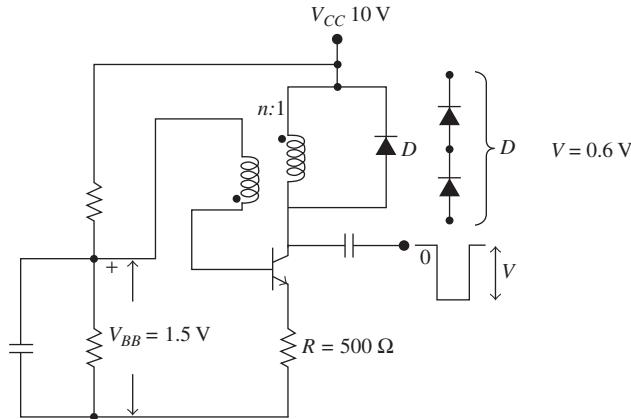


FIGURE 14.7 The diode-controlled astable blocking oscillator

duty cycle of the free oscillations; (b) the peak voltages and currents and (c) the current in the magnetizing inductance at the end of one cycle.

Solution: (a) Since $V_{BB} \ll V_{CC}$

$$t_p = \frac{nL}{R} = \frac{L}{R} = \frac{5.2 \times 10^{-3}}{0.5 \times 10^3} = 10.4 \mu s$$

$$\begin{aligned} t_f &= \frac{n}{n+1} \times \frac{L}{R} \times \frac{V_{CC}}{V_\gamma} \\ &= \frac{1}{1+1} \times 10.4 \mu s \times \frac{10}{0.6} = 87 \mu s \\ t_a &= 1.57\sqrt{LC} = 1.57 \times \left(5.2 \times 10^{-3} \times 90 \times 10^{-12} \right)^{1/2} = 1.07 \mu s \\ T &= t_p + t_f + t_a = 10.4 + 87 + 1.07 = 98.47 \mu s \end{aligned}$$

The duty cycle is defined as the ratio of t_p to T .

$$\text{Duty cycle} = \frac{10.4 \mu s}{98.47 \mu s} \times 100 = 10.56 \%$$

(b)

$$V = \frac{V_{CC}}{n+1} = \frac{10 \text{ V}}{1+1} = 5 \text{ V}$$

The collector voltage extends from:

$$V_{CC} - V = 10 - 5 = 5 \text{ V} \quad \text{to} \quad V_{CC} + V_\gamma = 10 + 0.6 = 10.6 \text{ V}$$

The base voltage extends from:

$$nV \text{ to } -nV_\gamma \text{ (i.e. } 5 \text{ V to } -0.6 \text{ V)}$$

The emitter current is constant and is given as:

$$i_E = \frac{nV}{R} = \frac{1 \times 5}{0.5 \times 10^3} = 10 \text{ mA}$$

The base current is maximum at $t = 0$ and is given as:

$$i_B(t=0) = \frac{nV_{CC}}{(n+1)^2 R} = \frac{1 \times 10}{4 \times 0.5 \times 10^3} = 5 \text{ mA}$$

The collector current is maximum at:

$$t = t_p = \frac{nL}{R} \quad \text{and} \quad i_C(t = t_p) = \frac{V_{CC}}{(n+1)^2} \left(\frac{n^2}{R} + \frac{t_p}{L} \right)$$

Therefore,

$$i_C = \frac{V_{CC}}{(n+1)^2} \left(\frac{n^2}{R} + \frac{n}{R} \right) = \frac{V_{CC}}{(n+1)^2} \times \frac{n}{R} (n+1) = \frac{V_{CC}}{R} \times \frac{n}{n+1} = \frac{10 \times 1}{0.5 \times 10^3 \times 2} = 10 \text{ mA}$$

The peak magnetizing current is:

$$I_o = \frac{nV_{CC}}{(n+1)R} = \frac{1}{2} \times \frac{10}{0.5 \times 10^3} = 10 \text{ mA}$$

(c) At $T = t_p + t_f$, the capacitor is charged to a voltage V_r and the magnetizing current is zero. The LC circuit then rings and in one quarter of a cycle (in time t_a) the capacitive energy is transformed to magnetic energy.

Since

$$\frac{LI_m^2}{2} = \frac{CV_\gamma^2}{2} \quad I_m^2 = \frac{C}{L} V_\gamma^2 \quad I_m = V_\gamma \sqrt{\frac{C}{L}}$$

Therefore,

$$I_m = 0.6 \sqrt{\frac{90 \times 10^{-12}}{5.2 \times 10^{-3}}} = 79 \mu\text{A}$$

The current i_m goes below zero by the amount I_m .

If we want a lower duty cycle (i.e., a pulse train rather than a typical square-wave output), we must increase t_f relative to t_p .

$$\begin{aligned} t_p &= \frac{nL}{R}, \quad t_f = \frac{n}{n+1} \times \frac{L}{R} \times \frac{V_{CC}}{V_\gamma} \\ \frac{t_p}{t_f} &= \frac{nL}{R} \times \frac{(n+1)RV_\gamma}{nLV_{CC}} = (n+1) \frac{V_\gamma}{V_{CC}} \end{aligned}$$

Hence, the duty cycle will be at minimum if in place of the diode combination, a single *p-n* Ge diode for which $V_\gamma \approx 0.1\text{V}$ is used. Then with $V_{CC} = 10\text{V}$, and $n = 1$,

$$\text{Duty cycle} \approx \frac{t_p}{t_f} = (n+1) \frac{V_\gamma}{V_{CC}} = 2 \times \frac{0.1}{10} = 0.02 = 2\%$$

Thus, t_p/t_f of 0.02 is possible.

If the duty cycle has to be large, in place of a diode, use a Zener diode with $V_Z = 3.8\text{V}$. Then the duty cycle is:

$$\text{Duty cycle} = \frac{t_p}{t_f} = (n+1) \frac{V_Z}{V_{CC}} = 2 \times \frac{3.8}{10} = 0.76 = 76\%.$$

14.3.2 RC-controlled Astable Blocking Oscillators

The circuit shown in Fig. 14.8(a) is an *RC*-controlled astable blocking oscillator. Here, the *RC* network, comprising R_1 and C_1 , is provided in the emitter circuit. V_{BB} now is a positive voltage.

The operation of the circuit can be explained as follows. Initially let Q be ON. Then the capacitor C_1 tries to charge to V_{CC} through the small dc resistance of the transformer winding in the collector lead and R , which is a relatively small resistance. The moment the voltage V_1 on C_1 is greater than $(V_{BB} - V_\gamma)$, as the base-emitter diode of Q gets reverse-biased, Q goes into the OFF state. Hence, the charge on C_1 discharges with a time constant $R_1 C_1$. Once again, when V_1 reaches $(V_{BB} - V_\gamma)$, there is a base current; as a result, there

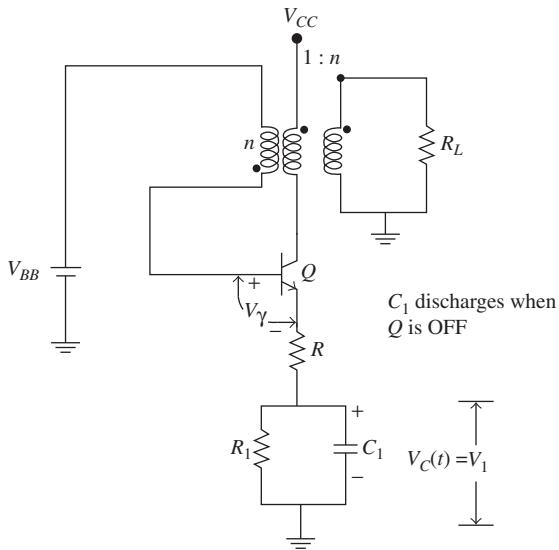


FIGURE 14.8(a) A RC -controlled astable blocking oscillator

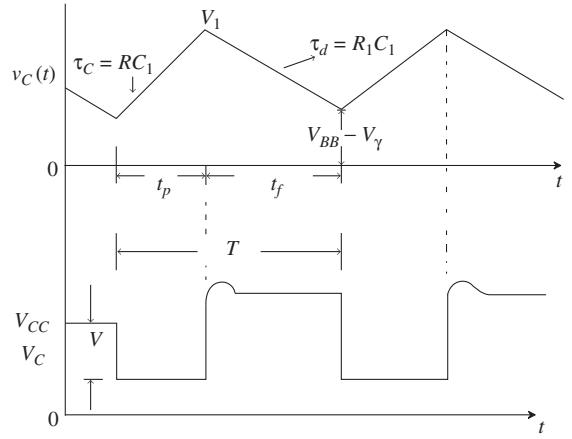


FIGURE 14.8(b) The waveforms of an RC -controlled astable blocking oscillator

is a collector current and the regenerative action takes place and Q once again switches into the ON state. This process is automatically repeated, resulting in an astable operation. As R_1 and C_1 control the timing operation, this astable circuit is called an RC -controlled astable blocking oscillator. The collector and base waveforms are similar to that of the monostable multivibrator with emitter timing as shown in Fig. 14.3(e).

During the pulse duration t_p , Q is ON and the capacitor is recharged and attains a voltage V_1 , which is larger than the voltage it had at the beginning of the pulse. Q now is OFF for a time period t_f , during which period C_1 discharges to the voltage $(V_{BB} - V_\gamma)$, at which instant Q again goes ON and the cycle repeats itself. The waveforms are shown in Fig. 14.8(b).

(i) Calculation of t_p :

Similar to the relation obtained earlier in the Eq. (14.30) we have for the circuit shown in Fig. 14.8(a):

$$\frac{t_p}{L} = \frac{n}{R} e^{-t_p/RC_1} - \frac{n_1^2}{R_L} \quad (14.35)$$

We can calculate t_p , using Eq. (14.35). If $t_p/RC_1 \ll 1$, expanding e^{-t_p/RC_1} as series and retaining only the 1st two terms:

$$e^{-t_p/RC_1} = 1 - \frac{t_p}{RC_1} + \frac{t_p^2}{2R^2C_1^2} - \dots$$

Substituting the 1st two terms of this expansion in Eq. (14.35):

$$\begin{aligned} t_p &= \frac{nL}{R} \left(1 - \frac{t_p}{RC_1} \right) - \frac{n_1^2 L}{R_L} & t_p \left(1 + \frac{nL}{R^2 C_1} \right) &= \frac{nL}{R} - \frac{n_1^2 L}{R_L} \\ t_p \left(1 + \frac{nL}{R^2 C_1} \right) &= \frac{n}{R} - \frac{n_1^2}{R_L} \end{aligned} \quad (14.36)$$

For a very large C_1 , $\frac{nL}{R^2 C_1} \ll 1$. Hence, Eq. (14.36) reduces to:

$$\frac{t_p}{L} = \frac{n}{R} - \frac{n^2}{R_L} \quad (14.37)$$

This gives the pulse width of the monostable blocking oscillator.

(ii) Calculation of t_f :

We have $v_C(t) = v_f - (v_f - v_i)e^{-t/\tau}$. From Fig. 14.8(b), we have $v_i = V_1$ and $v_f = 0$. Thus,

$$v_C(t) = V_1 e^{-t/R_1 C_1}$$

At

$$t = t_f, \quad v_C(t_f) = V_{BB} - V_\gamma$$

$$V_{BB} - V_\gamma = V_1 e^{-t_f/R_1 C_1}$$

$$t_f = R_1 C_1 \ln \frac{V_1}{V_{BB} - V_\gamma} \quad (14.38)$$

To calculate t_f , we need to know V_1 , the maximum voltage on C when Q is ON. The amplitude of the trigger V is calculated using the circuit in Fig. 14.8(c):

From Fig. 14.8(c):

$$V_{CC} = V + nV + V_{BB}$$

Therefore,

$$V(n+1) = V_{CC} - V_{BB}$$

The amplitude of the trigger is:

$$V = \frac{V_{CC} - V_{BB}}{(n+1)} \quad (14.39)$$

To get V_1 during charging, from the waveforms shown in Fig. 14.8(b):

$$v_C(t) = v_f - (v_f - v_i)e^{-t/\tau}$$

$$v_f = nV + V_{BB} \text{ and } v_i = V_{BB} - V_\gamma$$

$$v_C(t) = nV + V_{BB} - (nV + V_{BB} - V_{BB} + V_\gamma)e^{-t/R_1 C_1}$$

At

$$t = t_p, \quad v_C(t) = V_1$$

$$V_1 = nV + V_{BB} - (nV + V_\gamma)e^{-t_p/R_1 C_1}$$

Substituting Eq. (14.39)

$$V_1 = \frac{n(V_{CC} - V_{BB})}{n+1} + V_{BB} - \left[\frac{n(V_{CC} - V_{BB})}{n+1} + V_\gamma \right] e^{-t_p/R_1 C_1}$$

$$V_1(n+1) = n(V_{CC} - V_{BB}) + (n+1)V_{BB} - [n(V_{CC} - V_{BB})] e^{-t_p/R_1 C_1}$$

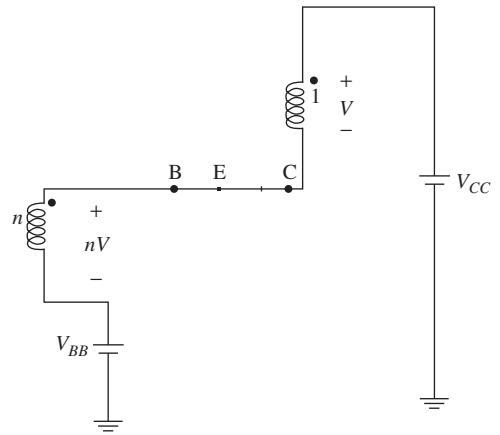


FIGURE 14.8(c) The circuit to calculate V

since V_γ is small. This equation is simplified as:

$$(n + 1)V_1 = nV_{CC} + V_{BB} - n(V_{CC} - V_{BB})e^{-t_p/RC_1} \quad (14.40)$$

To calculate the value of V_1 , we first calculate t_p , and then use that value of t_p in Eq. (14.40) to calculate V_1 . Having calculated V_1 , substitute this value of V_1 in Eq. (14.38) to calculate t_f . The time period of the oscillation, $T = (t_p + t_f)$ and the frequency of oscillations is the reciprocal T .

EXAMPLE

Example 14.4: For the RC -controlled astable blocking oscillator shown in Fig. 14.8(a) following are the parameters: $V_{CC} = 15 \text{ V}$, $n = n_1 = 1$, $V_{BB} = 2 \text{ V}$, $R = 100 \Omega$, $R_1 = 1000 \Omega$, $R_L = 1000 \Omega$, $C_1 = 0.01 \mu\text{F}$, $L = 5 \text{ mH}$.

(a) Calculate the amplitude of the trigger; (b) t_p , the pulse duration; (c) V_1 , the maximum voltage to which C_1 charges; (d) t_f , the discharge period of C ; (e) T , the time period of the astable multivibrator and its frequency of oscillations and (f) the duty cycle.

Solution:

(a) We have from Eq. (14.39):

$$V = \frac{V_{CC} - V_{BB}}{(n + 1)} = \frac{15 - 2}{(1 + 1)} = 6.5 \text{ V}$$

(b) From Eq. (14.37):

$$t_p = \frac{nL}{R} - \frac{n_1^2 L}{R_L} = \frac{1 \times 5 \times 10^{-3}}{0.1 \times 10^3} - \frac{1 \times 5 \times 10^{-3}}{1 \times 10^3} = 50 - 5 = 45 \mu\text{s}$$

(c) From Eq. (14.40):

$$(n + 1)V_1 = nV_{CC} + V_{BB} - n(V_{CC} - V_{BB})e^{-t_p/RC_1}$$

$$(1 + 1)V_1 = 1 \times 15 + 2 - 1(15 - 2)e^{\frac{-45 \times 10^{-6}}{0.1 \times 10^3 \times 0.01 \times 10^{-6}}}$$

$$2V_1 = 17 - 13 \times 0 = 17, \quad V_1 = 8.5 \text{ V}$$

(d) t_f is given by Eq. (14.38) as:

$$t_f = R_1 C_1 \ln \frac{V_1}{V_{BB} - V_\gamma} = 1 \times 10^3 \times 0.01 \times 10^{-6} \ln \frac{8.5}{2 - 0.5} = 17.35 \mu\text{s}$$

(e) $T = t_p + t_f = 45 + 17.35 = 62.35 \mu\text{s}$

$$f = \frac{1}{T} = \frac{1}{62.35 \times 10^{-6}} = \frac{1000 \times 10^3}{62.5} = 16 \text{ kHz}$$

(f) Duty cycle = $\frac{t_p}{T} = \frac{45}{62.5} \times 100 = 72.1\%$

14.3.3 Effect of Core Saturation on Pulse Width

So far the pulse width was calculated based on the assumption that magnetizing core is not saturated. Let V = Voltage across the primary

n = Number of turns on the primary

A = Area of cross section of the core

ϕ = Magnetic flux

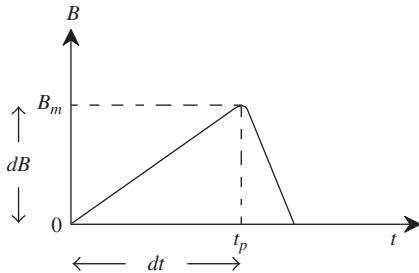


FIGURE 14.9(a) The variation of flux density with time

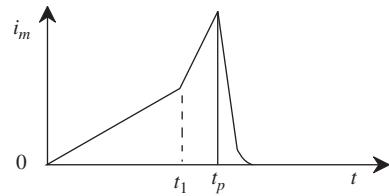


FIGURE 14.9(b) The variation of the magnetizing current with time

$$\frac{d\phi}{dt} = \text{Rate of change of flux linkages}$$

From Faraday's law of electromagnetic induction, the voltage induced in the primary winding is proportional to the rate of change of flux linkages.

$$V \propto \frac{d\phi}{dt}$$

If there are n turns in the primary then;

$$V = n \frac{d\phi}{dt} \quad (14.41)$$

If B is the flux density then

$$B = \frac{\phi}{A} \quad (14.42)$$

If there is a change in ϕ , B also changes incrementally. Therefore, from Eq. (14.42) we get:

$$d\phi = A \times dB \quad (14.43)$$

Putting Eq. (14.43) in Eq. (14.41) we get:

$$V = nA \frac{dB}{dt} \quad (14.44)$$

Figure 14.9(a) shows the variation of flux density as a function of time.

From Fig. 14.9(a), $dt = t_p$ and $dB = B_m$.

Therefore, Eq. (14.44) is written as:

$$V = nA \frac{B_m}{t_p} \quad (14.45)$$

We know that:

$$V = L \frac{di_m}{dt}$$

Therefore,

$$di_m = \frac{V}{L} dt \quad (14.46)$$

If we assume that the core losses are zero and the magnetizing core gets saturated, the magnetizing current i_m becomes large. For $0 \leq t \leq t_1$, i_m and i_C vary linearly as a function of time. During t_1 to t_p from Eq. (14.46), i_m and i_C increase rapidly, as shown in Figs. 14.9(b) and (c).

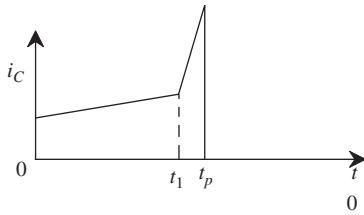


FIGURE 14.9(c) The variation of the collector current with time

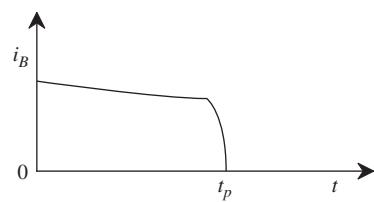


FIGURE 14.9(d) The variation of the base current with time

At $t = t_p$, i_C is equal to $h_{FE} i_B$. As a result, the device quickly switches into the OFF state and the pulse gets terminated, as shown in Fig. 14.9(d). From Eqs. (14.13) and (14.44), we have:

$$V = \frac{V_{CC}}{n+1} = nA \frac{dB}{dt}$$

Therefore,

$$\frac{V_{CC}}{n+1} = nA \frac{dB}{dt}$$

Let the flux density be increased from 0 to the maximum value (B_m) in the interval t_p then:

$$\frac{V_{CC}}{n+1} = nA \frac{B_m}{t_p}$$

Therefore,

$$t_p = nA \frac{B_m(n+1)}{V_{CC}} \quad (14.47)$$

It can be observed from Eq. (14.47) that the pulse width (t_p) is independent of the transistor parameter h_{FE} , which is temperature dependent. It depends only on V_{CC} and the parameters of the core. Thus, the pulse can be stable.

The initial value of the flux density depends on the magnetic properties of the core. The hysteresis curve of the core is shown in Fig. 14.10. Let us now try to calculate the pulse width using the entire hysteresis curve. At $t = 0$, there is no current in the winding, the core flux density $B = -B_m$. When the blocking oscillator is triggered, as H increases, B also increases from $-B_m$ to $+B_m$ till $H = H_C$. At $H = H_C$ the core gets saturated and the pulse ends. t_p can be thus calculated by substituting $B = 2B_m$ in Eq. (14.47).

Therefore,

$$t_p = 2nA \frac{B_m(n+1)}{V_{CC}} \quad (14.48)$$

As the core gets saturated, B the flux density remains at B_m . Subsequently, the rate of change of the flux density is zero, i.e., $dB/dt = 0$. So no voltages are induced in the transformer and regeneration is not possible. To trigger the oscillator after the pulse ends, it should be ensured that the flux density is reset to $-B_m$. This resetting to $-B_m$ can be accomplished by passing a current through an auxiliary winding with R_a connected in series, as shown in Fig. 14.11.

When the transistor is turned OFF, the current V_{CC}/R_a in the auxiliary winding supplies the necessary opposite ampere turns, so that H becomes more negative than $-H_C$ and hence, $B = -B_m$ and the oscillator comes back to the normal condition.

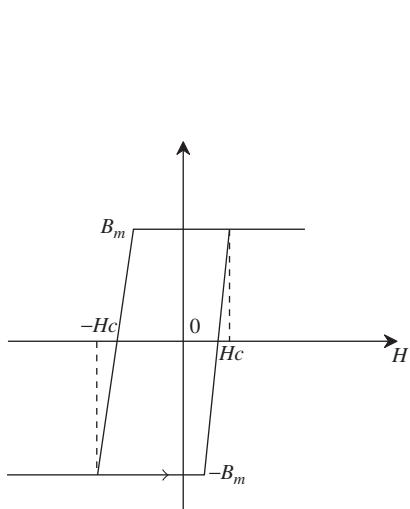


FIGURE 14.10 The hysteresis curve

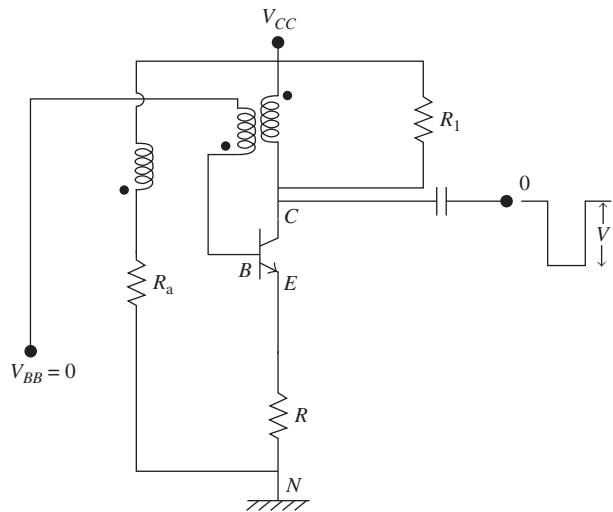


FIGURE 14.11 The resetting of the flux density

14.3.4 Applications of Blocking Oscillators

1. As a transformer is used as a coupling element for regeneration, the monostable blocking oscillator can be used to derive both positive and negative pulses by using a centre-tapped auxiliary winding. The pulses so derived may, if need be, be used to trigger other circuits.
2. When used in the astable mode, square waves with varying duty cycles can be derived using a blocking oscillator. In fact, the duty cycle can be very small. The smaller duty cycle means sharp pulses.
3. Unlike conventional multivibrators, blocking oscillators use a transformer. Thus, they can generate pulses with large peak power, i.e., pulses may have a large amplitude and the associated current can also be large. However, in cases where the duty cycle is small, the average power is small.
4. As blocking oscillators can generate pulses with small mark duration and varying repetitive frequencies, these circuits can be used in pulse synchronization where there is a need to synchronize the outputs of a number of generators (see Chapter 15 for a complete discussion).
5. Blocking oscillators find applications in frequency dividers and counters, discussed in detail in Chapter 15.

S O L V E D P R O B L E M S

Example 14.5: Calculate the pulse amplitude and the width for the triggered blocking oscillator shown in Fig. 14.12(a). Si transistor uses $h_{FE} = 50$, $V_{BE(\text{sat})} = 0.7$ V, $V_{CE(\text{sat})} = 0.2$ V, magnetizing inductance of the collector winding L is 5 mH, $V_{BB} = -2$ V, $V_{CC} = 10$ V, $R = 1.5$ k Ω .

Solution:

From the circuit in Fig. 14.12(b),

$$i_C = 2i_B + i_m$$

$$i_E = i_C + i_B = 2i_B + i_m + i_B = 3i_B + i_m$$

Writing for the voltage at node E:

$$10 - V - 0.2 = -2 + 2V - 0.7$$

$$3V = 10 + 2 + 0.7 - 0.2$$

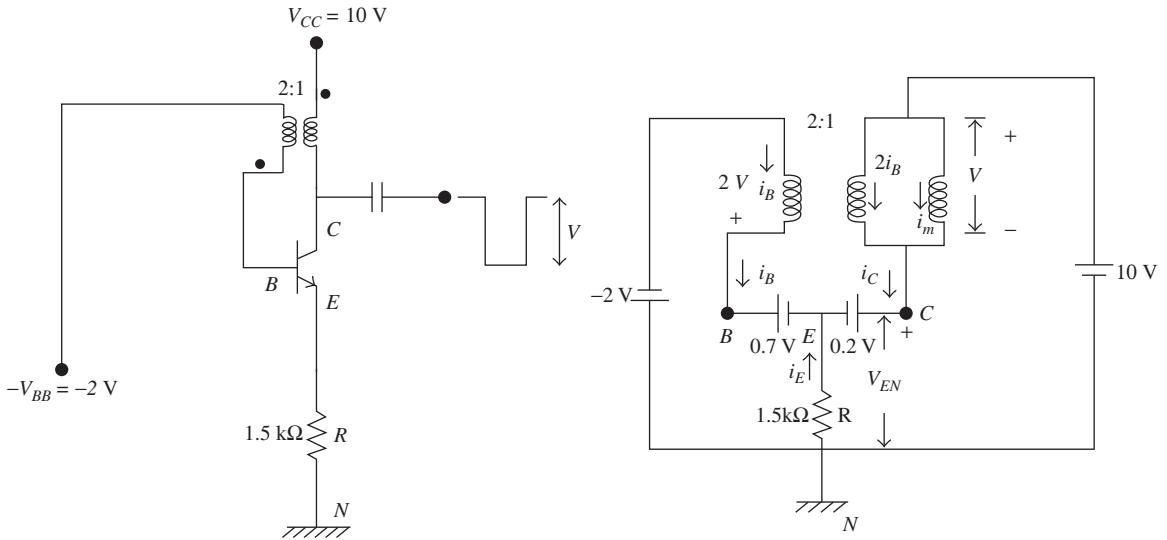


FIGURE 14.12(a) The triggered blocking oscillator

FIGURE 14.12(b) The equivalent circuit of Fig. 14.12(a) when core saturates

$$V = \frac{12.5}{3} = 4.16 \text{ V}$$

$$i_m = \frac{Vt}{L} = \frac{4.16t}{0.005} = 832t \text{ A}$$

$$\begin{aligned} i_E &= 3i_B + i_m = \frac{V_{EN}}{1.5 \text{ k}\Omega} = \frac{2V - 2 - 0.7}{1.5 \text{ k}\Omega} \\ &= \frac{2 \times 4.16 - 2 - 0.7}{1.5 \text{ k}\Omega} = 0.0037 \text{ A} \end{aligned}$$

$$i_B = \frac{0.0037 - 832t}{3} = 0.0012 - 277.3t$$

$$i_C = 2i_B + i_m = 0.0024 - 554.6t + 832t = 0.0024 + 277.4t$$

At $t = t_p$

$$i_C = h_{FE}i_B$$

$$0.0024 + 277.4t_p = 50(0.0012 - 277.3t_p)$$

$$0.0024 + 277.4t_p = 0.06 - 13865t_p$$

$$14142.4t_p = 0.0576$$

$$t_p = \frac{0.0576}{14142.4} = 4.07 \mu\text{s}$$

Example 14.6: For the RC -controlled astable blocking oscillator shown in Fig. 14.8(a), $V_{CC} = 18 \text{ V}$, $n = n_1 = 1$, $V_{BB} = 1.5 \text{ V}$, $R = 100 \Omega$, $R_1 = 1000 \Omega$, $R_L = \infty$, $C_1 = 0.01 \mu\text{F}$, $L = 3 \text{ mH}$. (a) Calculate the amplitude of the trigger; (b) t_p , the pulse duration; (c) V_1 , the maximum voltage to which C_1 charges; (d) t_f , the discharge period of C ; (e) T , the time period of the astable multivibrator and its frequency of oscillations and (f) the duty cycle.

Solution:

(a) We have from Eq. (14.39)

$$V = \frac{V_{CC} - V_{BB}}{(n + 1)} = \frac{18 - 1.5}{(1 + 1)} = 8.25 \text{ V}$$

(b) From Eq. (14.37)

$$t_p = \frac{nL}{R} = \frac{1 \times 3 \times 10^{-3}}{0.1 \times 10^3} = 30 \mu\text{s}$$

(c) From Eq. (14.40)

$$(n + 1)V_1 = nV_{CC} + V_{BB} - n(V_{CC} - V_{BB})e^{-t_p/RC_1}$$

$$(1 + 1)V_1 = 1 \times 18 + 1.5 - 1(18 - 1.5)e^{\frac{-30 \times 10^{-6}}{0.1 \times 10^3 \times 0.01 \times 10^{-6}}}$$

$$2V_1 = 19.5 - 16.5 \times 0 \quad 2V_1 = 19.5 \quad V_1 = 9.75 \text{ V}$$

(d) t_f is given by Eq. (14.38) as

$$t_f = R_1 C_1 \ln \frac{V_1}{V_{BB} - V_r} = 1 \times 10^3 \times 0.01 \times 10^{-6} \ln \frac{9.75}{1.5 - 0.5} = 22.77 \mu\text{s}$$

(e) $T = t_p + t_f = 30 + 22.77 = 52.77 \mu\text{s}$

$$f = \frac{1}{T} = \frac{1}{52.77 \times 10^{-6}} = \frac{1000 \times 10^3}{52.77} = 18.95 \text{ kHz}$$

(f) Duty cycle = $\frac{t_p}{T} = \frac{30}{52.77} \times 100 = 56.85\%$

SUMMARY

- (1) Blocking oscillators are regenerative circuits that use a pulse transformer and can be operated either in an astable or a monostable mode.
- (2) The main advantage of a blocking oscillator is that it can generate pulses of peak power.
- (3) In a monostable blocking oscillator using base timing, the disadvantage is that the pulse duration is dependent on h_{FE} of the transistor. As h_{FE} varies with temperature, its pulse width can not be stable.
- (4) A monostable blocking oscillator with emitter timing generates a pulse whose width is independent of h_{FE} . Hence, the duration of the pulse is stable.
- (5) In a diode-controlled astable blocking oscillator, the diode is responsible for regeneration and it is possible to vary the duty cycle by proper choice of the diode.
- (6) An RC -controlled astable blocking oscillator can give lower duty cycles.
- (7) Saturation of the magnetic circuit of the transformer influences the pulse width of a blocking oscillator.

MULTIPLE CHOICE QUESTIONS

- 1) The type of feedback that is employed in a blocking oscillator is:
 - (a) Regenerative feedback
 - (b) Degenerative feedback
 - (c) No feedback
 - (d) None of the above
- 2) The main advantage of a blocking oscillator is that it can generate a pulse of:
 - (a) High peak power
 - (b) Low output voltage
 - (c) Low peak power
 - (d) None of the above
- 3) In a blocking oscillator, on the application of a trigger, if the circuit generates a single pulse, it is called:
 - (a) Astable blocking oscillator
 - (b) Monostable blocking oscillator
 - (c) Bistable blocking oscillator
 - (d) Free-running blocking oscillator
- 4) In a blocking oscillator, on the application of a trigger, if the circuit generates a square wave, it is called:
 - (a) Monostable blocking oscillator
 - (b) Free-running blocking oscillator
 - (c) Flip-flop
 - (d) Counter
- 5) In a monostable blocking oscillator with base timing, the main disadvantage is that:
 - (a) T varies with the variation of h_{FE}
 - (b) T remains unchanged with the variation of h_{FE}
 - (c) T is inversely proportional to h_{FE}
 - (d) None of the above
- 6) The improvement in a monostable blocking oscillator with emitter timing when compared to the circuit that employs base timing is:
 - (a) T is independent of h_{FE}
 - (b) T is proportional to h_{FE}
 - (c) T is inversely proportional to h_{FE}
 - (d) T depends only on transistor parameters
- 7) The duty cycle in an astable blocking oscillator employing diode control can be varied by the choice of:
 - (a) Diode forward voltage
 - (b) Diode reverse voltage
 - (c) Turns ratio of the pulse transformer
 - (d) Magnetic circuit
- 8) An astable blocking oscillator can be used as a:
 - (a) Frequency divider and counter
 - (b) Time-base generator
 - (c) Sampling gate
 - (d) Logic gate

SHORT ANSWER QUESTIONS

1. Explain the principle of working of a blocking oscillator.
2. Name the two types of monostable blocking oscillators and discuss their relative performance.
3. Explain the principle of operation of an astable blocking oscillator with a diode control.
4. Compare the performance of a diode-controlled astable blocking oscillator with an RC -controlled astable blocking oscillator.

LONG ANSWER QUESTIONS

1. Draw the circuit of a monostable blocking oscillator with base timing and explain its operation. Calculate its pulse width. Draw the waveforms.
2. Explain with the help of a neat circuit diagram the working of a monostable blocking oscillator with emitter timing and obtain the expression for its pulse width. Plot the waveforms.
3. Draw the circuit of an astable blocking oscillator with a diode control and explain its operation. Plot the waveforms. Derive the expression for its frequency.
4. With the help of a neat circuit diagram and waveforms explain the working of an astable blocking oscillator with RC control. Obtain the expression for its frequency of oscillations.

UNSOLVED PROBLEMS

- For the monostable blocking oscillator in Fig. 14.1(a), following are the parameters: $V_{CC} = 15 \text{ V}$, $R = 0.5 \text{ k}\Omega$, $L = 3 \text{ mH}$, $h_{FE} = 20$ and $n = 1$.
(a) Calculate and plot the base current and collector current waveforms and calculate the pulse width. (b) If due to temperature variation, h_{FE} increases to 30, then calculate the pulse width.
 - For the blocking oscillator with emitter timing shown in Fig. 14.3(a), it is given that $n = 1$, $n_1 = 1$, $L = 3 \text{ mH}$, $R = 0.5 \text{ k}\Omega$, $h_{FE} = 20$ and $V_{CC} = 15 \text{ V}$. Calculate (a) the amplitude of the trigger; (b) the value of R_L that allows pulse formation; (c) pulse width with $h_{FE} = 20$ and also calculate t_p using the approximate relation; (d) the base, collector and emitter currents and (e) plot the current waveforms.
 - For the diode-controlled astable blocking oscillator shown in Fig. 14.4(a), $L = 3 \text{ mH}$, $C = 100 \text{ pF}$,
- $V_{CC} = 15 \text{ V}$, $R = 500 \Omega$, $V_Y = 4.4 \text{ V}$, $n = 1$ and $V_{BB} = 0.7 \text{ V}$, $R_L = \infty$.
- Calculate the amplitude of the trigger pulse; (b) time period of the oscillations and the frequency, and (c) the duty cycle.
- For the RC -controlled astable blocking oscillator shown in Fig. 14.8(a), following are the parameters: $V_{CC} = 20 \text{ V}$, $n = n_1 = 1$, $V_{BB} = 3 \text{ V}$, $R = 100 \Omega$, $R_1 = 1000 \Omega$, $R_L = 1000 \Omega$, $C_1 = 0.01 \mu\text{F}$, $L = 2 \text{ mH}$.
- Calculate the amplitude of the trigger; (b) t_p , the pulse duration; (c) V_1 , the maximum voltage to which C_1 charges; (d) t_f , the discharge period of C ; (e) T , the time period of the astable multivibrator and its frequency of oscillations and finally (f) the duty cycle.

CHAPTER 15

Synchronization and Frequency Division

LEARNING OBJECTIVES

After reading this chapter, you will be able to:

- Understand the principle of frequency synchronization and division using the UJT relaxation circuit
 - Describe the methods to achieve frequency synchronization and division in other relaxation circuits like astable and monostable multivibrators
 - Realize the circuit that eliminates jitter in a relaxation divider
 - Understand the principle of operation of the circuits that achieve frequency synchronization and division using symmetric circuits
-

15.1 INTRODUCTION

Many types of waveform generators (sinusoidal generators, square-wave generators, sweep generators, etc) are used in pulse and digital circuits. These different waveform generators may have the same frequency. In many applications, these generators are required to run in synchronism or in step with another—which means that they should arrive at some reference point in their cycle at the same time. Alternately, it is also possible that these waveform generators may operate at different frequencies. Also, it is possible that one generator completes one cycle, whereas the other may complete an integral number of cycles ($2, 3, \dots, n$) in the same time period. Still, it becomes necessary that these generators should run in synchronism, that is, they should arrive at some reference point in their cycles at the same time instant. Then these generators are again said to be running in synchronism, though with frequency division. In this chapter, we will discuss the methods of frequency synchronization and division using pulses and symmetric signals (sinusoidal signals) as synchronizing (sync) signals.

First, we consider the synchronization of relaxation circuits like sweep generators and multivibrators with pulses as synchronizing signals. Synchronization is possible only when the pulse amplitude is reasonably large and the repetitive frequency of the sync signal is greater than or equal to the frequency of the relaxation circuit. Also the synchronization with the division can only be achieved under certain conditions. However, when it comes to symmetric signals as sync signals, synchronization is always possible, may be with division. The various conditions under which synchronization takes place are discussed in detail.

15.2 PULSE SYNCHRONIZATION OF RELAXATION DEVICES

We are going to consider synchronization of the output of a UJT sweep generator using a pulse train. Consider a circuit where a capacitor charges during a finite time interval and the sweep is terminated abruptly by the discharge (relaxation) of the condenser. Such a circuit is called a relaxation circuit. Some relaxation circuits that we have already considered include sweep generators, blocking oscillators and multivibrators. Let us consider a UJT relaxation oscillator shown in Fig. 15.1(a).

Here, the UJT is simply used as a switch. Initially, let the capacitor be uncharged. When the switch is open the capacitor tries to charge to V_{BB} . The moment the voltage across C reaches V_P (peak voltage or the breakdown voltage of the UJT), the switch closes, allowing the charge on the capacitor C to discharge almost

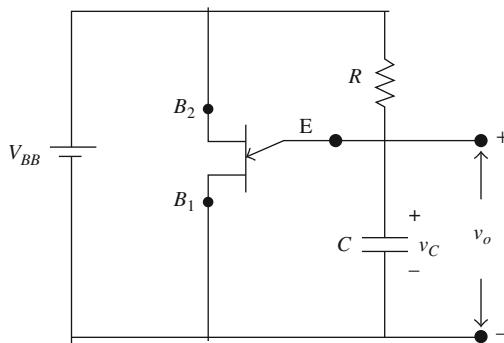


FIGURE 15.1(a) The UJT relaxation oscillator

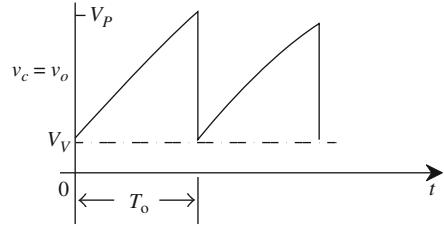


FIGURE 15.1(b) The output waveform

instantaneously. Again, when the voltage across C reaches V_V (valley voltage of the UJT), the switch opens, once again the capacitor charges. This process is repeated, resulting in a waveform as shown in Fig. 15.1(b).

It is now required to synchronize the output of this relaxation oscillator with an external signal, called the sync signal. This sync signal, which is essentially a negative pulse train, is connected to the UJT circuit such that it changes its peak voltage V_P . Thus, in a UJT circuit, the sync signal (negative pulses) is applied at B_2 to lower V_P , as shown in Fig. 15.2. The resistances R_{B1} and R_{B2} are added in series with B_1 and B_2 respectively.

Let us try to visualize the situation when the synchronizing pulses are applied. As already mentioned, the effect of the sync pulses is to lower the peak or breakdown voltage of the UJT. A repetitive pulse train, having a certain amplitude is shown in Fig. 15.3(a), starting at $t = 0$. For the first few cycles the sweep generator runs at its natural frequency $f_o (= 1/T_o)$ with $V_p = V_o$ as its amplitude. The sweep signal and the pulse train run at different frequencies and no synchronization is established. At time $t = T$, the negative pulse reduces the peak of the natural sweep and the relaxation device switches ON, thereby terminating the sweep prematurely. This results in a new sweep time of T_s , which is the same as the spacing between the successive sync pulses, T_p and has the amplitude V_s which is smaller than V_o . From now onwards, the sweep generator output and the pulse train run in synchronism, as shown in Fig. 15.3(a).

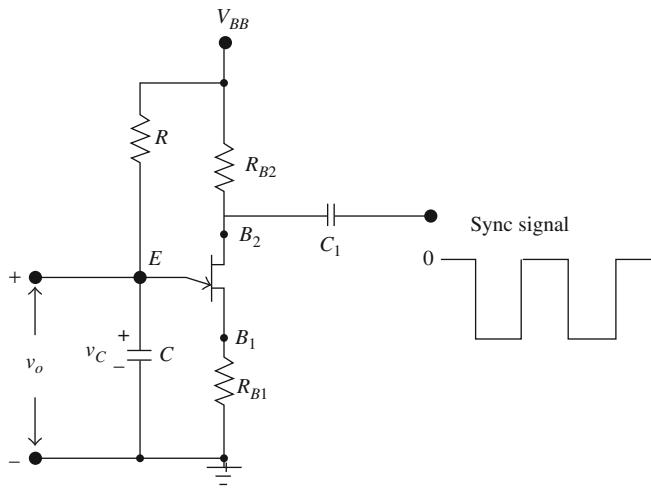


FIGURE 15.2 The synchronization of a relaxation device with external pulses

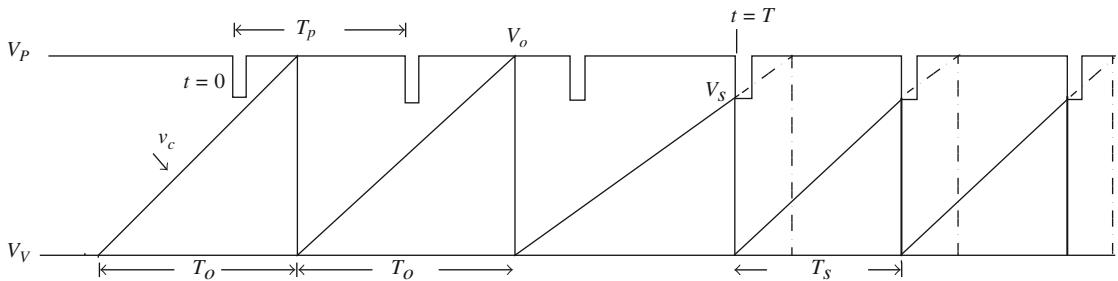


FIGURE 15.3(a) The synchronization takes place after a few cycles

Thus, initially the two generators are not synchronized. However, the unsynchronized generators run in synchronism after a few cycles (from $t = T$ onwards). The synchronization takes place only when the sync pulses occur at the time when they would terminate the sweep cycle prematurely. This means that for synchronization to be possible, the interval between the pulses, T_p must be less than the sweep duration T_o . Once synchronization takes place the sweep duration changes to T_s and the sweep amplitude to V_s . Now consider a case where $T_p > T_o$, as shown in Fig. 15.3 (b).

Here, $T_p > T_o$ and sync pulses occur at such instants of time that they will not be able to prematurely terminate the sweep cycle. Hence, no synchronization is possible between these two waveform generators. Obviously, synchronization cannot take place if T_p is greater than T_o . Let us consider another situation where $T_p < T_o$, but the amplitude of the sync pulses is small, as shown in Fig. 15.3(c).

It is said that synchronization is possible when $T_p < T_o$. However, in the present case, as the amplitude of the sync pulses is small, they will not be able to prematurely terminate the sweep cycle. Hence, here again, no synchronization is possible. Thus, it may be inferred from this discussion that for synchronization to take place: (a) T_p must be less than or equal to T_o , and (b) the amplitude of the sync pulses should be large enough to bridge the gap between the quiescent breakdown voltage V_p and the sweep voltage v_c .

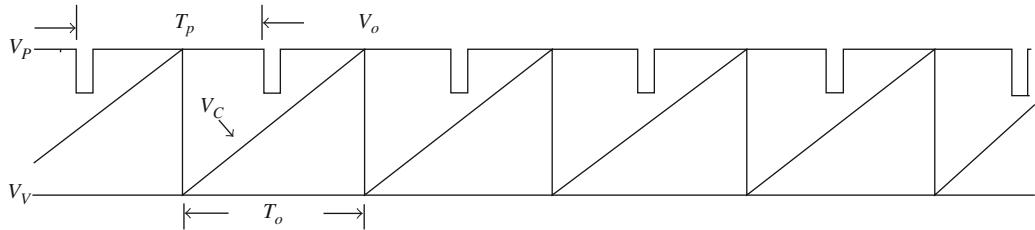


FIGURE 15.3(b) There is no synchronization for $T_p > T_o$

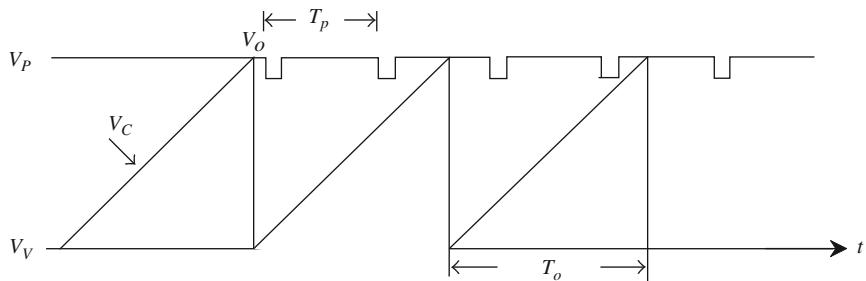


FIGURE 15.3(c) No synchronization is possible if the amplitude of the sync pulses is small

15.2.1 Frequency Division in a Sweep Circuit

Consider Fig. 15.4(a) in which $T_p < T_o$. We see that the first two pulses (marked 2 and 1) do not have sufficient amplitude so as to lower V_p and terminate the sweep cycle. Hence, there is no synchronization. However, the third pulse marked 2 though has the same amplitude as pulses marked 1, but occurs at such a time instant so as to be able to prematurely terminate the sweep cycle. The next sweep is initiated at this instant. However, the next pulse once again marked 1 may still have the same amplitude as the rest of the pulses, but will not be able to terminate the sweep. Once again the next pulse marked 2 occurs at such an instant that its amplitude may still be sufficient enough to prematurely terminate the sweep. Thus, we see that only pulses marked 2 will be able to terminate sweep cycle and not the pulses marked 1. For every two sync pulses there is one sweep cycle and these two generators are seen to be running in synchronization. The sweep generator is now called a divider—the division being by a factor 2. There is one sweep cycle for every two sync pulses, i.e., $T_s/T_p = 2$, because $T_s = 2T_p$, where T_s is the sweep duration after synchronization and T_p is the spacing between the sync pulses.

Consider Fig. 15.4(b) where pulses marked 1 and 2 are not large enough to terminate the sweep cycle prematurely. Only when the amplitude of the pulse 1 is as large as V_1 and that for pulse 2, it is V'_1 they will be able to terminate the cycle prematurely to effect synchronization. However, pulses marked 3, though have the same amplitude, occur at such instants that they will be able to effect synchronization. Hence, for every three sync pulses the sweep generator completes one cycle. Therefore, the two generators are said to be synchronized with the frequency division being by a factor 3.

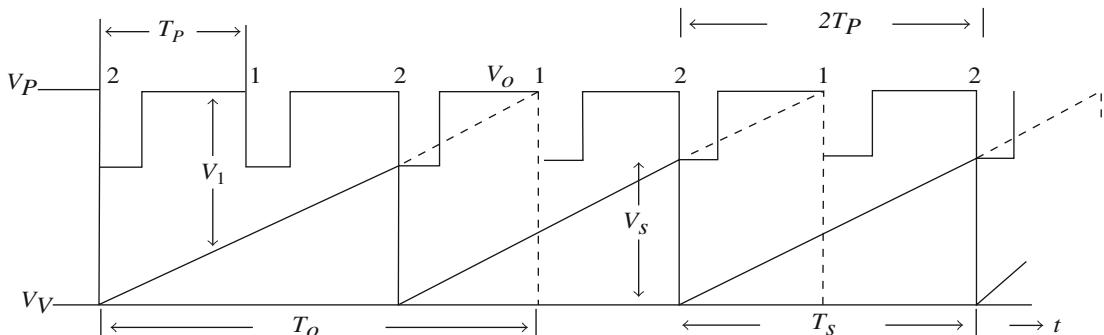


FIGURE 15.4(a) Frequency division by 2

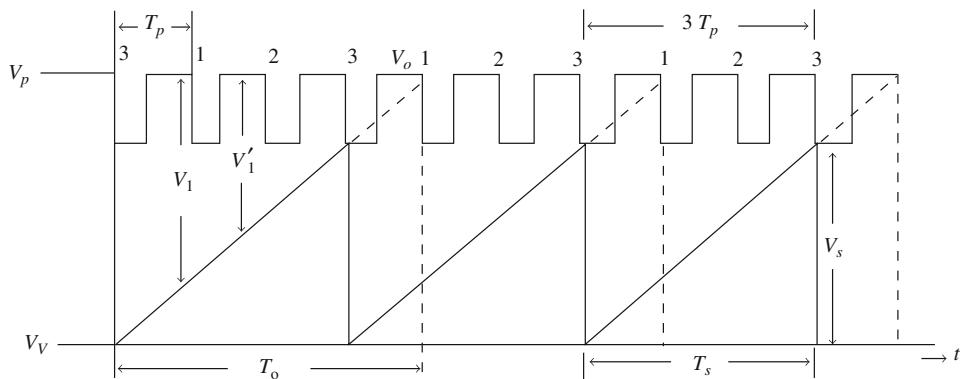


FIGURE 15.4(b) Frequency division by 3 in a sweep generator

We can infer from the previous conditions that:

- (i) No synchronization is possible for pulses of smaller amplitude.
- (ii) For a pulse amplitude large enough to prematurely terminate the sweep cycle, as T_p/T_s progressively decreases from 1 to 0, 1:1 synchronization holds, followed by 2:1 synchronization and then 3:1 synchronization and so on. T_s/T_p is called the counting ratio.
- (iii) For a pulse amplitude that is very large, synchronization is always possible. As T_p/T_s decreases from 1 to 0, the division, however, changes from 1:1 to 2:1 to 3:1 and so on.

15.3 SYNCHRONIZATION OF OTHER RELAXATION CIRCUITS

Frequency synchronization and division is also possible using other relaxation circuits such as astable multivibrators and monostable multivibrators. We will consider the blocking oscillator circuits and conventional astable and monostable multivibrators.

15.3.1 Synchronization of Astable Blocking Oscillators

Synchronization of the output of an astable blocking oscillator with frequency division by a factor of 5 using positive sync pulses is illustrated in Fig. 15.5(a). Q_2 acts as an inverter. The positive sync pulses that appear at the base of Q_2 , after amplification and polarity inversion by the CE configuration, appear as negative pulses at the collectors of Q_1 and Q_2 . Because of the polarity inversion by the pulse transformer, these negative pulses appear as positive pulses at the base Q_1 as per the chosen dot convention on the windings. Consequently, the base current of Q_1 increases, its collector current further rises, the voltage at the collector falls still further, the voltage at the base increases further and so on. A regenerative action takes place, the transistor Q_1 is quickly driven into saturation, and a pulse of duration t_p is generated. During this period of pulse generation, the capacitor C_1 charges, the voltage across the capacitor at $t = t_p$ being V_1 , as shown in Fig. 15.5(b). As this voltage reverse-biases the base – emitter diode of Q_1 , Q_1 now goes into the OFF state. As a result, the charge on C_1 discharges through R_1 and when the voltage across the capacitor terminals falls to $V_{BB} - V_\gamma$, then Q_1 is again ON and C_1 charges and this process is repeated. In the absence of sync pulses, a new sweep would have started at the voltage $(V_{BB} - V_\gamma)$, at which voltage Q_2 would have normally gone into the ON state. The output would have a time period T_o , as shown in Fig. 15.5(b).

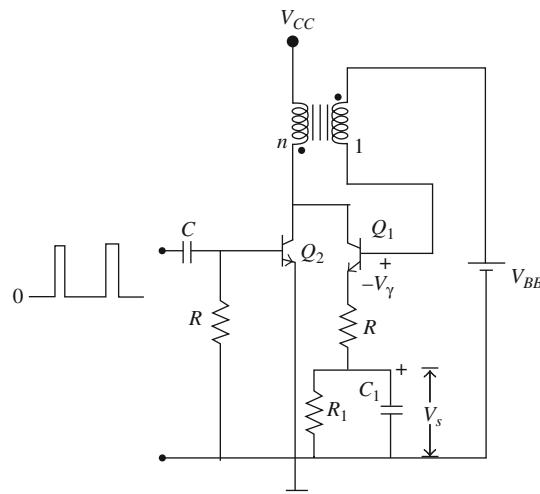


FIGURE 15.5(a) The sync signal applied to an astable blocking oscillator

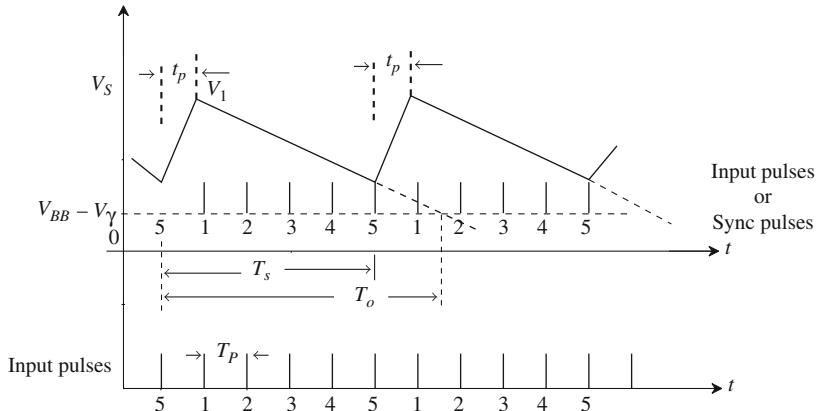


FIGURE 15.5(b) 5:1 synchronization in an astable blocking oscillator

However, the sync pulses appear as positive pulses at the base Q_1 (after polarity inversion in Q_2 and further polarity inversion in the pulse transformer). Pulses numbered 1, 2, 3 and 4 do not have sufficient amplitude to terminate the sweep prematurely. However, pulse 5 occurs at such an instant and has sufficient amplitude that it prematurely terminates the cycle as Q_2 goes into the ON state at the instant of occurrence of the 5th pulse, as regenerative action again takes place. C_1 again charges and so on. Thus, the cycle is prematurely terminated at T_s , and a new cycle starts. Synchronization with 5:1 division is accomplished. If, on the other hand, the amplitude of the sync pulses is increased, it could result in synchronization with 3:1 division, as shown in Fig. 15.5(c). Thus, we can say that with the proper spacing between the sync pulses (proper choice of pulse repetition frequency) and proper choice of amplitude for these pulses, it is possible to achieve synchronization with desired frequency division.

15.3.2 Synchronization of Transistor Astable Multivibrators

Synchronization with frequency division in a transistor astable multivibrator can be accomplished by applying either positive or negative pulses to both the transistors or to any of the transistors. Figs. 15.6 (a) and (b) depict the circuit and the waveforms to achieve synchronization with a frequency division of 6:1. Here, positive pulses are applied at the base B_1 of Q_1 .

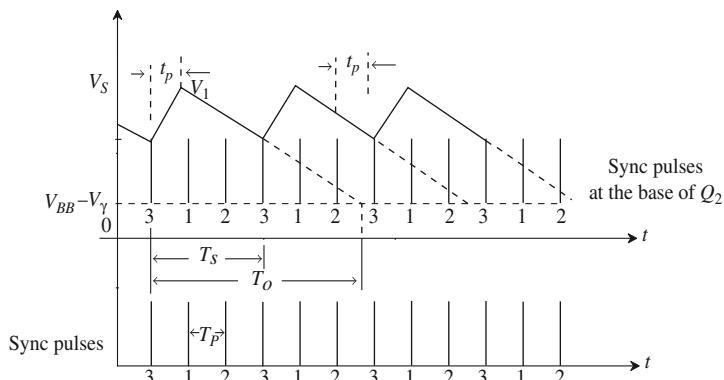
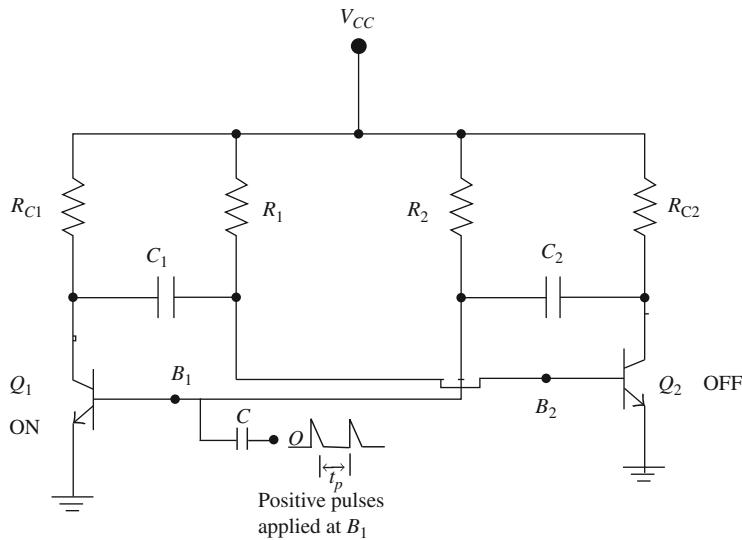
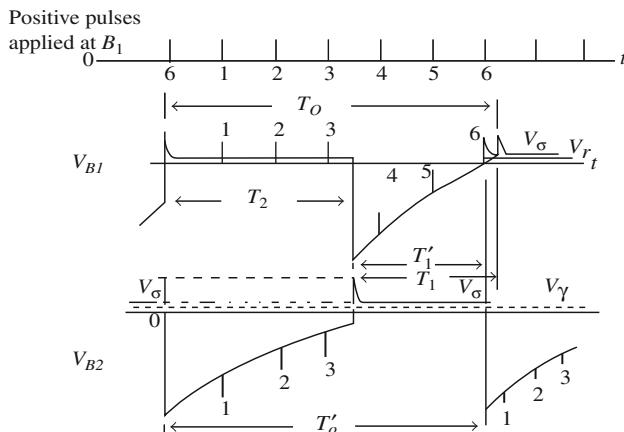


FIGURE 15.5(c) 3:1 synchronization in an astable blocking oscillator

FIGURE 15.6(a) An astable multivibrator with sync pulses applied at B_1 FIGURE 15.6(b) The waveforms of an astable multivibrator with positive sync pulses applied at B_1

In the absence of sync pulses, the astable must have had a time period T_o ($= T_1 + T_2$) when the cycle would have naturally terminated at V_{B1} or $V_{B2} = V_\gamma$. However, with sync pulses connected, the positive pulses applied at B_1 are amplified and inverted and appear as negative pulses at B_2 . During T_2 , the positive pulses at B_1 have no effect on the time period as Q_1 is already ON. Further the negative pulses 1, 2 and 3 appearing at B_2 will not be able to change T_2 . Hence, T_2 remains unchanged. However, during the time period T_1 , the pulses numbered 4 and 5 do not have sufficient amplitude to drive Q_1 into the ON state and terminate the time period T_1 prematurely. However, the 6th pulse has sufficient amplitude to prematurely terminate the time period T_1 as this pulse drives the base of Q_1 positive; and hence, Q_1 goes ON. The new time period for which Q_1 is OFF is T'_1 and the new sweep period is T'_o . In this arrangement, the multivibrator completes one cycle for every six sync pulses. Although the complete period is synchronized, the individual time periods are not synchronized. T_2 is the same as without synchronization.

15.3.3 Synchronization with Division of an Astable Multivibrator by Applying Negative Pulses at both the Bases (B_1 and B_2)

If an astable multivibrator is required to be synchronized during both the time periods T_1 , T_2 and also for T , then the negative pulses can be applied to both the bases B_1 and B_2 of transistors Q_1 and Q_2 . Let it be assumed that both the time periods are required to be synchronized with a division of 3:1 so that the total period is synchronized with a frequency division of 6:1, as shown in Fig. 15.7.

The negative pulses applied at B_1 get amplified, inverted appear as positive pulses at the base B_2 . Similarly, the negative pulses applied at B_2 get amplified and inverted and appear as positive pulses at the base B_1 . Thus, the positive pulses superimposed on the exponential portion of the waveform at B_2 during T_2 are a combination of negative pulses applied directly and the inverted and amplified negative pulses from the other transistor which appear as positive pulses. The pulses marked 1 and 2 do not have sufficient amplitude. However, the pulse marked 3 has an amplitude that can terminate T_2 earlier, resulting in a new time period T_2' . Similarly, during the period T_1 when Q_1 is OFF, pulses marked 4 and 5 will not have any influence on the time period T_1 . However, the pulse numbered 6 will terminate T_1 prematurely, resulting in a new time period T_1' . Each of these time periods are individually synchronized with a frequency division of 3:1 as the third and the sixth pulses prematurely terminate the time periods T_2 and T_1 . Hence, synchronization with a division of 6:1 occurs for the entire time period T of the astable multivibrator.

15.3.4 Positive Pulses Applied to B_1 Through a Small Capacitor from a Low-impedance Source

Synchronization with the division of both the time periods of an astable multivibrator can be achieved by applying the positive pulses to only one base instead of at both the bases, say, B_1 . During the period when Q_1 is ON, as its input resistance is very small, the time constant of the pulse input is also very small. This RC circuit behaves as a differentiator and the pulse is quasi-differentiated. The negative spikes in this differentiated signal at B_1 of Q_1 appear as the positive spikes during the exponential variation at B_2 . Pulses 1 and 2 may not be able to drive Q_2 ON and terminate T_2 prematurely. However, the positive spike appearing at the trailing edge of the pulse numbered 3 will prematurely terminate the OFF period T_2 of Q_2 . The new time period for

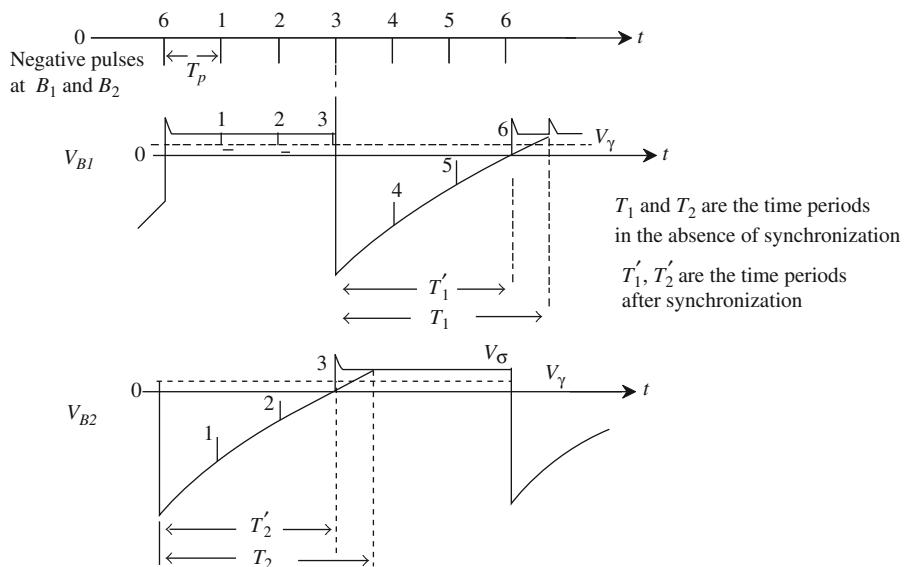


FIGURE 15.7 The synchronization of individual periods and the total period with a division of 6:1

which Q_2 is OFF is T_2' . During the exponential variation of the voltage at B_1 during T_1 , the positive pulses are superimposed and at the leading edge of the pulse numbered 6, the OFF period of Q_1 is prematurely terminated. The new time period for which Q_1 is OFF is T_1' . The original time period of the astable multivibrator was $T (= T_1 + T_2)$. Whereas, the new time period after synchronization is $T' (= T_1' + T_2')$. Thus, not only the entire cycle with time period T' of the astable is synchronized with a frequency division of 6:1 but the individual time periods T_1' and T_2' are also synchronized with a division of 3:1, as shown in Fig. 15.8.

15.4 A MONOSTABLE MULTIVIBRATOR AS A DIVIDER

A monostable multivibrator can be used for synchronization with frequency division [see Fig. 15.9(a)] and the waveforms are shown in Fig. 15.9(b). Here, the positive pulse train is applied at B_1 through a small capacitance from a low impedance source.

The positive pulse train applied at B_1 gets quasi-differentiated as discussed earlier in the Section 15.3.4. The negative spikes at the trailing edge of the pulses are amplified and inverted and appear as the positive spikes at B_2 . As a result, positive spikes due to the second pulse will prematurely terminate the time period resulting in synchronization with the frequency division of 2:1. On the other hand, if the amplitude of the pulses is large enough, pulse 1 may prematurely terminate the time period, thereby changing the counting ratio from 2 to 1.

15.4.1 A Relaxation Divider that Eliminates Phase Jitter

When a pulse train is applied to a divider, there could be a small time delay by the time it appears at the respective bases to cause a possible premature change in the state of the devices. This delay is called the phase delay. Also, as the pulse train is coupled to the divider circuit through an RC circuit, it could result in pulses

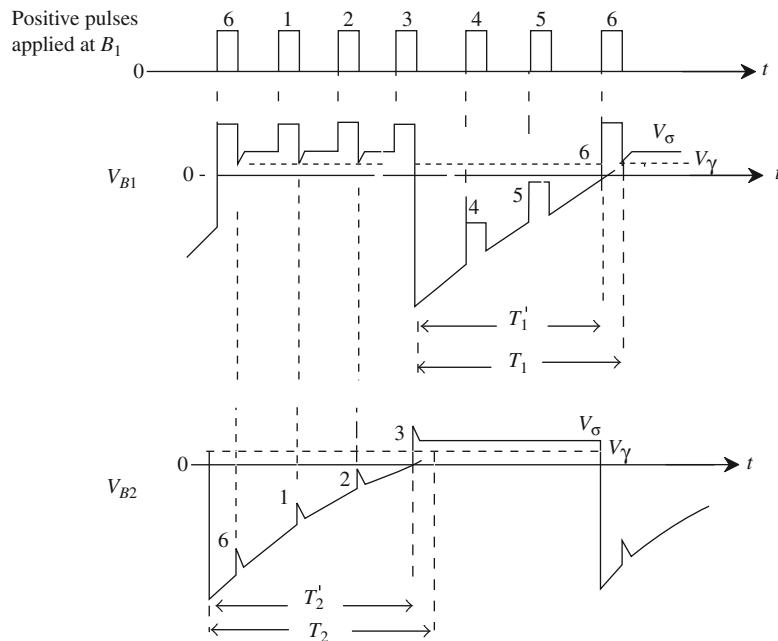


FIGURE 15.8 The synchronization of both the portions of astable multivibrators with positive pulses applied at B_1 through a small capacitor and low impedance source

having a finite rise time. Further the divider may have a certain response time which is liable to change with the frequency of the sync signals and the time constants associated with the circuit. As a result, this signal can influence the instant at which the base waveform would drive the device OFF. The phase delay could also be due to the variations in the device characteristics, supply voltages and the noise in the circuit. The phase delay that varies due to the cumulative effect of all these factors is termed as phase jitter. The frequency division without the phase jitter can be implemented using the schematic arrangement shown in Fig. 15.10.

The waveforms are shown in Fig. 15.11. The input to the divider is a train of pulses. The divider is an $n:1$ divider, i.e., for every n pulses, the n^{th} pulse is obtained at the output of the divider. This n^{th} pulse is applied as a trigger to the monostable multivibrator which generates a gated output, that is, a pulse of duration T . This pulse of duration T controls the sampling gate. A sampling gate is one which transmits the input to its output as long the enabling signal (the gating signal) is present. For the rest of the duration, there is no output for

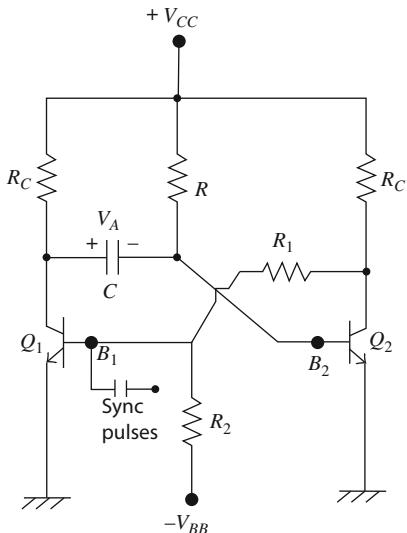


FIGURE 15.9(a) A monostable multivibrator

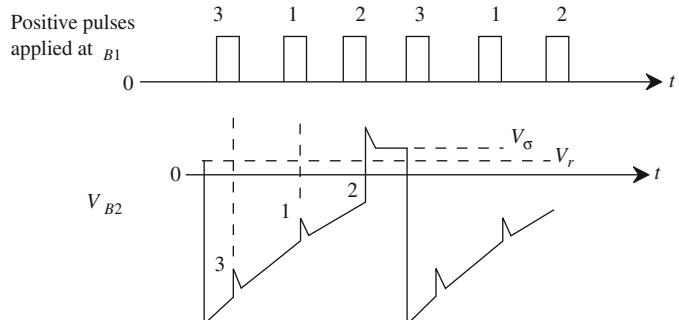


FIGURE 15.9(b) The waveform at B_2

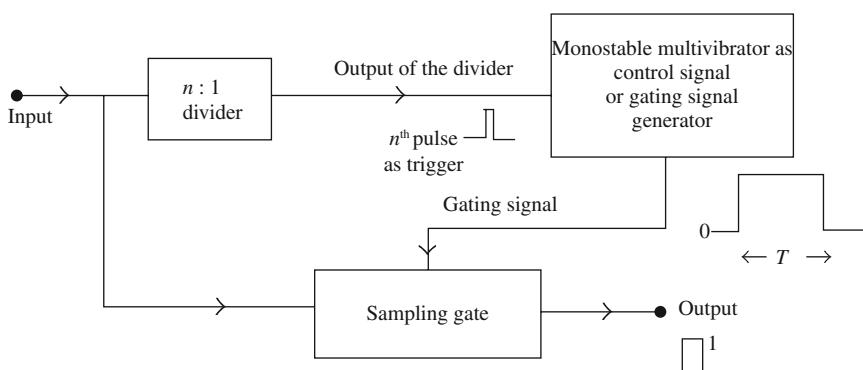


FIGURE 15.10 The frequency division without the phase jitter

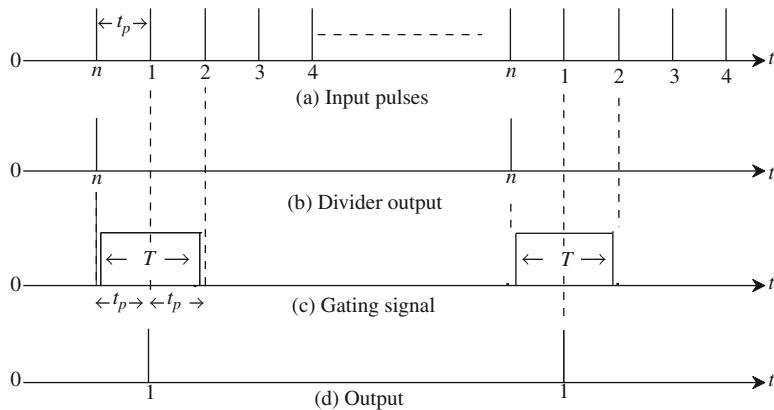


FIGURE 15.11 The waveforms of the divider that eliminates the phase jitter

the sampling gate. As only the output of the divider (n^{th} pulse) triggers the monostable multivibrator, a pulse of duration T occurs only at the end of the n^{th} pulse. Though a sequence of pulses is present at the input of the sampling gate, only the pulse marked 1 is transmitted to the output, as during the occurrence of this pulse the sampling gate is enabled. The output consists of the pulses labeled 1 only. By adjusting the pulse width of the gating signal such that $T_p < T < 2 T_p$, we can ensure that the n^{th} pulse does not pass to the output of the sampling gate. Thus, phase jitter can be eliminated.

Stability of the Relaxation Divider. In a frequency divider, due to phase jitter, if the n^{th} pulse is required to prematurely terminate a sweep cycle, it is possible that either the $(n-1)^{\text{th}}$ pulse or even the $(n-2)^{\text{nd}}$ pulse may terminate a sweep cycle. This accounts for the instability of the natural timing period of the oscillator, which in turn may cause a loss of synchronization or an incorrect division ratio. The typical voltage variation at the base of an astable multivibrator is shown in Fig. 15.12.

In order to calculate the time period of a monostable multivibrator, we use the relation: $v_o(t) = v_f - (v_f - v_i)e^{-t/\tau}$ where, v_i is the initial voltage from which the charge on the capacitor discharges and v_f is the final voltage to which the capacitor would discharge, if allowed to discharge, as $t \rightarrow \infty$. Assuming that τ remains fairly constant, it is the changes in v_i and v_f and $v_C (= V_\gamma)$ that could be responsible for the instability of the natural period. Let us consider the influence of these factors on the natural time period of the monostable multivibrator:

- The parameters of the transistor are likely to change due to temperature variations. Also, if the existing transistor is replaced by another for some reason the transistor parameters may be affected. This could influence v_i and v_C , the voltage at which the period terminates. v_C can be the cut in the voltage of a transistor (V_γ) and v_f can change due to loading. Normally, a regulated power supply with sufficient current rating is used for v_f . Hence, the instability of the time period T_o due to the variation of v_f can be minimized or eliminated. The time period T_o can now mainly change due to the variations in v_i and v_C . However, the choice of v_f may influence the natural time period.
- Let us consider the case when v_f is a large value, say, v_{f1} (curve 1). Then the variation between v_i and v_C can be approximately linear. Consequently, the change in T_o due to variation in v_C can be minimized to some extent. However, in curve 1, if v_i changes by a larger amount than v_C (with the same τ), then choosing a larger value of v_f may again give rise to instability of the time period.
- On the contrary, if v_f is reduced to v_{f2} , the variation of the voltage between v_i and v_C is exponential in nature and hence, non-linear. Now if v_i varies, then a given percentage change in $(v_C - v_i)$ could cause a lesser percentage change in T_o (curve 2).

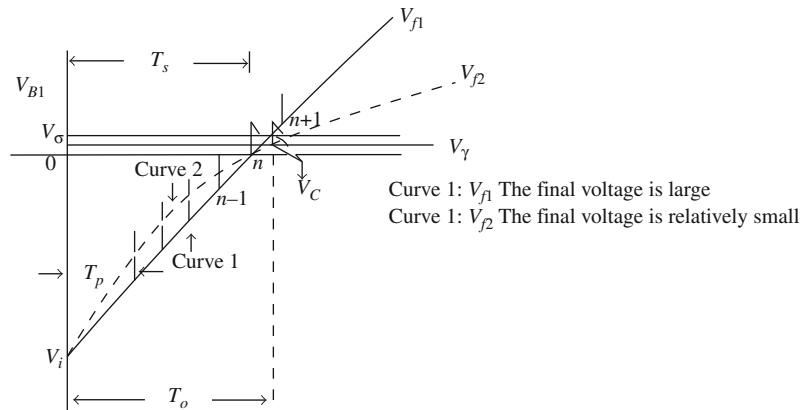


FIGURE 15.12 The factors that account for the instability of a relaxation divider

Hence, the variation in T_o i.e., instability of the time period, can be minimized by the proper choice of v_f , depending on whether the instability has occurred either due to the variation in v_C or v_i .

15.5 SYNCHRONIZATION OF A SWEEP CIRCUIT WITH SYMMETRICAL SIGNALS

So far, we have considered the synchronization of relaxation circuits with external sync signals that are essentially pulses only. However, we can also synchronize a relaxation circuit such as a sweep generator with sync signals that could as well be gradually varying signals like sinusoidal signals. Let us consider the output of a UJT sweep generator that is to be synchronized with a slowly varying sinusoidal signal, as shown in Fig. 15.13(a).

Let it be assumed that the breakdown voltage of the UJT varies sinusoidally in the presence of the sync signal. Here, V_{po} is the quiescent breakdown voltage of the UJT and V_p is the breakdown voltage in the presence of the sync signal. It is possible that synchronization can be effected with $T = T_o$. If this happens, then the period of the sweep is not altered by the sync signal and the sweep amplitude is also unaffected. The sweep cycle, as a result, terminates at V_{po} , which means that the sweep terminates on its own at points labeled 'o' in Fig. 15.13(a).

Earlier, when synchronization was achieved using a pulse train as sync signals, it was observed that for synchronization to take place it was imperative that the spacing between pulses (T_p) should be less than or equal

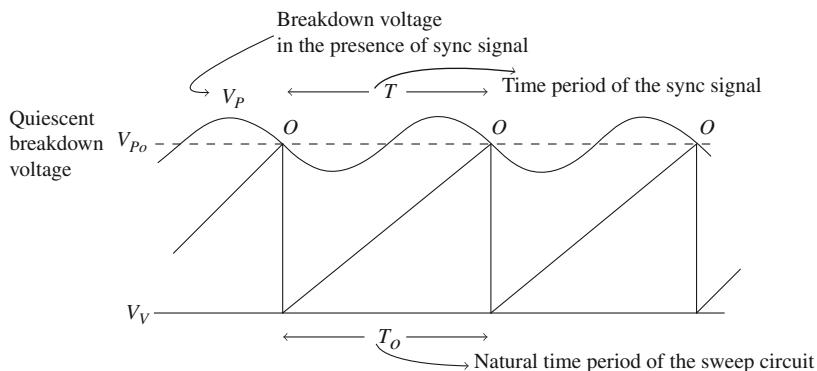


FIGURE 15.13(a) The synchronization of a sweep generator with sinusoidal sync signal

to the natural time period (T_o) of the relaxation circuit. It was also observed that a pulse could prematurely and reliably terminate a sweep cycle (reduce the sweep duration) but will not be able to extend the sweep duration. However, when it is a case of synchronization with symmetric signals, synchronization is always possible whether T (T_p in the case of a pulse train) is less than or equal to T_o or T is greater than T_o .

It is seen from Fig. 15.13(b) that if the sweep voltage meets the V_p curve at a point above V_{po} for $T > T_o$, say X , then the duration of the sweep is lengthened ($T'_o > T_o$). On the other hand, if the sweep voltage meets the V_p curve at a point below V_{po} for $T < T_o$, the duration of the sweep is shortened ($T''_o < T_o$).

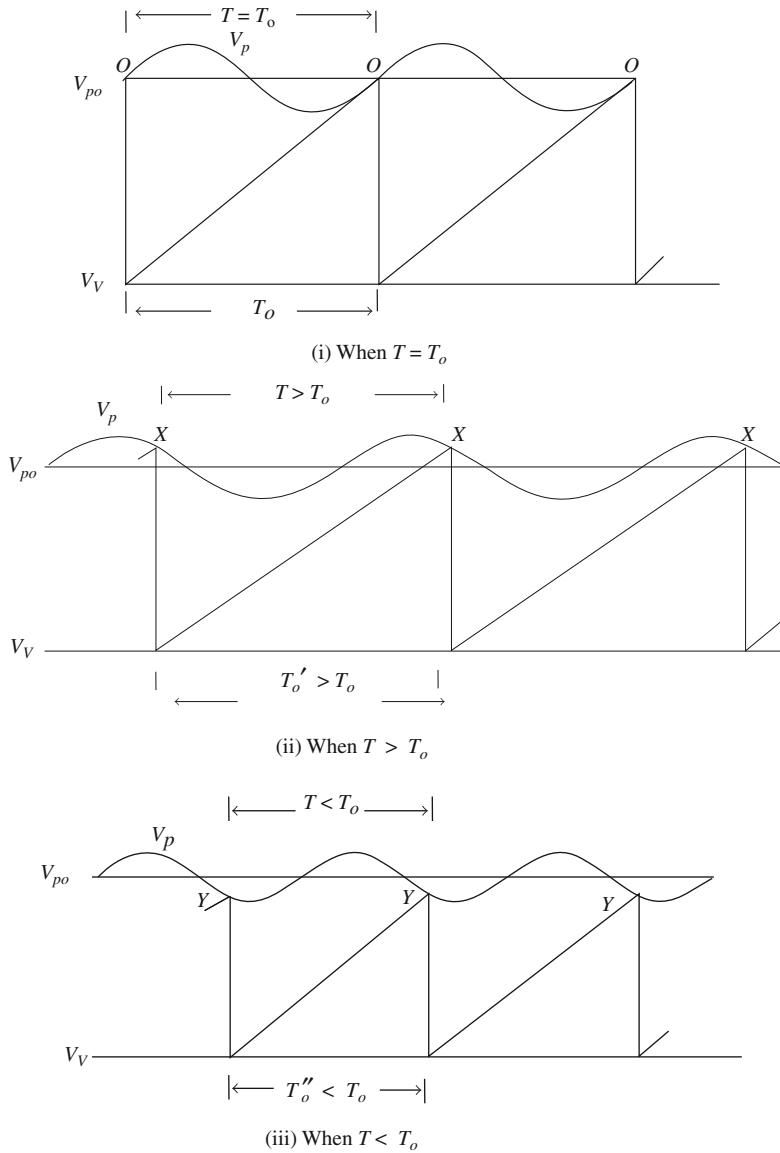


FIGURE 15.13(b) The timing relationship between the sweep voltage and the time-varying breakdown voltage when (i) $T = T_o$, (ii) $T > T_o$, then $T'_o > T_o$ and (iii) $T < T_o$, then $T''_o < T_o$

Let us summarize this with the help of Fig. 15.13(c):

1. When $T = T_o$, the sweep is terminated at 'o' on the V_{po} line, leaving the period and the amplitude of the sweep unaltered.
2. When $T > T_o$, if the sweep terminates at a point say, X that lies between 'o' and positive maximum, at A , then the sweep is lengthened and its duration T' is greater than T_o . This lengthening is maximum when the sweep terminates at A .
3. When $T < T_o$, if the sweep terminates at a point, say Y , that lies between 'o' and the negative maximum at B , then the sweep is shortened and its duration T'' is smaller than T_o . This shortening is maximum when the sweep terminates at B . To calculate the range of synchronization let us consider an example.

EXAMPLE

Example 15.1: A UJT sweep operates with a valley voltage of 4 V and peak voltage of 16 V. A sinusoidal synchronizing voltage of 3 V peak is applied as a sync signal. $\eta = 0.5$. If the natural frequency of the sweep is 1 kHz, over what range of sync signal frequency will the sweep remain in 1:1 synchronization with the sync signal.

Solution:

The quiescent breakdown voltage, $V_{po} = 16$ V.

Peak-to-peak amplitude of the synchronizing signal = 3 V

$$V_m = \frac{3}{2} = 1.5 \text{ V}$$

In the absence of the sync signal, the peak-to-peak swing of the sweep = $V_{po} - V_V = 16 - 4 = 12$ V

In the presence of the sync signal, the sweep amplitude must therefore lie in the range

$$(12 - 1.5) = 10.5 \text{ V} \quad \text{and} \quad (12 + 1.5) = 13.5 \text{ V}.$$

Time period of the sync signal,

$$T = \frac{1}{f} = \frac{1}{1 \times 10^3} = 1 \text{ ms}$$

Amplitude of the natural sweep signal = $16 - 4 = 12$ V.

And this sweep amplitude is generated in 1ms. Therefore, the time required to generate a sweep of, 10.5 V is

$$\frac{10.5}{12} \times 1 \text{ ms}$$

and the corresponding frequency is,

$$\frac{12}{10.5} \text{ kHz} = 1.143 \text{ kHz}$$

The time required to generate a sweep of 13.5 V is

$$\frac{13.5}{12} \times 1 \text{ ms}$$

and the corresponding frequency is

$$\frac{12}{13.5} \text{ kHz} = 0.899 \text{ kHz}$$

It is seen from the above calculations that the sweep generator remains synchronized as the frequency of the sync signal varies from 889 c/s to 1143 c/s.

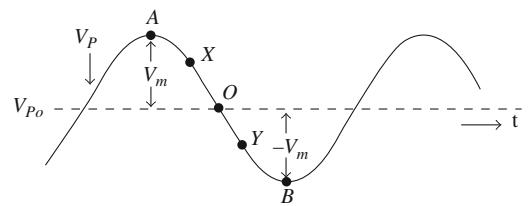


FIGURE 15.13(c) The synchronization when $T \neq T_o$

15.5.1 Frequency Division with Symmetric Sync Signals

Let us now consider the operation of a sweep circuit as a frequency divider using sinusoidal signal as sync signal, as shown in Fig. 15.14(a). The solid lines represent the sweep with a time period T_o and the sync signal with a time period T . The natural sweep terminates on V_{po} line. In the presence of the sinusoidal sync signal, if the sweep meets the sync signal above the V_{po} line at X, the new time period of the sweep is T_s . Thus, the sweep period T_o changes to T_s as a result of the sync signal. The sync signal completes three cycles during the period T_s , resulting in the division by a factor 3 as $T_s = 3T$ (counting ratio of 3).

If now the amplitude of the sync signal is increased (dashed line), keeping the time period the same as T , as shown in Fig. 15.14(b), the sweep meets the sync signal at Y between O and B. The duration of the sweep is shortened (dashed line) resulting in a 2:1 synchronization (a counting ratio of 2). If the amplitude of the sync signals further increases, it could result in a counting ratio of 1. Hence, this circuit can operate as a counter.

Increasing the amplitude of the sync signal, in principle, can cause 1:1 synchronization. The sweep is terminated prematurely when it meets the sync signal below the V_{po} line. Beyond this point once again the sweep voltage increases and this time it will terminate on the sync signal above the V_{po} line. Therefore, the actual sweep waveform consists of the alternate sweeps of short and long durations. The suggestion therefore is that if this sweep is used to cause deflection of the electron beam along the X -axis in a CRO, it is preferable to use a sync signal of smaller amplitude, as shown in Fig. 15.14(c).

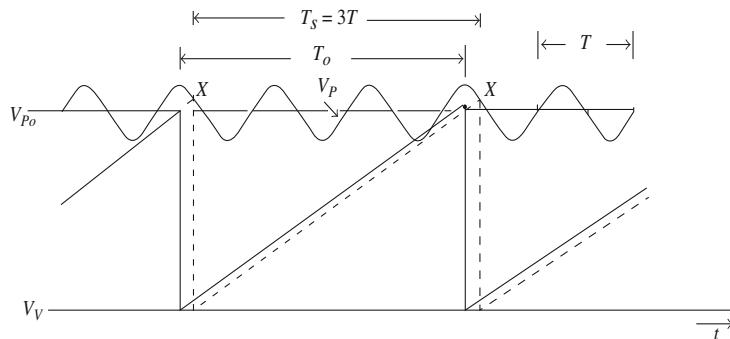


FIGURE 15.14(a) 3:1 synchronization of the sweep with symmetric sync signal

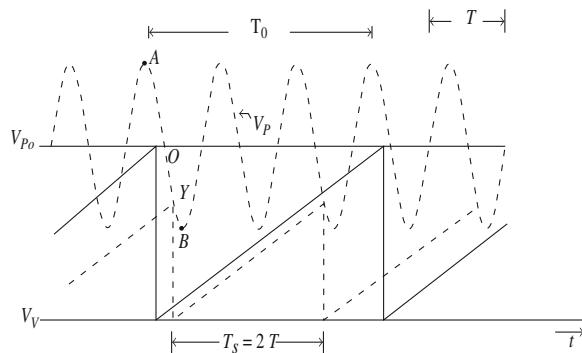


FIGURE 15.14(b) 2:1 Synchronization of the sweep with a symmetric sync signal

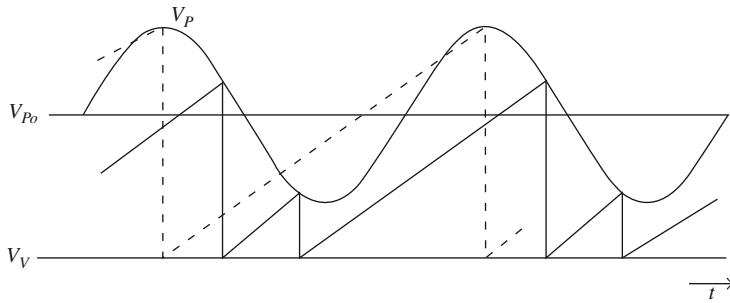


FIGURE 15.14(c) The excessive amplitude of the sync signal in a sweep resulting in sweeps of long and short durations

S O L V E D P R O B L E M S

Example 15.2: The UJT relaxation oscillator shown in Fig. 15.15(a) is to be used as 3:1 divider for pulses which occur at 2.5 kHz rate. The available supply voltage is 30 V. The pulses are applied at the base B_2 . Draw the waveforms and calculate the pulse amplitude. Given $R = 2\text{k}\Omega$, $C = 0.5\text{\mu F}$, $\eta = 0.5$ and $V_\gamma = 0.6\text{V}$.

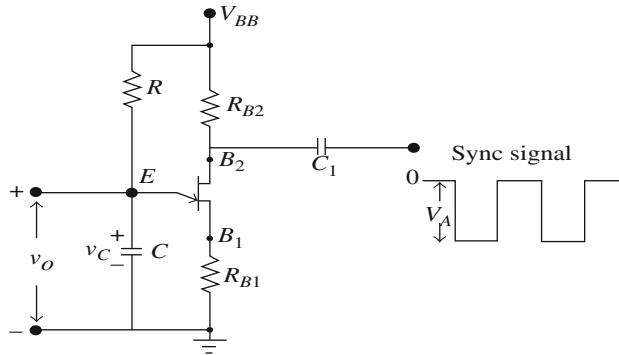


FIGURE 15.15(a) The UJT relaxation circuit with a sync signal

Solution: From the given data:

Pulse frequency $f = 2.5\text{ kHz}$

$$\text{Pulse time period } T_p = \frac{1}{f} = \frac{1}{2500} = 0.4\text{ ms}$$

For 3:1 synchronization, the frequency of the UJT oscillator should be 1/3rd of the pulse frequency.

$$f_o = \frac{1}{3} \times f = \frac{1}{3T_p}$$

Output time period $T_o = 3T_p = 3 \times 0.4\text{ ms} = 1.2\text{ ms}$

Let V_A be the peak-to-peak pulse input and it is negative.

$$v_C = v_f(1 - e^{-t/\tau})$$

At $t = 1.2\text{ ms}$, $v_C = V_{Pf}$

Where

$$V_{Pf} = V_P - (-V_A) = V_P + V_A \quad V_P = \eta V_{BB} + V_\gamma$$

At

$$t = 1.2 \text{ ms}, \quad v_o = V_P + V_A$$

$$v_f(1 - e^{-t/\tau}) = (\eta V_{BB} + V_\gamma) + V_A$$

$$30(1 - e^{-1.2 \times 10^{-3} / 2 \times 10^3 \times 0.5 \times 10^{-6}}) = (0.5 \times 30 + 0.6) + V_A$$

$$V_A = 30(1 - 0.3) - 15.6 = 21 - 15.6 = 5.4 \text{ V}$$

The waveforms are drawn as shown in Fig. 15.15(b).

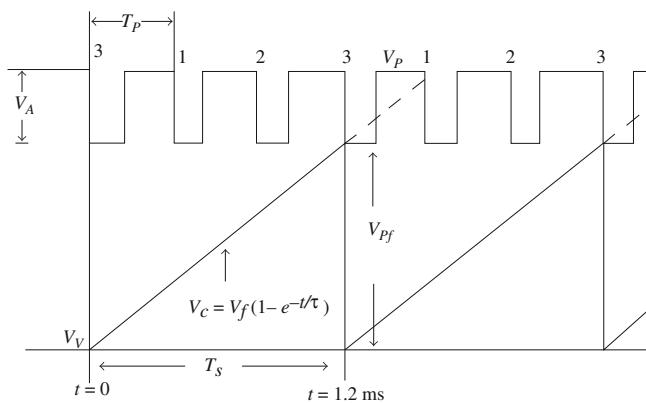


FIGURE 15.15(b) The waveforms

Example 15.3: A free running relaxation oscillator shown in Fig. 15.16(a) has sweep amplitude of 100 V and a period of 1 ms. Synchronizing pulses are applied to the device such that the breakdown voltage is lowered by 50 V at each pulse. The synchronizing pulse frequency is 4 kHz. What is the amplitude and the frequency of the synchronized oscillator waveform?

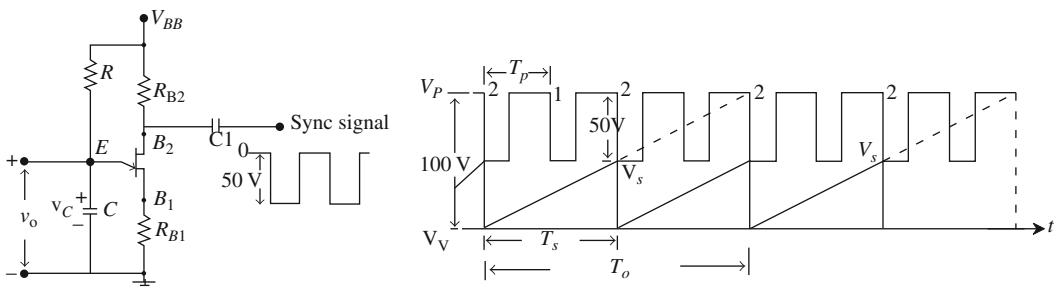


FIGURE 15.16(a) The UJT oscillator; (b) the waveforms

Solution:

Given that

$$T_o = 1 \text{ ms} (f_o = 1 \text{ kHz}) \text{ and } V_s = 100 \text{ V}$$

$$T_p = \frac{1}{f} = \frac{1}{4} \times 10^{-3} = 0.25 \text{ ms} \text{ since } f_p = 4 \text{ kHz} \quad T_p < T_o$$

Therefore, synchronization is possible.

The unsynchronized sweep amplitude reaches 100 V in 1ms. So it reaches 50 V in $(50 \times 1)/100 = 0.5$ ms.

In 0.5 ms, two sync pulses occur and consequently, 2:1 synchronization is achieved. The amplitude of the sweep is 50 V. The waveforms are shown in Fig. 15.16(b).

SUMMARY

- If, there are a number of waveform generators in a pulse or a digital system and all of them arrive at some reference point in their cycle at the same time, then these waveform generators are said to be running in synchronism.
- If two waveform generators operate at two different frequencies — one completes only one cycle and during the same time the other generator completes precisely a fixed integral number of cycles, then these two generators are said to be running in synchronism but with the frequency division.
- A relaxation circuit is one in which a capacitor charges during a finite time interval and abruptly discharges when the voltage across the capacitor reaches a predetermined level.
- Sweep generators, blocking oscillators and multivibrators are some examples of relaxation circuits.
- Synchronization of a relaxation circuit can be achieved by either the external pulse train or the symmetrical signals like sinusoidal signals as sync signals.
- To establish synchronization using pulse train as sync signals, it becomes necessary that the spacing between the sync pulses should be less than or equal to the sweep duration of the relaxation circuit.
- Synchronization cannot be achieved if the spacing between the sync pulses is larger than the sweep duration or if the amplitude of the sync signals is very small.
- If the magnitude of the sync signals is appreciably large, synchronization is always possible.
- A monostable multivibrator can be used as a frequency divider.
- When a synchronizing input pulse is applied to a frequency divider, there will be a finite time delay before the output is available. This time delay is called phase delay.
- If the phase delay is subjected to periodic variations then it is called the phase jitter.
- When symmetric signals like sinusoidal signals are used as sync signals, synchronization is possible even if the time period T (T_p in the case of pulse train) is more than the natural time period of the relaxation circuit T_o .
- When $T > T_o$, the duration of the sweep cycle is lengthened (T_o') and when $T < T_o$, the duration of the sweep cycle is shortened (T_o'').

MULTIPLE CHOICE QUESTIONS

1. Sweep generators, multivibrators and blocking oscillators are classified as:
 - Relaxation circuits
 - Multistage amplifiers
 - Sampling gates
 - Clipping and clamping circuits
2. When synchronization with the frequency division is implemented in a pulse or a digital system, this circuit can be called as a:
 - Scale-of-two circuit
 - Counting circuits
 - Schmitt trigger
3. Timing interval in a relaxation circuit is established by the:
 - Charging and discharging of a capacitor
 - Charging of a capacitor
 - Discharging of a capacitor
 - None of the above
4. A relaxation circuit can be synchronized by a train of sync pulses. For synchronization to take place:
 - $T_p > T_o$ and the amplitude of the pulses should be reasonably large

- (b) $T_p \leq T_o$ and the pulses can have any amplitude
 (c) $T_p \leq T_o$ and the amplitude of the pulses should be reasonably large
 (d) $T_p > T_o$ and the pulses can have any amplitude
5. It is possible to synchronize the output of a UJT relaxation circuit with symmetric sync signals when:
 (a) $T \geq T_o$
 (b) $T \leq T_o$
 (c) $T \leq T_o$ and $T \geq T_o$
 (d) None of the above
6. The time interval between the instant the input pulse is applied to a frequency divider to the instant it appears at the output is called:
 (a) Phase delay
 (b) Resolution time
 (c) Propagation delay
 (d) Storage time
7. The phase delay that varies due to the cumulative effect of the variations in the device characteristics, supply voltage and noise is termed as:
- (a) Noise margin
 (b) Resolution time
 (c) Propagation delay
 (d) Phase jitter
- (a) Lengthened
 (b) Shortened
 (c) Remains unchanged
 (d) None of the above
9. When synchronizing the output of a UJT relaxation circuit with symmetric signals, if $T < T_o$, the duration of the sweep is:
 (a) Lengthened
 (b) Shortened
 (c) Remains unchanged
 (d) None of the above

SHORT ANSWER QUESTIONS

- (1) Explain the principle of frequency synchronization and division.
- (2) It is said that synchronization with pulses is not possible if the spacing between the pulses (T_p) is larger than the time period (T_o) of the UJT oscillator. Is synchronization possible with symmetric signals if $T > T_o$. Explain.
- (3) What is meant by jitter in a frequency divider?
- (4) What are the factors responsible for the instability in the natural time period of a frequency divider?
- (5) Is it possible to achieve frequency synchronization with division using symmetric signals as sync signals?
- (6) What is the effect of amplitude of the symmetric sync signals on frequency synchronization of a relaxation oscillator, with division?

LONG ANSWER QUESTIONS

- (1) With the help of a neat circuit diagram and waveforms, explain the method to achieve frequency synchronization using pulse train as sync signals.
- (2) What is meant by synchronization with frequency division? Explain, with suitable waveforms, the procedure to obtain 3:1 and 5:1 synchronization.
- (3) Explain suitable methods to synchronize both the time periods in an astable multivibrator. It is required that the time period T_2 be synchronized with a division of 2:1 and the time period T_1 be synchronized with a division of 3:1.
- (4) Show, with the help of suitable waveforms, how a monostable multivibrator can be used as a frequency divider.
- (5) What is phase jitter? Explain the method to eliminate it.
- (6) Explain how synchronization and synchronization with division is possible with symmetric signals as sync signals.

UNSOLVED PROBLEMS

- (1) A UJT sweep operates with a valley voltage of 3 V and a peak voltage of 15 V. A sinusoidal synchronizing voltage peak of 6 V is applied as a sync signal. If the natural frequency of the sweep is 2 kHz over what range of sync signal frequency will the sweep remain in 1:1 synchronization with the sync signal.
- (2) The UJT relaxation oscillator shown in Fig. 15p.2 is to be used as 2:1 divider for pulses which occur at a

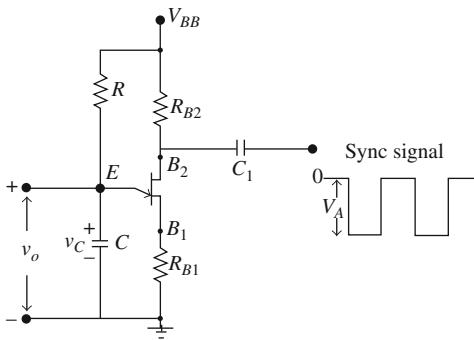


FIGURE 15p.2 The given UJT relaxation circuit with sync signal

2 kHz rate. The available supply voltage is 30 V. The pulses are applied at the base B_2 . Calculate the pulse amplitude and plot the waveforms. Given

$$R = 2 \text{ k}\Omega, C = 0.5 \text{ }\mu\text{F}, \eta = 0.5 \text{ and } V_\gamma = 0.6 \text{ V.}$$

- (3) A free running relaxation oscillator shown in Fig. 15p.3 has a sweep amplitude of 100 V and a period of 0.5 ms. Synchronizing pulses are applied to the device such that the breakdown voltage is lowered by 50 V at each pulse. The synchronizing pulse frequency is 4 kHz. What is the amplitude and frequency of the synchronized oscillator waveform.

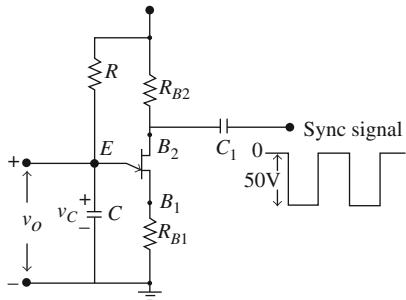


FIGURE 15p.3 The given UJT circuit

MODEL QUESTION PAPERS

MODEL QUESTION PAPER-I

II B.Tech. I Semester Regular Examinations

PULSE AND DIGITAL CIRCUITS

(Common to Electrical & Electronics Engineering, Electronics & Communication Engineering, Electronics & Instrumentation Engineering and Electronics & Telematics)

Time: 3 hours

Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks

1. (a) Prove that an RC circuit behaves as a reasonably good integrator if $RC > 15T$, where T is the period of an input ' $E_m \sin wt$ '.
(b) Obtain the response of an RLC circuit under critically damped conditions. [8+8]
2. (a) Draw the circuit diagram of slicer circuit and explain its operation with the help of its transfer characteristic.
(b) Draw the circuit diagram of series coupled clipper. Draw its transfer characteristics indicating all intercepts, slopes and voltage levels derive the necessary equations. [8+8]
3. (a) Explain the terms pertaining to transistor switching characteristics.
 - i. Rise time.
 - ii. Delay time.
 - iii. Turn-on time.
 - iv. Storage time.
 - v. Fall time.
 - vi. Turn-off time.
(b) Give the expression for risetime and falltime in terms of transistor parameters and operating currents. [6+10]
4. Explain the switching characteristics of Zener diode with suitable equations. [16]
5. (a) Draw and clearly explain Bootstrap Sweep Generator.
(b) Derive the relation between the slope, transmission and displacement errors
(c) Explain how UJT is used for sweep circuit? [6+4+6]
6. (a) What do you mean by synchronization?
(b) What is the condition to be met for pulse synchronization?
(c) Compare sine wave synchronization with pulse synchronization? [4+6+6]
7. (a) Why are sampling gates called Selection circuits?
(b) What are the advantages of unidirectional sampling gates?
(c) What are the applications of sampling gates? [6+4+6]
8. Draw and explain TTL Gates. [16]

MODEL QUESTION PAPER-II

II B.Tech. I Semester Regular Examinations PULSE AND DIGITAL CIRCUITS

(Common to Electrical & Electronics Engineering, Electronics & Communication Engineering, Electronics & Instrumentation Engineering and Electronics & Telematics)

Time: 3 hours

Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks

1. (a) The input of low-pass RC circuit is a step of V. Obtain the expression for the output Voltage.
 (b) With the help of waveforms, explain how a comparator is used for:
 i. Measurement of time delays
 ii. Measurement of phase and
 iii. Generating timing markers [8+8]
2. (a) State and prove clamping-circuit theorem.
 (b) The input shown in Figure 1(a) is applied to the clamping circuit [see Figure 1(b)]. Plot the output waveform. Given that $R_s = R_f = 50\Omega$, $R = 10\text{ k}\Omega$, $R_r = \infty$, $C = 1\mu\text{F}$. [8+8]

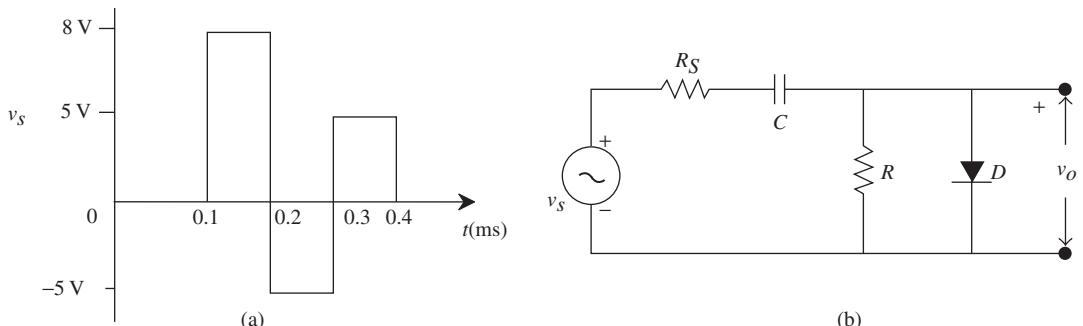


Figure 1 (a) The given input and (b) the given clamping circuit

3. Write short notes on:
 (a) Diode switching times
 (b) Switching characteristics of transistors
 (c) FET as a switch. [4+8+4]

4. (a) The blocking oscillator with emitter timing shown in Figure 2 has the following parameters: $n = 1$, $n_1 = 1$, $L = 5 \text{ mH}$, $R = 0.5 \text{ k}\Omega$, $h_{FE} = 25$ and $V_{CC} = 10 \text{ V}$. Calculate (a) the amplitude of the trigger; (b) the value of R_L that allows the pulse formation; (c) the pulse width with $h_{FE} = 25$ and also calculate t_p using the approximate relation; (d) the base, collector and emitter currents and (e) plot the current waveforms.

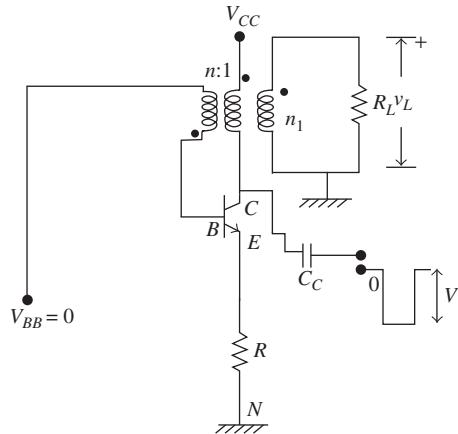


Figure 2 A monostable blocking oscillator with emitter timing

- (b) The astable blocking oscillator (diode-controlled) shown in Figure 3 has the following parameters: $L = 5.2\text{mH}$, $C = 90\text{ pF}$, $V_{CC} = 10\text{V}$, $R = 500\Omega$, $V_r = 0.6\text{V}$, $n = 1$ and $V_{BB} = 0.5\text{V}$. Calculate (a) the period and the duty cycle of the free oscillations; (b) the peak voltages and currents and (c) the current in the magnetizing inductance at the end of one cycle. [8+8]

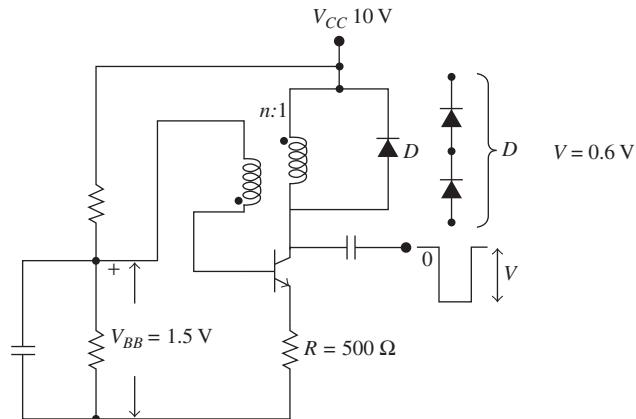


Figure 3 The diode-controlled astable blocking oscillator

5. (a) Draw the circuit of a simple current sweep generator and explain its operation. Derive the expression for its slope error e_s .

- (b) For the circuit shown in Figure 4, at $t = 0$, the driving waveform is applied to the base of the transistor.
- Calculate the time required for the inductor current to reach the maximum value. Assume that the inductor is ideal, the saturation resistance of the transistor is zero and $h_{FE} = 20$.
 - Calculate the time required for the inductor current to decay to 10 mA.
 - If the sum of saturation resistance and inductive resistance is 20Ω , determine the time required for sweep, T_s , to reach its maximum value I_L .
 - Calculate the collector-emitter voltage at the time when the transistor is reverse-biased. [8+8]

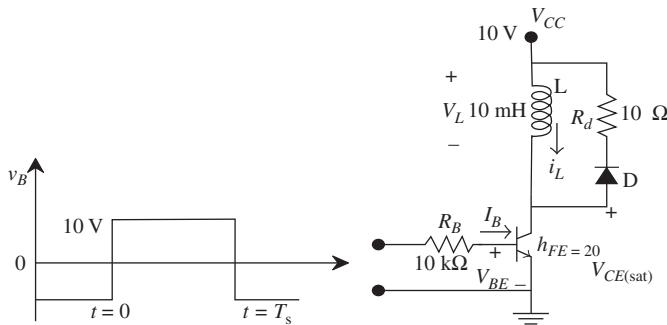


Figure 4 The given current sweep circuit and the input

6. (a) Explain the factors which influence the stability of a relaxation divider with the help of a neat waveforms.
- (b) A UJT sweep operates with a valley voltage of 4 V and peak voltage of 16 V. A sinusoidal synchronizing voltage of 3 V peak is applied as a sync signal. $\eta = 0.5$. If the natural frequency of the sweep is 1 kHz, over what range of sync signal frequency will the sweep remain in 1:1 synchronization with the sync signal. [8+8]
7. (a) What is sampling gate? Explain how it differ from Logic gates?
- (b) What is pedestal? How it effects the output of a sampling gates?
- (c) What are the drawbacks of two diode sampling gate? [6+6+4]
8. (a) Draw and explain the circuit diagram of integrated positive RTL NOR gate
- (b) Compare the RTL and DTL logic families in terms of Fan out, propagation delay, power dissipated per gate and noise immunity. [8+8]

MODEL QUESTION PAPER-III

II B.Tech. I Semester Regular Examinations **PULSE AND DIGITAL CIRCUITS**

(Common to Electrical & Electronics Engineering, Electronics & Communication Engineering, Electronics & Instrumentation Engineering and Electronics & Telematics)

Time: 3 hours

Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks

1. (a) Verify $V_2 = (V/2)(e^{2x} - 1)/(e^{2x} + 1) = (V/2) \tanh x$ for a symmetrical square wave applied to a low pass RC circuit.
 (b) Derive the expression for percentage tilt(P) of a square wave output of RC high pass circuit. [8+8]
2. (a) Give the circuits of different types of shunt clippers and explain their operation with the help of their transfer characteristics.
 (b) Draw the diode differentiator comparator circuit and explain the operation of it when ramp input signal is applied. [8+8]
3. Write short notes on:
 (a) Diode switching times
 (b) Switching characteristics of transistors
 (c) FET as a switch. [4+8+4]
4. (a) Draw the circuit diagram of a Schmitt trigger circuit and explain its operation. Derive the expressions for its UTP and LTP.
 (b) Explain how an Schmitt trigger circuit acts as a comparator. [12+4]
5. (a) Explain the basic principles of Miller and bootstrap time base generators.
 (b) A transistor bootstrap ramp generator is to produce a 15V, 5ms output to a 2kohms load resistor. The ramp is to be linear within 2%. Design a suitable circuit using $V_{cc} = 22V$, $-V_{EE} = -22V$ and transistor with $h_{fe(min)} = 25$. The input pulse has an amplitude of $-5V$, pulse width = 5ms and space width = 2.5ms. [8+8]
6. (a) What is relaxation oscillator? Name some negative resistance devices used as relaxation oscillators and give its applications.
 (b) With the help of a circuit diagram and waveforms, explain the frequency division by an astable multivibrator? [8+8]

- 7.** (a) Why are sampling gates called linear gates?
(b) What are the other names of a gate signal?
(c) Compare the unidirectional and bi-directional sampling gates. [6+4+6]
- 8.** (a) Why totem pole is used in DTL? Draw the circuit diagram and explain a DTL gate with this.
(b) Verify the truth table of RTL NOR gate with the circuit diagram of two inputs. [8+8]

MODEL QUESTION PAPER-IV

II B.Tech. I Semester Regular Examinations PULSE AND DIGITAL CIRCUITS

(Common to Electrical & Electronics Engineering, Electronics & Communication Engineering, Electronics & Instrumentation Engineering and Electronics & Telematics)

Time: 3 hours

Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks

1. (a) What is the function of a comparator? Explain its operation.
 (b) Explain the response of a low pass circuit to an exponential input is applied.
 (c) Explain the response of RL circuit when a rectangular pulse is applied [4+6+6]
2. (a) For the circuit shown in figure 5, V_i is a sinusoidal voltage of peak 100 volts. Assume ideal diodes. Sketch one cycle of output voltage. Determine the maximum diode current.

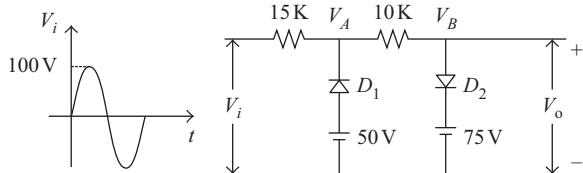


Figure 5

3. (b) Explain positive peak clipping with reference voltage. [12+4]
3. Write short notes on:
 - (a) Diode switching times
 - (b) Switching characteristics of transistors
 - (c) FET as a switch [4+8+4]

4. In the monostable circuit of the given figure 6 the resistor R is connected to an auxiliary supply V_1 instead of V_{YY} . If A_2 is in saturation or clamp and if A_1 is OFF in the stable state, verify that the gate time T is given by Eq. $T = \tau \ln(V_{YY} + I_1 R_Y - V\sigma) / (V_{YY} - V\gamma)$ with V_{YY} replaced by V_1 . [16]

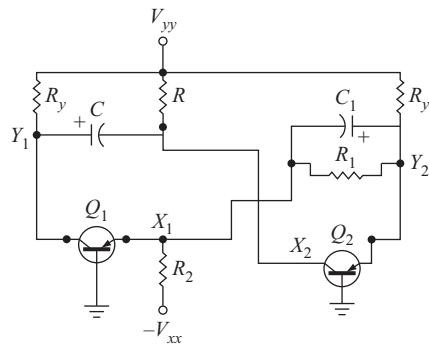


Figure 6

5. (a) How are linearly varying current waveforms generated?

(b) In the boot strap circuit shown in figure 7 $V_{CC} = 25V$, $V_{EE} = -15V$, $R = 10K$ ohms, $R_B = 150K$ ohms, $C = 0.05\mu F$. The gating waveform has a duration of $300\ \mu s$. The transistor parameters are $h_{ie} = 1.1K$ ohms, $h_{re} = 2.5 \times 10^{-4}$ K ohms $h_{fe} = 50$ $h_{oe} = 1/40K$ ohms.

 - Draw the waveform of IC1 and Vo, labeling all current and voltage levels,
 - What is the slope error of the sweep?
 - What is the sweep speed and the maximum value of the sweep voltage?
 - What is the retrace time T_r for C to discharge completely?
 - Calculate the recovery time T_1 and C_1 to recharge completely.

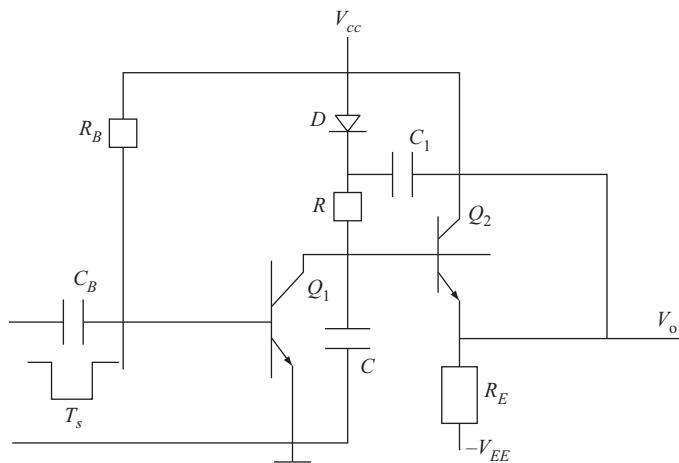


Figure 7

6. (a) Explain how monostable multivibrator is used as frequency divider.
(b) Draw and explain the block diagram of frequency divider without phase jitter. [8+8]
7. (a) Why are sampling gates called linear gates?
(b) What are the other names of a gate signal?
(c) Compare the unidirectional and bi-directional sampling gates. [6+4+6]
8. (a) What are the basic logic gates which perform almost all the operations in digital communication systems.
(b) Give some applications of logic gates.
(c) Define a positive and negative logic systems.
(d) Draw a pulse train representing a 11010111 in a synchronous positive logic digital system. [4+4+4+4]

SOLUTIONS TO MODEL QUESTION PAPER-I

- 1.** (a) Refer Pg. no. 3.19.
(b) Refer Pg. no. 3.34.
- 2.** (a) Refer Pg. no. 4.15.
(b) Refer Pg. no. 4.6.
- 3.** (a) (i), (ii), (iii) Refer Pg. no. 6.21.
(iv), (vi) Refer Pg. no. 6.25.
(v) Refer Pg. no. 6.26.
(b) Refer Pg. nos. 6.21, 6.26.
- 4.** Refer Pg. no. 6.1.
- 5.** (a) Refer Pg. no. 12.21.
(b) Refer Pg. no. 12.3.
(c) Refer Pg. no. 12.6.
- 6.** (a) Refer Pg. no. 15.5.
(b) Refer Pg. no. 15.8.
(c) Refer Pg. no. 15.12.
- 7.** (a), (b) Refer Pg. no. 11.1.
(c) Refer Pg. no. 11.4.
- 8.** Refer Pg. no. 10.18.

SOLUTIONS TO MODEL QUESTION PAPER-II

- 1.** (a) Refer Pg. no. 3.2.
(b) Refer Pg. no. 4.30.
- 2.** (a) Refer Pg. no. 5.26.
(b) Refer Pg. no. 5.27.
- 3.** (a) Refer Pg. no. 6.3.
(b) Refer Pg. no. 6.9.
(c) Refer Pg. no. 6.19.
- 4.** (a) Refer Pg. no. 14.11.
(b) Refer Pg. no. 14.14.
- 5.** (a) Refer Pg. no. 13.1.
(b) Refer Pg. no. 13.10.
- 6.** (a) Refer Pg. no. 15.11.
(b) Refer Pg. no. 15.14.
- 7.** (a) Refer Pg. no. 11.1.
(b) Refer Pg. no. 11.4.
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- 8.** (a) Refer Pg. no. 10.7.
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