Lokesh Subramany, M.S

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Professional Summary

- Engineer with over 12 years in data analysis and machine learning within the semiconductor sector, skilled in leading teams of analysts and developers, adept in project management
- Deep domain expertise in semiconductor data analysis, yield, lithography, statistical process control, and metrology

Skills

Programming: Python, SQL, scikit-learn, PyTorch, imbalance-learn
DataBase: Snowflake,Oracle
Other: Spotfire,Power BI, AWS, Airflow
Domain Expertise: Semiconductor data analysis, Machine learning,

Employment History

Qualcomm/ Senior Staff Engineer
May 2021 - PRESENT, Santa Clara, CA

- Product owner/Lead for an internal data analysis tool; FSDO (Foundry System Data Optimization). My responsibilities include
    - Collaborating with stakeholders from semiconductor test engineering to understand their problem statements and translate them into data analysis use cases
    - Ensuring that data in the data lake is accurate, complete, and analysis-ready
    - Creating mockups/proof of concepts for the model, analysis, and final reports, securing buy-in from stakeholders on the approach
    - Generating detailed requirement and design documents, managing developers distributed across various time zones, to develop the final model, and validating that it meets stakeholder requirements
    - Working with DevOps to deploy the model in the cloud, generate predictions, and monitor the quality of model results.
    - Managing a team of developers to create dashboards for executives to drive decisions based on model outputs.
    - Mentoring interns and junior developers in their professional growth and career development.

- Some examples of ML analyses in FSDO are below

    - Final test parameter prediction:- Applying the Kriging algorithm to generate electrical test data for over 100 chips on a wafer, based on measured data from 13 chips. This data is then utilized to create a model predicting specific final test parameters, estimating the quality of unmeasured wafers.
    - ATPG test data analysis:- ATPG tests fail on specific clock cycles, by analyzing the pattern of these failures we can identify design issues in the chip and correct it, thereby improving yield.
    - Wafer Yield Prediction:- Generating wafer yield predictions from Fab electrical test data. The yield prediction is used to prioritize testing of wafers with lower expected yield. Techniques from the imbalance-learn library were employed to create a model with sufficient quality due to the minority status of wafers with low yield
    - Lean Coverage:- Reduce the number of redundant tests in the test program to improve tester throughput while meeting quality thresholds. This led to a 10% reduction in test time and a savings of over $2M/year

- Subject matter expert for Qualcomm engineers on using Exensio (A custom version of Spotfire) for data analysis of semiconductor metrology and yield data
    - I conduct weekly office hours for users to drop in and seek guidance on conducting specific analyses in Exensio
    - I create libraries of Python scripts for custom analyses and visualizations that can be used by other users
    - I also participate in vendor management, collaborating closely with the tool vendor to assess and implement new features, as well as address any application bugs

Globalfoundries / Principal Engineer

Jan 2017 - May 2021, Malta, NY

- Product owner, team lead and developer for a self service data analysis platform based on C#, Spotfire and Python. The platform was used by 500+ users to extract, analyze, visualize data, and publish their analysis. This project led to a cost savings of 2 million/year
- Developed several machine learning models
    - Pump lifetime prediction:- Time series analysis to predict lifetime of pumps based on sensor data, leading to a savings of $1.5M/year.
    - Virtual metrology:- Use measurement data from previous measurements and tool sensor data to predict measured values at a future step. This led to a 10% reduction in the number of wafers needed to be measured
    - Used Image processing algorithms to classify defect distribution on wafers into different patterns. These patterns can then be used to troubleshoot root cause and improve wafer quality. This reduced the root cause analysis time by 20%.

Globalfoundries / Senior Engineer

SEP 2011 - JAN 2017, Malta, NY

- Led various projects to improve overlay performance on lithography tools. The biggest project involved developing and implementing CPE and dual zone modeling which was a key enabler of 14nm technology in GlobalFoundries
- Improved APC performance for 14nm node by implementing overlay feedforward

- Developed Perl/Python scripts to automate recipe creation on NXT DUV scanners leading to savings of ~20 man hours per week and reducing errors in the scanner recipe by 50%.
- Worked on a project to reduce capex by optimizing sampling on thickness measurement tools leading to savings of 4 million

Aricent / Software Engineer
SP 2006 - JUL 2008, Bangalore

- Worked with customers to understand their requirements and prepared Software Requirement Specification documents for the development team
- Developed new features in SMS (Short Message Service) based on customer requests
- Fixed bugs and ran sanity tests while working with testing teams to ensure code quality is maintained

Education

University of Massachusetts / M.S Electrical and computer engineering
SEP 2008 - SEP 2011, Amherst,MA

Bangalore Institute of Technology / B.E Electronics and communications engineering
JUN 2002 - JUL 2006, Bangalore, India

Select Courses/Certifications

Executive coaching program - Qualcomm

Advanced Learning Algorithms
https://www.coursera.org/account/accomplishments/certificate/MPQK3FHEZRMN

Supervised Machine Learning: Regression and Classification
https://www.coursera.org/account/accomplishments/certificate/6KSTB5BMPV73

Python for Time Series Analysis
https://www.udemy.com/certificate/UC-7bb2cfba-d113-45d3-951e-661d85bcee05/

Select Publications

- Analysis of Wafer Heating in 14nm DUV Layers, SPIE 2016
- Advanced Overlay Sampling and Modeling for Optimized Run-to-Run Control, SPIE2016
- High-volume manufacturing capabilities of run-to-run CPE overlay control, SPIE 2015
- Overlay target selection for 20nm process on A500 LCM, SPIE 2015
- Investigation of trench and contact hole shrink mechanism in the negative-tone develop process, SPIE 2013
- High Order Wafer Alignment for 20nm node Logic Process, SPIE2013
- Detecting Shorts and Open Faults in a Mask Using Lithography Simulation, NATW (North Atlantic Test Workshop), MAY 2010

Patents and trade secrets

- 5 Trade secrets at GLOBALFOUNDRIES
- Patents granted
  - A novel method of Si Pad Formation for metrology measurement on FinFET Wafer, 9,121,890; 9,129,905
  - Systems and methods for fabricating semiconductor device structures, 20150033201
  - Decoupling measurement of layer thicknesses of a plurality of layers of a circuit structure, 14/155,504
  - Planar metrology pad adjacent a set of fins of a fin field effect transistor device, 14/155,504
- Patents pending
  - Adaptive Scatterometry Model Optimization
  - Si Pad Formation for FinFET Wafer
  - Resolution enhancement by filling high reflective index material between mask and projection lens, 20140211175
  - Novel methodology to characterize High-k/Interfacial layer FinFET structure inline