

## JAYPEE UNIVERSITY OF ENGINEERING & **TECHNOLOGY**

A.B. ROAD, P.B. No. 1, RAGHOGARH, DIST: GUNA (M.P.) INDIA **DIGITAL ELECTRONICS (14B11EC317)** TUTORIAL -45

Q.1 Simplify the following Boolean functions together with the don't care conditions using Karnaugh Map:

a) 
$$F(x,y,z) = \sum (2,3,4,6,7)$$
  
 $d(x,y,z) = \sum (0,1,5)$ 

b) 
$$F(A,B,C,D) = \sum (0,6,8,13,14)$$
  
 $d(A,B,C,D) = \sum (2,4,10)$ 

F(A,B,C,D) = 
$$\sum (4,5,7,12,13,14)$$
  
 $d(A,B,C,D) = \sum (1,9,11,15)$ 

c) 
$$F(A,B,C,D) = \sum (4,5,7,12,13,14)$$
 d)  $F(A,B,C,D) = \sum (1,3,8,10,15)$  d  $A(A,B,C,D) = \sum (1,9,11,15)$  d  $A(A,B,C,D) = \sum (0,2,9)$ 

Where d represent don't care condition.

Q.2 Simplify the following Boolean functions using Quine-McCluskey method:

c) 
$$F(x,y,z) = \sum_{x} (0,1,2,5,7)$$

d) 
$$F(A,B,C,D) = \sum (0,1,2,3,5,7,8,9,11,14)$$

Q.3 Draw a NAND logic diagram that implements the complement of the function:  $F(A,B,C,D) = \sum (0,1,2,3,4,8,9,12)$ 

Q.4 Draw a NOR logic diagram that implements following function:  $F(A,B,C,D) = \sum (0,1,3,5,7,9,10,11,12,15)$ 



## JAYPEE UNIVERSITY OF ENGINEERING & **TECHNOLOGY**

Digital Systems & Microprocessor (1811EC311) **TUTORIAL-7** 

## **Topic: Combinational Circuits**

Q.1 Design a combinational circuit with three inputs and one output.

(a) The output is 1 when the binary value of the inputs is less than or equal to 3. The output is 0 otherwise.

(b) The output is 1 when the binary value of the inputs is an even number.

Q.2 A majority circuit is a combinational circuit whose output is equal to 1 if the input variables have more 1's than 0's. The output is 0 otherwise. Design a 3-input majority circuit by finding the circuit's truth table, Boolean equation, and a logic diagram.

Q.3 Design a four-bit combinational circuit 2's complementer. (The output generates the 2's complement of the input binary number.) Show that the circuit can be constructed with exclusive-OR gates. Can you predict what the output functions are for a five-bit 2's complementer?

Q.4 Design a combinational circuit that generates the 9's complement of a BCD digit.

Q.5 Design half adder and half subtractor using five NAND gates only.

## JAYPEE UNIVERSITY OF ENGINEERING & TECHNOLOGY, GUNA TUTORIAL -8, Digital Systems & Microprocessor (18B11EC311) 2023-24

- Q.1 Implement the following Boolean expression using:  $F(A,B,C,D) = \pi(5,6,7,10,11,12,13,14)$
- (b) 16 x 1 Multiplexer b) 8 x 1 Multiplexer c) 4 x 1 Multiplexer
- Q.2 A combinational circuit is defined by the following three Boolean functions:

$$F_1 = x'y'z' + xz$$
  $F_2 = xy'z' + x'y$   $F_3 = x'y'z + xy$   
Design a combinational circuit with decoder and or gates only.

- Q3. Implement the function using 3x8 decoder and OR gate.  $F(w_1, w_2, w_3) = m (0, 1, 3, 4, 6, 7)$
- Q4. Design Full subtracter using suitable
- (ii) Decoder and logic gates. (ii) Multiplexer Q5. Implement using 4x1 Mux, taking B, C as select lines:
  - F(A, B, C) = m(1, 3, 5, 6)
- Q6. Implement the function using suitable decoder: F = ABD +CD +ACD +ABC +ABCD
- Q7. Implement using 8x1 Mux, taking B, C, D as select lines: F(A, B, C, D) = m(0, 1, 3, 4, 8, 9, 15)
- Q8. Implement Full adder using 4x1 Mux.
- Q9. Implement using 8x1 Mux, taking A, C, D as select lines:  $F(A, B, C, D) = \Pi(0, 3, 5, 6, 8, 9, 10, 12, 14)$
- Q.10 Construct 5x32 decoder with the help of suitable number of 3x8 line decoder and 2x4 line decoder.
- Q.11 Implement 16x1 Mux using 8x1, 4x1, and 2x1 Mux.
- Q12. Implement a 4:16 decoder with only 2:4 decoder.

