



Formality SOP



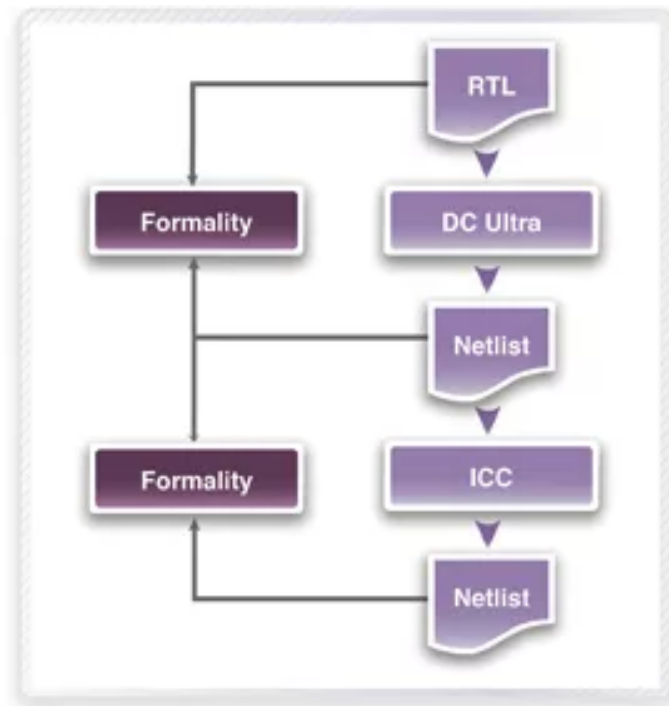
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三大用途： Logic Equivalence 驗證、Low power design 驗證、ECO 驗證

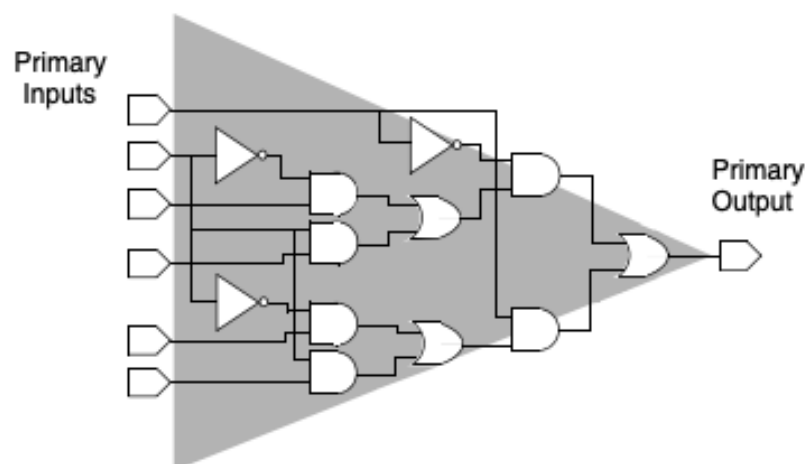
相關 tool： LEC conformal (Cadence)

驗證對象： RTL vs Post-Synthesis, Post-Synthesis vs post-APR ,
ECO_RTL vs ECO_APR



驗證時機： 合成有做 Retiming、設計有 Pipeline、APR 有做 ECO 等等

驗證方法： 設定多個 Compare point，每個 Compare point 中間可以框出一塊 Logic cones，比較此區域是否邏輯等價



Compare point :

BBpin : Black-box pins

Loop : loop compare point

BBNet : Black-box-resolved multiply-driven nets

Cut : Cut-points (You can cut the net and add compare point by yourself)

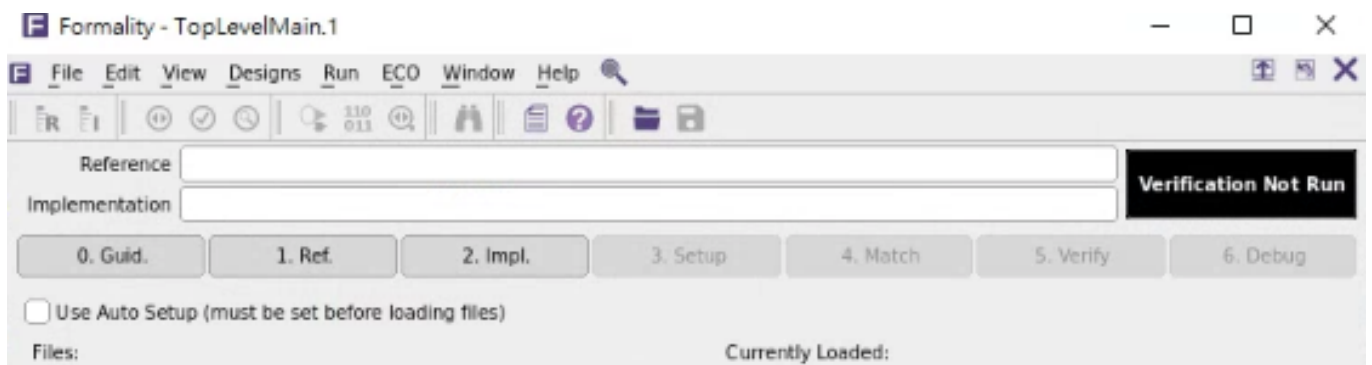
Port : Primary input & output

DFF : Register

LAT : Latch

Flow :

0.Guidance → 1.Reference → 2.Implement → 3.Setup → 4.Match → 5.Verify



*此份 SOP 以指令說明為主，GUI 介面非常簡單，自行隨意按一按即可

0. Guidance

引入 SVF 檔(Setup Verification for Formality)

此檔為使用 design compiler 合成時產生的檔案，紀錄合成過程中 change name 等等行為，避免比較 RTL vs post-syn 時 compare point unmatched

```
set synopsys_auto_setup true           #在引入 svf 前設定
set_svf -append { /home/louis/svm/default.svf }  #引入 svf
report_guidance -summary
report_svf_operation -summary -status rejected
#若 unmatched point 過多，可以查詢 guidance 是否很多被 reject
```

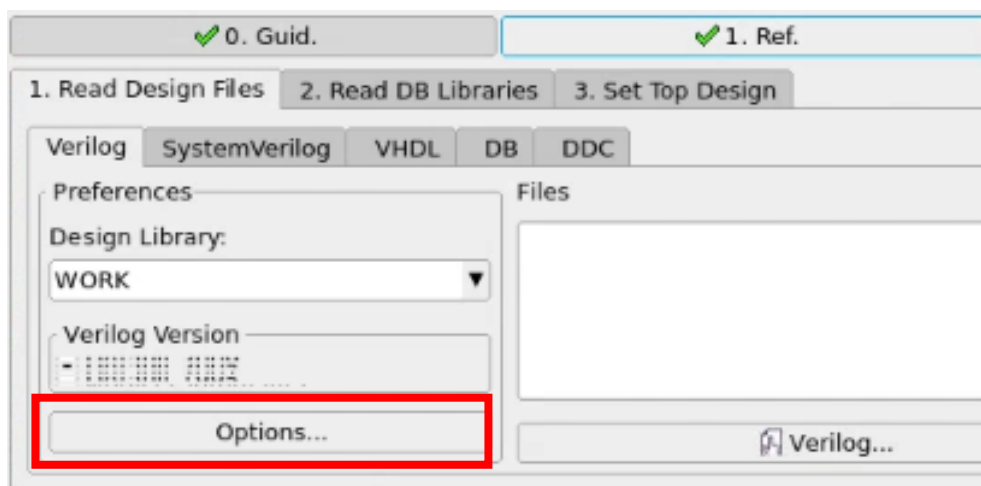
***** Guidance Summary *****						
		Status				
Command		Accepted	Rejected	Unsupported	Unprocessed	Total
change_names	:	0	0	0	378	378
environment	:	1	0	0	6	7
scan_input	:	0	0	0	1	1
uniquify	:	0	0	0	22	22
Total	:	1	0	0	407	408

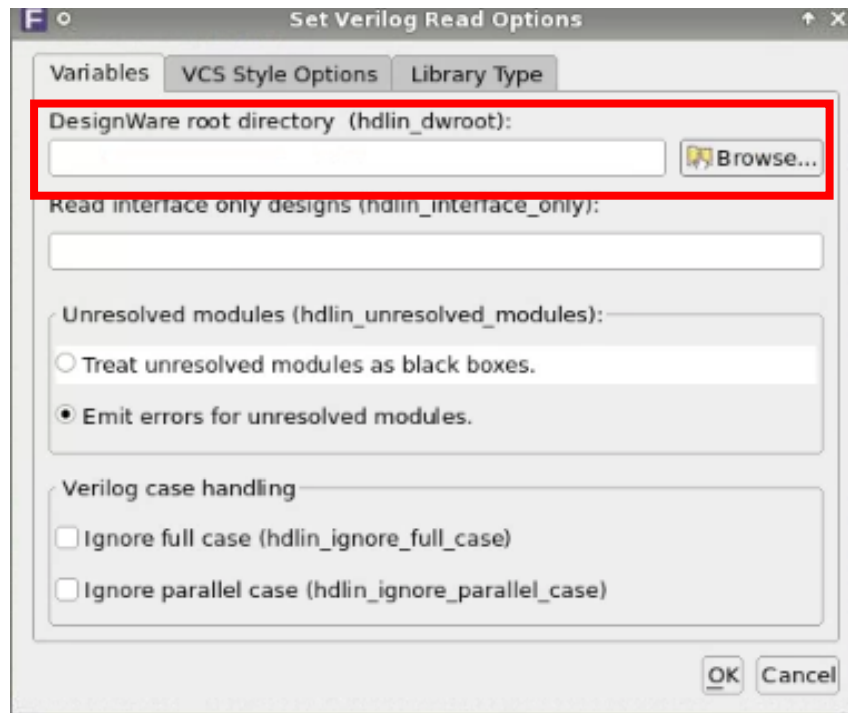
Note: If verification succeeds you can safely ignore unaccepted guidance commands.

Guidance summary

1. Reference

```
set top_module_name top
set hdlin_dwroot /usr/cad/synopsys/synthesis/cur
#有使用 DesignWare 合成請設定此行
read_verilog -container r -libname WORK -05 { /home/louis/svm/top.v }
read_db {
/usr/cad/CBDK/CBDK_TSMC40_Arm_f2.0/CIC/SynopsysDC/db/sc9_base
_hvt/sc9_cln40g_base_hvt_ss_typical_max_0p81v_125c.db }
#若有使用 Multi-Vt、Macro，自行加入對應的 db 檔路徑
set_top r:/WORK/${top_module_name}    #設定 top
```





第二行指令(對 DW 的設定)，在 GUI 介面中如上圖所示

2. Implement

引入要比較的.v 檔, library 的 db file 在 1.Ref 已設定過則此處無需再設定

```
read_verilog -container i -libname WORK -05  
{ /home/louis/svm/top_syn.v }  
set_top i:/WORK/${top_module_name}
```

3. Setup

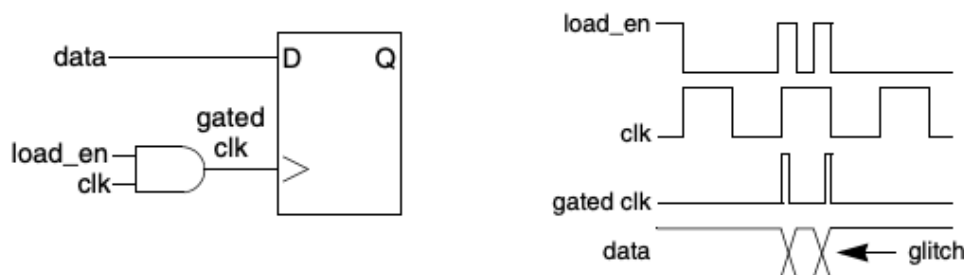
此部分為本 tool 重點，有使用 Clock gating、DFT 都需要特別設定，否則會導致驗證錯誤

```
set verification_failing_point_limit 50  
#tool 預設超過 20 的 fail point 就會自動停止，更改停止條件  
Set verification_verify_unread_compare_points true  
# Unread point 指沒有 drive anything 的點，讓 tool 也對其進行驗證，
```

If use clock gating in synthesis

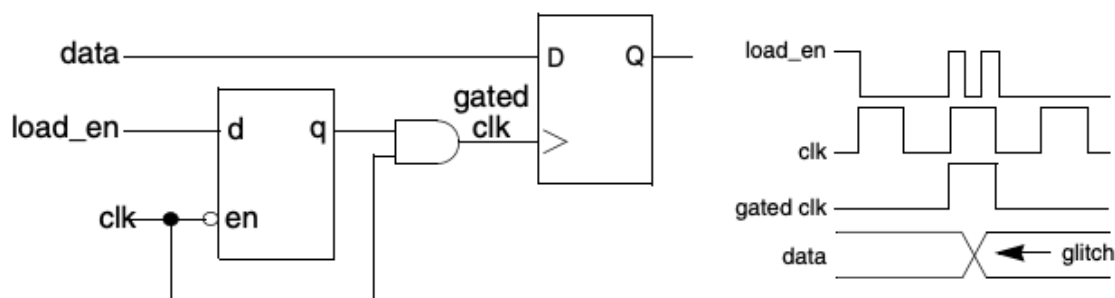
```
set verification_clock_gate_hold_mode low  
#and-based icg 請設 low, or-based icg 請設 high，詳情看下圖
```

Figure 7-8 Combinational Clock Gating Using AND Gate



You see that if glitches occur on the signal `load_en`, invalid data can be loaded into the register. Hence, this circuit is functionally nonequivalent to that in [Figure 7-7](#). In default mode, Formality considers this glitch a possible input pattern and produces a failing point! Formality disregards such a nonequivalence if you set the `verification_clock_gate_hold_mode` variable to `low`.

Figure 7-9 Latched-Based Clock Gating Using AND Gate



During verification, when the `verification_clock_gate_hold_mode` variable is set, Formality recognizes clock-gating latches and takes into account their role in the design under verification.

關於 clock gating 導致 verify 不通過原因可參考此圖

The `verification_clock_gate_hold_mode` variable can have the following values:

- `none` (off) is the default.
- `low` allows clock gating that holds the clock low when inactive.
- `high` allows clock gating that holds the clock high when inactive.
- `any` allows both high and low styles of clock gating to be considered within the same design.
- `collapse_all_cg_cells` has the same effect as the `any` value, in addition, if a clock-gating cell is in the fanin of a register and in the fanin of a primary output port or black box input pin it will be treated as a clock gating cell in all of those logic cones.

如何設定可參考此圖

If insert scan-chain in synthesis

```
set_constant -type port i:/WORK/top/test_se 0
```

If reorder scan-chain in APR(placement)

#將 test_se 角位設 0，告訴 tool 不要驗證 test_si 角位

```
current_design r:/WORK/top
```

```
set t [get_ports -hierarchical test_se]
```

```
set t2 [list [get_ports -hierarchical test_si1] [get_ports -hierarchical  
test_si2] [get_ports -hierarchical test_so1] [get_ports -hierarchical  
test_so2]]
```

```
set_constant -type port $t 0
```

```
set_dont_verify_points $t2 -propagate
```

```
set_constant -type port $t3 0
```

*若比較 post-syn vs post-apr 這邊要在設定一次

```
current_design i:/WORK/top
```

```
set t3 [get_ports -hierarchical test_se]
```

```
set t4 [list [get_ports -hierarchical test_si1] [get_ports -hierarchical  
test_si2] [get_ports -hierarchical test_so1] [get_ports -hierarchical  
test_so2]]
```

```
set_constant -type port $t3 0
```

```
set_dont_verify_points $t4 -propagate
```

*查看設置不進行驗證的點

```
report_dont_verify_points
```

自行增加 compare point

```
set_cutpoint -type POINT_NAME
```

```
report_cutpoint
```

查看使用的 SRAM 等 Macro 及 library

report_black_box

report_libraries -defect all

Low power design 驗證

*此部分需要引入 UPF，驗證時會多兩個 compare point 有興趣者自行研究

load_upf -type NAME

set verification_verify_power_off_status true

Matched Compare Points	BBPin	Loop	BBNet	Cut	Port	PDCut	PGPin	DFF	LAT	TOTAL
Passing (equivalent)	2	0	0	1	66	654	6392	715	0	7830
Failing (not equivalent)	150	0	0	0	0	274	67	0	0	491
Not Compared										
Unread	0	0	0	0	0	259	0	1	0	260

Compare point for low power design

4. Match

Match

此部分進行 compare point 比對，有時 compare point 難免會有不一制，比如:APR 後為了避免 antenna rule 會加入 diode，只要 5.verify 能過就行，但仍然要確認不一致的原因，可參考下圖

Table 6-1 Unmatched Compare Points Action

Symptom	Possible cause	Action
More unmatched points in reference than in implementation design	Unused cells	No action necessary
	full_case directive in RTL code ignored	Set hdlin_ignore_full_case to false.
	Black box created for missing cells	Reread reference design, including the missing cells. Make black box in implementation design.
More unmatched points in the implementation design than in the reference design	Design transformation created extra logic	Account for design transformation; see "Design Transformations" on page 7-28.
	Black box created for missing cells	Reread reference design, including the missing cells. Make black box in reference design.

5.Verify

verify

analyze_points -failing

*return setup stage for adding constraints

setup

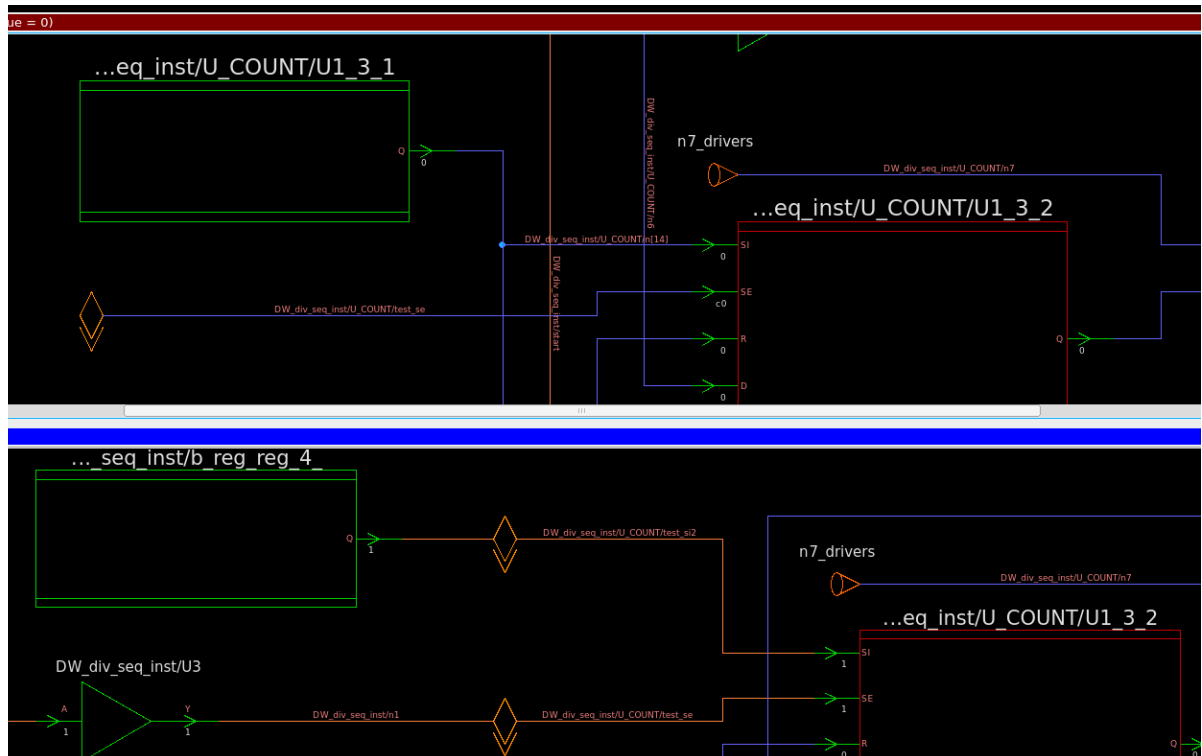
verify -restart

```
***** Verification Results *****
Verification SUCCEEDED
  ATTENTION: synopsys_auto_setup mode was enabled.
             See Synopsys Auto Setup Summary for details.
-----
Reference design: r:/WORK/top
Implementation design: i:/WORK/top
5179 Passing compare points
-----
Matched Compare Points   BBPin   Loop   BBNet   Cut   Port   DFF   LAT   TOTAL
-----
Passing (equivalent)      709      0      0      0      8   4462      0   5179
Failing (not equivalent)    0      0      0      0      0      0      0      0
Not Compared
  Clock-gate LAT                                37      37
*****
```

上圖即表示驗證成功

6.Debug

直接切 failing point 出來，利用 analyze 給出的訊息搭配 gui 介面 debug，藍色和橘色線分別表示接 0 和 1



Description - Unmatched Cone Input:

Unmatched cone inputs result either from mismatched compare points or from differences in the logic within the cones. Only unmatched inputs that are suspected of contributing to verification failures are included in the report.

The source of the matching or logical differences may be determined using the schematic, cone and source views.

Recommendations:

[r:/WORK/top/update w bias2/test se](#)

Matched with pin [i:/WORK/top/update w bias2/test se](#)

Exists in the ref cone but not in the impl cone for 36 compare point(s):

- [i:/WORK/top/update w bias2/acc1 r reg 0](#)
- [i:/WORK/top/update w bias2/acc1 r reg 10](#)
- [i:/WORK/top/update w bias2/acc1 r reg 11](#)
- [i:/WORK/top/update w bias2/acc1 r reg 12](#)