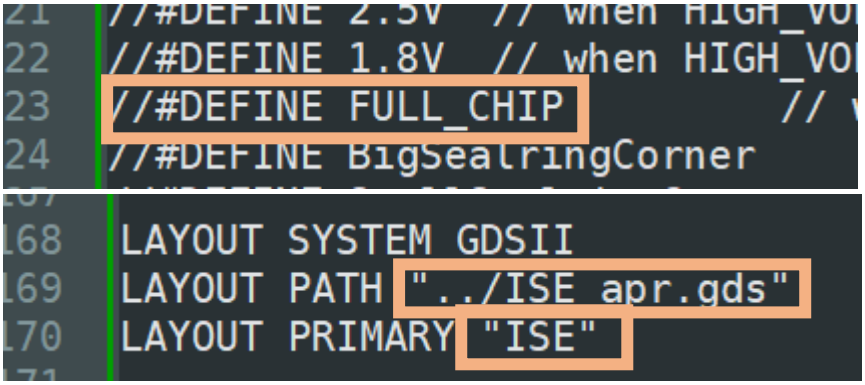
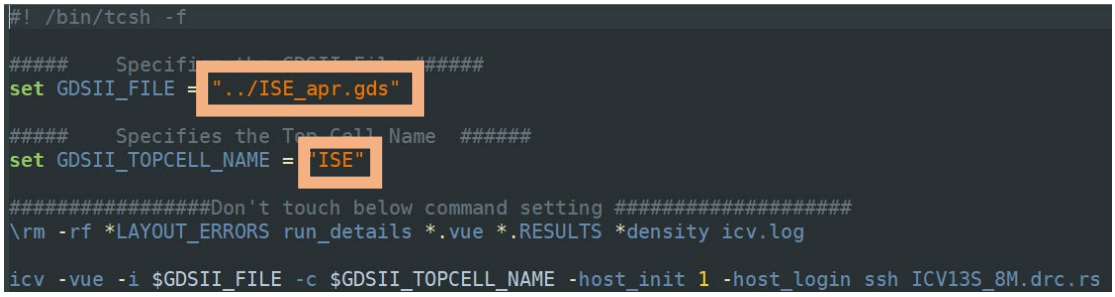
1. 準備：GDS 檔
2. 複製 DRC 檔案，可使用如下指令：
   [1] Calibre： cp -R /cad/CBDK/CBDK_IC_Contest_v2.5/Calibre/drc .
   [2] IC Validator： cp -R /cad/CBDK/CBDK_IC_Contest_v2.5/icv/drc .

3. 修改 DRC 檔案，請先進入 drc 資料夾
   [1] Calibre：
      i. 開啟文檔 CL13S_8M.22d
      ii. 註解第 23 行的#DEFINE FULL_CHIP
      iii. 修改第 169 行的雙引號內容，改為自己的 GDS 路徑
      iv. 修改第 170 行的雙引號內容，改為自己的 TOP MODULE 名稱



   [2] IC Validator
      i. 開啟文檔 run_icv_drc
      ii. 修改第 4 行的雙引號內容，改為自己的 GDS 路徑
      iii. 修改第 7 行的雙引號內容，改為自己的 TOP MODULE 名稱



4. 執行 DRC，使用如下指令：
   [1] Calibre： calibre -drc -hier CL13S_8M.22d
   [2] IC Validator： ./run_icv_drc

5. 確認結果

[1] Calibre： 看畫面中的 TOTAL RESULTS GENERATED 是否為 0

```
Cumulative INSIDE/EXTENT CELL Time: CPU = 0  REAL = 0
Cumulative POLYGON TOPOLOGICAL Time: CPU = 0  REAL = 0
Cumulative POLYGON MEASUREMENT Time: CPU = 0  REAL = 0
Cumulative HOLES Time: CPU = 0  REAL = 0
Cumulative SIZE Time: CPU = 1  REAL = 1
Cumulative EDGE TOPOLOGICAL Time: CPU = 0  REAL = 0
Cumulative EDGE MEASUREMENT Time: CPU = 0  REAL = 0
Cumulative STAMP Time: CPU = 0  REAL = 0
Cumulative ONE-LAYER DRC Time: CPU = 1  REAL = 1
Cumulative ONE-LAYER(A) DRC Time: CPU = 0  REAL = 0
Cumulative TWO-LAYER DRC Time: CPU = 2  REAL = 2
Cumulative NET AREA (RATIO) Time: CPU = 0  REAL = 0
Cumulative DENSITY Time: CPU = 0  REAL = 0
Cumulative SHIFT/GROW/SHRINK Time: CPU = 0  REAL = 0
Cumulative RECTANGLE ENCLOSURE Time: CPU = 0  REAL = 0
Cumulative WITH EDGE Time: CPU = 0  REAL = 0
Cumulative MISCELLANEOUS Time: CPU = 0  REAL = 0
Cumulative CONNECT Time: CPU = 1  REAL = 1
Cumulative RDB Time: CPU = 0  REAL = 0

--- CALIBRE::DRC-H EXECUTIVE MODULE COMPLETED.  CPU TIME = 21  REAL TIME = 22
--
--  TOTAL RESULTS GENERATED = 8 (8)
--                                 ES.db (ASCII)

--- CALIBRE::DRC-H COMPLETED - Sat Apr 22 17:27:54 2023
--- TOTAL CPU TIME = 21  REAL TIME = 22
--- PROCESSOR COUNT = 1
--- SUMMARY REPORT FILE = DRC.rep

[alex@tiffany apr/drc]$
```

[2] IC Validator： 開啟文檔“某某.LAYOUT_ERRORS”，某某為 TOP MODULE 名稱，只要最上面是 CLEAN 即可

```
                  LAYOUT ERRORS RESULTS: CLEAN

                   #### #     #####   ##   #   #
                  #    #     #      #  #  ##  #
                  #    #     ####  ###### # # #
                  #    #     #     #    # #  ##
                   #### ##### ##### #    # #   #

================================================================================

Library name:     ../ISE_apr.gds
Structure name:   ISE
Generated by:     IC Validator RHEL64 R-2020.09-SP3-3.6450417 2021/04/23
Runset name:      ICV13S_8M.drc.rs
User name:        alex
Time started:     2023/04/21 05:31:18PM
Time ended:       2023/04/21 05:31:45PM

Called as: icv -vue -i ../ISE_apr.gds -c ISE -host_init 1 -host_login ssh ICV1

                         ERROR SUMMARY

 BJT.R.1 : RPO needs to cover 0.3 on EM OD edge from
 OD and STI sides
   xor ..................................................... 0 violations found.

 CDU.R.1 : CDUDMY must be inside the assembly
 isolation, beside the seal ring.
   copy .................................................... 0 violations found.
```

6. 看有哪些錯

[1] Calibre： calibre -rve DRC_RES.db

[2] IC Validator： 開啟文檔“某某.LAYOUT_ERRORS”，某某為 TOP MODULE 名稱，查看問題