

# 國立中山大學 SNSD-IC LAB

## IC Compiler (Memory Flow)

### SOP



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# 1. EDA Cloud 使用

## Step-1 取得 EDA Cloud 的登入密碼

進入 CIC 首頁 → EDA Cloud OTP 取得



The screenshot shows the NARLabs CIC homepage. On the left, there is a 'Quick Links' sidebar with several options: '客戶諮詢系統', 'EDA Cloud', 'EDA Cloud OTP 取得' (which is circled in red), '製程服務說明', and '研發成果'. The main content area features a '最新焦點' (Spot Light) section with an illustration of a chalkboard labeled 'E-LEARNING' and a laptop. To the right, there is a '中心公告' (NEWS) section listing various news items, such as U18-105C審查結果報告 and SiGe18-105D梯次下線晶片資料.


The screenshot shows the 'Member Area' login page. The left sidebar has links for '會員登入', '加入會員', '忘記密碼', and '個人資料'. The main form is titled '會員登入 Member Log In' and asks for '您的 E-Mail' (Email) and '輸入密碼' (Password). It includes links for '忘記密碼' (Forgot Password) and '加入會員' (Join Member).

輸入 EDA Cloud 帳號(跟 CIC 申請時的帳號)與信箱，並且按  
“同意並取讀 OTP”

EDA CLOUD帳號 :	<input type="text" value="pw7003"/>
Email :	<input type="text" value="tom@snss.ee.nsysu.edu.tw"/>
本人茲此確認： I hereby confirm that:	
(I) 本人充分明瞭，本人自財團法人國家實驗研究院晶片中心（以下稱「CIC」）EDA Cloud 所取得之資訊（包括但不限於：cell、library 或 PDK 等）屬於 CIC 或某 CIC 協力廠商（例如：台積電（TSMC，即「台灣積體電路製造股份有限公司」））之機密資訊（Confidential Information）。 I fully understand that the information I may obtain from the National Chip Implementation Center of National Applied Research Laboratories ("CIC") through the EDA Cloud (including but not limited to: cell, library or PDK) is considered the confidential information of CIC or a certain CIC's supplier (e.g. Taiwan Semiconductor Manufacturing Company Limited, a.k.a. TSMC).	
(II) 本人必須依本人與 CIC 或本人與 CIC 及 CIC 協力廠商所簽訂之保密合約（Nondisclosure Agreement），以合理的注意義務，妥善保護前述之機密資訊，使其不會洩漏予任何未經 CIC 或該 CIC 協力廠商許可之人知悉或使用，且除非 CIC 下單至該 CIC 協力廠商製造本人所設計之積體電路而使用前述之機密資訊外，本人不可為任何其他之目的而使用前述之機密資訊。 I must, in accordance with the nondisclosure agreements that I signed with CIC, or with CIC and a certain CIC's supplier, and with a reasonable standard of care, properly protect such confidential information from being leaked to, or being used by, any person who is not authorized by CIC or such CIC's supplier to have access to such confidential information. I must not make use of such confidential information other than for the purpose of having CIC placing orders to such CIC's supplier for the manufacturing of integrated circuits designed by me.	
(III) 本人充分了解，本人如有違反前述保密合約之相關規定，本人將遭致資訊所有人（例如：台積電）之刑事追訴及民事賠償請求。 I fully understand that I will be subject to criminal prosecution and civil lawsuit initiated by the information owner (e.g. TSMC) if I violate the terms and conditions of the aforementioned nondisclosure agreement.	
<input type="button" value="同意並取得OTP"/>	

到輸入的信箱取得 EDA Cloud 登入密碼

[CIC EDA CLOUD] 使用者登入密碼通知信 收件匣 x



edacloudotp.cic@narlabs.org.tw

寄給 我 ▾

劉岳衡 教授/學生 您好：

您的 EDA CLOUD 使用者登入密碼為 : PVwQE0VZXJ

有效時間至: 2016/11/05 10:04

請您於時效內使用您的帳號及此密碼登入，

如已過期請重新取得登入密碼, 網址為:

<http://140.126.24.42>

請使用 NX Clinet 軟體登入 EDA CLOUD，

登入的 IP 及 PORT 為 [edac2.cic.org.tw:6578](http://edac2.cic.org.tw:6578)

謝謝！

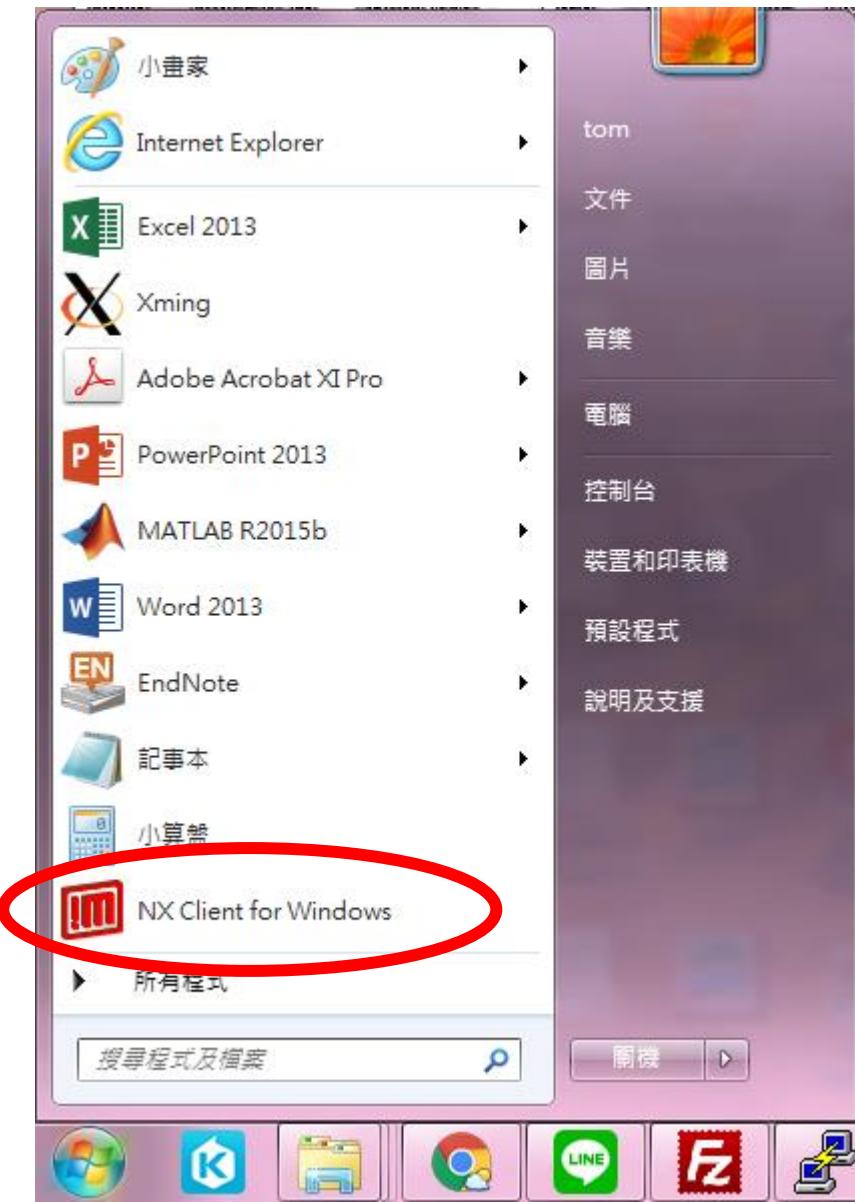
如有任何疑問，請洽諮詢專線：

TEL : (03) 577-3693 ext.885

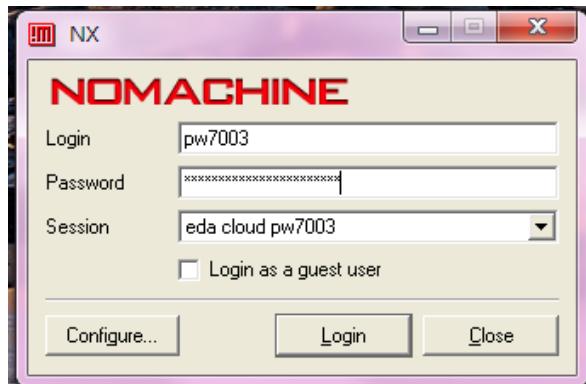
E-mail : [hotline@cic.narl.org.tw](mailto:hotline@cic.narl.org.tw)

## Step-2 進入 EDA Cloud 使用環境

從工作列表中找到 “NX Client for Windows” ，並開啟它



輸入 EDA Cloud 帳號與上一步驟取得的密碼登入



## 順利進入 EDA Cloud 使用環境

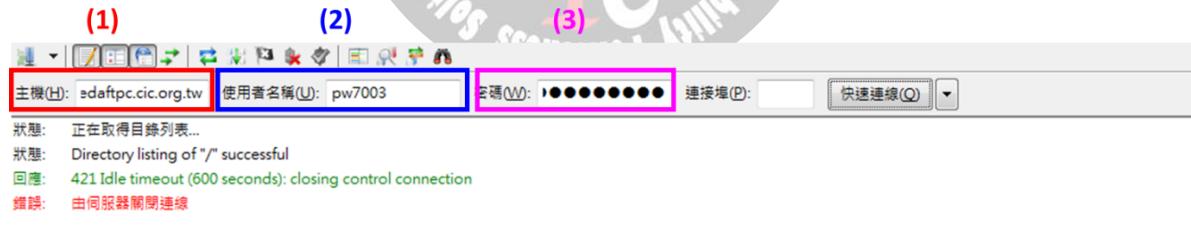


### Step-3 FTP 上傳檔案

請先將要上傳的檔案放入壓縮檔內，並使用 Zip 格式壓縮

#### 開啟 FTP

- (1) 輸入: edaftp.cic.org.tw
- (2) 輸入帳號
- (3) 輸入密碼(CIC 官網取得的 OTP 密碼)



#### 開啟 EDA Cloud 的 Terminal

- (1) 輸入 : ftp edaftpl

```
= lawsuit initiated by the information owner (e.g. TSMC) if I leak any of the =
= information I obtain from the EDA Cloud to anyone without obtaining such =
= information owner's prior written approval, or if I use such information =
= other than for the purposes permitted by such information owner.
=====
FAQ:
==== open firefox failed ====
If you failed open firefox and receive the following messages:
"Firefox is already running, but is not responding ..."
"Your Firefox profile cannot be loaded. It may be missing or inaccessible"
Try fix it by delete ~/.mozilla directory.
Example:
    rm -rf ~/.mozilla
=====
[pw7003@st2318 ~]$ ftp edaftpl
Connected to edaftpl (192.168.70.211).
220----- Welcome to Pure-FTPD [privsep] [TLS] -----
220-You are user number 1 of 50 allowed.
220-Local time is now 20:16. Server port: 21.
220-IPv6 connections are also welcome on this server.
220 You will be disconnected after 5 minutes of inactivity.
Name (edaftpl:pw7003):
```

- (2) 輸入帳號與密碼(CIC 官網取得 OTP 密碼)
- (3) 登入成功後，輸入 :get XXX.zip (XXX.zip 為你上傳的檔案名稱)
- (4) 完成讀取檔案後，立刻輸入 :del XXX.zip (XXX.zip 為你上傳的檔案名稱)
- (5) 輸入 :exit ，退出
- (6) 輸入 :unzip XXX.zip (XXX.zip 為你上傳的檔案名稱) 將檔案解壓縮

## Step-4 FTP 產生 Memory FRAM View-Milkyway

準備檔案

### (1) lef2fram.scm

90nm 路徑:/cad/CBDK/CBDK\_TSMC90GUTM\_Arm\_V1.2/CIC/ICC/ lef2fram.scm

40nm 路徑:

/cad/CBDK/CBDK\_TN40G\_Arm/CBDK\_TSMC40\_core\_Arm\_v2.0/CIC/ICC/  
lef2fram.scm

Memory 的 VClef 檔 (此檔案於 Memory Compiler 產生 Memory 時產生的)

開啟 lef2fram

(1) 為你想產生的 fram 檔的檔名

(2) 直接按照 SOP 內的路徑打

(3) 為你的 VClef 檔路徑位置



TSMC90nm

```

(1) define lib_name "SRAM S4 300 1024"
(2) define tech_file "/CBDK/CBDK_TSMC90GUTM_Arm_v1.2/CIC/ICC/tsmc090_9lm_2thick_cic.tf"
(3) define data_path "./"

cmCreateLib
setFormField "Create Library" "Library Name" lib_name
setFormField "Create Library" "Technology File Name" tech_file
setFormField "Create Library" "Set Case Sensitive" "1"
formOK "Create Library"

cmSetBusNameStyle
formDefault "Set Bus Naming Style"
setFormField "Set Bus Naming Style" "Library Name" lib_name
setFormField "Set Bus Naming Style" "Bus Naming Style" "[%d]"
formOK "Set Bus Naming Style"

read_lef
formDefault "Read LEF"
setFormField "Read LEF" "Library Name" lib_name
setFormField "Read LEF" "Manual Library Prep Mode" "1"
setFormField "Read LEF" "Cell LEF Files" (string-append data_path "/" lib_name ".vclef")
setFormField "Read LEF" "Manual Library Prep Mode" "0"
formOK "Read LEF"

;----;
;Note: Uncomment following to load ANTENNA lef data
;----;

```

TSMC40nm

```

(1) define lib_name "SRAM S3 300M 4"
(2) define tech_file "/cad/CBDK/CBDK_TN40G_Arm/CBDK_TSMC40_core_Arm_v2.0/CIC/ICC/sc9_tech.tf"
(3) define data_path "./"

```

最後於 Terminal 中輸入 :RMilkyway -galaxy -nogui -load lef2fram.scm ,

即可產稱 fram 檔

Note : 若有多顆種類的 Memory 請每次更改 lib name 並產生對應的 fram 檔

## Step-5 APR 流程

### (1). 使用前需準備檔案

- A. 合成後的 Gate Level 檔案 (因為實驗室工作站的版本問題，會導致合成後的檔案在 EDA Cloud 無法使用，因此請使用 EDA Cloud Design Compiler 做合成)
- B. .sdc 檔 (因為實驗室工作站的版本問題，會導致合成後的檔案在 EDA Cloud 無法使用，因此請使用 EDA Cloud Design Compiler 做合成)
- C. Memory 的 .fram 檔 (於上一步驟中介紹如何產生)
- D. Memory 的.db 檔案 (因為版本問題，請使用 EDA Cloud 的 Memory Compiler 產生 Memory 的相關檔案)
- E. 修改過後適用於 EDA Cloud 的 .setup 檔
- F. 修改後的 Gate Level 檔案
- G. I/O Pad 的.tdf 檔
- H. 完成 DFT 後產生的 scandef 檔

### (2). 修改.setup 檔案路徑

#### TSMC90nm 有 Memory 的寫法

此為 EDA Cloud 上的db檔路徑(請照打)

```
set search_path          $search_path
..lib /cad/CBDK/CBDK_TSMC90GUTM_Arm_v1.2/CIC/SynopsysDC/db/
..lib /project/dr158/pw70/pw7003/Layout_6/                         $search_path
set target_library        $search_path
stow.db                  $search_path
fast.db                  此為你自己的Memory db檔路徑
typical.db               (請根據自己放置的位置來設定)
fast_leakage.db
fastZ.db
scx3_tsmc_cln90god_tt_lp26v_0c.db
scx3_tsmc_cln90god_ff_lp26v_125c.db
scx3_tsmc_cln90god_ff_lp26v_m40c.db
scx3_tsmc_cln90god_ss_lp08v_125c.db
scx3_tsmc_cln90god_tt_lp2v_25c.db
scx3_tsmc_cln90god_tt_lp2v_50c.db
typical_leakage.db

SRAM_S3_300M_4_tt_1.0_25.0_syn.db
SRAM_S3_300M_4_ss_0.9_125.0_syn.db
SRAM_S3_300M_4_ff_1.1_125.0_syn.db
SRAM_S3_300M_4_ff_1.1_-40.0_syn.db

SRAM_S4_300_1024_tt_1.0_25.0_syn.db
SRAM_S4_300_1024_ss_0.9_125.0_syn.db
SRAM_S4_300_1024_ff_1.1_125.0_syn.db
SRAM_S4_300_1024_ff_1.1_-40.0_syn.db

SRAM_S4_300_736_tt_1.0_25.0_syn.db
SRAM_S4_300_736_ss_0.9_125.0_syn.db
SRAM_S4_300_736_ff_1.1_125.0_syn.db
SRAM_S4_300_736_ff_1.1_-40.0_syn.db

SRAM_S3_300M_4_tt_1.0_25.0_syn.db
SRAM_S3_300M_4_ss_0.9_125.0_syn.db
SRAM_S3_300M_4_ff_1.1_125.0_syn.db
SRAM_S3_300M_4_ff_1.1_-40.0_syn.db

SRAM_S4_300_1024_tt_1.0_25.0_syn.db
SRAM_S4_300_1024_ss_0.9_125.0_syn.db
SRAM_S4_300_1024_ff_1.1_125.0_syn.db
SRAM_S4_300_1024_ff_1.1_-40.0_syn.db

SRAM_S4_300_736_tt_1.0_25.0_syn.db
SRAM_S4_300_736_ss_0.9_125.0_syn.db
SRAM_S4_300_736_ff_1.1_125.0_syn.db
SRAM_S4_300_736_ff_1.1_-40.0_syn.db

set link_library    ** $target_library dw_foundation.sldb
```

其餘的設定請參閱Memory設定

## TSMC40nm 有 Memory 和 I/O PAD 的寫法

```

set company "CIC"
set designer "Student"
set search_path ".lib /cad/CBDK/CBDK_TN40G_Arm/CBDK_TSMC40_core_Arm_v2.0/CIC/SynopsysDC/db/sc9_base_lvt/ $search_path
..lib /cad/CBDK/CBDK_TN40G_Arm/CBDK_TSMC40_io_TSMC_v2.0/CIC/SynopsysDC/db/ $search_path
..lib /project/dr438/pd35/pd3503/TSMC40/APR "

```

此為40nm的db檔路徑

set target\_library "sc9\_cln40g\_base\_lvt\_ff\_typical\_min\_0p99v\_125c.db  
sc9\_cln40g\_base\_lvt\_ff\_typical\_min\_0p99v\_m40c.db  
sc9\_cln40g\_base\_lvt\_ffg\_typical\_min\_0p99v\_125c.db  
sc9\_cln40g\_base\_lvt\_ss\_typical\_max\_0p81v\_i25c.db  
sc9\_cln40g\_base\_lvt\_ss\_typical\_max\_0p81v\_m40c.db  
sc9\_cln40g\_base\_lvt\_tt\_typical\_max\_0p90v\_25c.db  
tpan45gsgv2od3bc.db  
tpan45gsgv2od3bc1.db  
tpan45gsgv2od3bc2.db  
tpan45gsgv2od3lt1.db  
tpan45gsgv2od3lt2.db  
tpan45gsgv2od3ml1.db  
tpan45gsgv2od3ml2.db  
tpan45gsgv2od3mlg.db  
tpan45gsgv2od3mlg1.db  
tpan45gsgv2od3mlg2.db  
tpan45gsgv2od3tc.db  
tpan45gsgv2od3tc1.db  
tpan45gsgv2od3tc2.db  
tpan45gsgv2od3wc.db  
tpan45gsgv2od3wc1.db  
tpan45gsgv2od3wc2.db  
tpan45gsgv2od3wcl.db  
tpan45gsgv2od3wcl1.db  
tpan45gsgv2od3wcl2.db  
tpan45gsgv2od3wcz.db  
tpan45gsgv2od3wcz1.db  
tpan45gsgv2od3wcz2.db  
tpzn45gsgv2od3bc.db  
tpzn45gsgv2od3lt.db  
tpzn45gsgv2od3ml.db  
tpzn45gsgv2od3mlg.db  
tpzn45gsgv2od3tc.db  
tpzn45gsgv2od3wc.db  
tpzn45gsgv2od3wcl.db  
tpzn45gsgv2od3wcz.db

Logic Gate 的db檔

SRAM\_S3\_300M\_4\_nldm\_tt\_0p90v\_0p90v\_25c\_syn.db  
SRAM\_S4\_300\_736\_nldm\_tt\_0p90v\_0p90v\_25c\_syn.db  
SRAM\_S4\_300\_1024\_nldm\_tt\_0p90v\_0p90v\_25c\_syn.db

I/O Pad 的db檔

Memory 的db檔

### (3). 修改 Gate Level 檔案

#### 1. 找到 IO PAD 的 DOC.，並且確認需使用的 Cell name

TN40G Doc. location :

/cad/CBDK/CBDK\_TN40G\_Arm/CBDK\_TSMC40\_io\_Arm\_v2.0/CIC/doc/tpzn45gsgv2od3\_120a

Technology	TN40G	TN90
Input	PDIDGZ	PDIDGZ_33
Output	PDO02CDG PDO04CDG PDO06CDG : PDO24CDG	PDO02CDG_33 PDO04CDG_33 PDO06CDG_33 : PDO24CDG_33
Corner	PCORNER	PCORNERG_33
Core VDD/VSS	PVDD1DGZ PVSS1DGZ	PVDD1DGZ_33 PVSS1DGZ_33
IO VDD/VSS	PVDD2POC PVSS2DGZ	PVDD2POC_33 PVSS2DGZ_33
Filler	PFILLER20 PFILLER10 PFILLER5 PFILLER1 PFILLER05 PFILLER0005	PFILLER20G_33 PFILLER10G_33 PFILLER5G_33 PFILLER1G_33 PFILLER05G_33 PFILLER0005G_33

#### Input pad



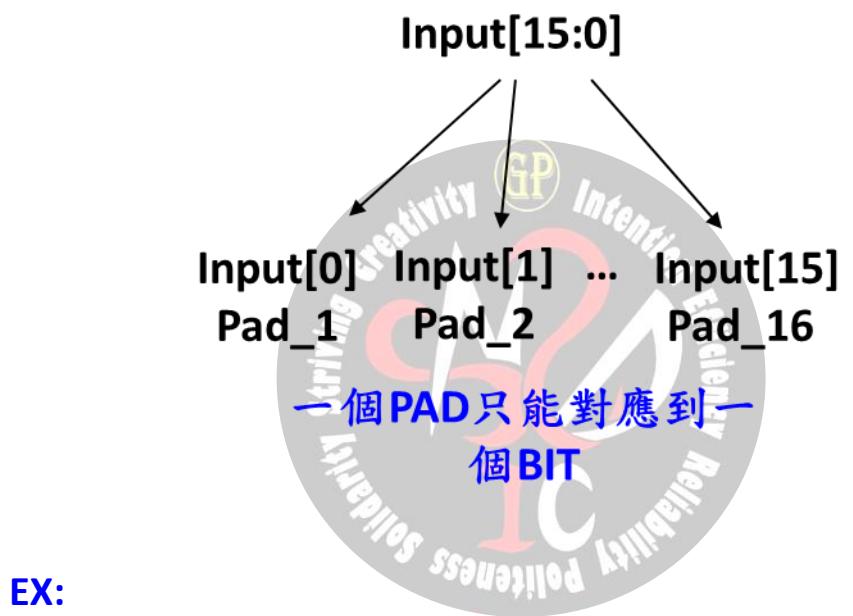
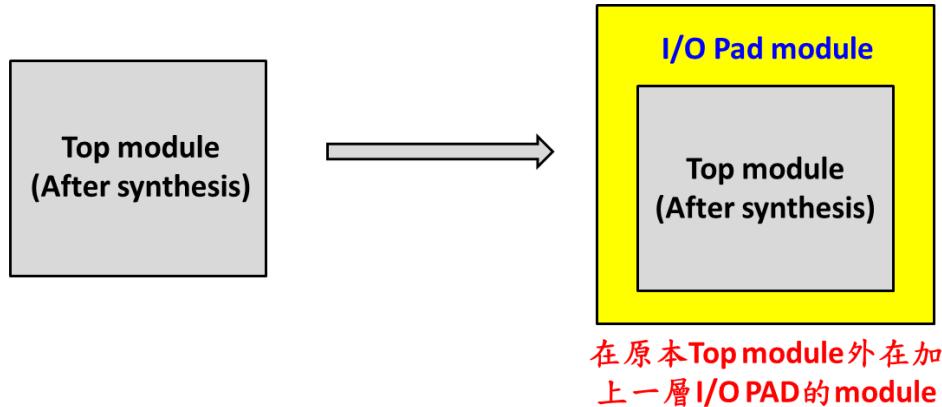
Cell name : PDIDGZ

#### Output pad



Cell name : PDO02CDG, PDO04CDG,  
PDO06CDG, PDO08CDG,... ,PDO24CDG

## 2. 將原本的 Gate Level 檔案在加上一層 I/O PAD 的 module



**EX:**

PDIDGZ	PADI_clk	(.C(clk), .PAD(PI_clk));
PDIDGZ	PADI_reset	(.C(reset), .PAD(PI_reset));
PDIDGZ	PADI_Input_R_0	(.C(Input_R[0]), .PAD(PI_Input_R[0]));
PDIDGZ	PADI_Input_R_1	(.C(Input_R[1]), .PAD(PI_Input_R[1]));
PDIDGZ	PADI_Input_R_2	(.C(Input_R[2]), .PAD(PI_Input_R[2]));
PDIDGZ	PADI_Input_R_3	(.C(Input_R[3]), .PAD(PI_Input_R[3]));

**Cell name      Instance name**

:

## (4). 建立 TDF 檔

建立 TDF 檔之前，必須先計算電路所需 Core VDD/VSS 與 IO VDD/VSS 數量

Core VDD/VSS:

1. 先從 Design Compiler 中查看 Power 並計算相關資訊(Report Power)

```
Global Operating Voltage = 0.9  
Power-specific unit information :  
    Voltage Units = 1V  
    Capacitance Units = 1.000000pf  
    Time Units = 1ns  
    Dynamic Power Units = 1mW      (derived from V,C,T units)  
    Leakage Power Units = 1uW
```

```
Cell Internal Power = 20.1094 mW (75%)  
Net Switching Power = 6.7893 mW (25%)  
-----  
Total Dynamic Power = 26.8986 mW (100%)  
Cell Leakage Power = 5.4236 mW
```

$$\text{Total Power} = 26.90 + 5.42 = 32.32 \text{ mW}$$

$$\text{Total Current} = 32.32 / 0.9 = 35.91 \text{ mA}$$

2. 根據選擇的 Core VDD/VSS 規格並根據 EM Table 去計算所需的數量  
(這裡選擇 PVDD1DGZ 為範例)

$$\begin{aligned}\text{Core VDD Count} &= [\text{Total Current}/\text{Pad EM Value}] \\ &= [35.91/38.25] = [0.94] = 1\end{aligned}$$

$$\text{Core VSS Count} = \text{Core VDD Count}$$

EM Table

Cell Name	6M	7M	8M	9M	10M
PVDD1DGZ	38.25	38.25	38.25	38.25	38.25
PVDD2DGZ	102.18	102.18	102.18	102.18	102.18
PVDD2POC	102.18	102.18	102.18	102.18	102.18
PVSS1DGZ	91.87	91.87	91.87	91.87	91.87
PVSS2DGZ	91.87	91.87	91.87	91.87	91.87
PVSS3DGZ	91.87	91.87	91.87	91.87	91.87
PVDD1ANA	38.25	38.25	38.25	38.25	38.25
PVDD2ANA	94.22	94.22	94.22	94.22	94.22
PVSS1ANA	91.87	91.87	91.87	91.87	91.87
PVSS2ANA	91.87	91.87	91.87	91.87	91.87

Document Location(EDA Cloud): /cad/CBDK/CBDK\_TN40G\_ARM/CBDK\_TSMC40\_io\_TSMC\_v2.0/CIC/doc/tpzn45gsgv2od3\_120a/RN\_TPZN45GSGV2OD3\_130A.pdf

## IO VDD/VSS:

此部份根據設計中 Output 的 IO PAD 規格與 DF Table 去計算所需數量  
(此部分以 31 個 PDO16CDG 為範例)

DF Table		Output Pad	mA				
I/O Type	C	5pF	15pF	30pF	50pF		
02:02mA	2.1nH	0.052	0.039	0.031	0.025	PDO02CDG	2
	5.2nH	0.114	0.075	0.055	0.043	PDO04CDG	4
	7.8nH	0.155	0.097	0.070	0.054	PDO06CDG	6
	10.5nH	0.195	0.118	0.084	0.065	PDO08CDG	8
04:04mA	2.1nH	0.150	0.097	0.071	0.055	PDO12CDG	12
	5.2nH	0.306	0.172	0.119	0.091	PDO16CDG	16
	7.8nH	0.410	0.227	0.152	0.115	PDO24CDG	24
	10.5nH	0.505	0.280	0.184	0.137		
08:08mA	2.1nH	0.373	0.207	0.141	0.107		
	5.2nH	0.699	0.429	0.268	0.194		
	7.8nH	0.914	0.571	0.368	0.259		
	10.5nH	1.214	0.696	0.465	0.324		
12:12mA	2.1nH	0.572	0.355	0.229	0.169		
	5.2nH	1.196	0.709	0.495	0.345		
	7.8nH	1.479	0.951	0.651	0.476		
	10.5nH	2.281	1.237	0.798	0.589		
16:16mA	2.1nH	0.735	0.517	0.359	0.258		
	5.2nH	1.554	1.111	0.715	0.540		
	7.8nH	3.219	1.358	0.940	0.705		
	10.5nH	4.404	1.833	1.213	0.847		
24:24mA	2.1nH	1.153	0.789	0.611	0.483		
	5.2nH	3.444	1.946	1.217	0.885		
	7.8nH	6.064	3.580	1.636	1.218		
	10.5nH	7.284	4.683	2.650	1.405		

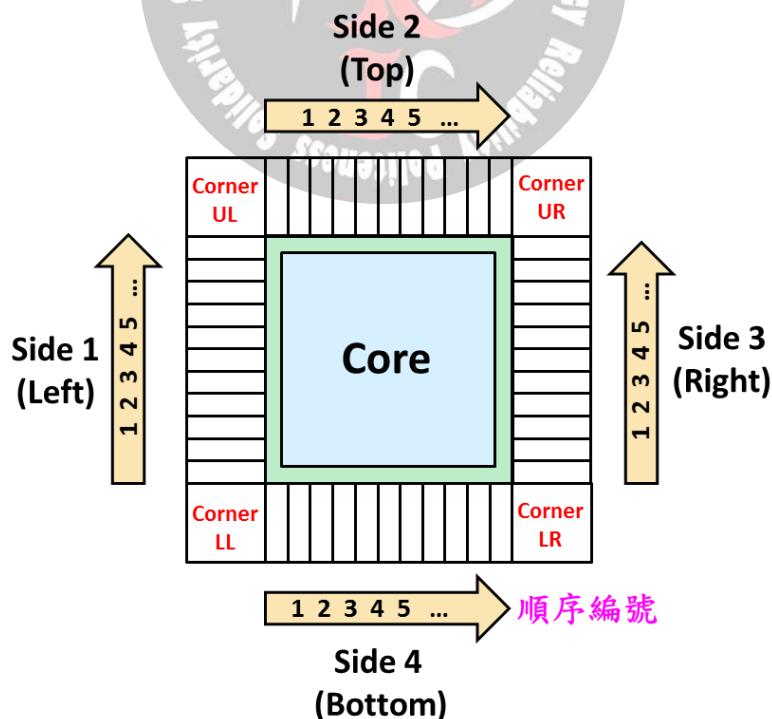
$$\text{Total DF Value} = 31 * 0.54 = 16.74$$

$$\text{IO VDD Count} = [\text{Total DF Value}/1.6] = [16.74/1.6] = 11$$

$$\text{IO VSS Count} = [\text{Total DF Value}/1.5] = [16.74/1.5] = 12$$

在一般情況下會讓IO VDD與IO VSS的數量一致  
=> IO VDD = IO VSS = 12.

接著使用者先自行排列四個邊上所需放置的腳位，排序編號如下：



撰寫 TDF 檔，將排列的順序按照以下格式撰寫

## 1. 設定 Corner 位置

```
set_pad_physical_constraint -pad_name cornerUL -side 1  
set_pad_physical_constraint -pad_name cornerUR -side 2  
set_pad_physical_constraint -pad_name cornerLR -side 3  
set_pad_physical_constraint -pad_name cornerLL -side 4
```

Entry : set\_pad\_physical\_constraint -pad\_name **XXXX** **YYYY**

## 2. 針對四個邊去設定對應的腳位

```
set_pad_physical_constraint -pad_name PADI_Input_R_0      -side 1 -order 1  
set_pad_physical_constraint -pad_name PADI_Input_R_1      -side 1 -order 2  
set_pad_physical_constraint -pad_name PADI_Input_R_2      -side 1 -order 3  
set_pad_physical_constraint -pad_name PADI_Input_R_3      -side 1 -order 4  
set_pad_physical_constraint -pad_name io_vssl           -side 1 -order 5  
set_pad_physical_constraint -pad_name PADI_Input_R_4      -side 1 -order 6  
set_pad_physical_constraint -pad_name PADI_Input_R_5      -side 1 -order 7  
set_pad_physical_constraint -pad_name PADI_Input_R_6      -side 1 -order 8  
set_pad_physical_constraint -pad_name PADI_Input_R_7      -side 1 -order 9  
set_pad_physical_constraint -pad_name core_vssl          -side 1 -order 10  
set_pad_physical_constraint -pad_name PADI_Input_R_8      -side 1 -order 11  
set_pad_physical_constraint -pad_name PADI_Input_R_9      -side 1 -order 12  
set_pad_physical_constraint -pad_name PADI_Input_R_10     -side 1 -order 13  
set_pad_physical_constraint -pad_name PADI_Input_R_11     -side 1 -order 14
```

Entry : set\_pad\_physical\_constraint -pad\_name **XXXX** **YYYY** -order **ZZ**

### Note :

**XXXX** : Pad name  
(Instance name)

**YYYY** : 根據使用者需求設定  
座落在哪個邊上  
(Left: -side 1 Top: -side2  
Right: -side3 Bottom:-side4)

**ZZ** : 順序編號

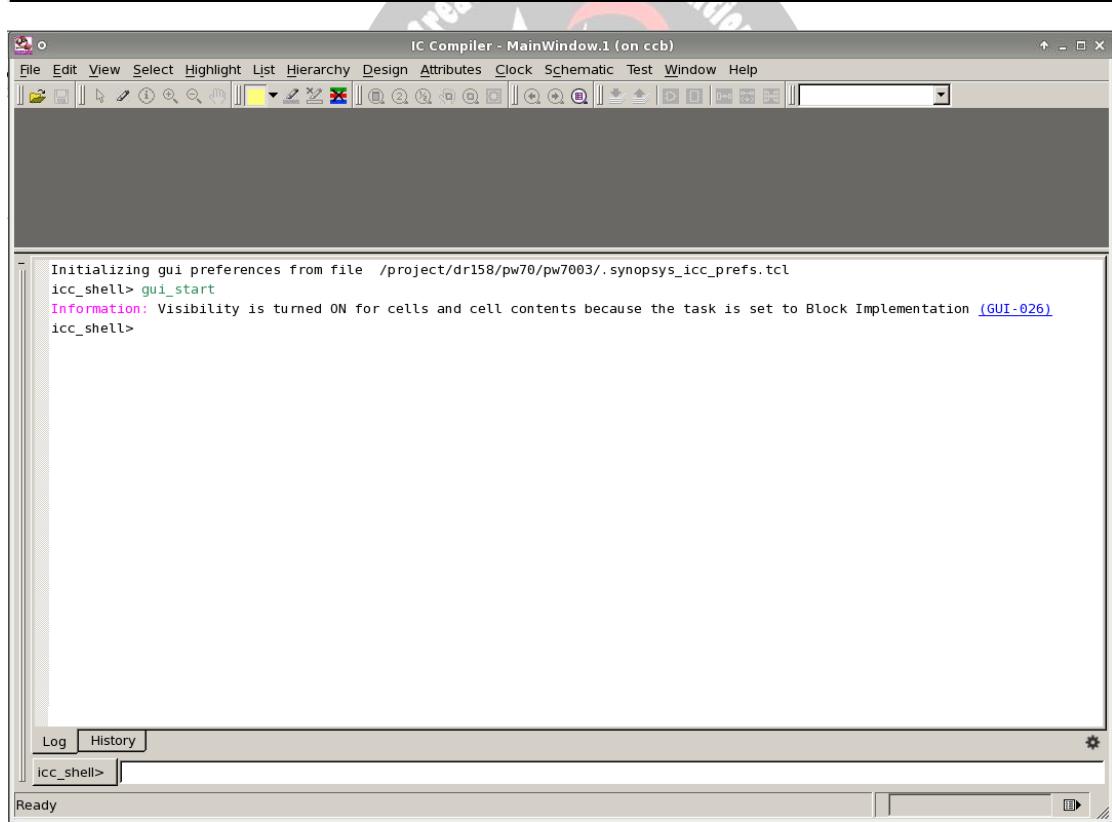
## (5). 進入 IC Compiler

從 Terminal 中輸入: Ricc\_shell -gui

```
=====
= I fully understand that I will be subject to criminal prosecution and civil =
= lawsuit initiated by the information owner (e.g. TSMC) if I leak any of the =
= information I obtain from the EDA Cloud to anyone without obtaining such    =
= information owner's prior written approval, or if I use such information    =
= other than for the purposes permitted by such information owner.          =
=====

FAQ:
==== open firefox failed ====
If you failed open firefox and receive the following messages:
"Firefox is already running, but is not responding ..."
"Your Firefox profile cannot be loaded. It may be missing or inaccessible"
Try fix it by delete ~/.mozilla directory.
Example:
  rm -rf ~/.mozilla
=====

[pw7003@st2318 ~]$ cd Layout_6/
[pw7003@st2318 ~/Layout_6]$ Ricc_shell -gui
```



## (6). 建立 library

File → Create library

(1).請自己設定 Library 的名稱

(2).載入 TF 檔，

90nm 路徑 : /CBDK/CBDK\_TSMC90GUTM\_Arm\_V1.2/CIC/ICC/tsmc090\_9lm\_2thick\_cic.tf

40nm 路徑 : /cad/CBDK/CBDK\_TN40G\_Arm/CBDK\_TSMC40\_core\_Arm\_v2.0  
/CIC/ICC/sc9\_tech.tf

(3).按“Add” 載入 fram 檔，此部份有兩類 fram 檔需要載入，

第一部份是 TSMC 的檔案，

90nm 路徑 :

/CBDK/CBDK\_TSMC90GUTM\_Arm\_V1.2/CIC/ICC/ 路徑內共有四個檔案，  
“tpbn90v” “tpzn90gv3” “tsmc090hvt\_fram” “tsmc090nvt\_fram” 請依序全部  
載入。

40nm 路徑 :

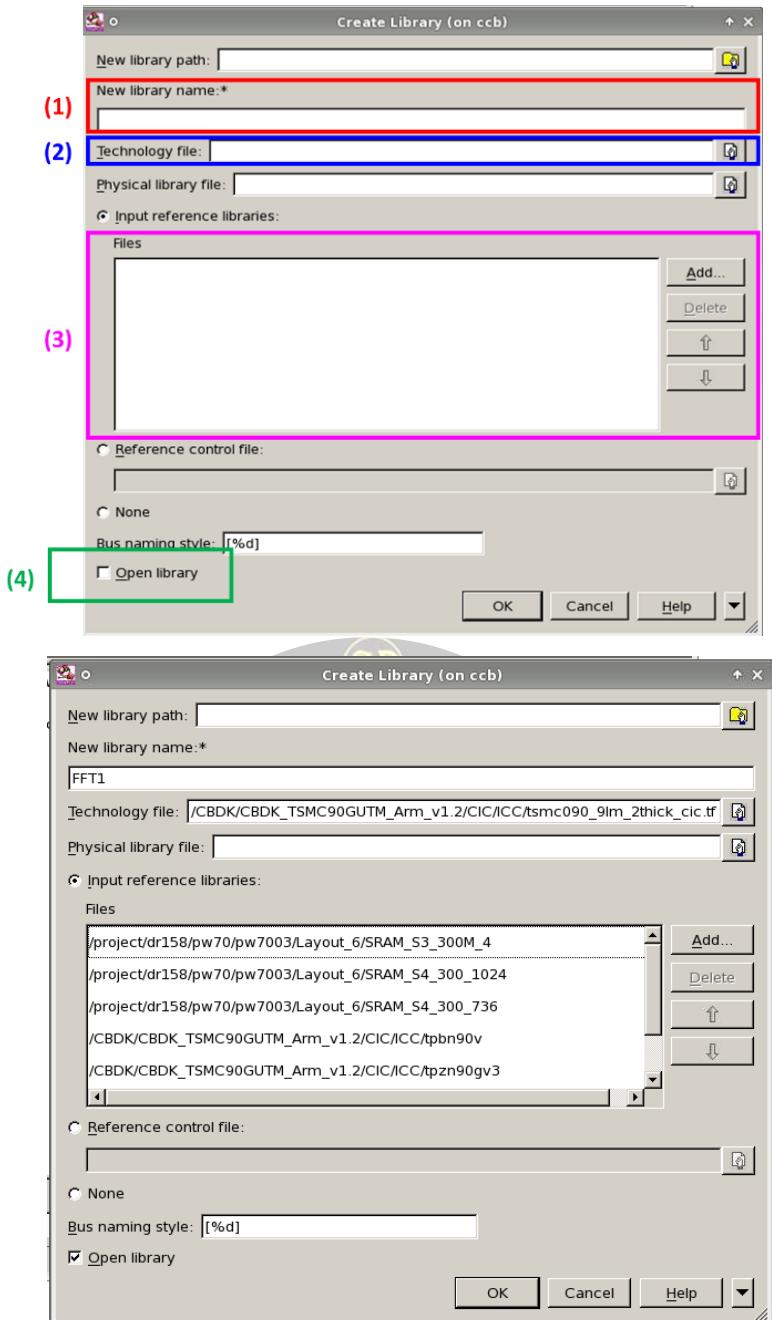
/cad/CBDK/CBDK\_TN40G\_Arm/CBDK\_TSMC40\_core\_Arm\_v2.0/CIC/ICC/  
“sc9\_cln40g\_base\_hvt” “sc9\_cln40g\_base\_lvt” “sc9\_cln40g\_base\_rvt”  
“sc9\_cln40g\_pmk\_hvt” “sc9\_cln40g\_pmk\_lvt” “sc9\_cln40g\_pmk\_rvt”  
請依序全部載入。

有 IO PAD 的話請載入以下檔案

/cad/CBDK/CBDK\_TN40G\_Arm/CBDK\_TSMC40\_io\_Arm\_v2.0/CIC/ICC  
“tpan45gsgv2od3” “tpbn45v” “tpzn45gsgv2od3”  
請依序全部載入。

第二部份是 Memory 的 fram 檔請將所有使用到的 Memory fram 檔全部載入。

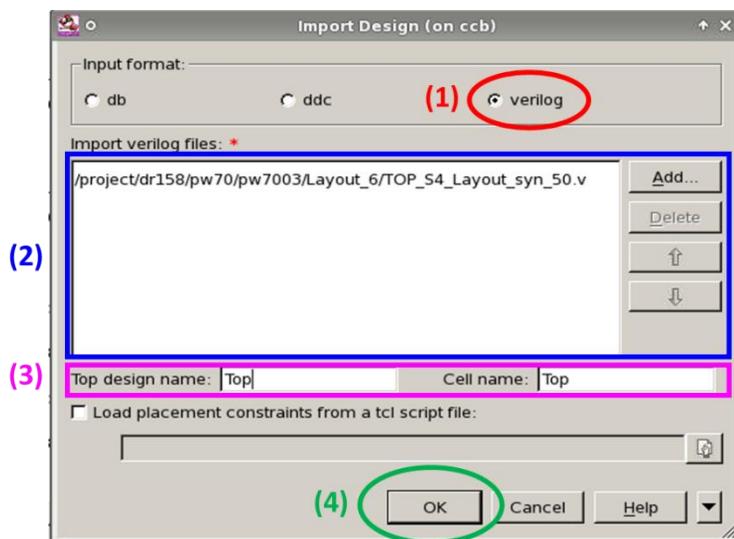
#### (4).Open library 請勾選



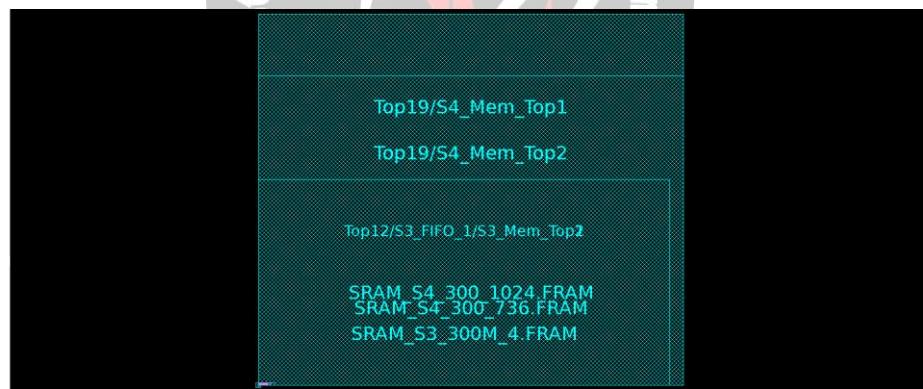
## (7). 載入相關檔案

載入 Gate Level 檔案 “File→ Import Designs ”

- (1).選取 Verilog
- (2).按”Add”，並選取 Gate Level 檔案
- (3).輸入妳的 Code 的 Top module name
- (4)按”OK”

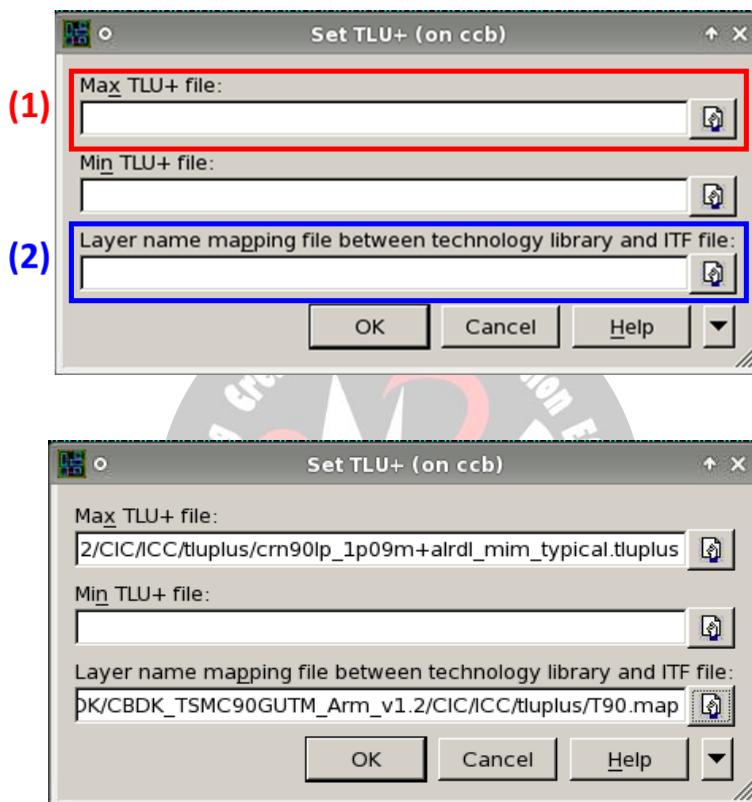


點選完 OK 之後會出現下列的視窗



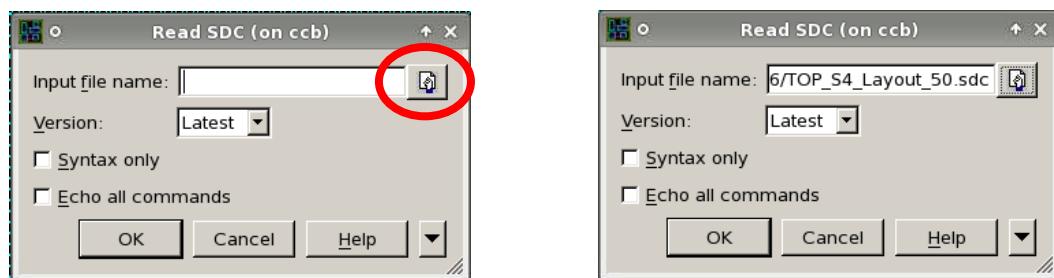
載入檔案 “File→ Set TLU+...”

- (1). 90m 路徑 : /cad/CBDK/CBDK\_TSMC90GUTM\_Arm\_v1.2/CIC/ICC/  
tluplus/crn90lp\_1p09m+alrdl\_mim\_typical.tlu plus  
40m 路徑 : /cad/CBDK/CBDK\_TN40G\_Arm/CBDK\_TSMC40\_core\_Arm\_v2.0/CIC/ICC  
tluplus/typical.tluplus
- (2). 90nm 路徑 : /cad/CBDK/CBDK\_TSMC90GUTM\_Arm\_v1.2/CIC/ICC/ tluplus/T90.map  
40m 路徑 : /cad/CBDK/CBDK\_TN40G\_Arm/CBDK\_TSMC40\_core\_Arm\_v2.0/CIC/ICC  
tluplus/ tluplus.map



載入 SDC 檔案 “File→ Import→Read SDC...”

選取 Input file name，載入妳的 SDC 檔案

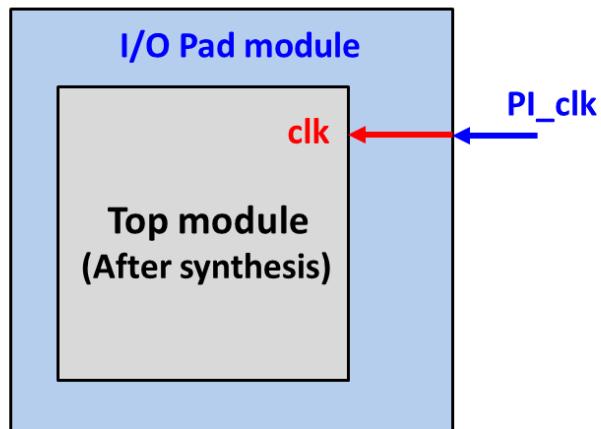


注意：若 clock 的腳位因為增加 I/O Pad 後更改名稱，請自行修改 sdc 檔案內的名稱

```
set sdc_version 2.0

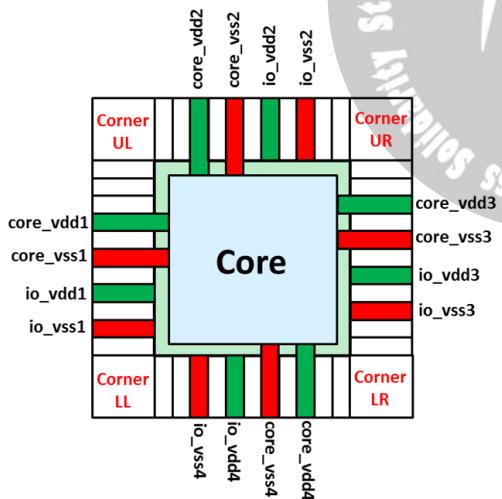
set_units -time ns -resistance kOhm -capacitance pF -voltage V -current mA
create_clock [get_ports PI_clk] -name CLK_0 -period 2.5 -waveform {0 1.25}

clk → PI_clk
```



## (8). 加入 IO 及 Core 的 P/G pad, POC pad 及 Corner pad

請先根據使用者需求計算所需要的 Power Pad 數量



**Core power(core\_vdd & core\_vss) :**

提供 Core 所需的電壓

**Io power(core\_vdd & core\_vss) :**

提供 IO PAD 所需的電壓

在 Message/Input Area 輸入: Create\_cell {Pad\_name} cell name

EX:

```
create_cell {cornerLL cornerUL cornerLR cornerUR} PCORNER
create_cell {core_vdd1 core_vdd2 core_vdd3 core_vdd4} PVDD1DGZ
create_cell {core_vss1 core_vss2 core_vss3 core_vss4} PVSS1DGZ
create_cell {io_vdd1 io_vdd2 io_vdd3 io_vdd4} PVDD2POC
create_cell {io_vss1 io_vss2 io_vss3 io_vss4} PVSS2DGZ
```

## (9). Read TDF file

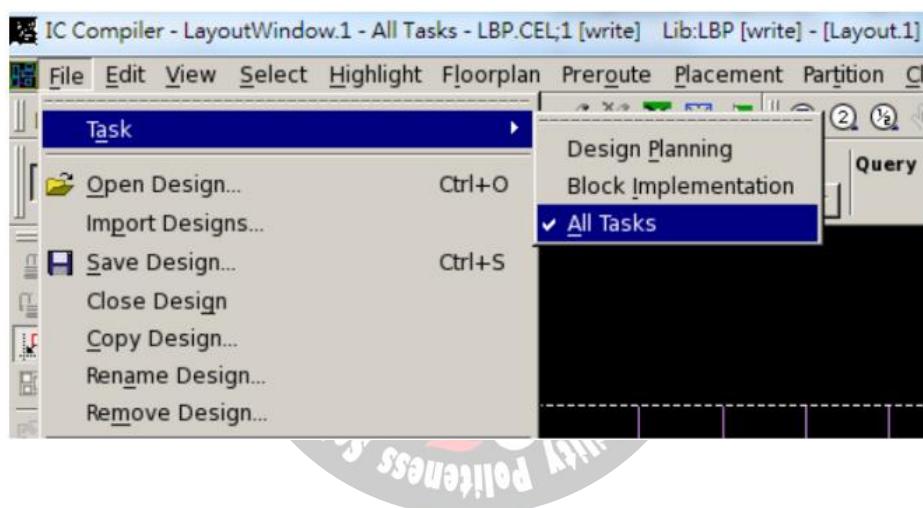
“ Floorplan > Read Pin/Pad Physical Constraints ”

選擇 TDF 檔案位置



## (10). 設定 Core utilization 與設定 Cell 位置

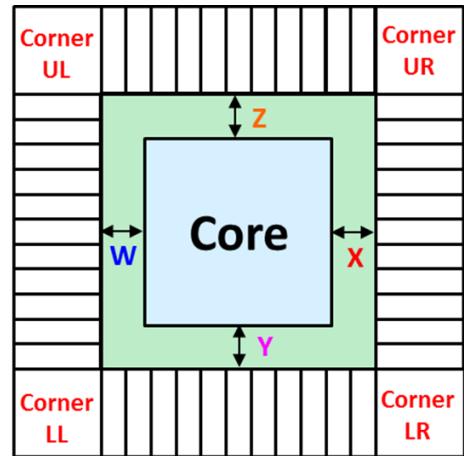
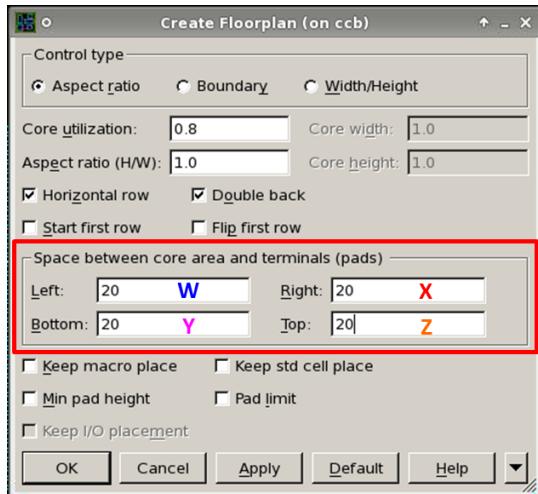
File → Task → ALL Tasks



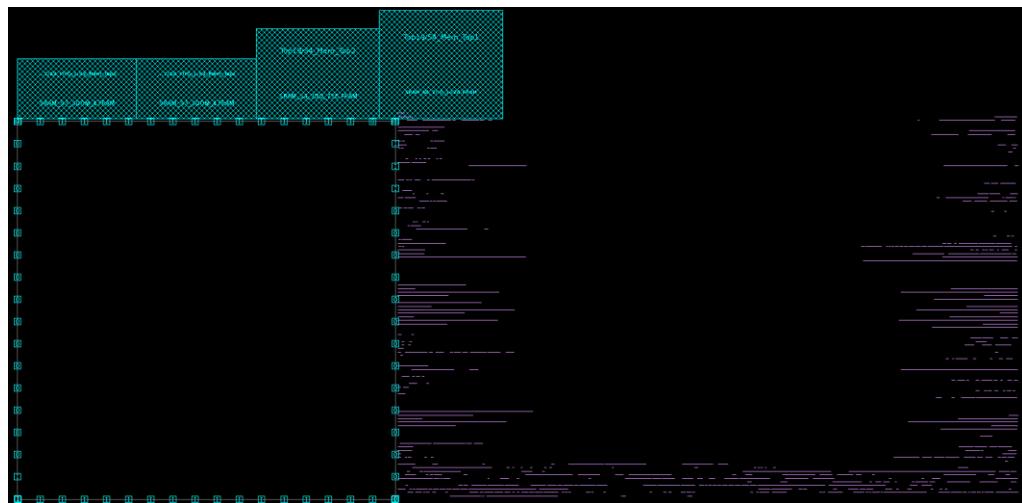
設定繞線比 Floorplan → Create Floorplan...

下圖中的 X W Y Z 為 Core 和 Pad 的距離，根據使用者需求設定

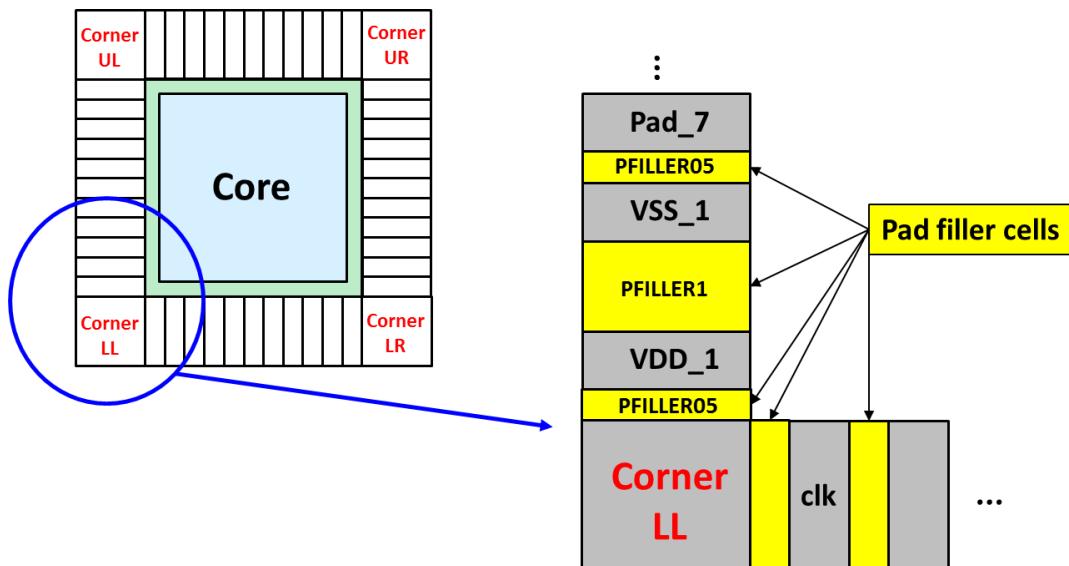
Control type	Aspect ratio
Core utilization	0.6
Aspect ratio (H/W)	1
Horizontal row	Enable
Double back	Enable
Start first row	Disable
Flip first row	Enable

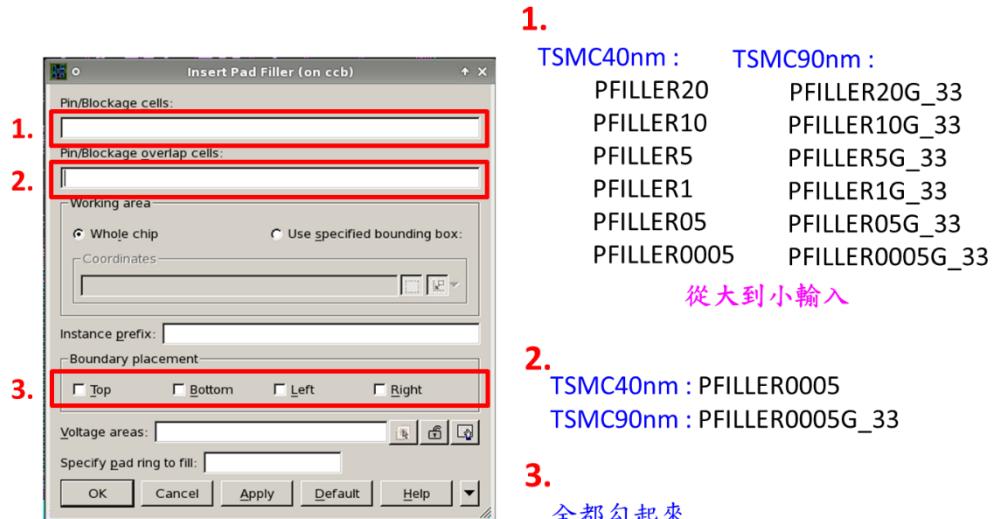


**Core utilization** 是繞線比,為你的電路占整體面積的比例,設定好你所需要的 Core utilization 之後按 OK 會出現下列視窗

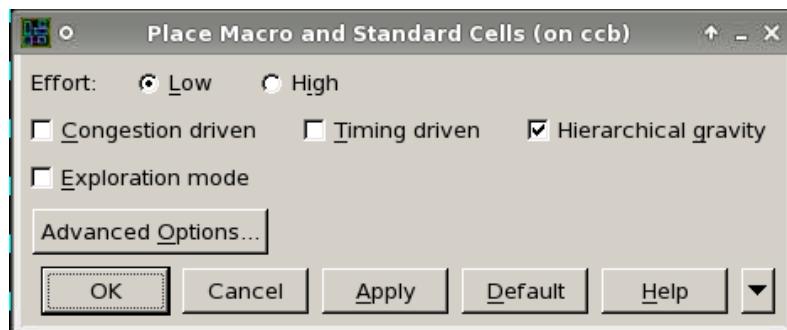


Insert pad filler 位置 “Finishing > Insert Pad Filler”

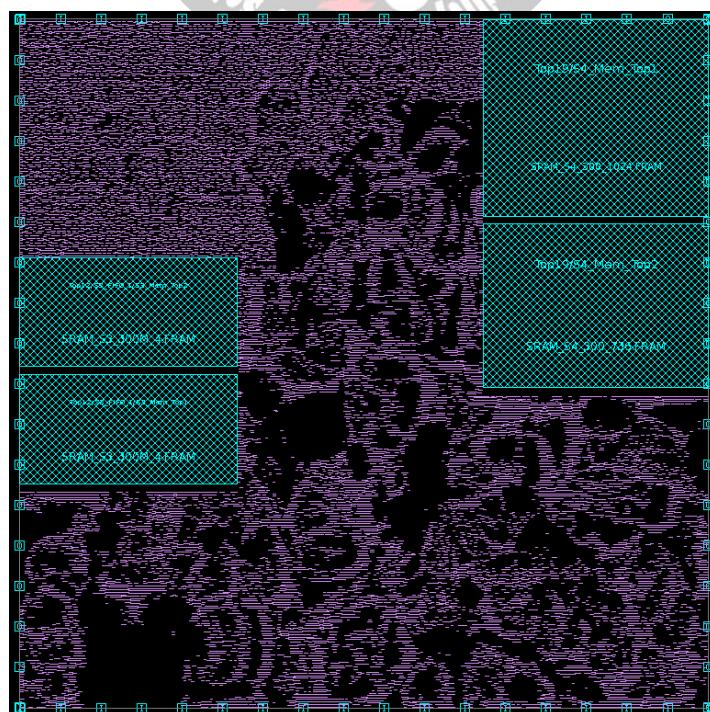




### 自動擺放 Cell 位置 “Placement → Place Macro and Standard Cells”



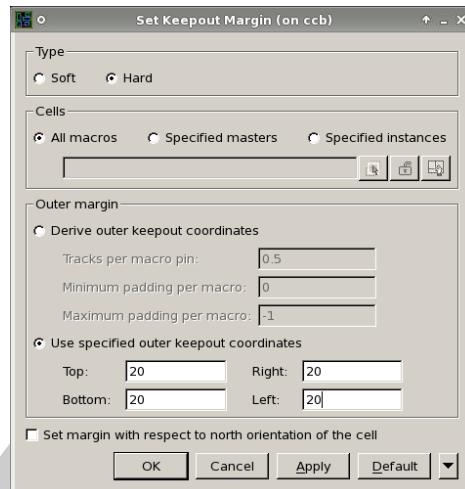
直接按“OK” 就會跑出以下視窗，可以觀察到所有的 Macro 與 Standard Cell 皆放置完成



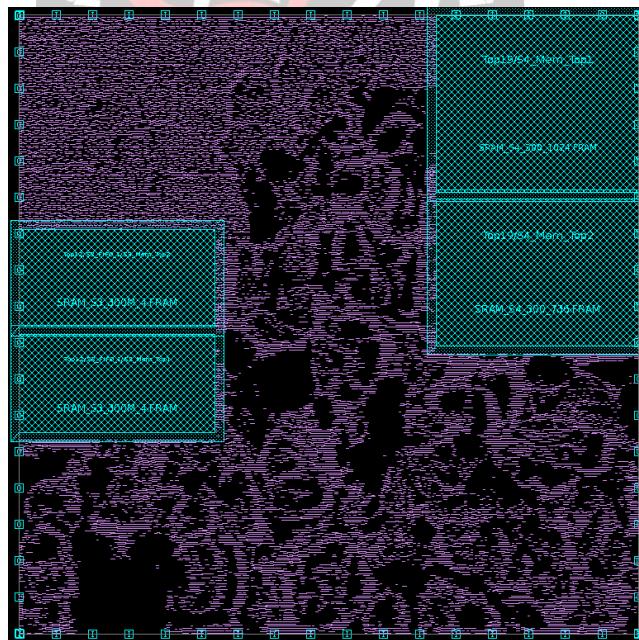
設定所有的 macro 四周圍各 20um 的 keepout margin

“Placement → Set Keepout Margin...” 設定好後按“OK”

Type	Hard
Cell	All macros
Use specified outer keepout coordinates	Top: 20 Right: 20 Bottom: 20 Left: 20



設定好後可以觀察到 Macro 周圍多了一圈 keepout margin



若 macro 不需要更改位置請跳過此步驟，若需要請根據以下步驟設定

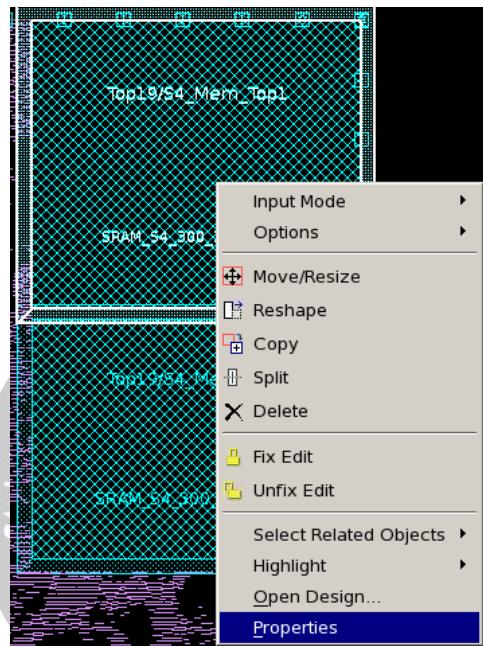
在 Message/Input Area 輸入

“ move\_object -x 000 -y 000 [get\_cells -object\_id XXXXXX] ”

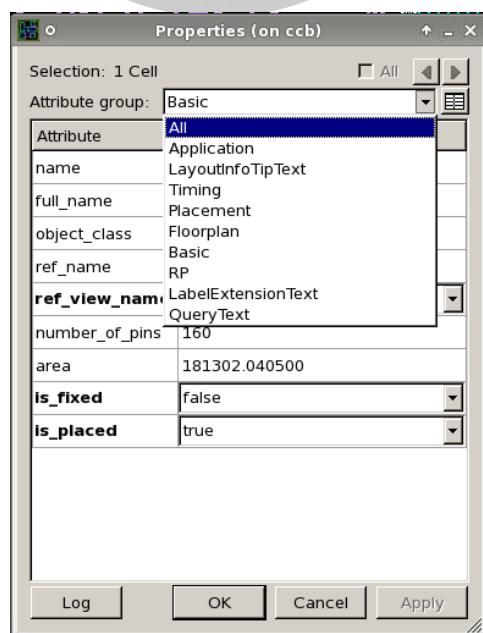
000：分別代表您想把 macro 移到的 XY 座標值 (這部份請使用者自行推算座標值)

XXXXXX：為您想要移動的 macro 編號，編號查詢的方法如下

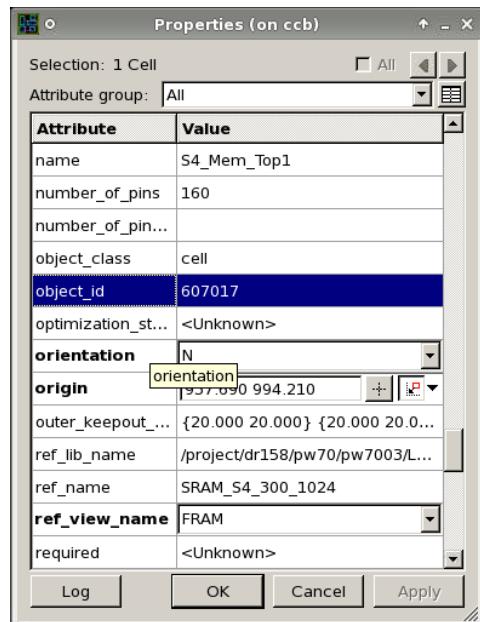
反白你想要查詢的 macro，並且對它按右鍵，選擇 Properties



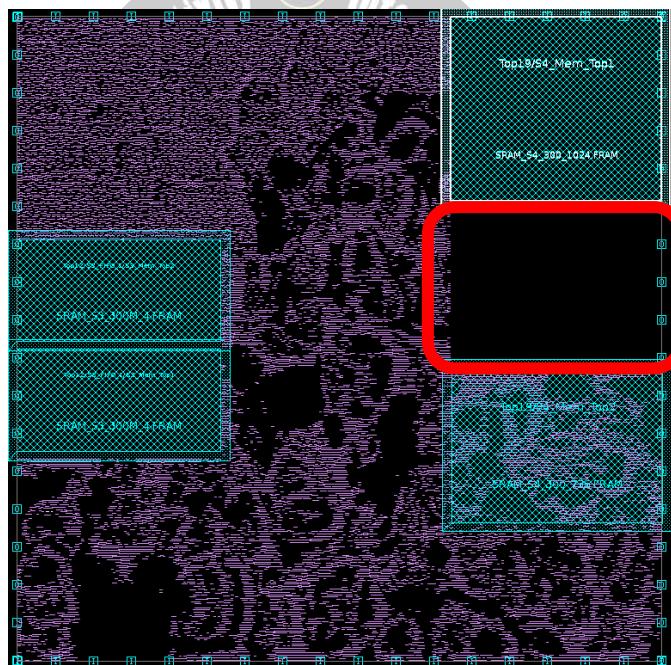
跑出下列視窗後，Attribute group 選擇 All



並往下拉，可以看到一欄 **object\_id**，此為 marco 的 id 編號

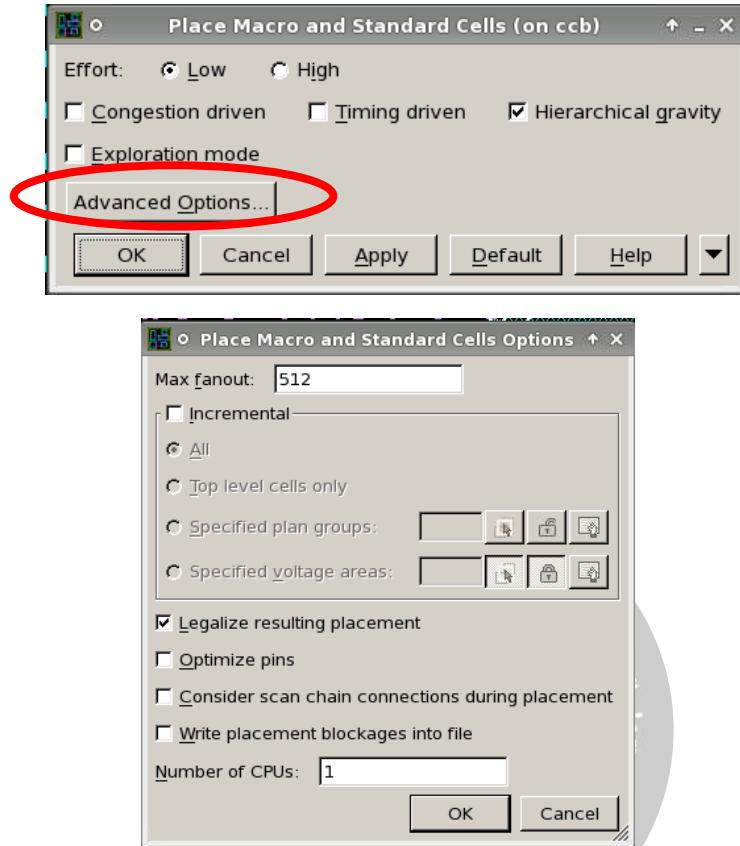


Macro 移動新位置後可以看到原本的位置空出一塊

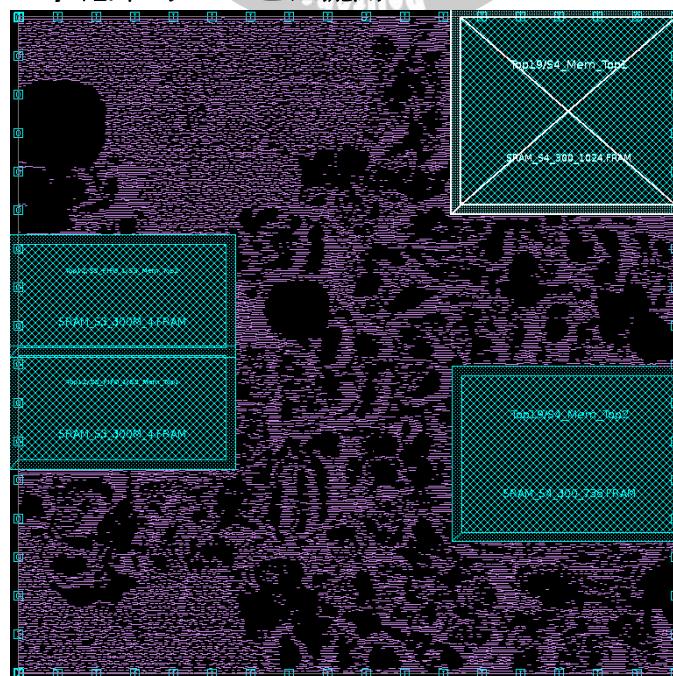


將所有 macro fix 住  
在 Message/Input Area 輸入  
`set_dont_touch_placement [all_macro_cells]`

將 memory 底下的 cell 擺開，載執行一次以下步驟  
自動擺放 Cell 位置 “Placement → Place Macro and Standard Cells  
選取 Advanced Options 後，按“OK”

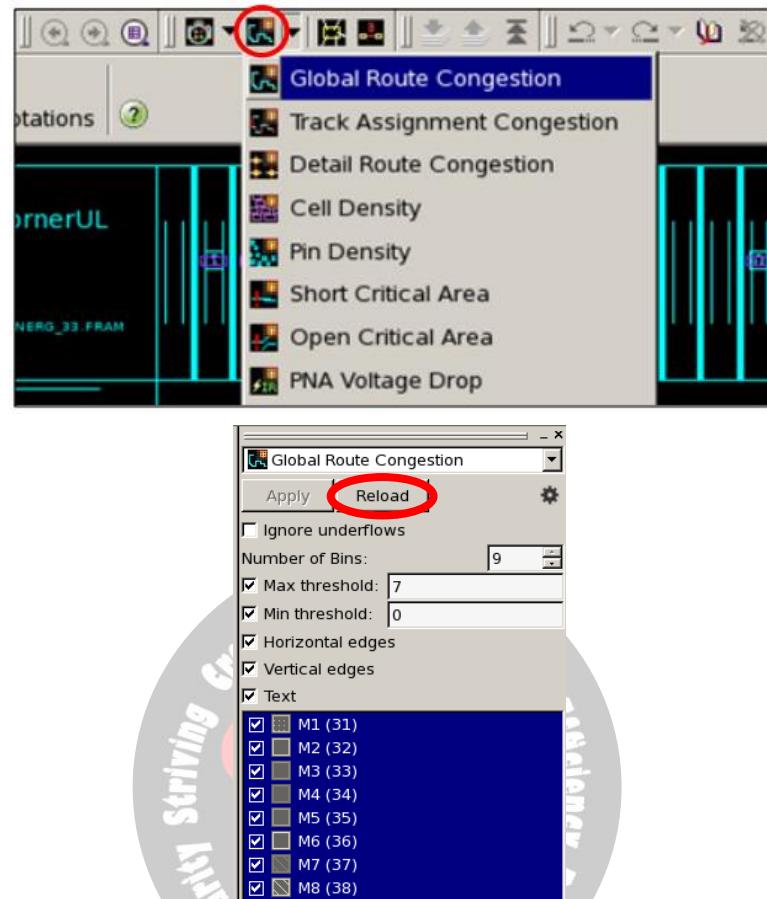


可以觀察到 memory 底下的 cell 已經擺開



## (11). 分析 Congestion 狀態

點選 Global Route Congestion 視窗，再按下 “reload” 在按“OK”，即可觀察



OK, 即可觀察如果皆為 0 以下為最佳狀況

<input checked="" type="checkbox"/>	7	0
<input checked="" type="checkbox"/>	6	0
<input checked="" type="checkbox"/>	5	0
<input checked="" type="checkbox"/>	4	0
<input checked="" type="checkbox"/>	3	0
<input checked="" type="checkbox"/>	2	0
<input checked="" type="checkbox"/>	1	0
<input checked="" type="checkbox"/>	0	0
<input type="checkbox"/>	-39 ... -1	400512
<input type="checkbox"/>	Blocked	0

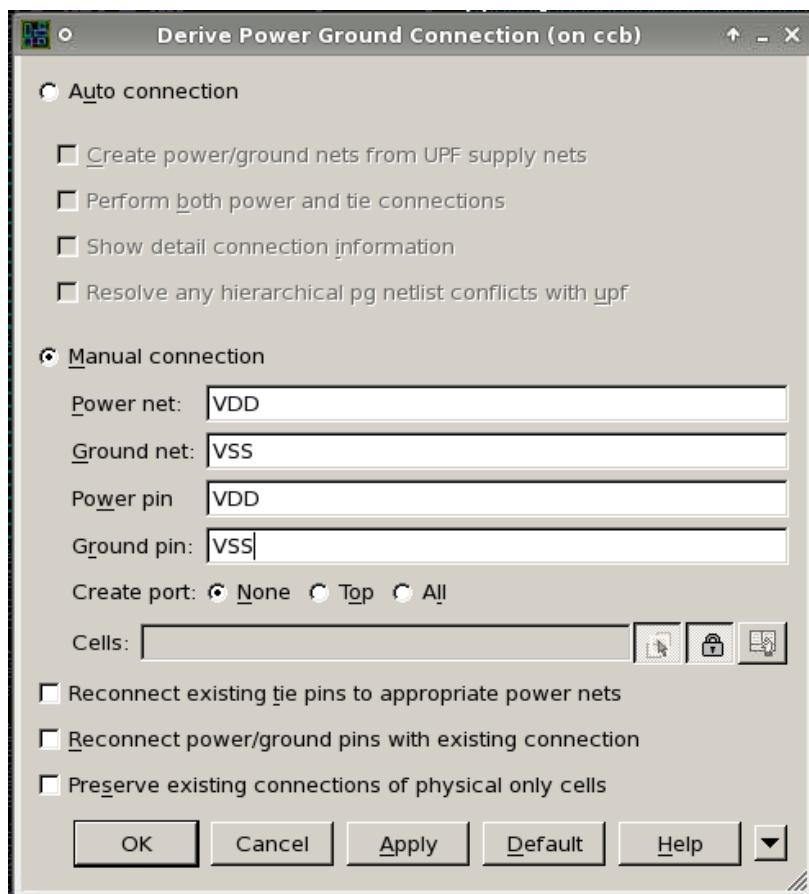
Note: 如果有 congestion 問題，如發生在 macro 附近，可以試著將 keepout margin 加大，或是將 macro 與 macro 之間的距離加大。

## (12). 連接 cell 的 P/G nets

點選 “Preroute → Derive PG Connection” 開啟視窗

Manual connection	selected
Power net	VDD
Ground net	VSS
Power pin	VDD
Ground pin	VSS
Other	Default value

輸入好之後按 “OK”

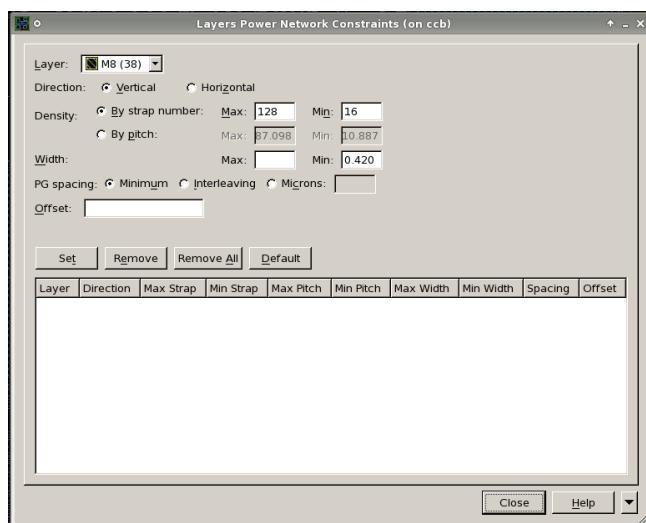


## (13). 設定 PNS Constraints

點選 “Preroute → Power Network Constraints → Strap Layers Constraints” 開啟視窗

TN90		TN40G	
Layer	M4	M5	Layer
Direction	Vertical	Horizontal	Direction
Density (By strap number)	Max: 10 Min: 3	Max: 10 Min: 3	Density (By strap number)
Width	Max: 8 Min: 8	Max: 8 Min: 8	Width

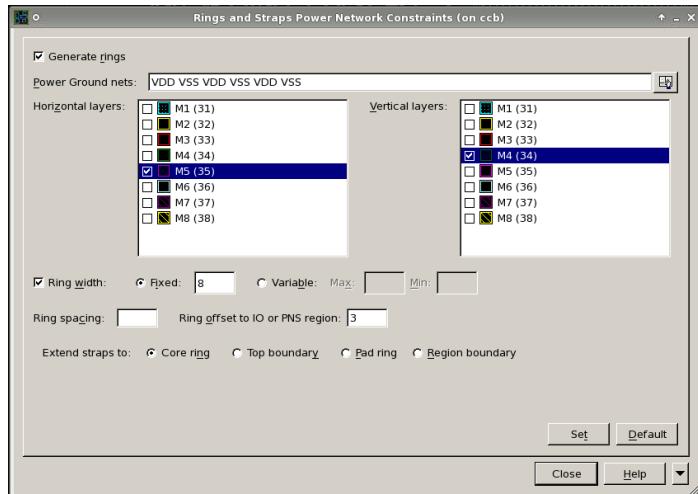
分別依照製程輸入好數值後按“Set”做設定，兩個都設定好後按“Close”退出



點選 “Preroute → Power Network Constraints → Ring Constraints” 開啟視窗

TN90		TN40G	
Power Ground nets	VDD VSS VDD VSS VDD VSS (6圈共3對)	Power Ground nets	VDD VSS VDD VSS VDD VSS (6圈共3對)
Horizontal layers	M5	Horizontal layers	M4
Vertical layers	M4	Vertical layers	M5
Ring width	enable	Ring width	enable
Variable	Fixed (8 um)	Variable	Fixed (4 um)
Ring offset to IO or PNS region	3	Ring offset to IO or PNS region	3
Extend straps to	Core ring	Extend straps to	Core ring

按 Set 後按 Close 離開

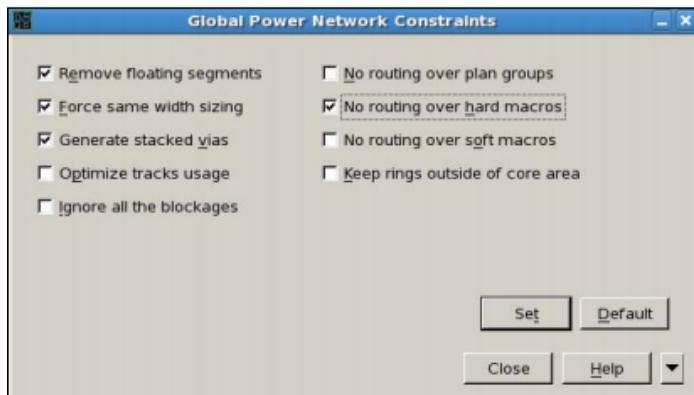


## (14). 自動建立 CHIP 的 Strap 連接

“Preroute > Power Network Constraints > Global Constraints”

No routing over hard macros	enable
Other	Default value

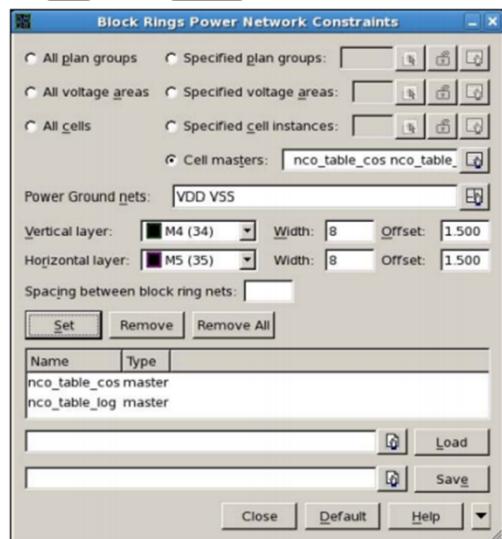
按 Set 後按 Close 離開。



“Preroute > Power Network Constraints > Block Ring Constraints”

Cell master	輸入你使用的Memory Name
Other	Default value
Power Ground nets	VDD VSS
Vertical layer	M4 (Width:8 Offset:1.5)
Horizontal layer	M5 (Width:8 Offset:1.5)

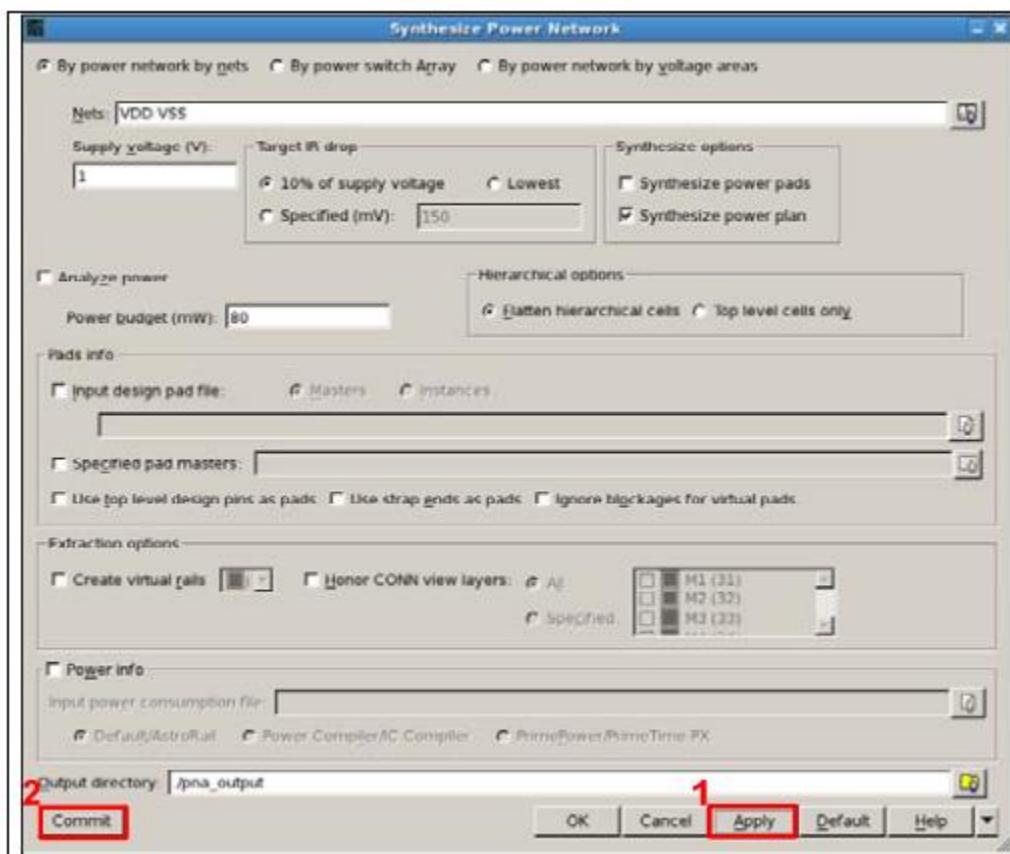
按 Set 後按 Close 離開。



“ Preroute > Synthesize Power Network”

By power network by nets	VDD VSS
Supply voltage	1
Target IP drop	10% of supply voltage
Power budget (mW)	80
Other	Default value

按 Apply 觀察 IR drop map 後，按 Commit 連接 P/G net。

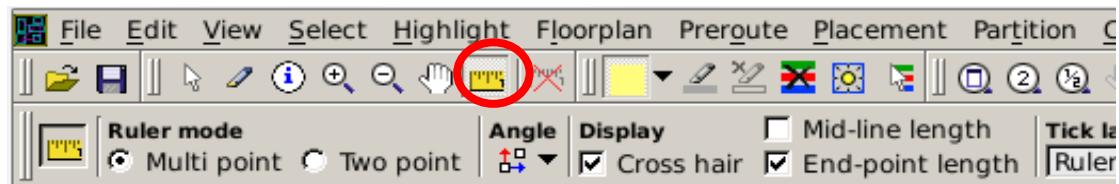


## (15). 手動建立 CHIP 的 Strap 連接

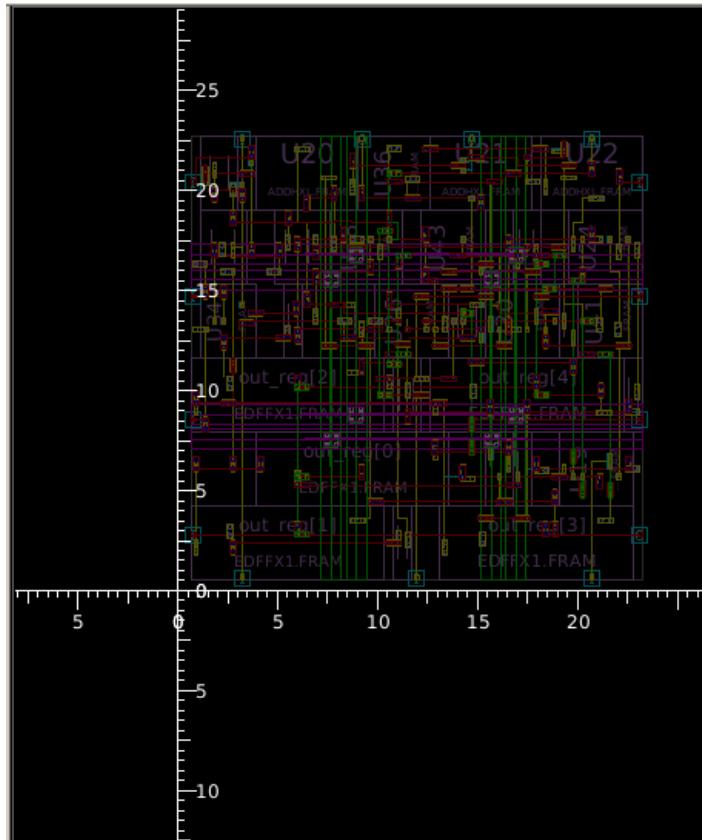
1. 點選 “Preroute → Create Power Straps...” 進入視窗

2. 這裡要對應好 Vertical 要用 M4，Horizontal 要用 M5 與我們設定的 X Y 值，但不能超過 Core 的長跟寬，不然會看不到!! 其他設定就如同下面範例。看你要設定幾條就重覆這個動作幾次，以下範例是水平跟垂直各兩條

3. 點選 Options Gap 設定為 16



可點選上方紅框內的圖式，來協助做 XY 軸的位置計算



Nets : VDD VSS

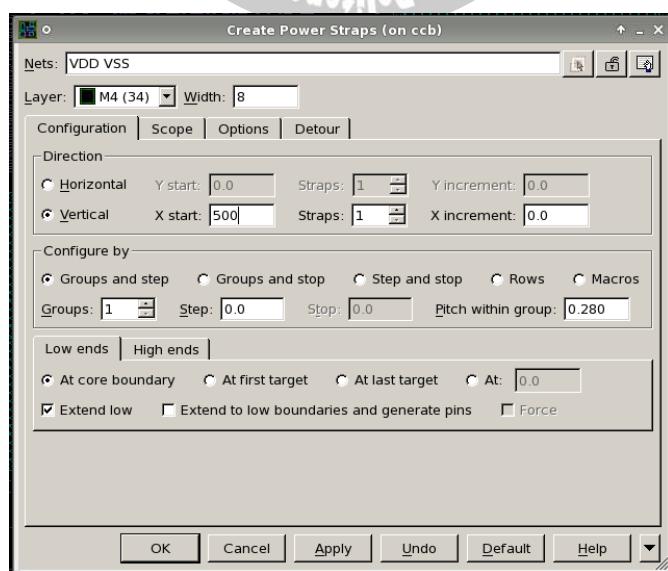
Layer : M4(vertical) , M5 (Horizontal)

Width : 8

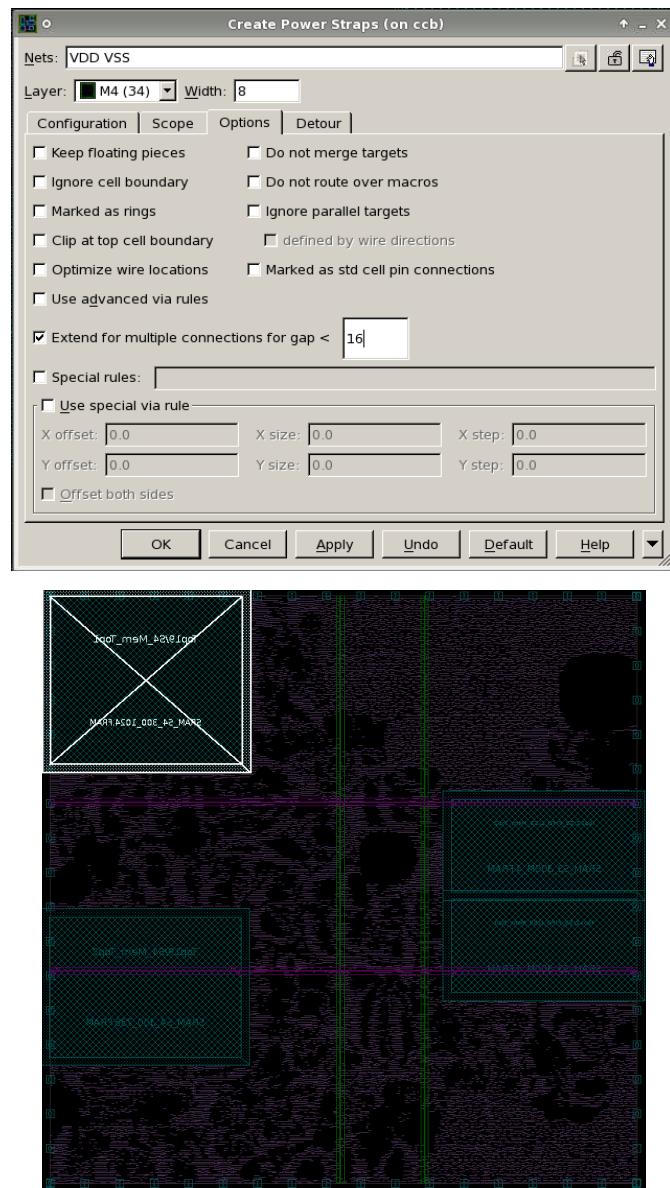
Direction : Horizontal (M5) , vertical(M4)

X start(vertical)請根據你想放的位置輸入座標

Y start(Horizontal)請根據你想放的位置輸入座標



Extend for multiple connections for gap 打勾並且輸入 16

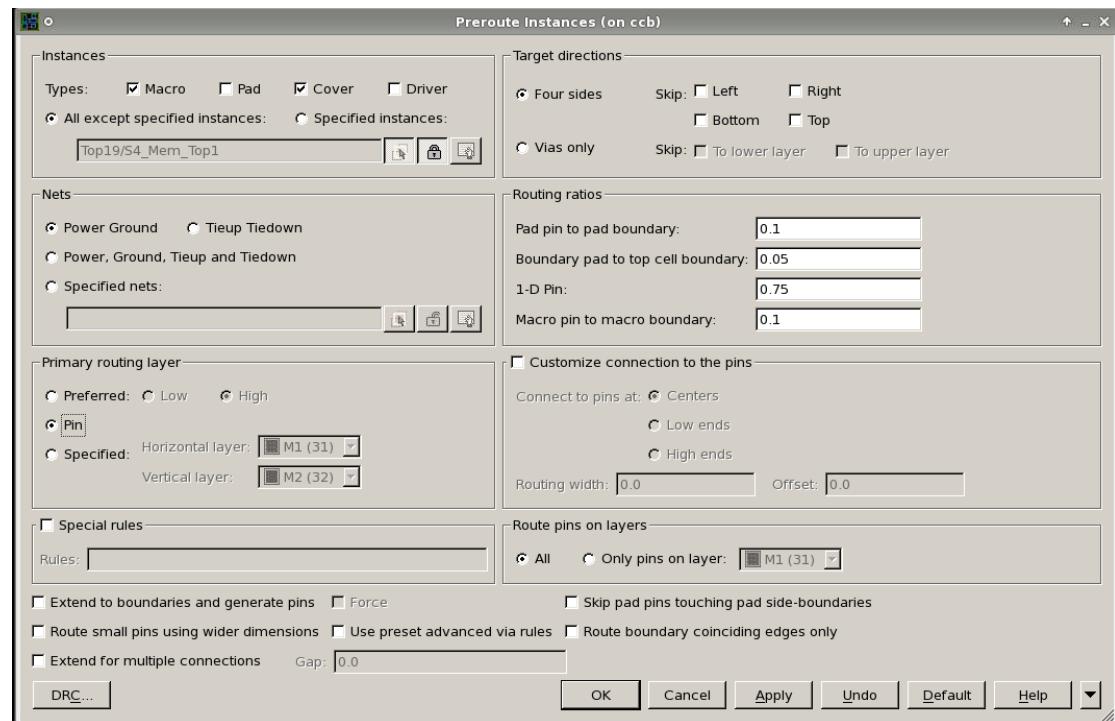


## (16). 建立 Block Ring 到 P/G Ring 的連接

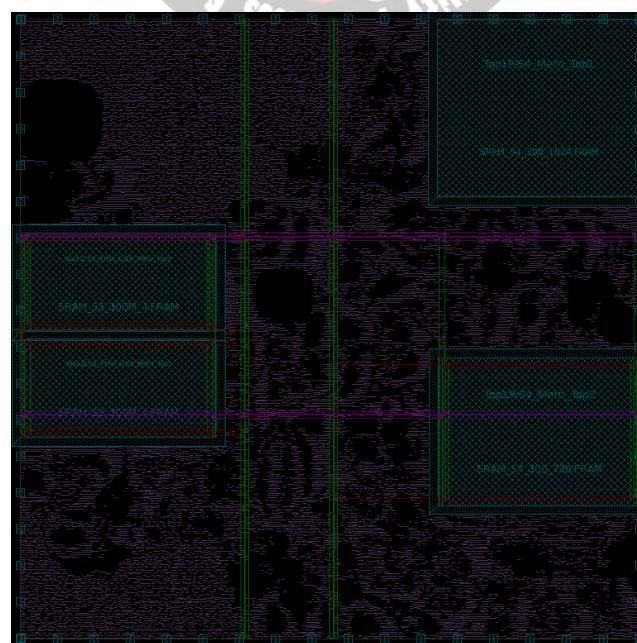
點選 “Preroute → Preroute Instances” 開啟視窗

Instances Types	Macro (只留 Macro 其餘 disable)
Primary routing layer	Pin

設定好後按 “OK”



觀察是否每個 marco 都有連接到 Strap

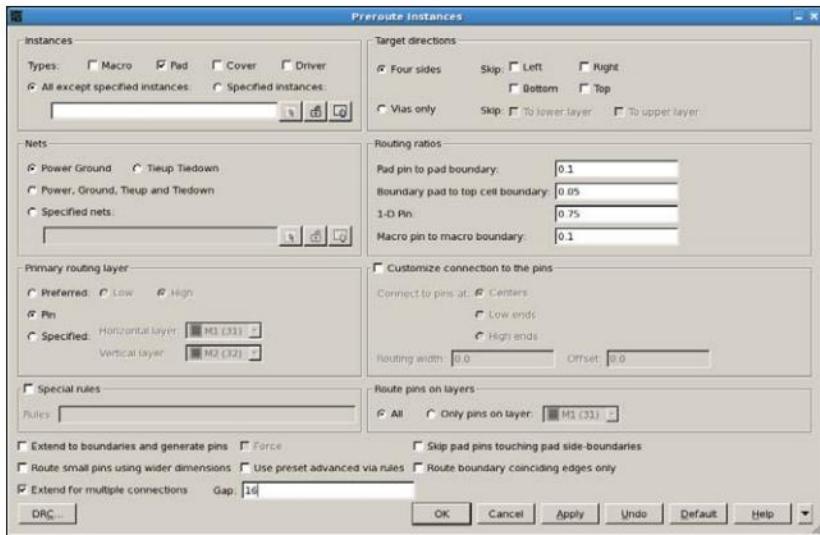


## (17). 建立 I/O Pad 到 P/G Ring 的連接

“Preroute > Preroute Instances”

Instances	Pad (只勾選 Pad 其餘 disable)
Target directions	default value
Primary routing layer	Pin
Extend for multiple connections	Enable
Gap	16

按 **Apply** 之後再按 **Default**

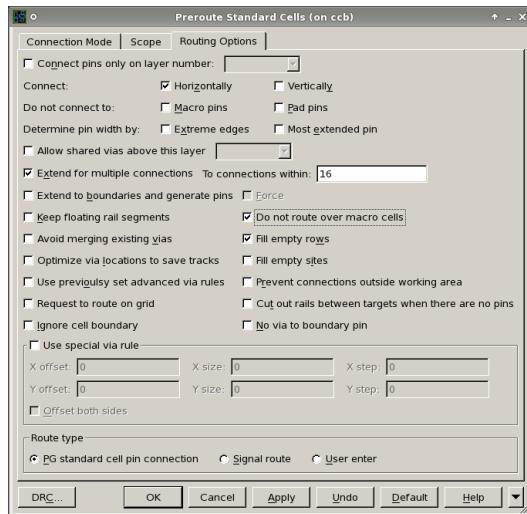


## (18). Preroute Standard Cell Rail

點選 “Preroute → Preroute Standard Cells...” 進入視窗  
選 Routing Option

Extend for multiple connections	Enable
To connections within	16
Keep floating rail segments	disable
Do not route over macro cells	enable
Fill empty rows	enable

按“OK”



設定 Strap 下不要擺放 Standard Cell

在 Message/Input Area 輸入

```
set_pnet_options -partial "M4 M5"
```

```
create_fp_placement -incremental all
```

## (19).Placement

Load the SCANDEF file:

在 Message/Input Area 輸入

```
read_def ..//YYYY/XXXX.scandef
```

**XXXX**: 檔案名稱

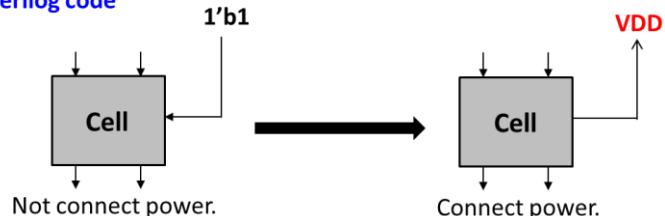
**YYYY**: 檔案位置



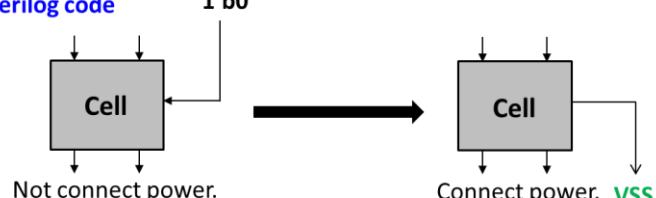
Setup the tie cell option:

在 Verilog 撰寫若有直接設定“1”或“0”，之後連接電源會直接字 VDD VSS 連接，這樣會產生 ESD 問題

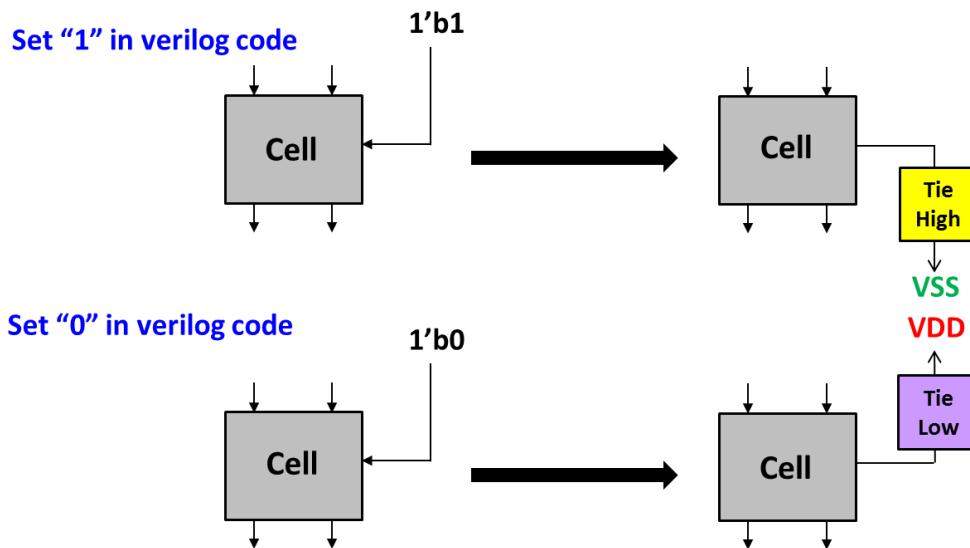
Set “1” in verilog code



Set “0” in verilog code



因此要在電壓輸入的地方設定一個 Cell，防止問題產生



add\_tie.tcl 檔案放置位置如下，請從下方位置找到此檔複製到自己的資料夾位置:

[/cad/CBDK/CBDK\\_TN40G\\_Arm/CBDK\\_TSMC40\\_core\\_Arm\\_v2.0/CIC/ICC/add\\_tie.tcl](/cad/CBDK/CBDK_TN40G_Arm/CBDK_TSMC40_core_Arm_v2.0/CIC/ICC/add_tie.tcl)

Message/Input Area 輸入

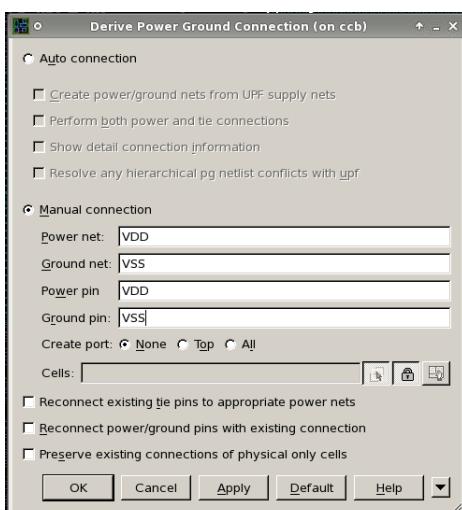
source ..//檔案位置/add\_tie.tcl

連接 Cell 的 P/G nets

點選 “Preroute → Derive PG Connection” 開啟視窗

Manual connection	selected
Power net	VDD
Ground net	VSS
Power pin	VDD
Ground pin	VSS
Other	Default value

輸入好之後按 “OK”

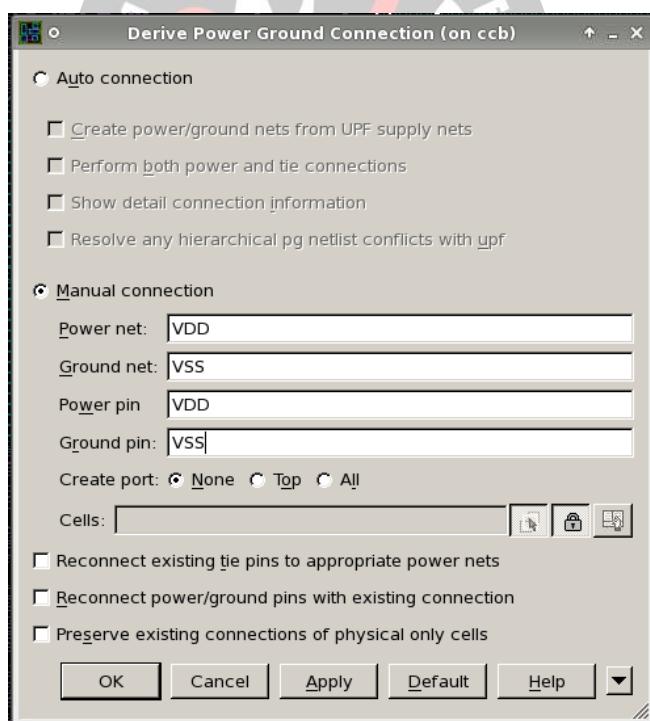


## (20).CTS

1. 在 `icc_shell` 打上”`check_physical_design -stage pre_place_opt`”
2. 在 `icc_shell` 輸入“`check_physical_design -stage pre_clock_opt`” 檢查是否有 error
3. 輸入 `report_constraint -all` 檢查是否有 violation
4. 輸入 `set_separate_process_options -placement false` (TN40G 才需使用)
5. 輸入 `clock_opt -fix_hold_all_clocks -no_clock_route`
6. 點選 “Preroute → Derive PG Connection” 開啟視窗

Manual connection	selected
Power net	VDD
Ground net	VSS
Power pin	VDD
Ground pin	VSS
Other	Default value

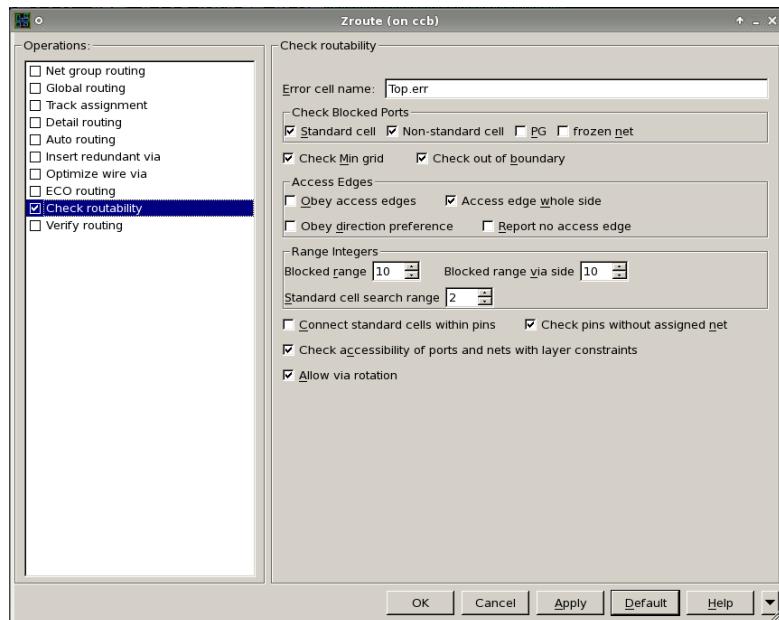
輸入好之後按 “OK”



## (21).Route

“ Route > Check Routability...”

直接按“OK”

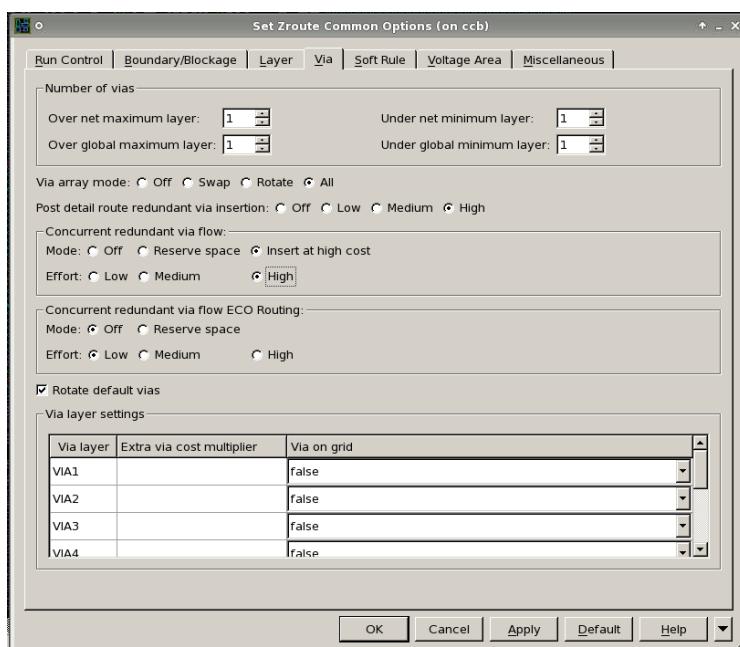


“ Route > Routing Setup > Set common Route Option”

選 Via Tab

Post detail route redundant via insertion	High
Concurrent redundant via flow	Mode: Insert at High Cost
Concurrent redundant via flow	Effort: High

直接按“OK”



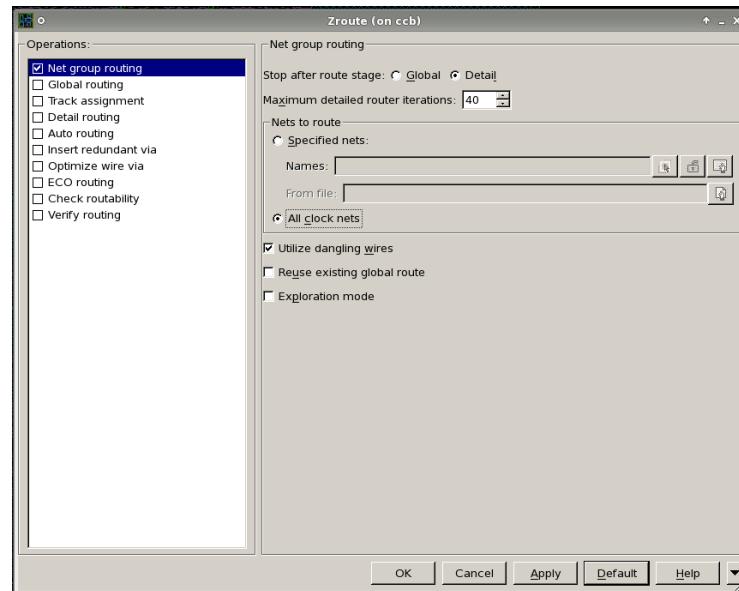
在 Message/Input Area 輸入 source

TN40G: /cad/CBDK/CBDK\_TN40G\_ARM/CBDK\_TSMC40\_core\_TSMC\_v2.0/CIC/ICC  
/antenna\_9lm\_CIC.clf

TN90: /cad/CBDK/CBDK\_TSMC90GUTM\_Arm\_v1.2/CIC/ICC/antenna\_9lm\_CIC.clf  
“Route > Net Group Route...”

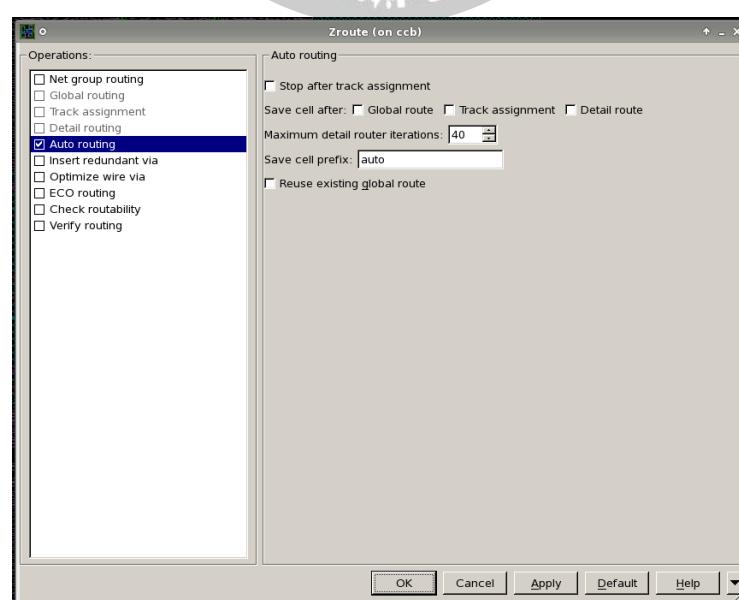
Net to route	All clock nets
other	default value

直接按“OK”



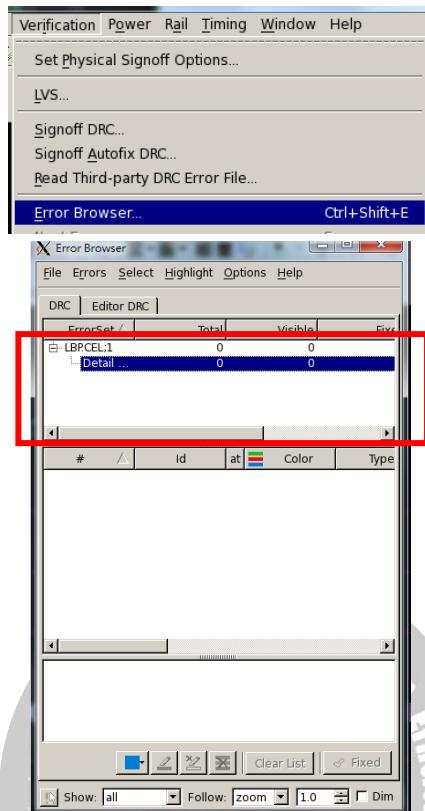
“Route > Auto Route...”

直接按“OK”



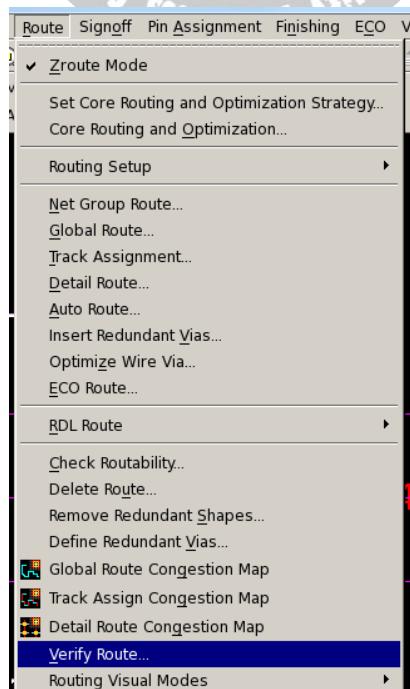
## (22). Verification

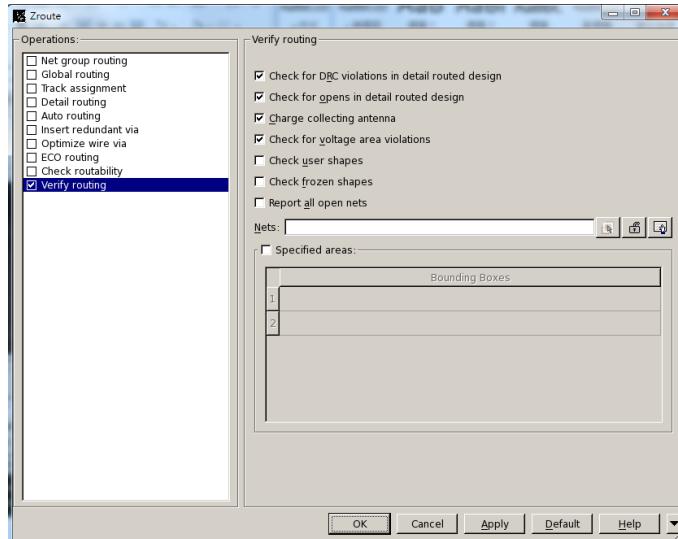
點選 Verification→Error Browser... 選取 Detail Route 之後按 OK



出現 0 為正常，如果是其他數字代表有錯誤

點選 Route→Verify Route 直接按 OK





#### Verify Summary:

Total number of nets = 604, of which 0 are not extracted  
Total number of open nets = 0, of which 0 are frozen  
Total number of excluded ports = 0 ports of 0 unplaced cells connected to 0 nets  
    0 ports without pins of 0 cells connected to 0 nets  
    0 ports of 0 cover cells connected to 0 non-pg nets  
Total number of DRCs = 0  
Total number of antenna violations = no antenna rules defined  
Total number of voltage-area violations = no voltage-areas defined  
Total number of tie to rail violations = not checked  
Total number of tie to rail directly violations = not checked

```
1  
icc_shell>
```

圈圈內必須為 0，如果不為 0 請執行 STEP23

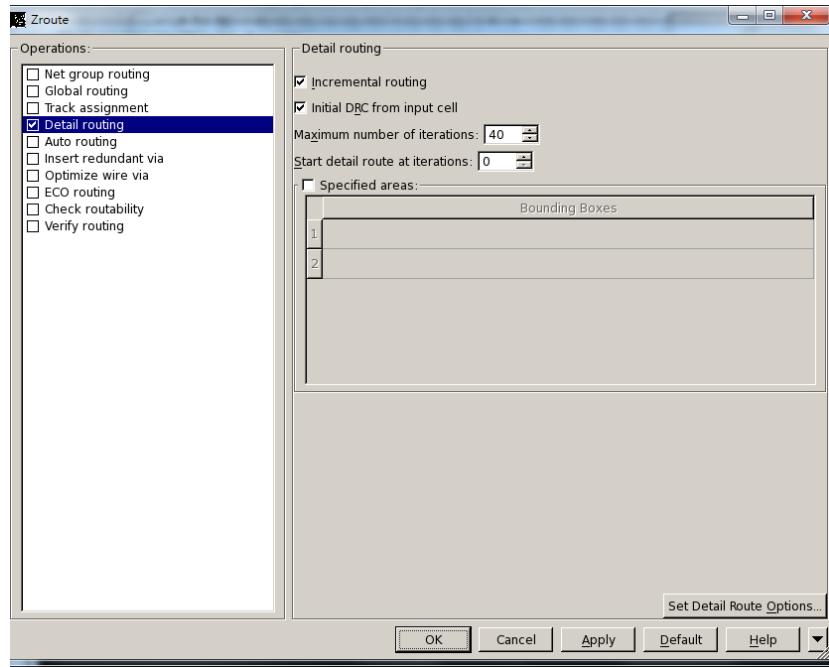
在 **icc\_shell** 中，輸入"**report\_timing**"檢查 slack，如果 slack 為負的話就在 **icc\_shell** 中輸入"**route\_opt**"並重複此動作，修正到正為止。

## (23). 修正 DRCs

(若 DRCs 為 0，請跳過此步驟)

點選 Route→Detail Route

並且把 Incremental routing & Initial DRC from input cell 都勾起來如圖按 OK



## (24). 輸出檔案

輸出 SDF 檔:在 icc\_shell 輸入

“ write\_sdf -version 2.0 -context verilog -load\_delay net LBP.sdf ”

上方指令中 LBP.sdf 請自行命名

輸出.v 檔

點選 File→Export→Write Verilog...按照下圖勾選完之後按 OK

