

Politecnico di Torino

# Testing and Fault tolerance

# Report Contest

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The first approach to the contest has been the translation of groups 4 and 8 that had good results in the previous contest. All the store operation has been changed to access only the data section. Furthermore, to preserve the status a PUSH\_ALL() and POP\_ALL() functions were written in the PUSH\_POP.h file. These two functions are used to preserve the content of the registers in a dedicated part of the data by handling a stack pointer. This section will be unused for the rest of the test. At the end of each test, the content of the register is restored. The figure below shows the memory map.

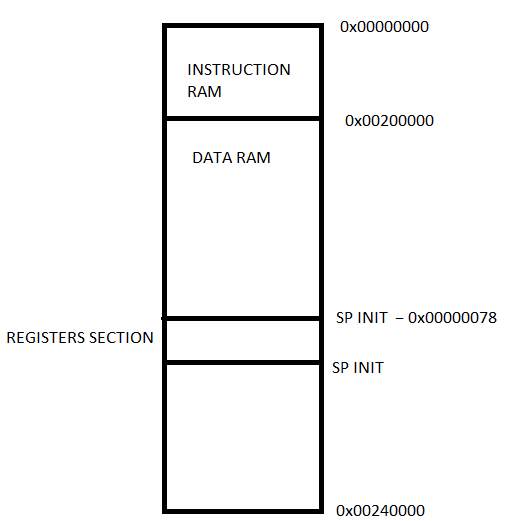


Figure 1 - Memory map

After the first simulation, we saw GR8 and GR4 weren’t enough so after trying the effectiveness of the other group's codes according to not covered faults. Finally, we found the very good optimized combination of codes included below:

* **GR20\_ALU.s**
* **GR20\_INTEGRATION.S**
* **GR19\_test\_ls.S**
* **GR19\_test\_if.S**
* **GR14\_TEST\_CSR.S**

“Running a complete simulation for these groups".

However, the ***CSR*** unit is not part of the test, we decide to update and add the **GR14\_TEST\_CSR.S** to trigger as much instruction as possible in the fetch and decode stage. Lastly, we add the remaining percentage performing an incremental simulation using the **simple\_hwl.S** and **my\_ls\_test.S** files; in particular, the first is used to improve the hardware loop. ( we noticed that the **CSR** related to this unit changed concerning the 2017 one. So we changed the CSR from 0x7B- to 0x7C-). Lastly **my\_ls\_test.S** is a test written by us to reach 90% covering the remaining percentage of the Load and Store unit.

The overall simulation result is reported in the figure below :

|  |  |  |
| --- | --- | --- |
| **instance** | **faults** | **cumulative** |
| / | 162146 | 90% |
| /if\_stage\_i | 17028 | 69% |
| /if\_stage\_i/prefetch\_128\_prefetch\_buffer\_i | 10588 | 76% |
| /if\_stage\_i/prefetch\_128\_prefetch\_buffer\_i/L0\_buffer\_i | 3780 | 70% |
| /if\_stage\_i/hwloop\_controller\_i | 1628 | 64% |
| /if\_stage\_i/compressed\_decoder\_i | 1504 | 86% |
| /id\_stage\_i | 65582 | 91% |
| /id\_stage\_i/registers\_i | 39590 | 99% |
| /id\_stage\_i/registers\_i/riscv\_register\_file\_i | 39590 | 99% |
| /id\_stage\_i/decoder\_i | 4136 | 80% |
| /id\_stage\_i/controller\_i | 2278 | 41% |
| /id\_stage\_i/int\_controller\_i | 184 | 7% |
| /id\_stage\_i/hwloop\_regs\_i | 3222 | 78% |
| /ex\_stage\_i | 72788 | 96% |
| /ex\_stage\_i/alu\_i | 32094 | 94% |
| /ex\_stage\_i/alu\_i/alu\_popcnt\_i | 340 | 100% |
| /ex\_stage\_i/alu\_i/alu\_ff\_i | 416 | 100% |
| /ex\_stage\_i/alu\_i/int\_div\_div\_i | 5280 | 96% |
| /ex\_stage\_i/mult\_i | 39780 | 97% |
| /load\_store\_unit\_i | 5608 | 78% |
| /cs\_registers\_i | 30680 | NAN |
| /RISCY\_PMP\_pmp\_unit\_i | 76610 | NAN |

Figure 2 - Report faults hierarchy

Concerning the size the elf file requires about 60 kbytes considering all the sections.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **text** | **data** | **bss** | **dec** | **hex** |  |
| **56410** | **2116** | **2104** | **60630** | **ecd6** | bytes |

The duration of the simulation requires 5:15 minuntes in Det server and abou 2 min in DAUIN server.

Resuming the results:

* Test coverage 90,18%
* Code size 60 Kbytes.
* 5:15 minutes.

Due to an issue on DAUIN server was not possible to complete the last complete simulation, so the test coverage (figure 2) refers to the increamental one.