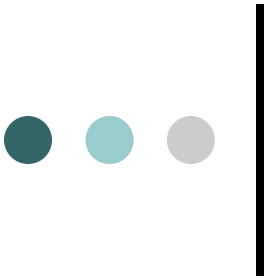
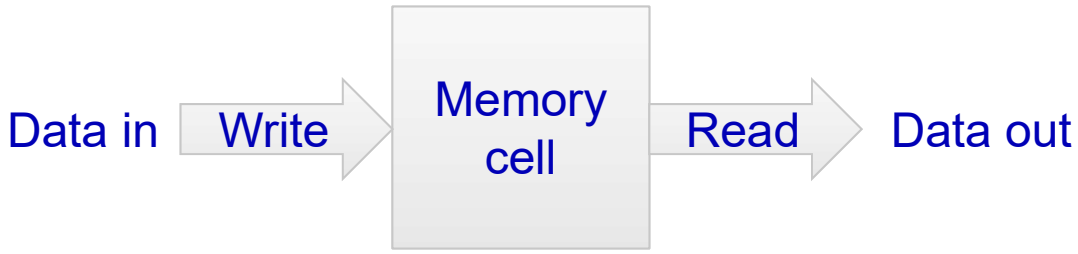


Semiconductor memories

Semiconductor Memories



Some design issues :

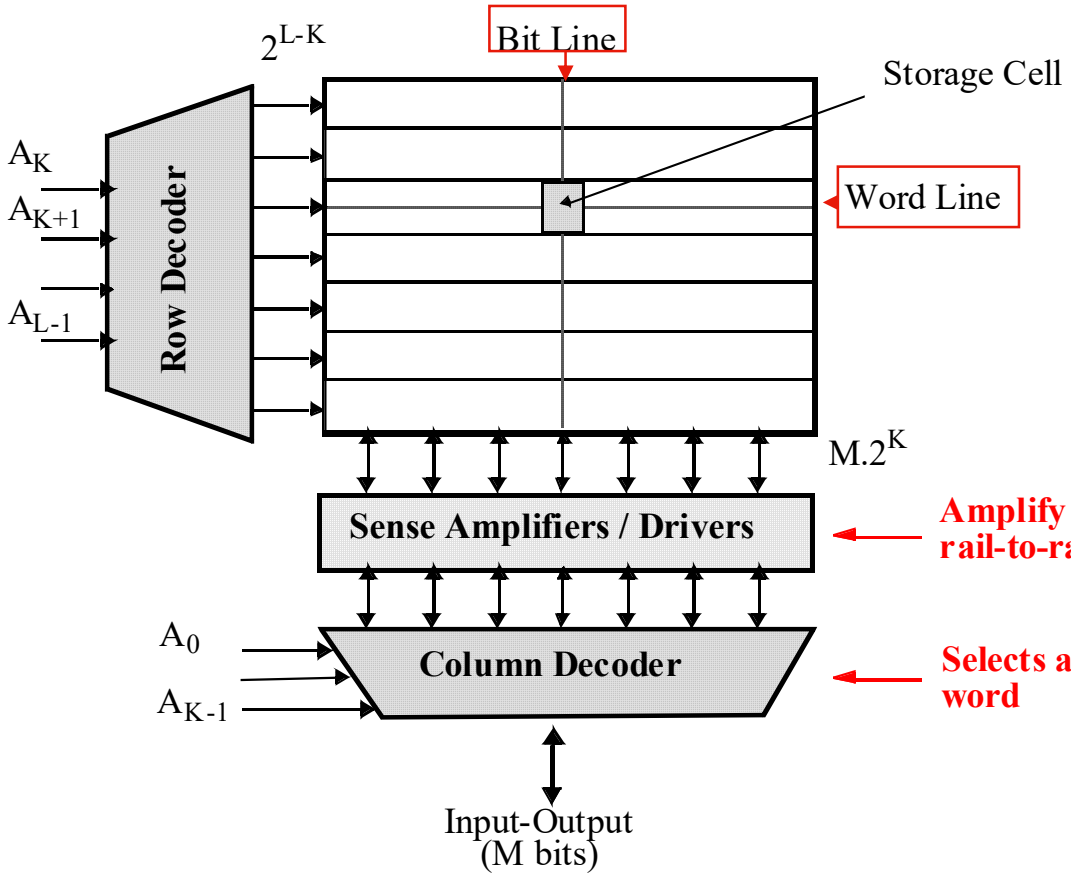
- How many cells ?
- Function ?
- Power consuption ?
- Access type ?
- How fast are read/write operations ?

Semiconductor Memories

RWM		NVRWM	ROM
Random Access	**Non-Random Access**	EPROM E^2PROM FLASH	Mask-Programmed Programmable (PROM)
SRAM DRAM	FIFO LIFO Shift Register CAM		

Architecture

Problem: ASPECT RATIO or HEIGHT >> WIDTH



M = bit group (byte: M=8)
L = byte address bits
K = column address bits

$M \cdot 2^K$ Bit Lines
2^{L-K} Word Lines

Architecture: example

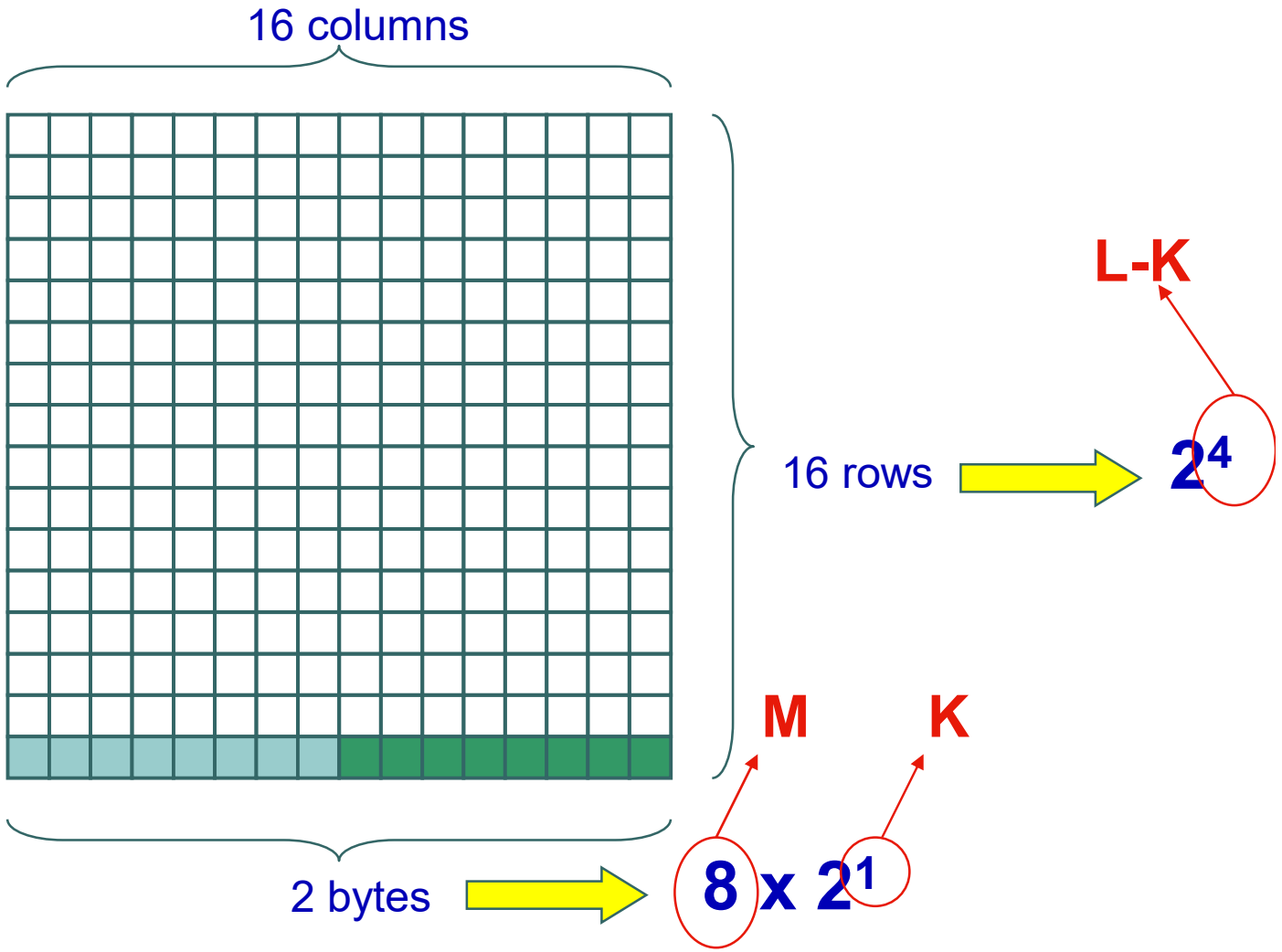
256 cells

32 bytes

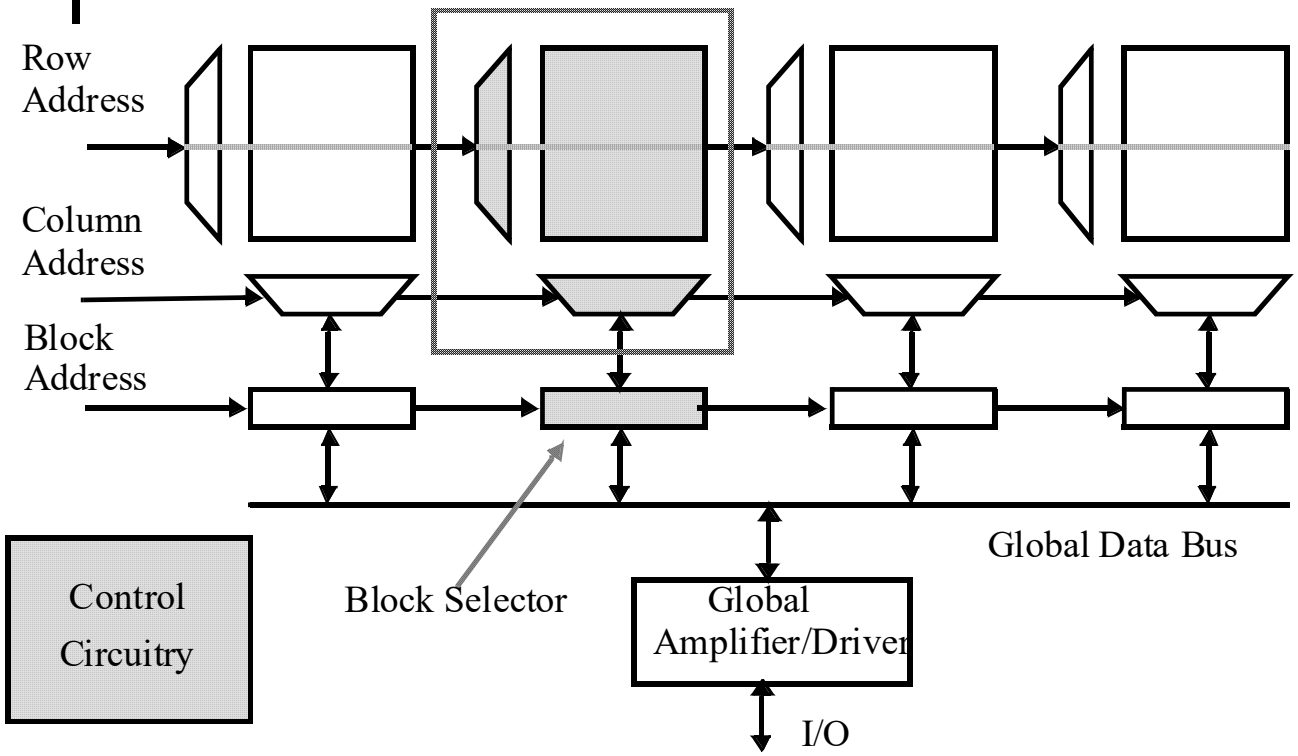
2^5 bytes

L=5

M = 8
K = 1
L-K=4

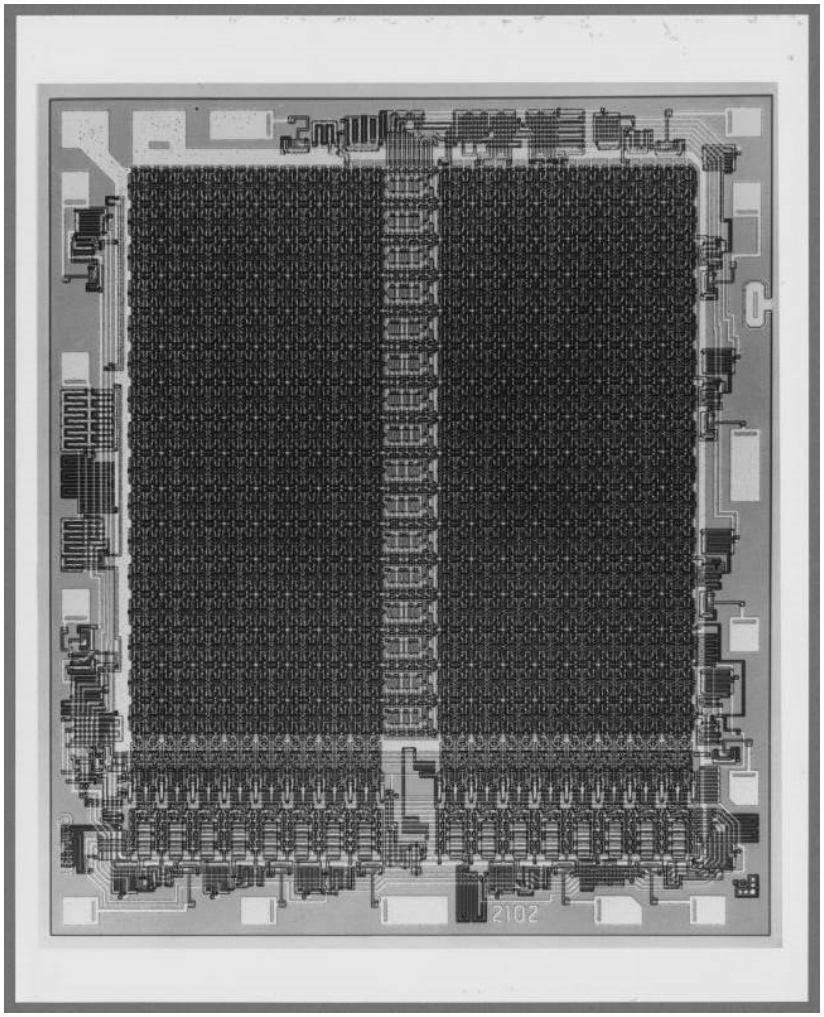


Blocks (≥ 1Mbit)



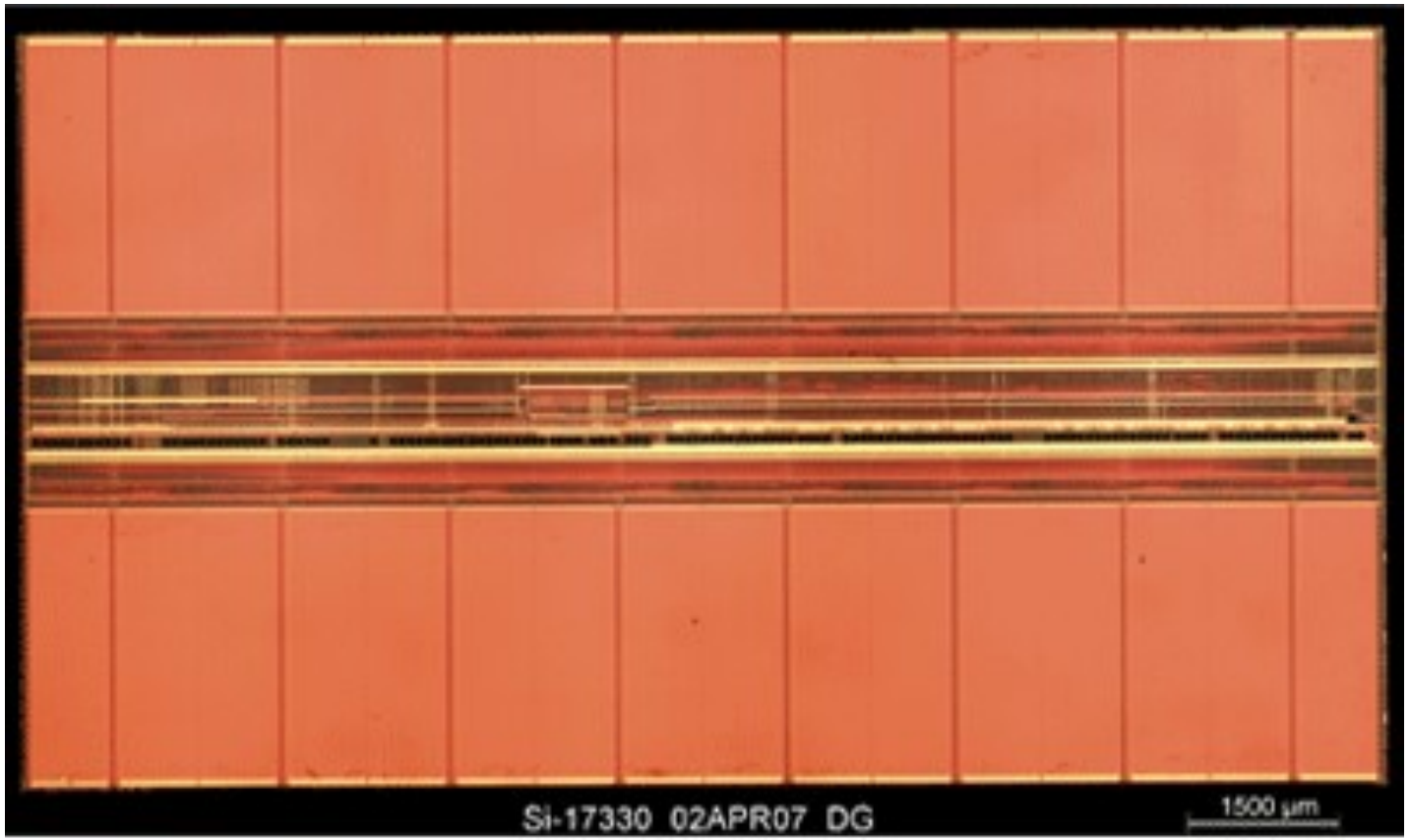
Advantages:
1. Shorter wires within blocks
2. Block address activates only 1 block => power savings

Area occupation



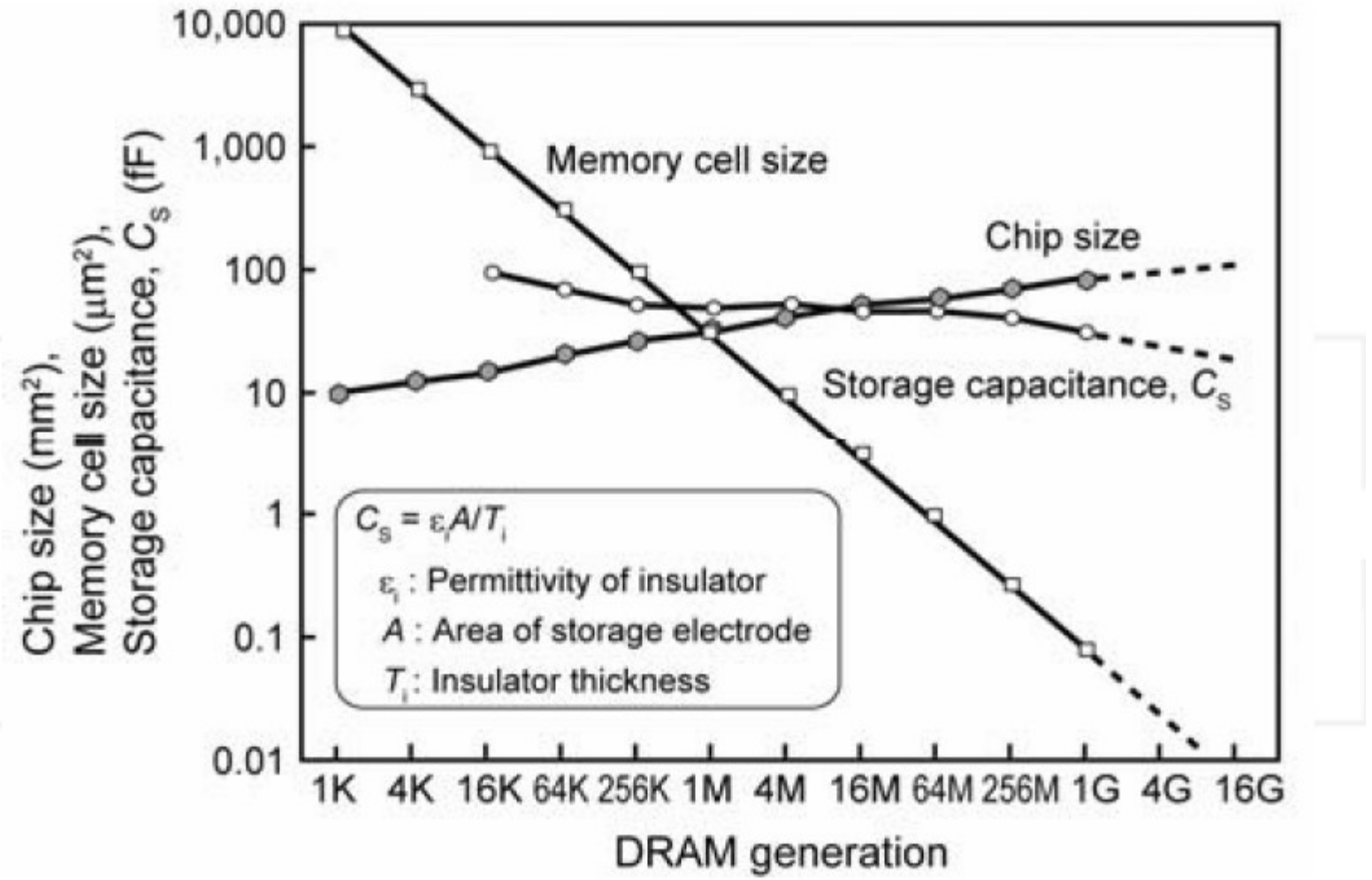
INTEL 2102
1Kx1bit SRAM
1972

Area occupation

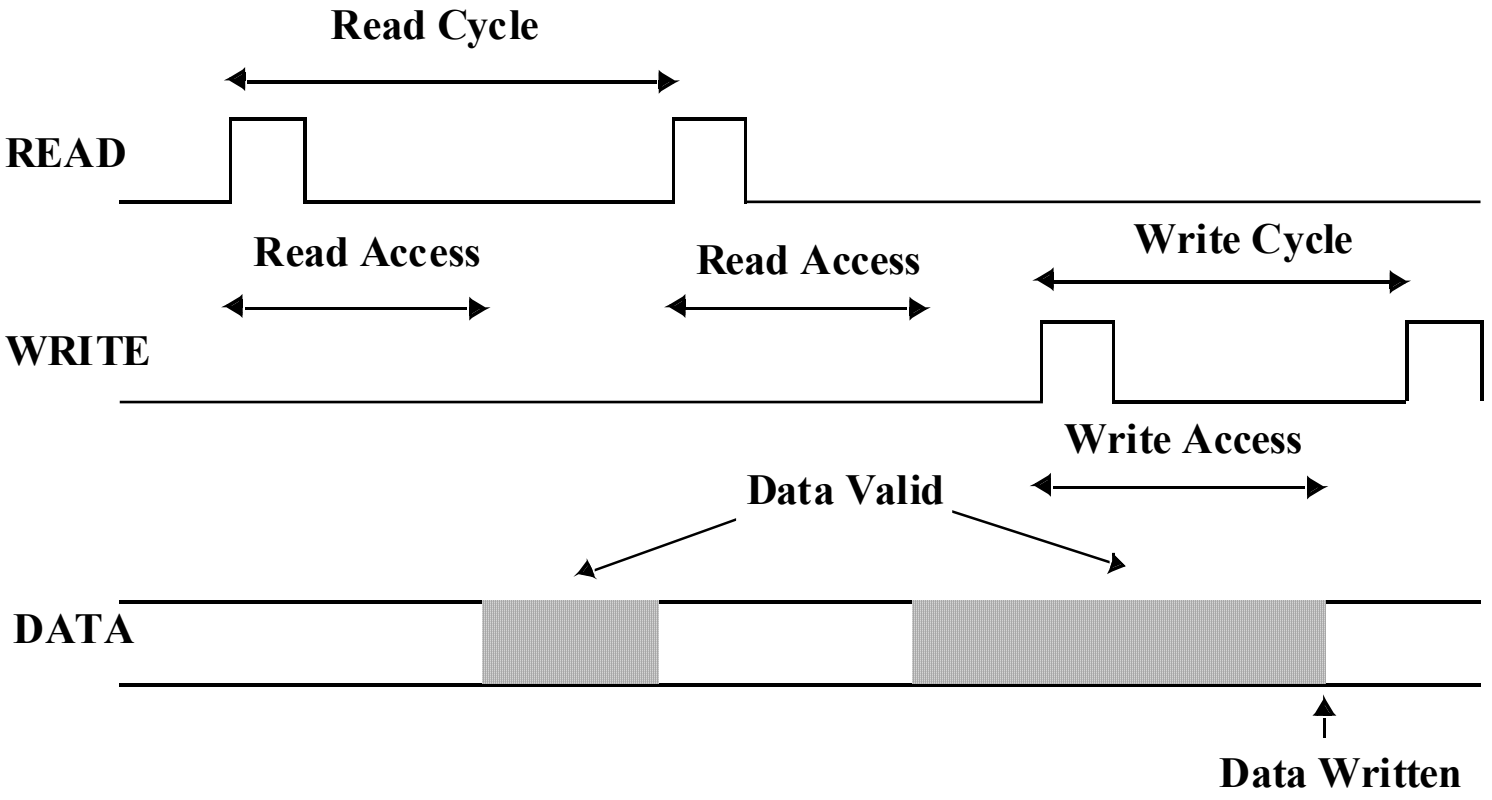


Micron
1 Gbit DRAM
Today

Area occupation

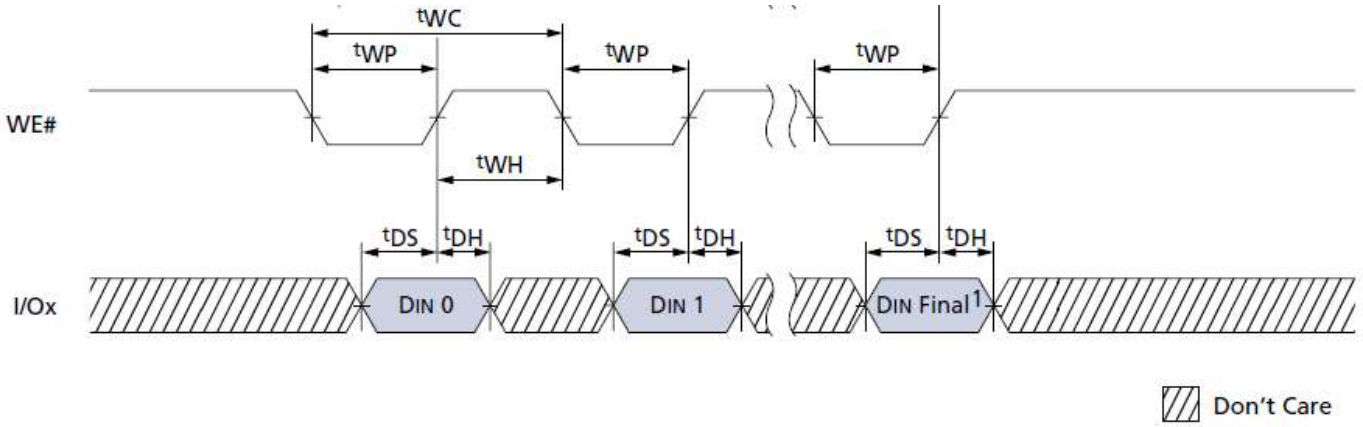


Write/read cycles

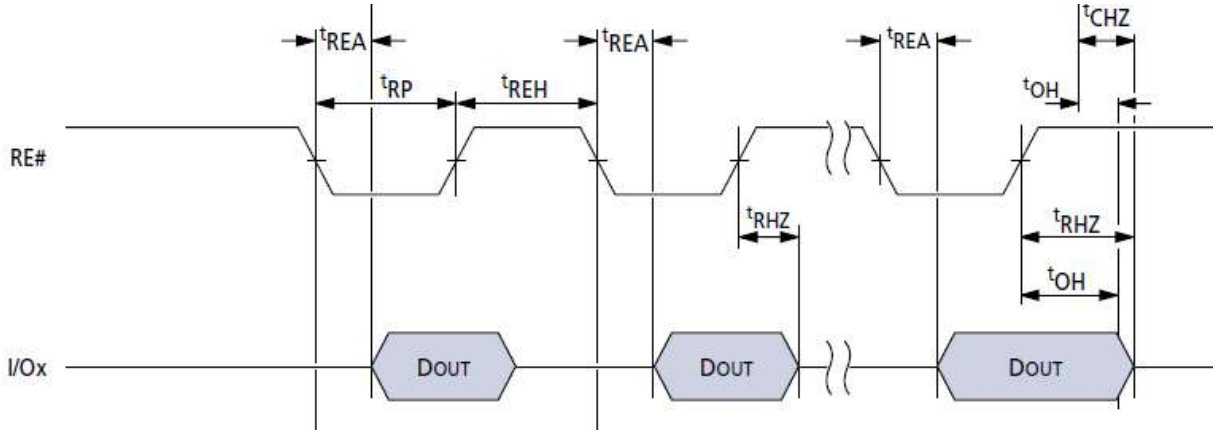


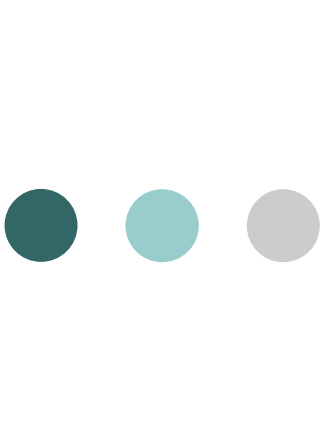
Semiconductor Memories

Write cycle



Read cycle





SRAM & DRAM

Read-Write Memories (RAM)

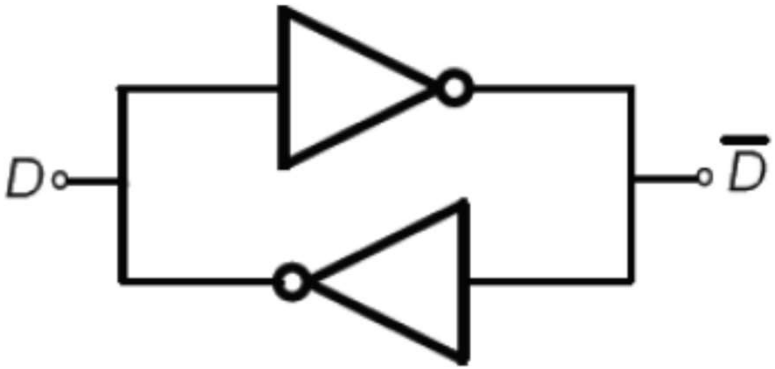
- **STATIC (SRAM)**

  Data stored as long as supply is applied
  Large (6 transistors/cell)
  Fast
  Differential

- **DYNAMIC (DRAM)**

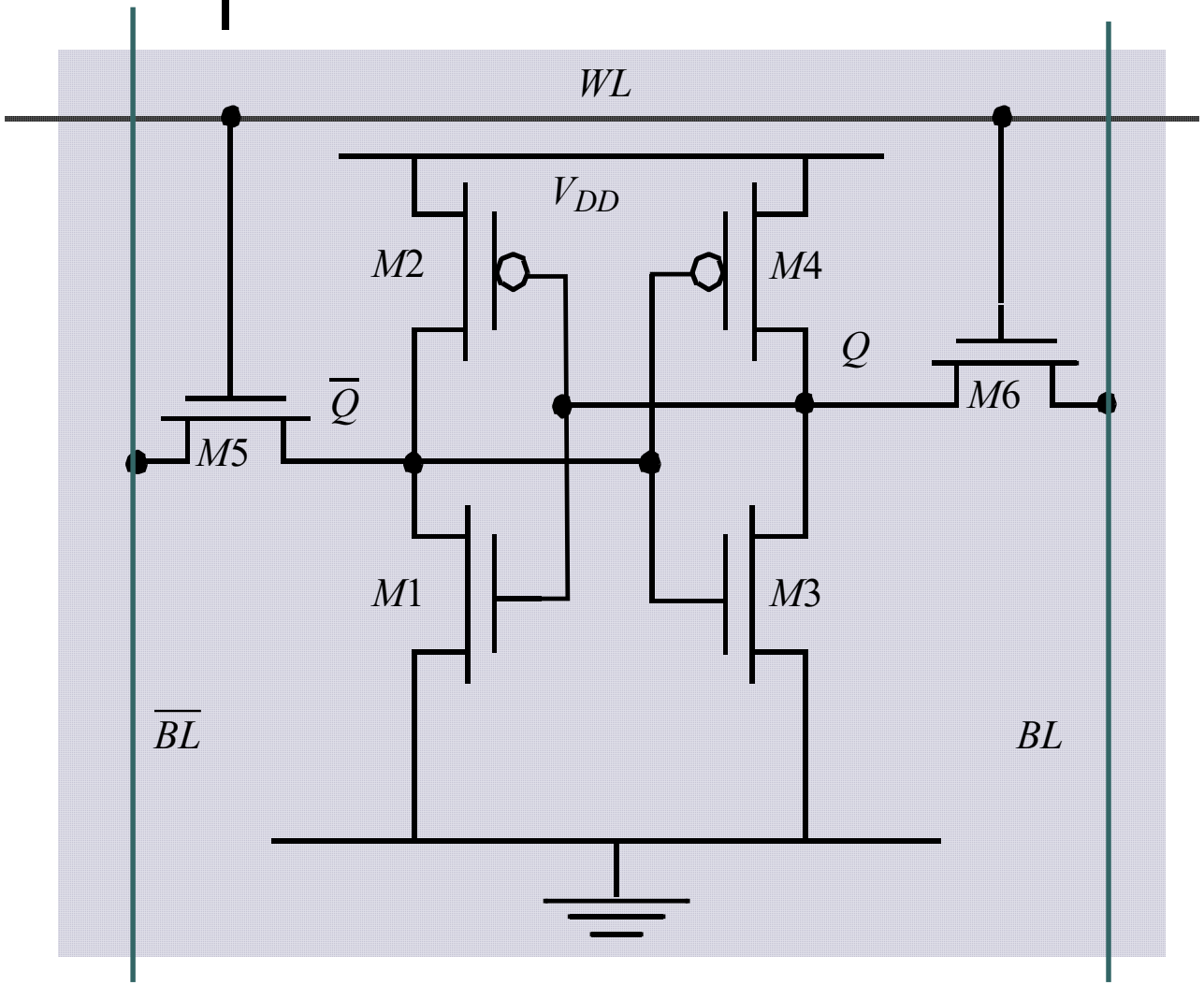
  Periodic refresh required
  Small (1-3 transistors/cell)
  Slower
  Single Ended

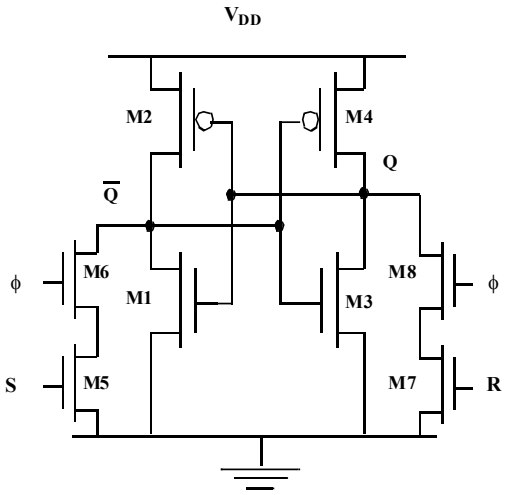
Basic Static Memory Element



- If D is high, $\overline{D}$ will be driven low
  - Which makes D stay high
- Positive feedback

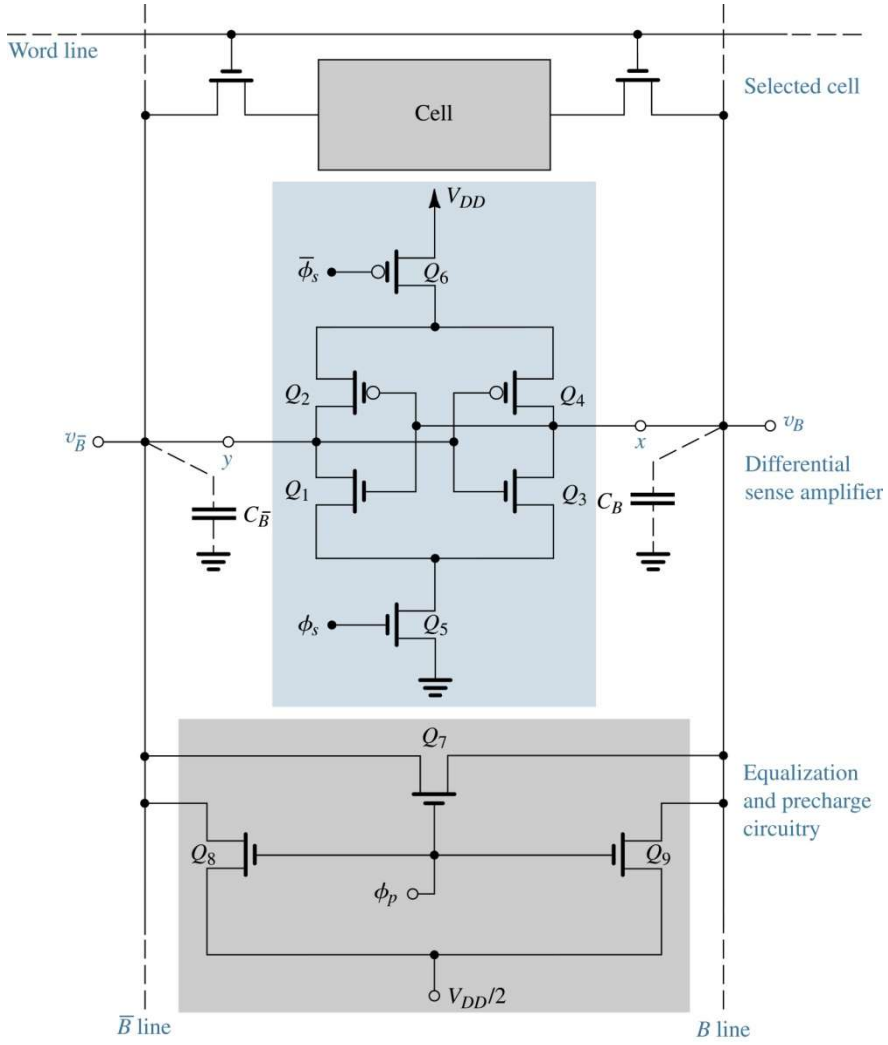
6-transistor CMOS SRAM Cell



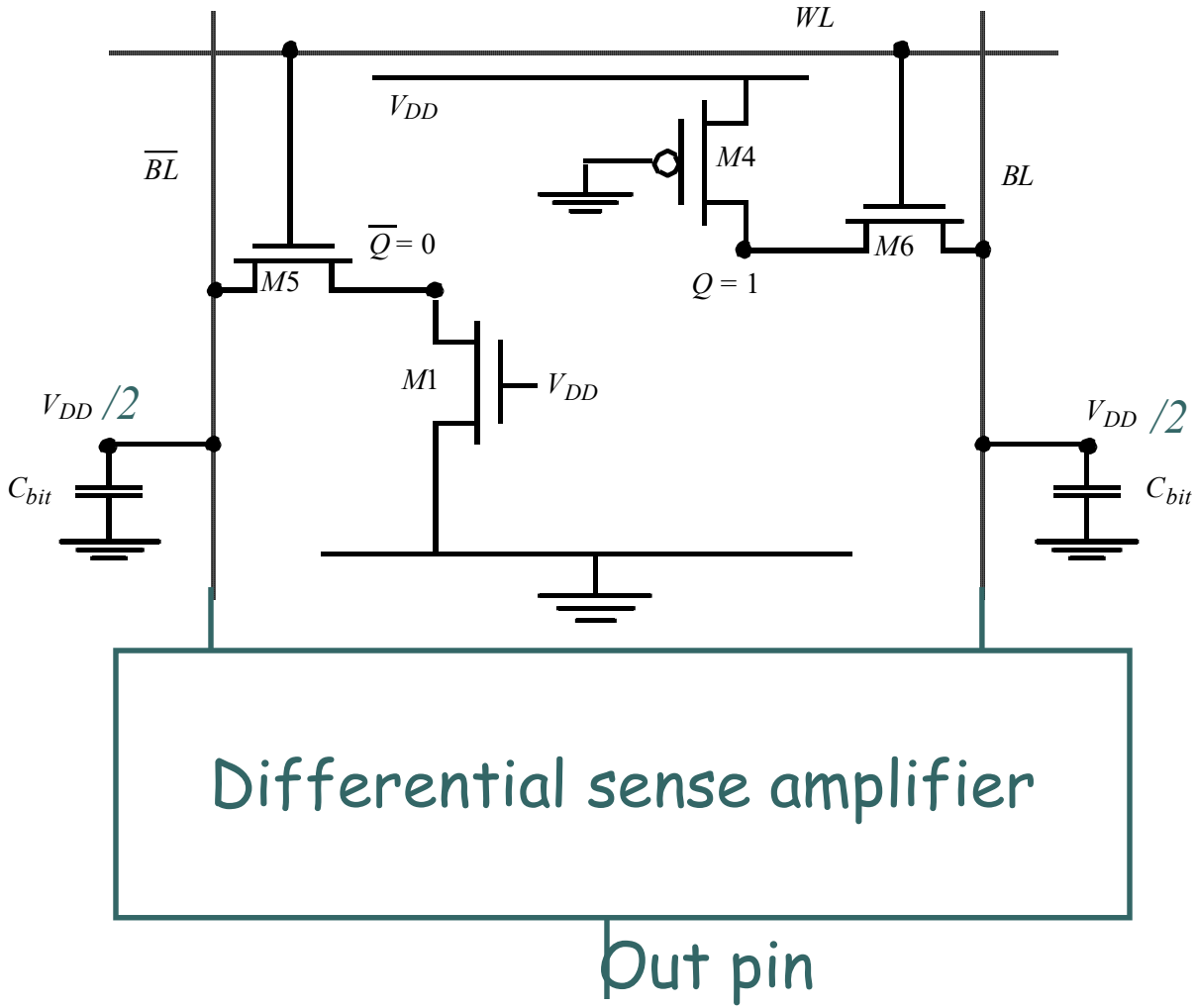


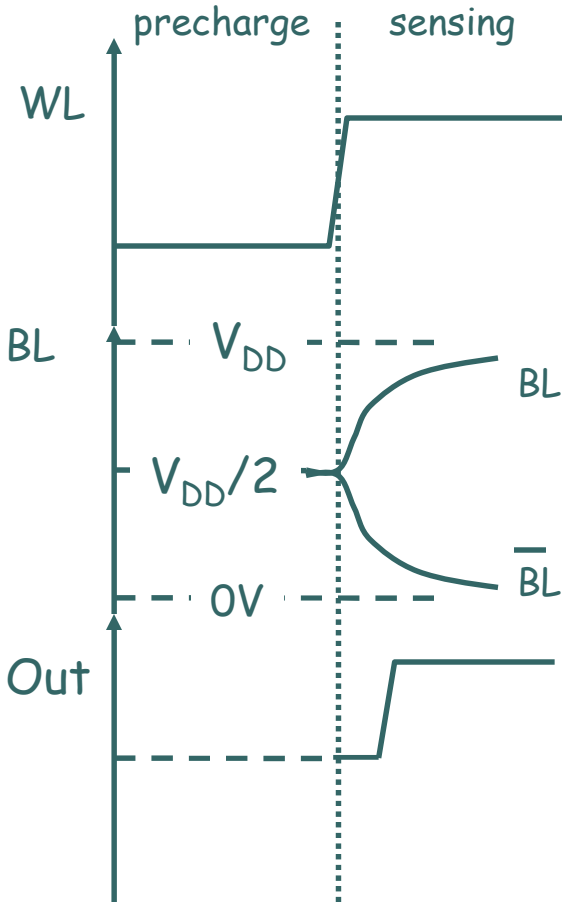
SR Flip-Flop

CMOS SRAM Analysis (Read)

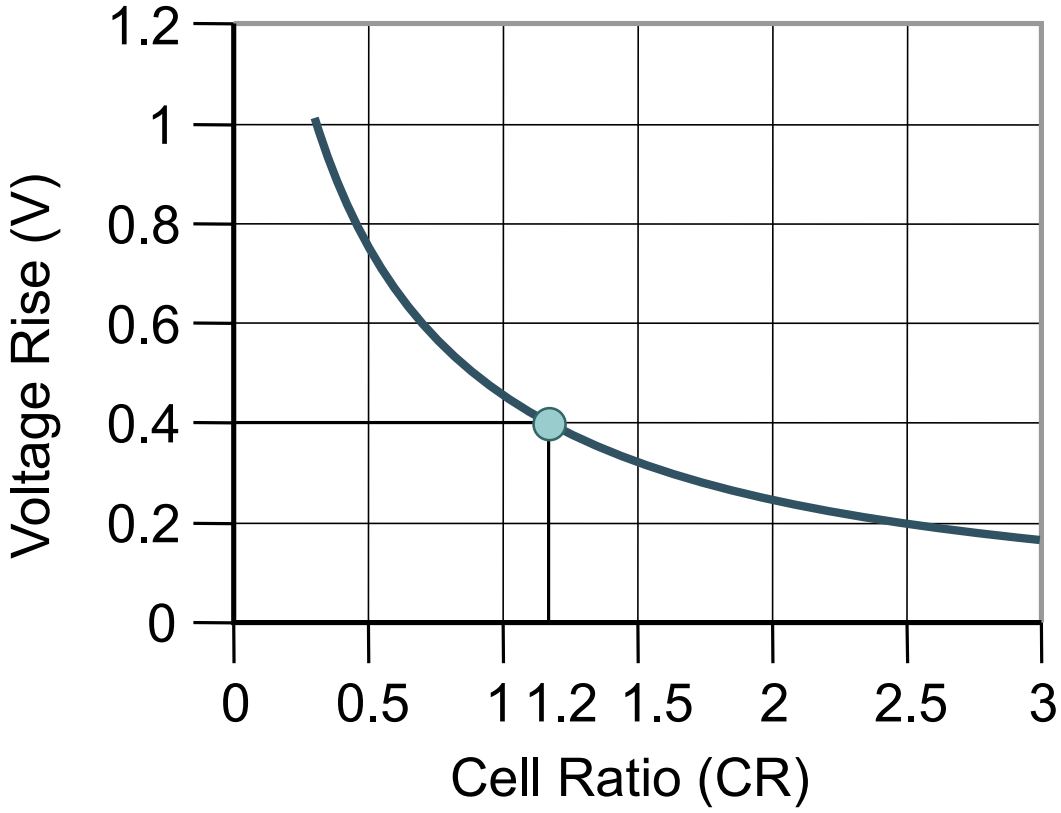


CMOS SRAM Analysis (Read)



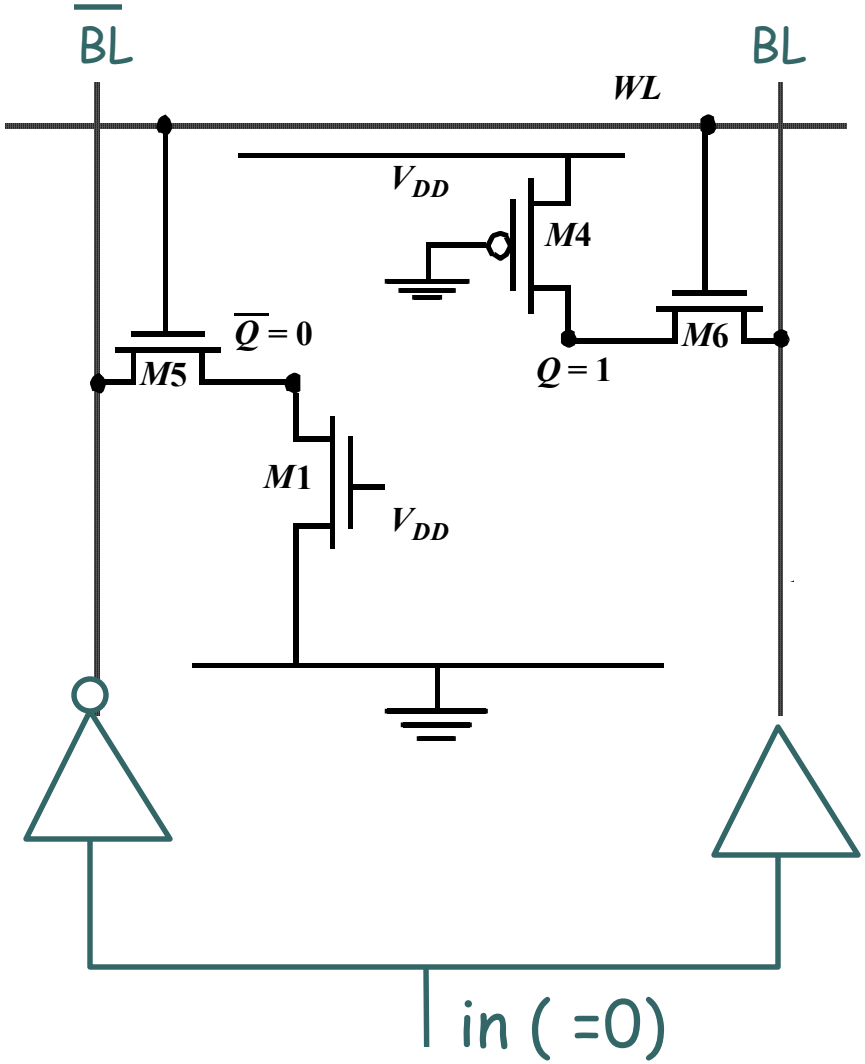


CMOS SRAM Analysis (Read)



$$CR = \frac{W_1/L_1}{W_5/L_5}$$

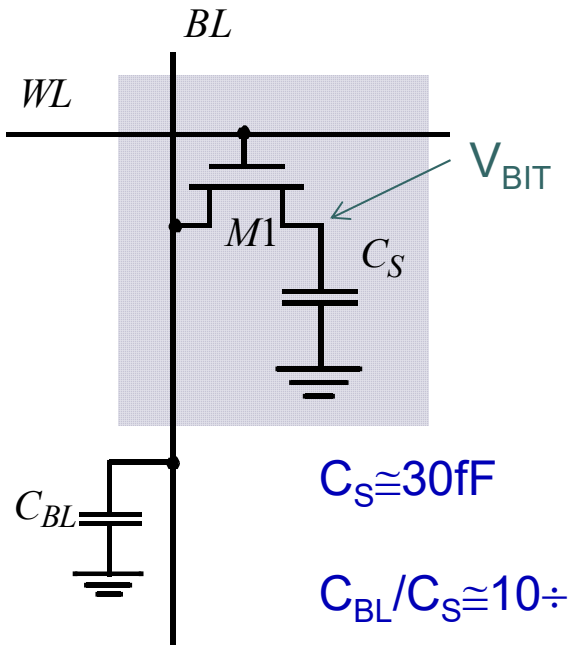
CMOS SRAM Analysis (Write)



6 transistor SRAM : features

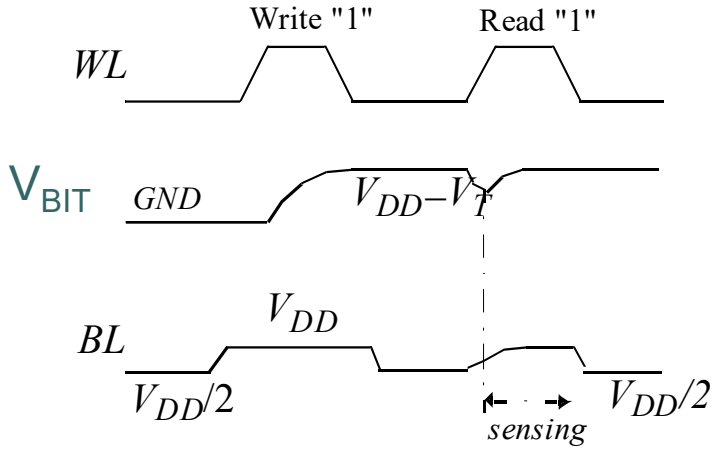
- 6 transistors cell (large number !)
- nMOS and PMOS in the cell → wells
- 5 lines : $\overline{BL}$, BL, WL, VDD, GND
- Critical read driven by small cell transistors → increase access time

1-Transistor DRAM Cell (1T DRAM)



$C_S \cong 30fF$

$C_{BL}/C_S \cong 10 \div 100$

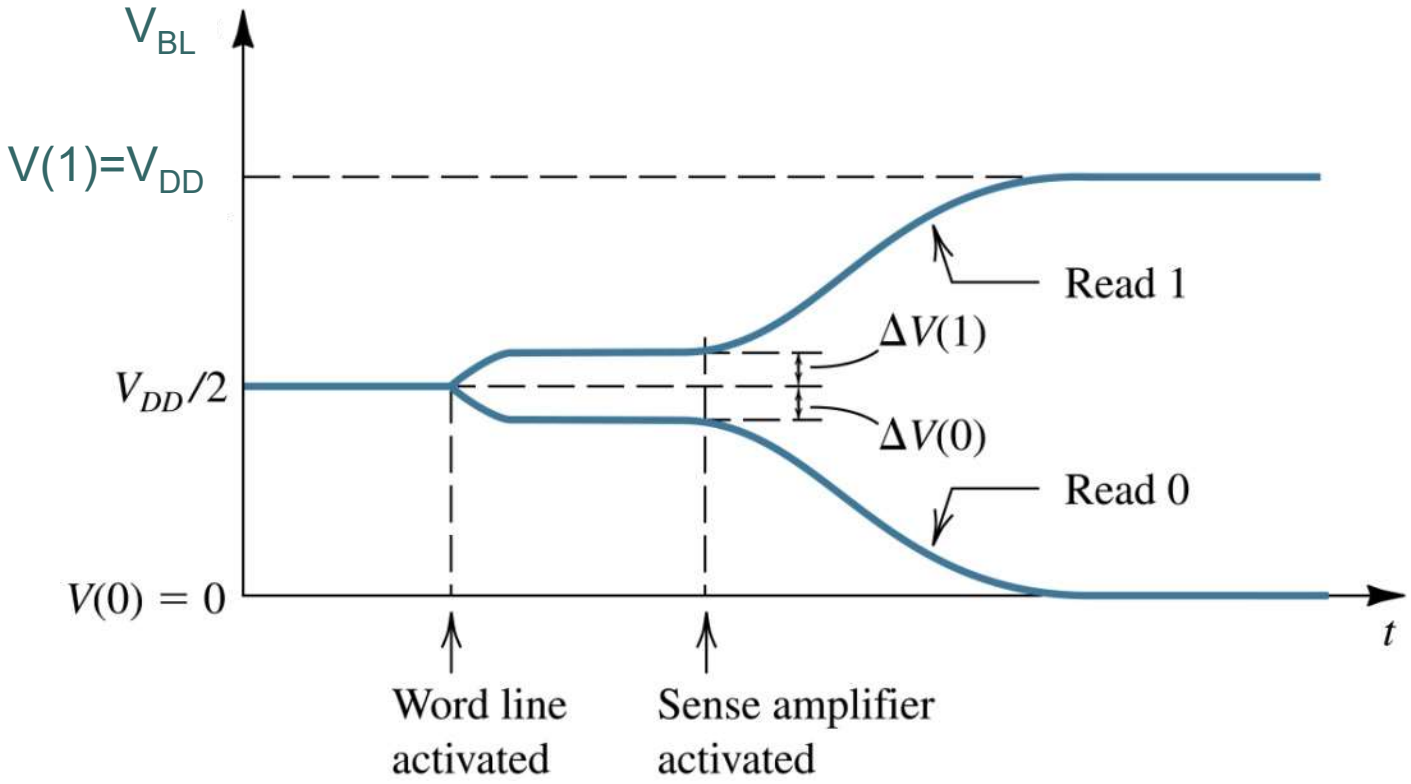


Write: C_S is charged or discharged by asserting WL and BL.
Read: Charge redistribution takes places between bit line and storage capacitance

$$\Delta V = V_{BL} - V_{PRE} = (V_{BIT} - V_{PRE})\frac{C_S}{C_S + C_{BL}}$$

Voltage swing is small; typically around 250 mV.

Sense Amp Operation



DRAM Cell Observations

1T DRAM requires a sense amplifier for each bit line, due to charge redistribution read-out.

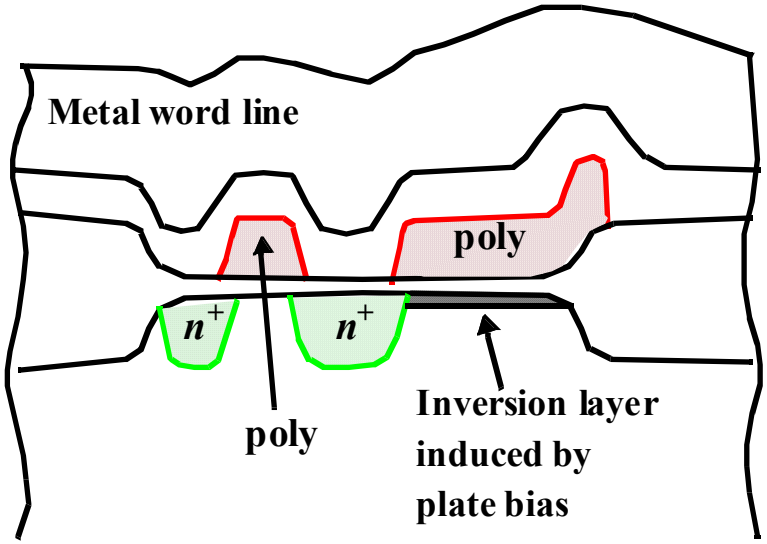
DRAM memory cells are single ended in contrast to SRAM cells.

The read-out of the 1T DRAM cell is destructive; read and refresh operations are necessary for correct operation.

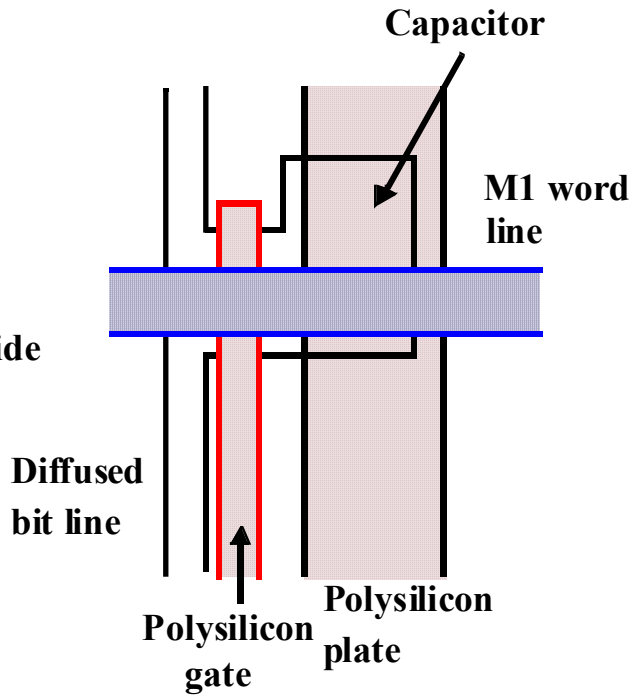
When writing a "1" into a DRAM cell, a threshold voltage is lost.

This charge loss can be circumvented by bootstrapping the word lines to a higher value than V_{DD}.

1-T DRAM Cell



(a) Cross-section

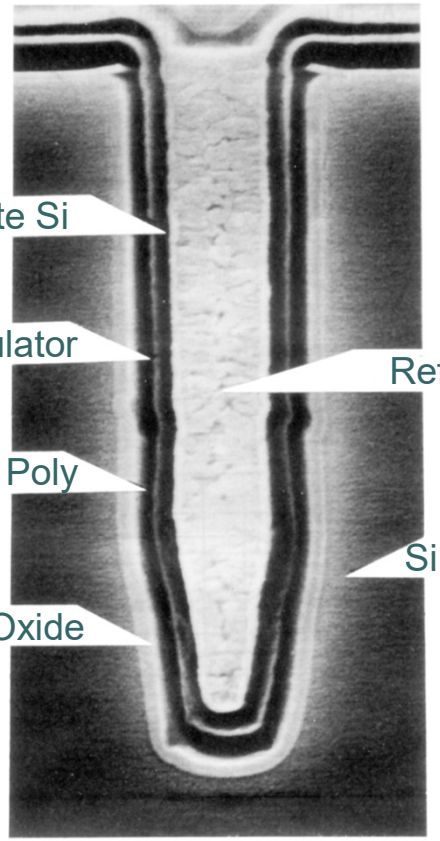


(b) Layout

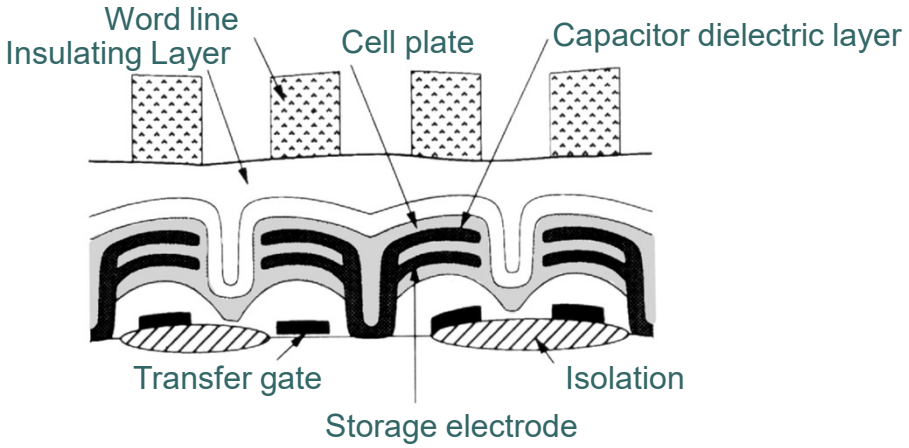
Used Polysilicon-Diffusion Capacitance

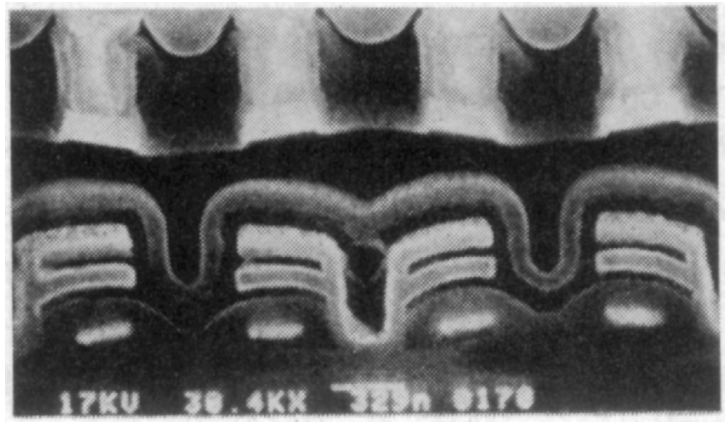
Expensive in Area

Advanced 1T DRAM Cells



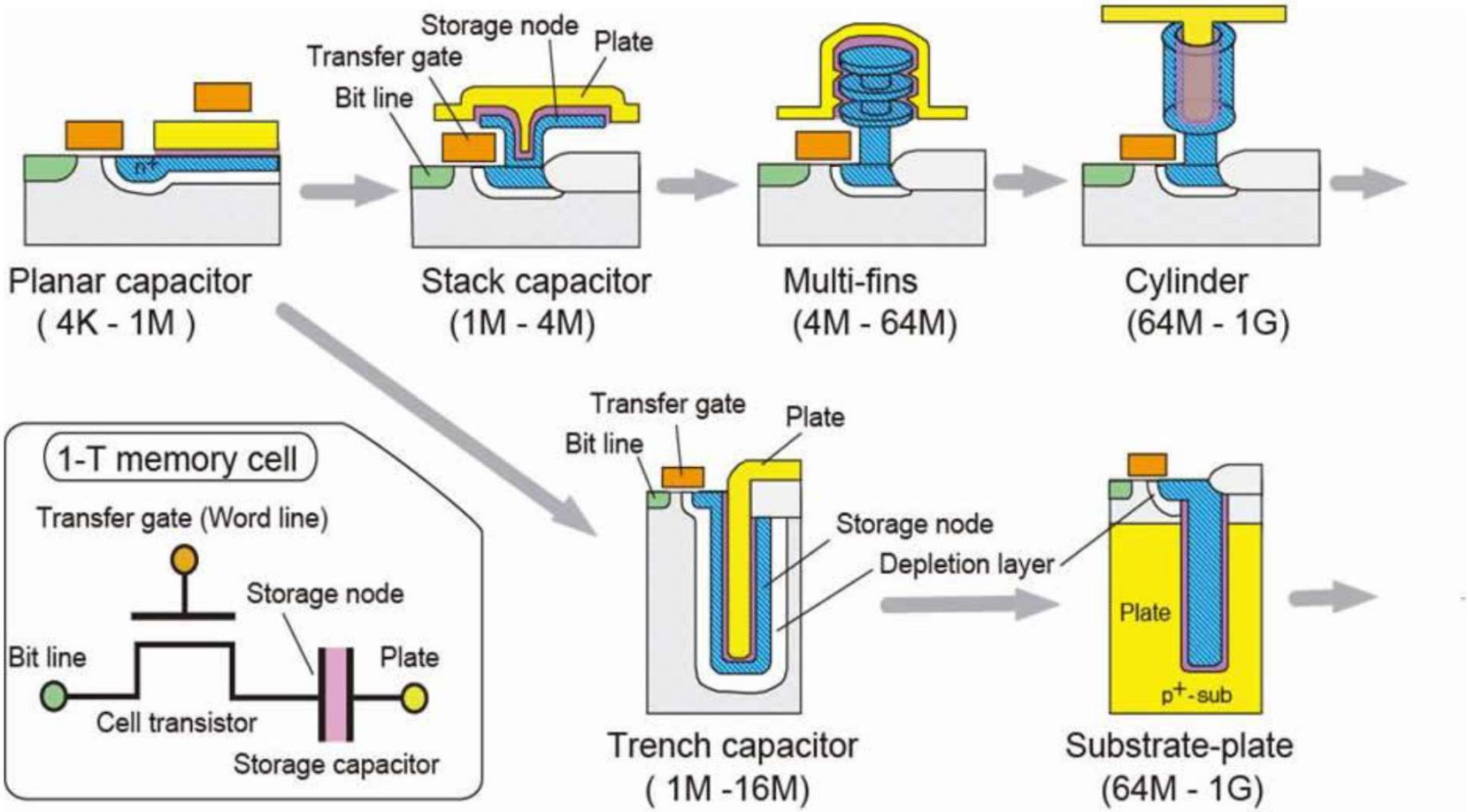
Trench Cell





Stacked-capacitor Cell

1T DRAM Capacitors



Periphery

- **Decoders**
- **Sense Amplifiers**
- **Input/Output Buffers**
- **Control / Timing Circuitry**

Row Decoders

Collection of 2^M complex logic gates
Organized in regular and dense fashion

(N)AND Decoder

$$WL_0 = A_0 A_1 A_2 A_3 A_4 A_5 A_6 A_7 A_8 A_9$$

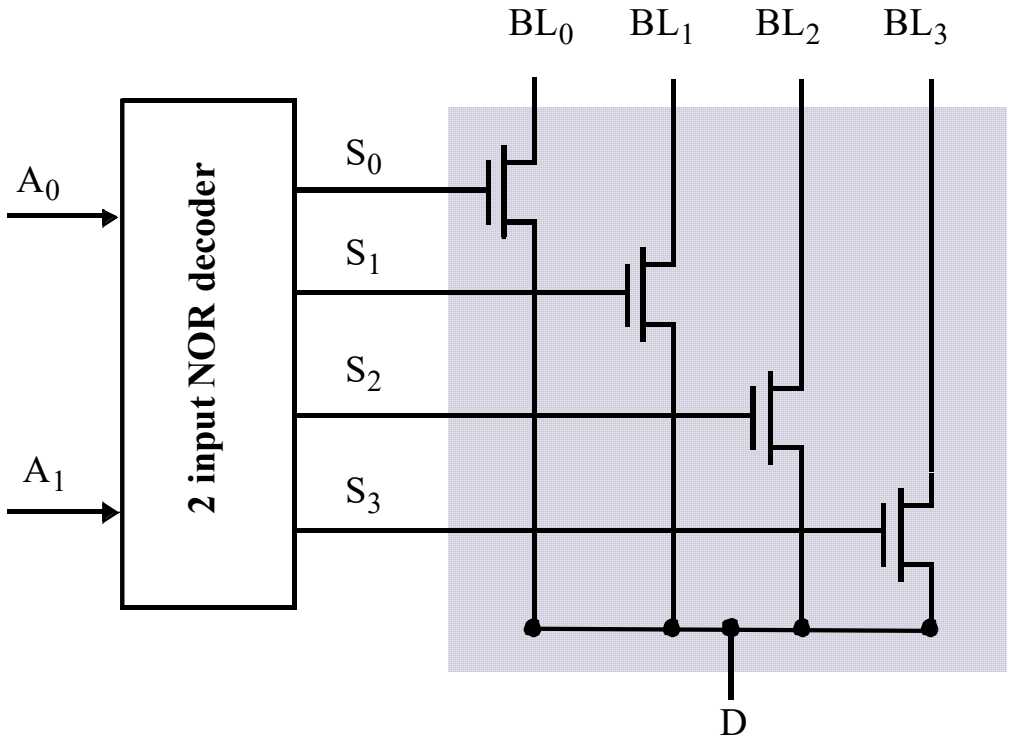
$$WL_{511} = \bar{A}_0 A_1 A_2 A_3 A_4 A_5 A_6 A_7 A_8 A_9$$

NOR Decoder

$$WL_0 = \overline{A_0 + A_1 + A_2 + A_3 + A_4 + A_5 + A_6 + A_7 + A_8 + A_9}$$

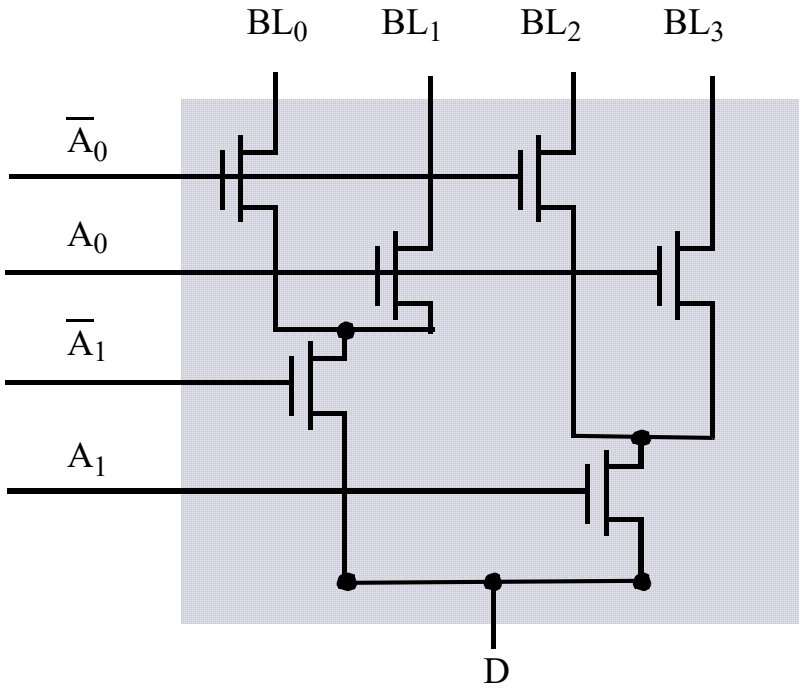
$$WL_{511} = \overline{A_0 + \bar{A}_1 + \bar{A}_2 + \bar{A}_3 + \bar{A}_4 + \bar{A}_5 + \bar{A}_6 + \bar{A}_7 + \bar{A}_8 + \bar{A}_9}$$

4 input pass-transistor based column decoder



lvantage: speed (t_{pd} does not add to overall memory access time)
only 1 extra transistor in signal path
sadvantage: large transistor count

4-to-1 tree based column decoder



Number of devices drastically reduced

Delay increases quadratically with # of sections; prohibitive for large decoders

Solutions: **buffers**

progressive sizing

combination of tree and pass transistor approaches

Sense Amplifiers

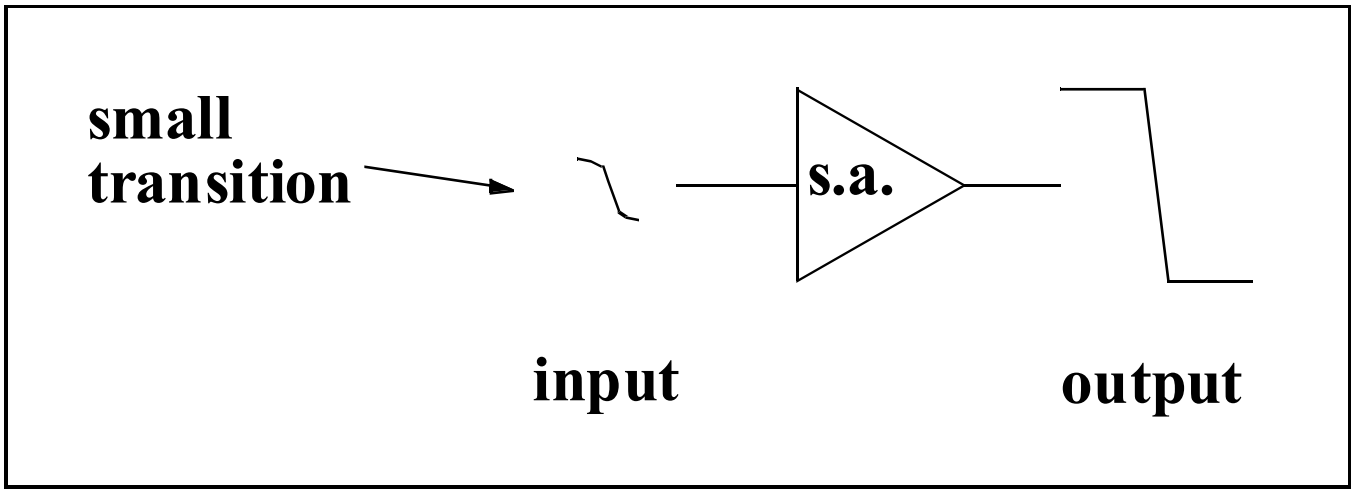
$$t_p = \frac{C \cdot \Delta V}{I_{av}}$$

make ΔV as small as possible

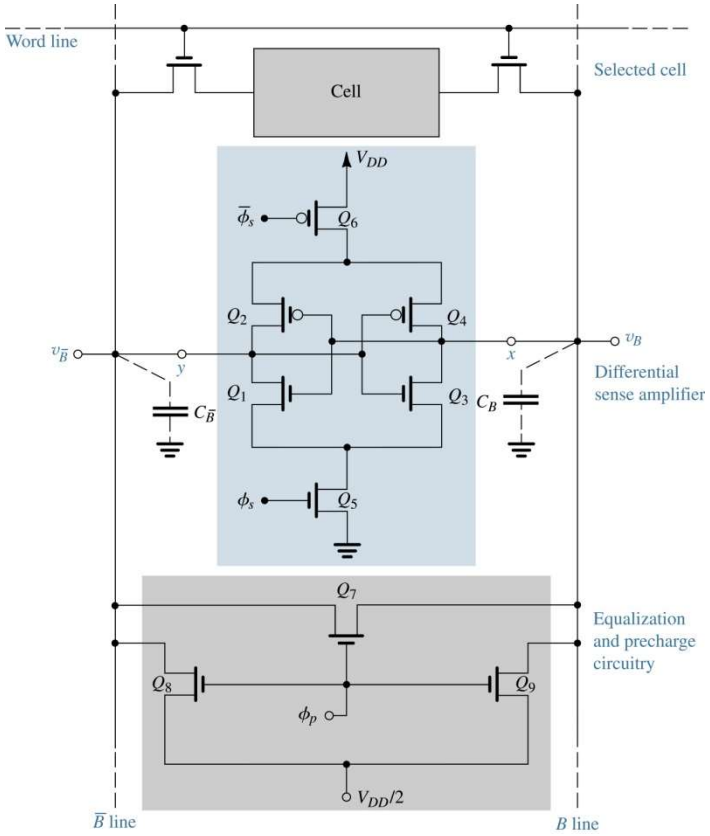
large

small

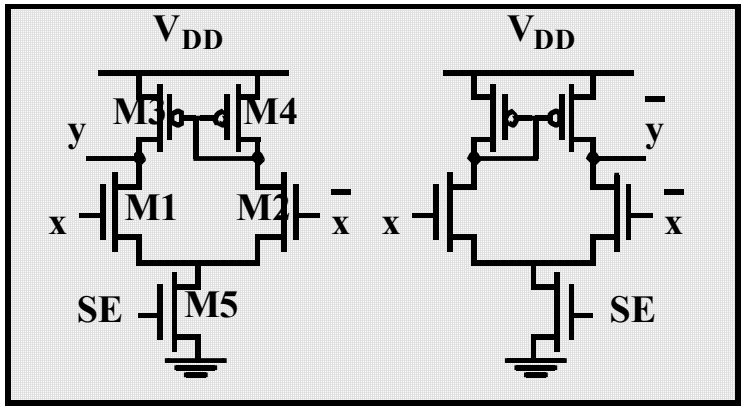
Idea: Use Sense Amplifer



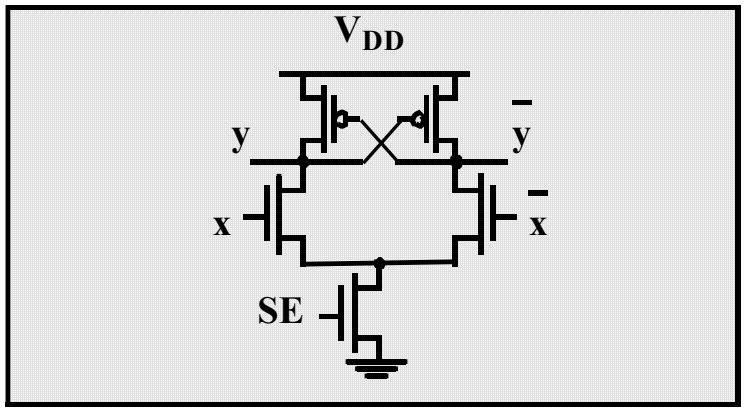
Differential Sensing - SRAM



(a) SRAM sensing scheme.

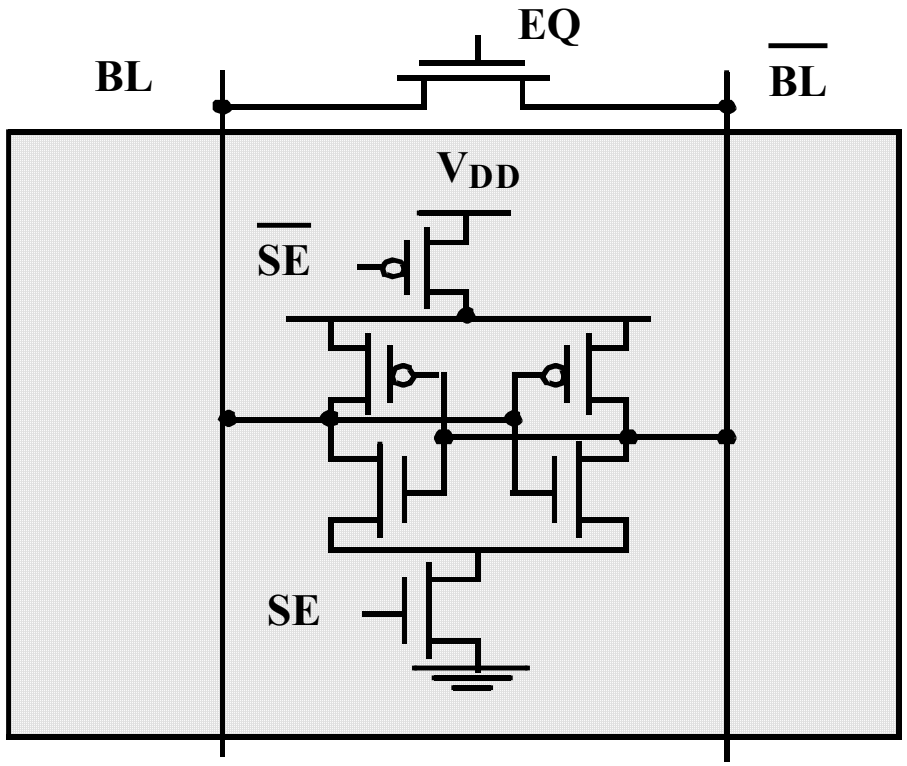


(b) Doubled-ended Current Mirror Amplifier



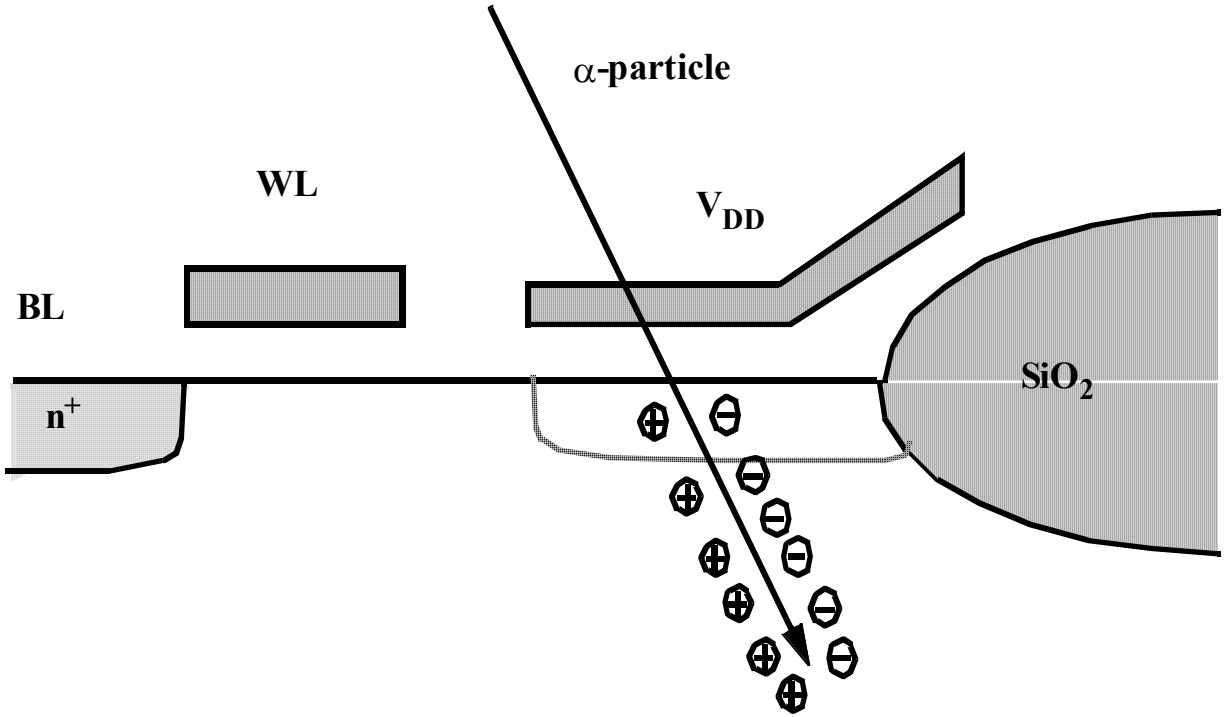
(c) Cross-Coupled Amplifier

Latch-Based Sense Amplifier



Initialized in its meta-stable point with EQ
Once adequate voltage gap created, sense amp enabled with SE
Positive feedback quickly forces output to a stable operating point.

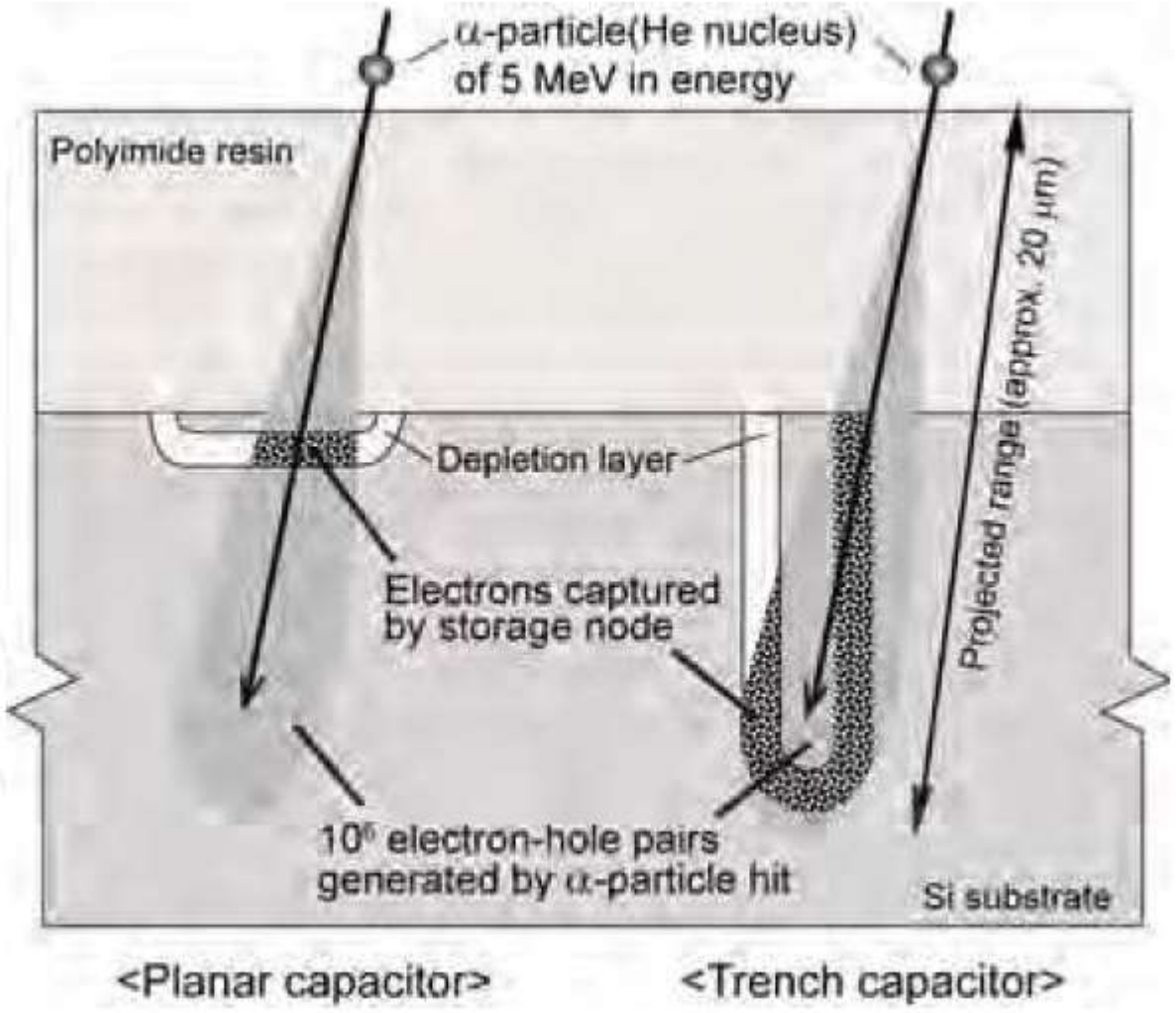
Alpha-particles



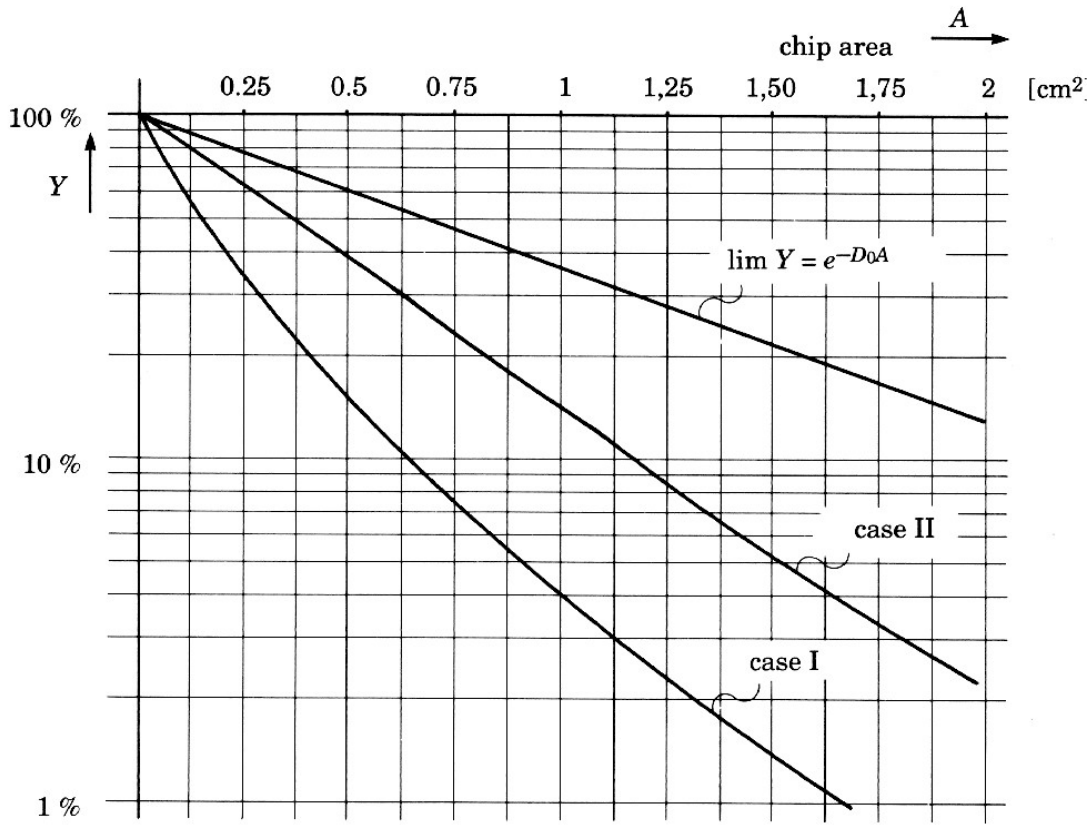
1 particle ~ 1 million carriers

Paper on soft error

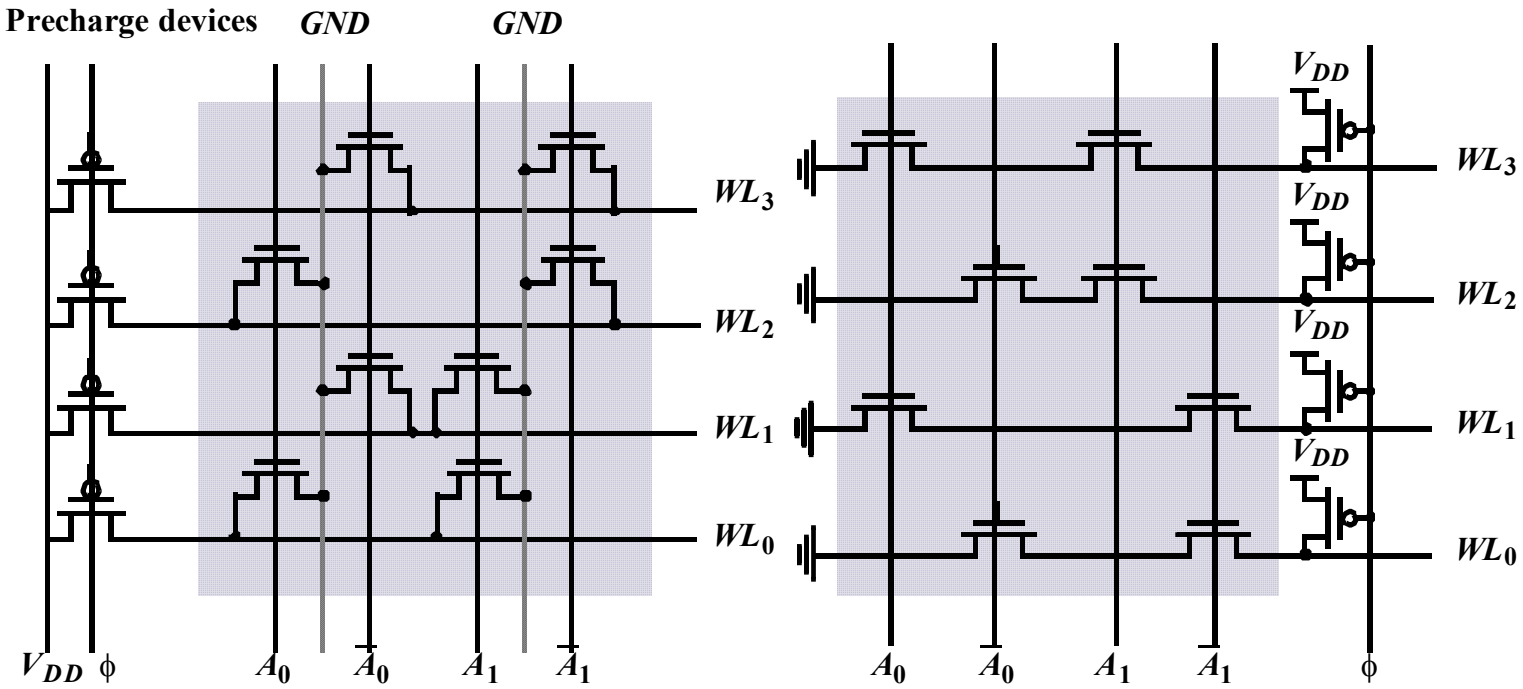
Alpha-particles



Yield


A
chip area
0.25
0.5
0.75
1
1,25
1,50
1,75
2
[cm²]
100 %
Y
10 %
1 %
lim Y = e^{-D0A}
case II
case I

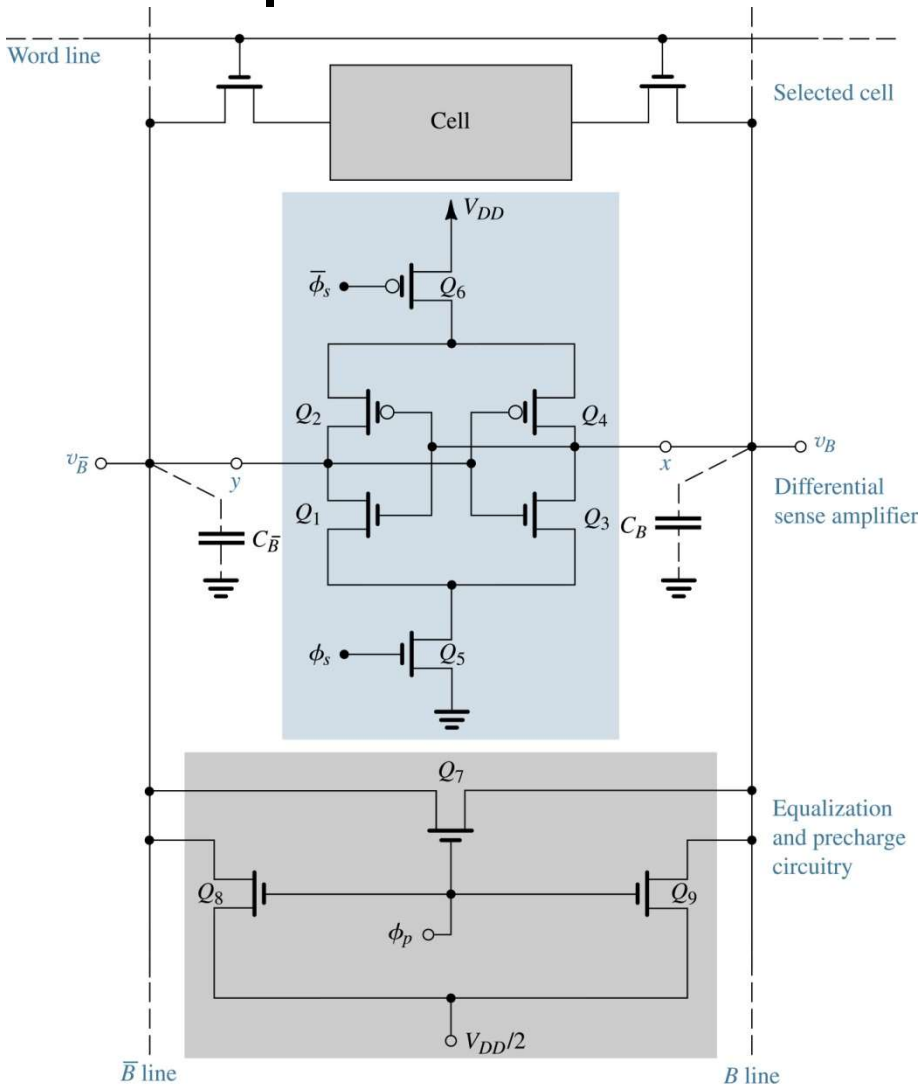
Dynamic Decoders

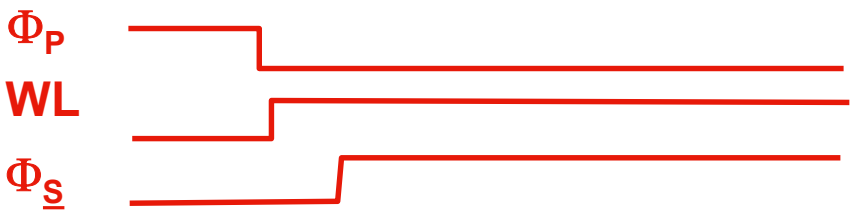


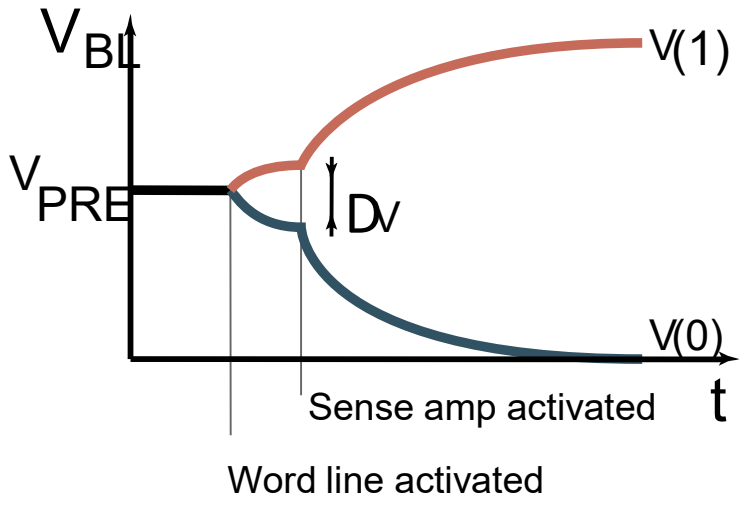
Dynamic 2-to-4 NOR decoder **2-to-4 MOS dynamic NAND Decoder**

Propagation delay is primary concern

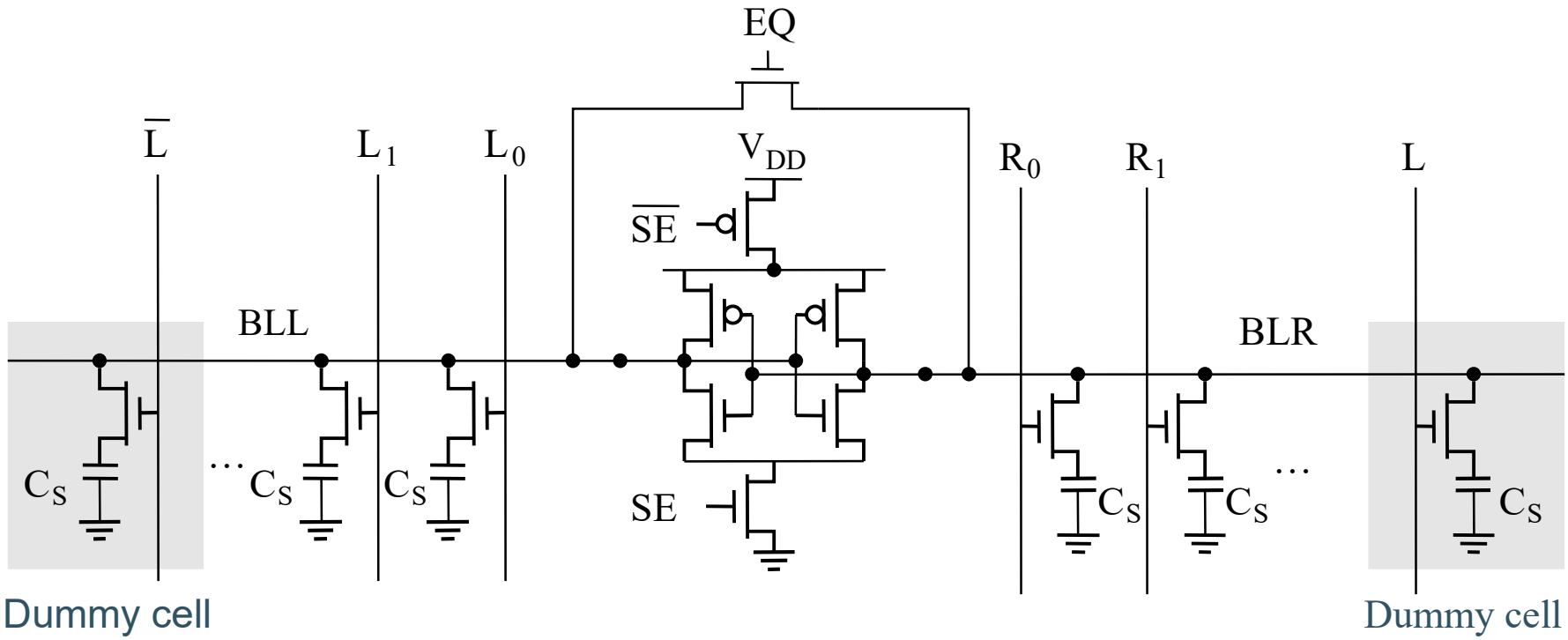
Differential Sensing - SRAM



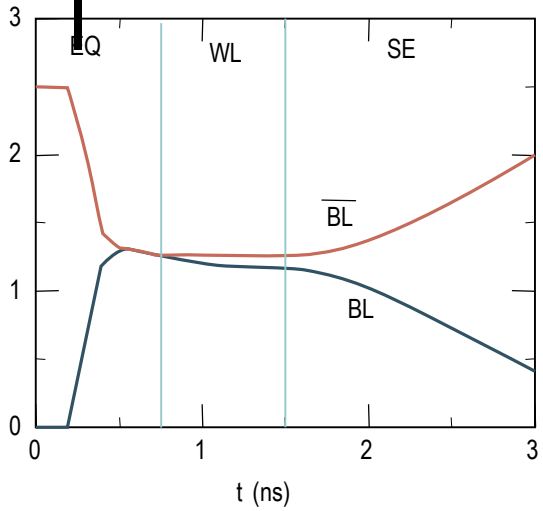




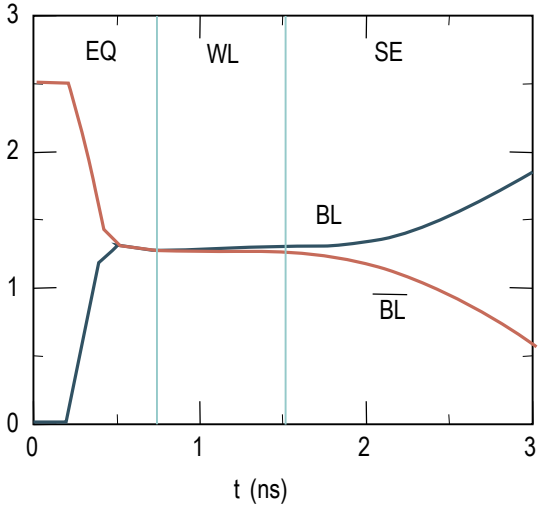
Open bitline architecture



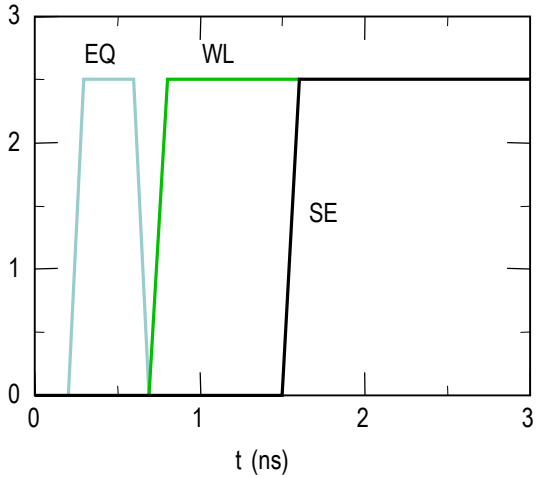
DRAM Read Process with Dummy Cell



reading 0

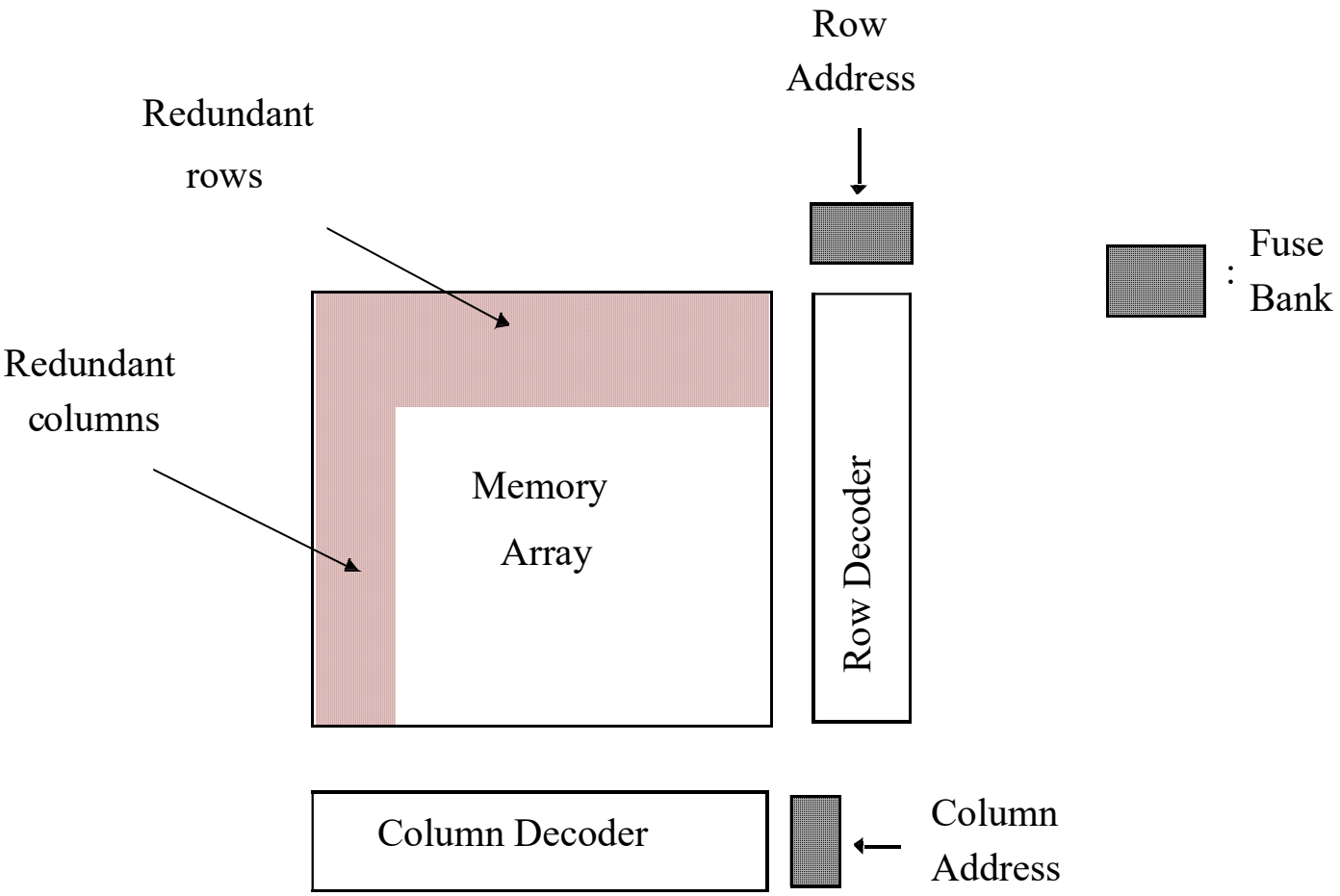


reading 1



control signals

Redundancy


Row
Address
Redundant
rows
Redundant
columns
Memory
Array
Row Decoder
Fuse
Bank
Column Decoder
Column
Address

Redundancy and Error Correction