



Dispositivi elettronici

Circuiti elettronici → Dispositivi Elettronici → non lineari

Dispositivi elettronici moderni → Dispositivi a stato solido
(es. transistori MOS, diodi)

Dispositivi a stato solido → **Tecnologia planare**

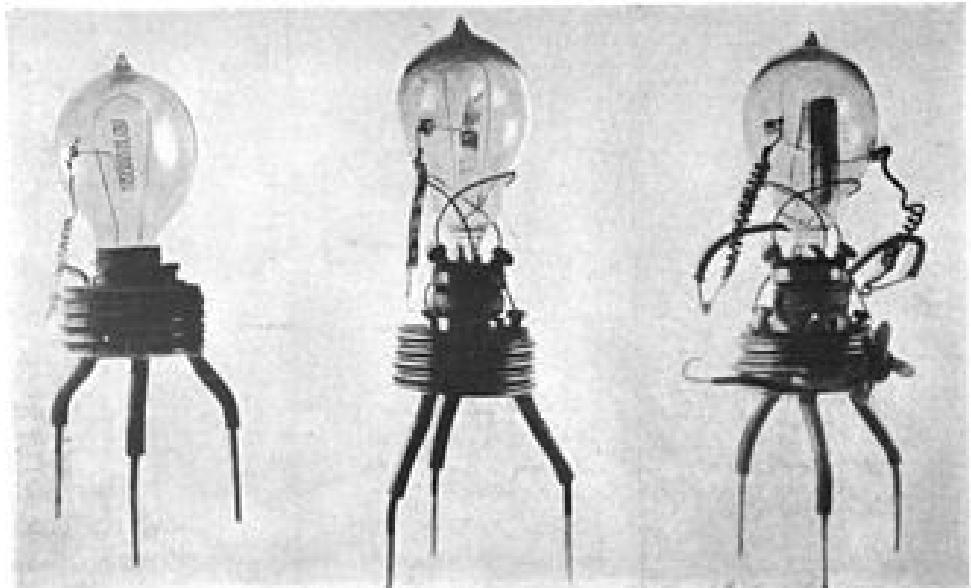


Dispositivi elettronici



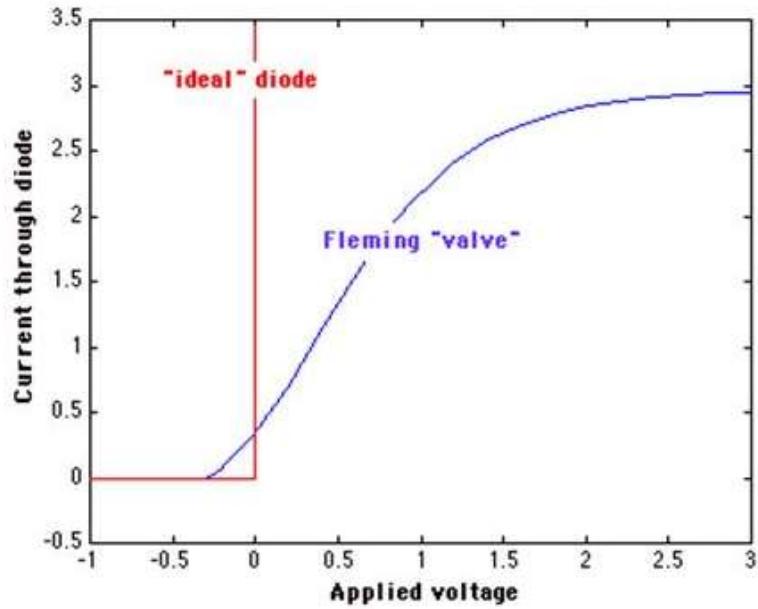
John Ambrose Flaming (1849-1945)

Diodo di Flaming (1904)

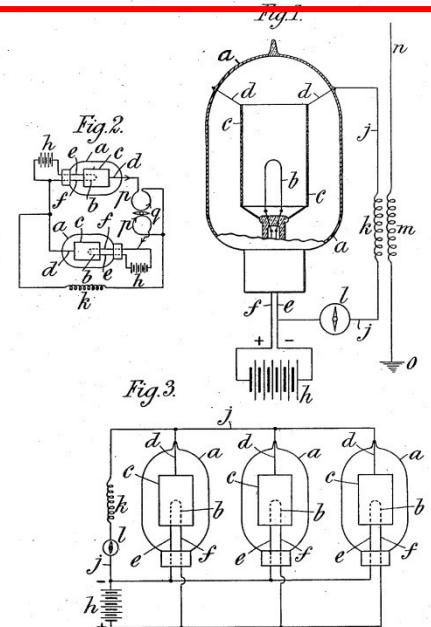




Dispositivi elettronici



No. 803,684.
PATENTED NOV. 7, 1905.
J. A. FLEMING.
INSTRUMENT FOR CONVERTING ALTERNATING ELECTRIC CURRENTS
INTO CONTINUOUS CURRENTS.
APPLICATION FILED APR. 19, 1905.



Witnesses
William H. Davis
James F. Grayson

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by his attorney
Wm. G. Shiffman, Atto

No. 803,684.

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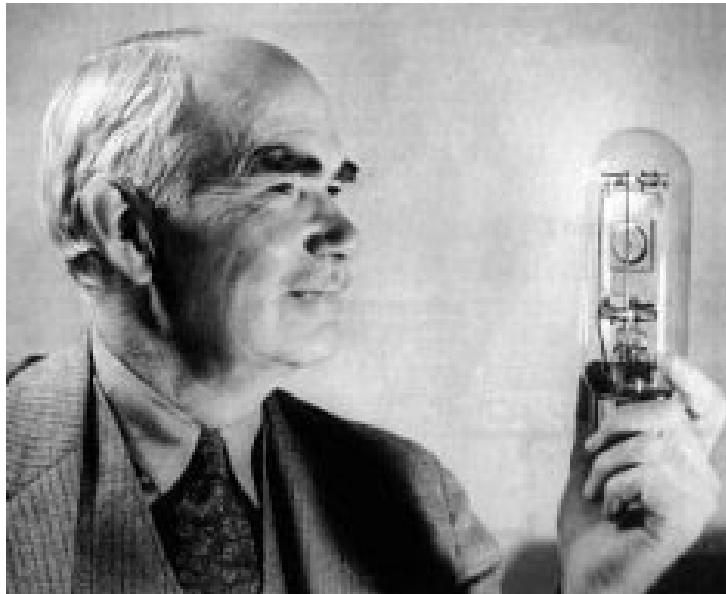
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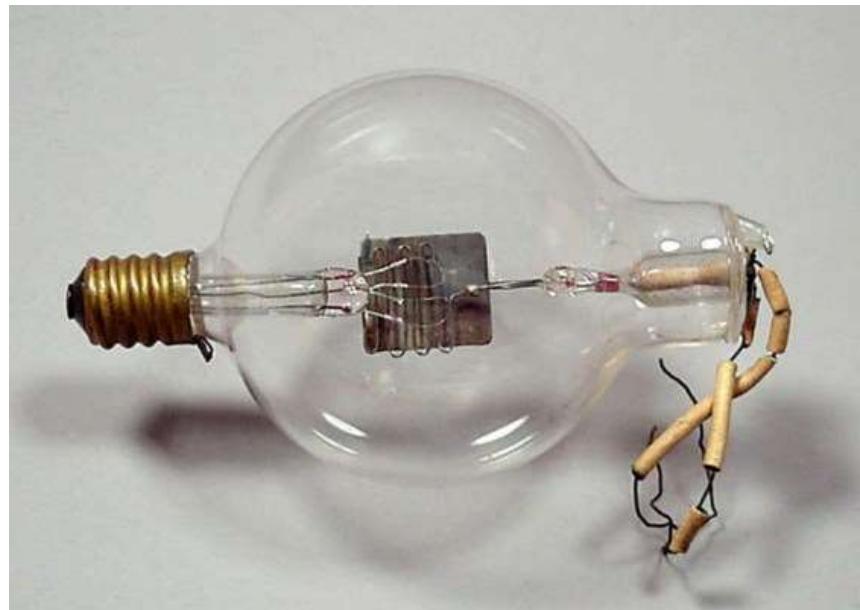


Dispositivi elettronici

Triodo di de Forest (Audion) 1906



Lee de Forest (1873-1961)





Dispositivi elettronici





Dispositivi elettronici

ENIAC (1946)
(Electronic Numerical Integrator and Calculator)
Scopo : calcoli balistici



Tecnologia : valvole termoioniche
Circuito: 18000 valvole, 1500 Relè
Consumo : 150 KW
MTBF : 1-2 giorni
Costo finale: 500.000 \$
Peso: 30 tons
Ingombro: 180 mq

Memoria: 20 numeri 10 cifre
Capacità di calcolo : 5 KFLOPS



Dispositivi elettronici a stato solido



Figura 1.1

John Bardeen, William Shockley e Walter Brattain nel laboratorio di Brattain nel 1948.

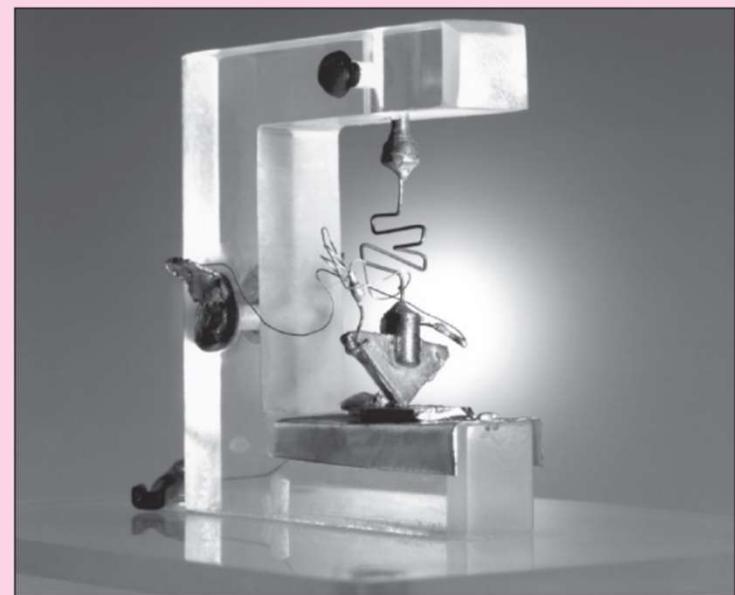


Figura 1.2

Il primo transistore bipolare al germanio.



Dispositivi elettronici

Figura 1.3

(a) Tubi a vuoto, (b) transistori,
(c) circuiti integrati ad alta
densità in package dual-in-line,
(d) circuiti integrati in package
surface mount [Mark J. Wilson,
American Radio Relay League,
The ARRL Handbook, 1992.]



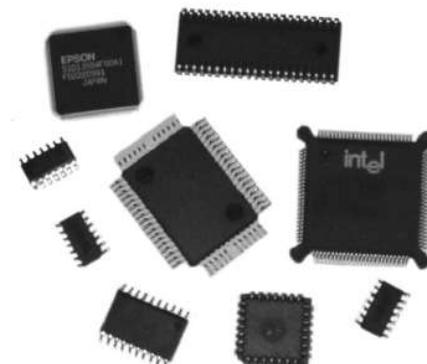
(a)



(b)



(c)



(d)



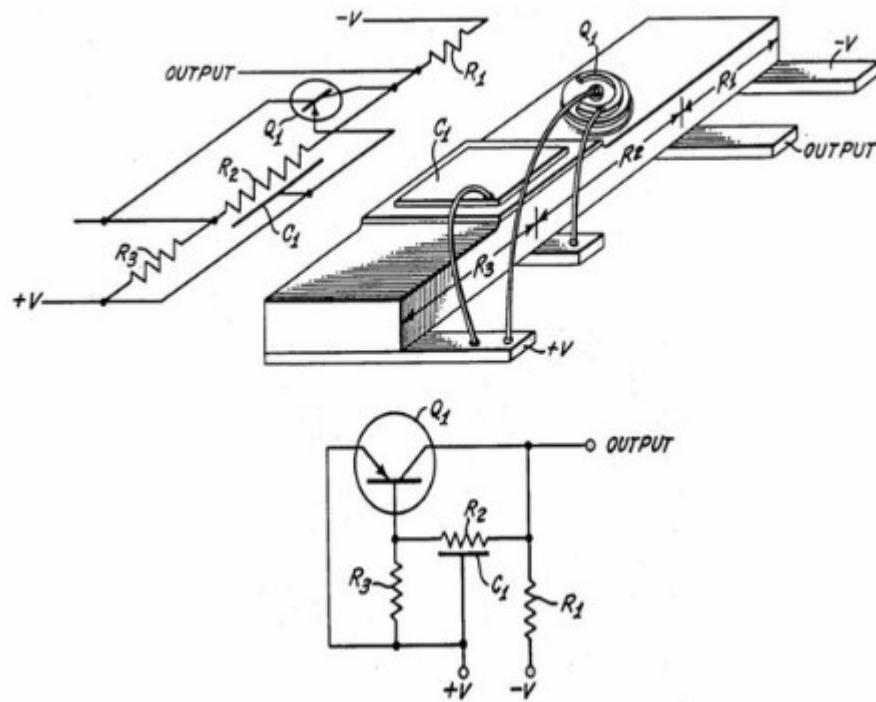
Apparati elettronici a stato solido



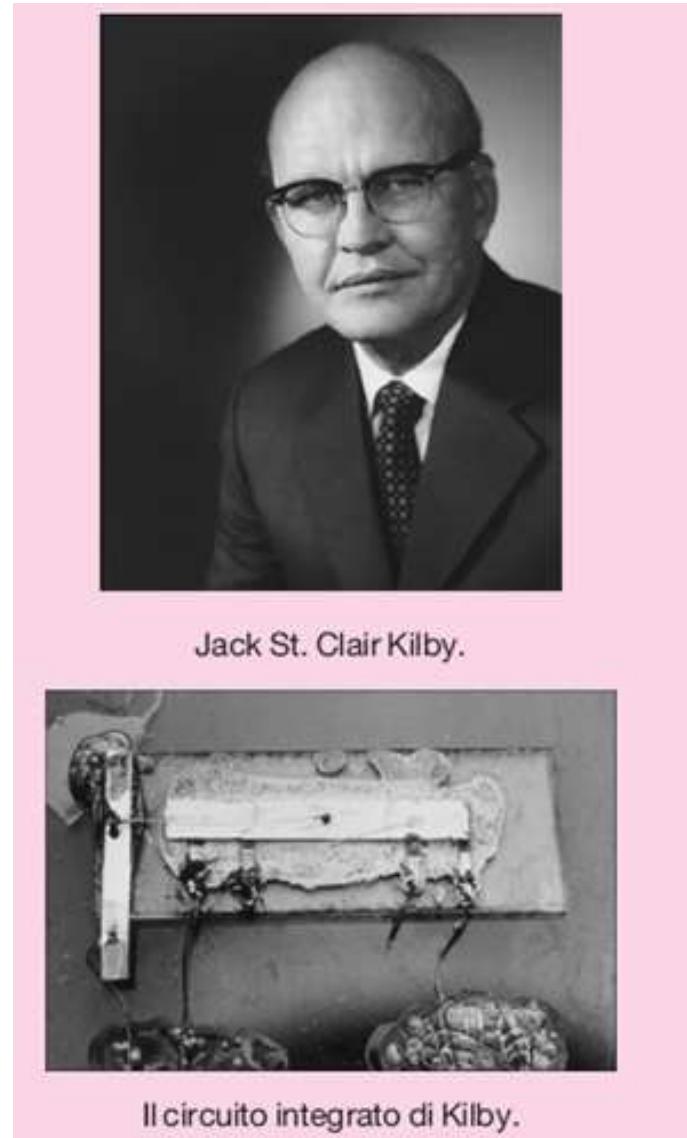


1958

Circuiti integrati



Oscillatore sinusoidale - Germanio



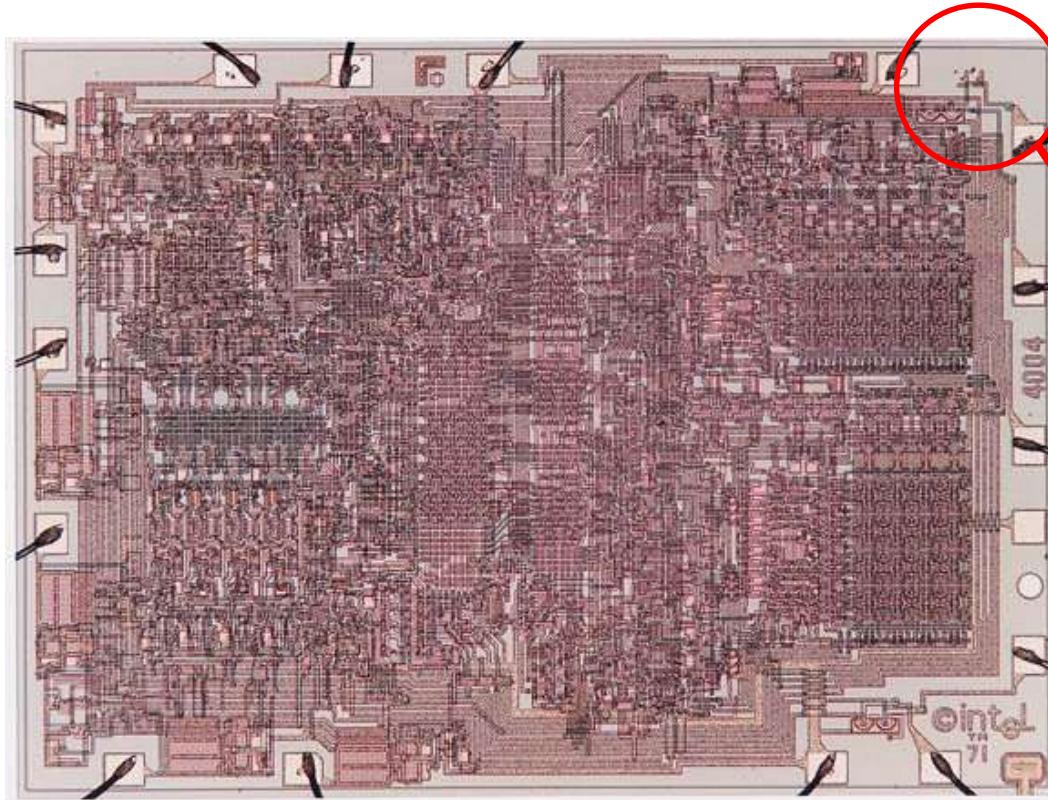
Jack St. Clair Kilby.

Il circuito integrato di Kilby.



1972

Circuiti integrati – Tecnologia “planare”



Federico Faggin

Intel 4004 (2300 transistori MOS, tecnologia 10 μ m)



Circuiti integrati

Busicom 141-PF

Impiega il chipset MCS-4
di cui fa parte la CPU 4004

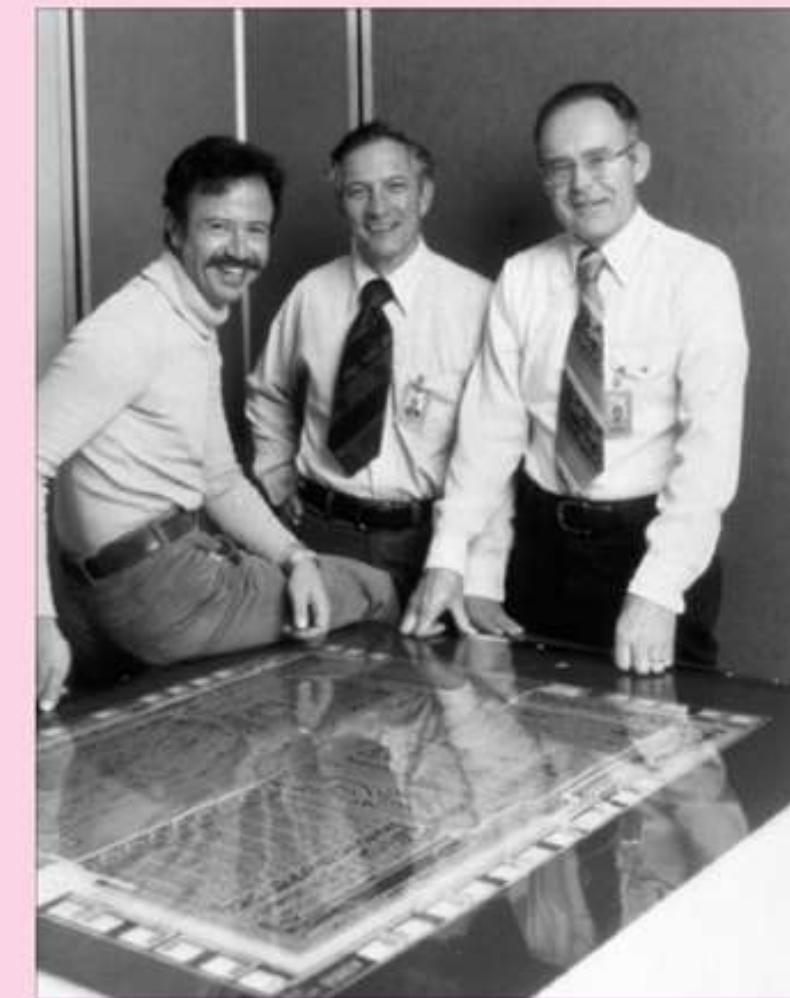




1978

Intel 8080

Circuiti integrati

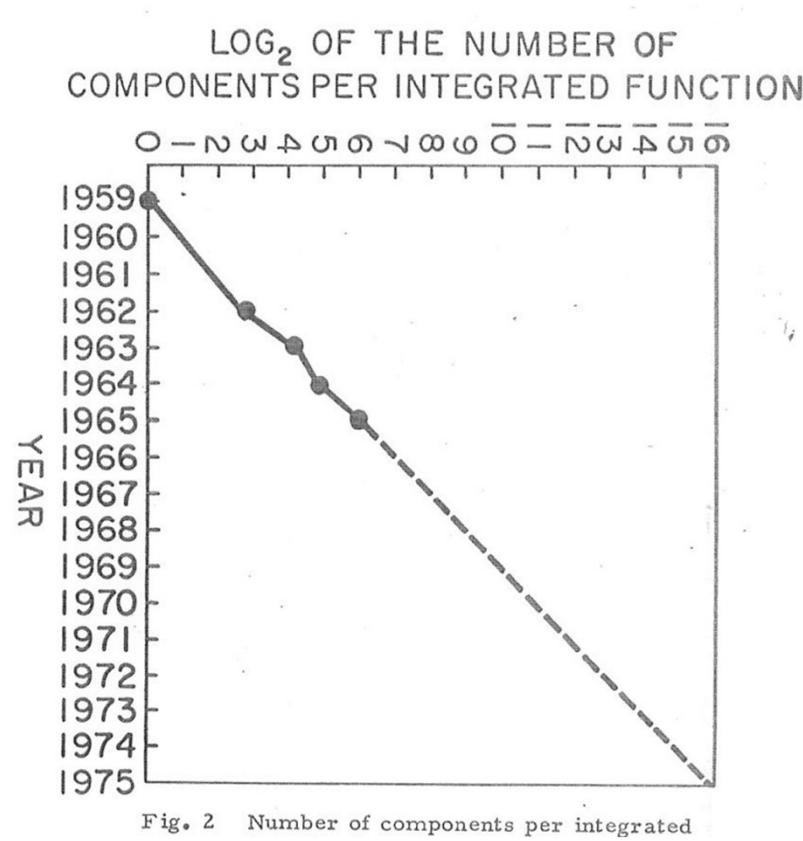


And Grove, Robert Noyce e Gordon Moore con le maschere del processore Intel 8080 nel 1978.



Legge di Moore (empirica - 1965)

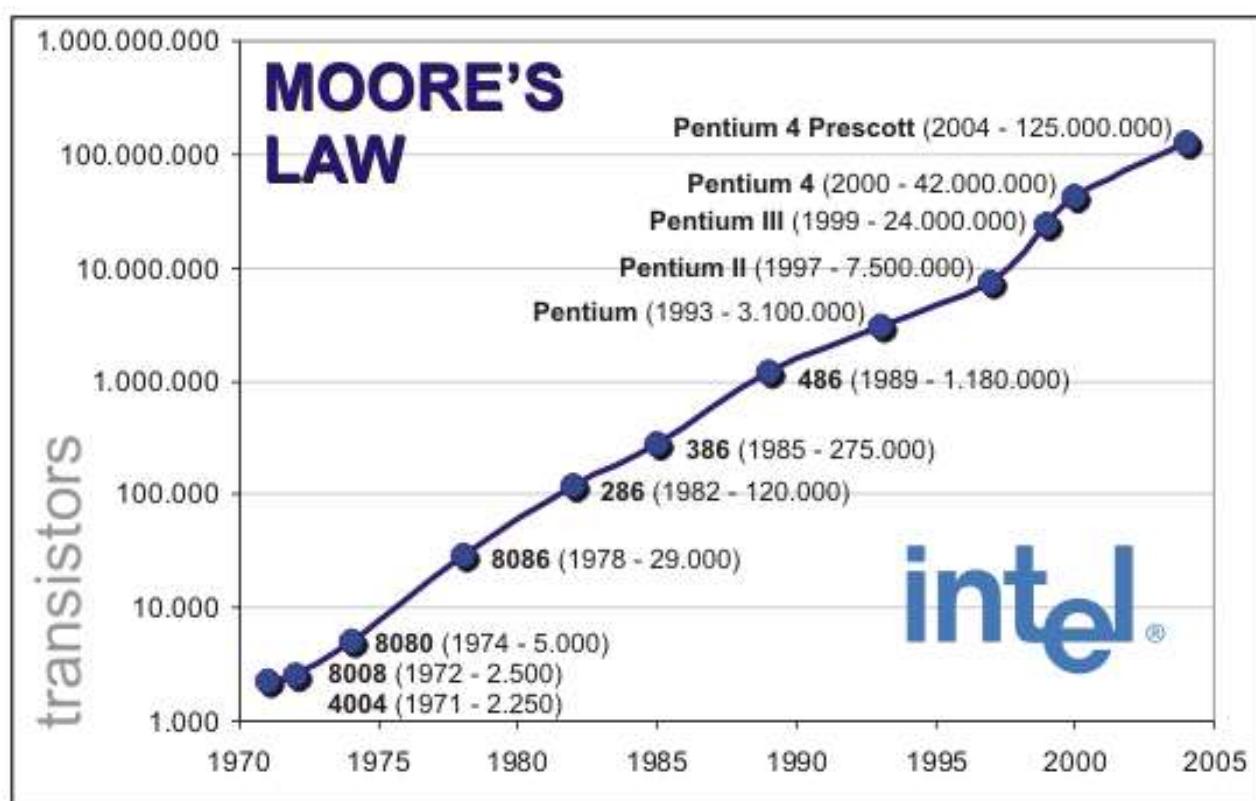
“La complessità di un circuito integrato espressa in numero di transistori per singolo die raddoppia ogni 18 mesi”





Legge di Moore (empirica)

“ La complessità di un circuito integrato espressa in numero di transistori per singolo die raddoppia ogni 18 mesi ”



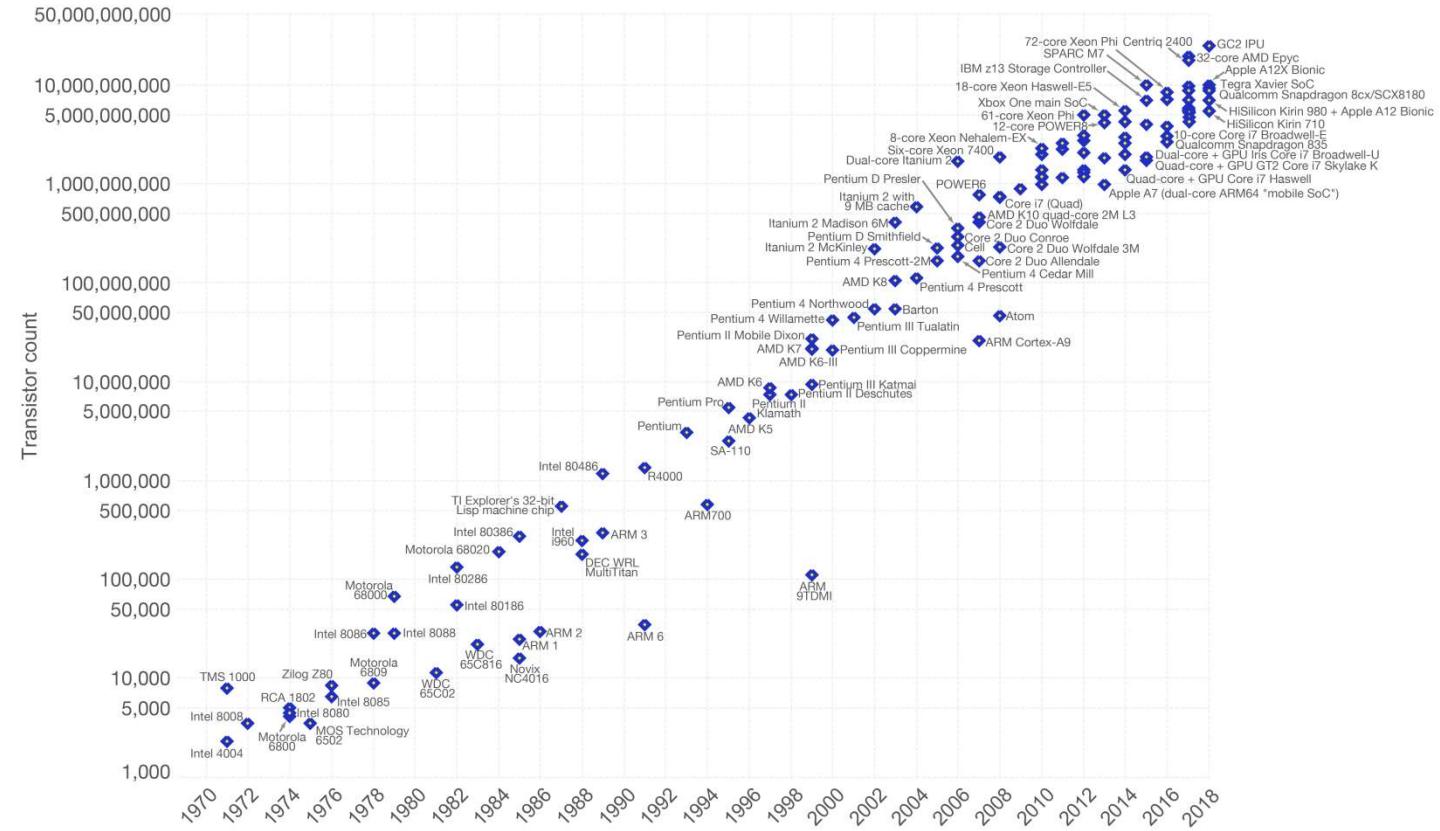


Legge di Moore (empirica)

OurWorld
in Data

Moore's Law – The number of transistors on integrated circuit chips (1971-2018)

Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important as other aspects of technological progress – such as processing speed or the price of electronic products – are linked to Moore's law.



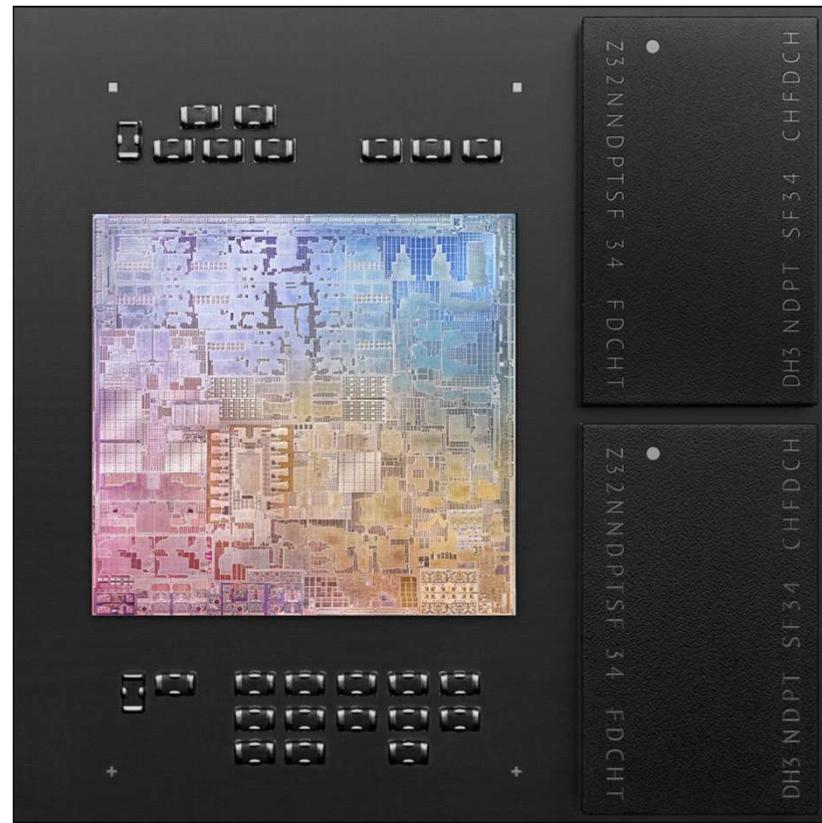
Data source: Wikipedia (https://en.wikipedia.org/wiki/Transistor_count)

The data visualization is available at OurWorldinData.org. There you find more visualizations and research on this topic.

Licensed under CC-BY-SA by the author Max Roser.

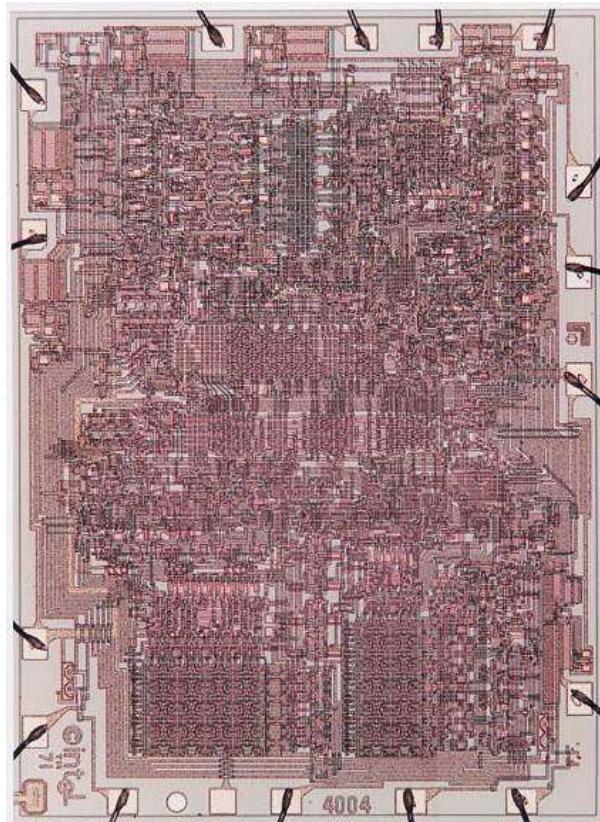


System on Chip (SoC)

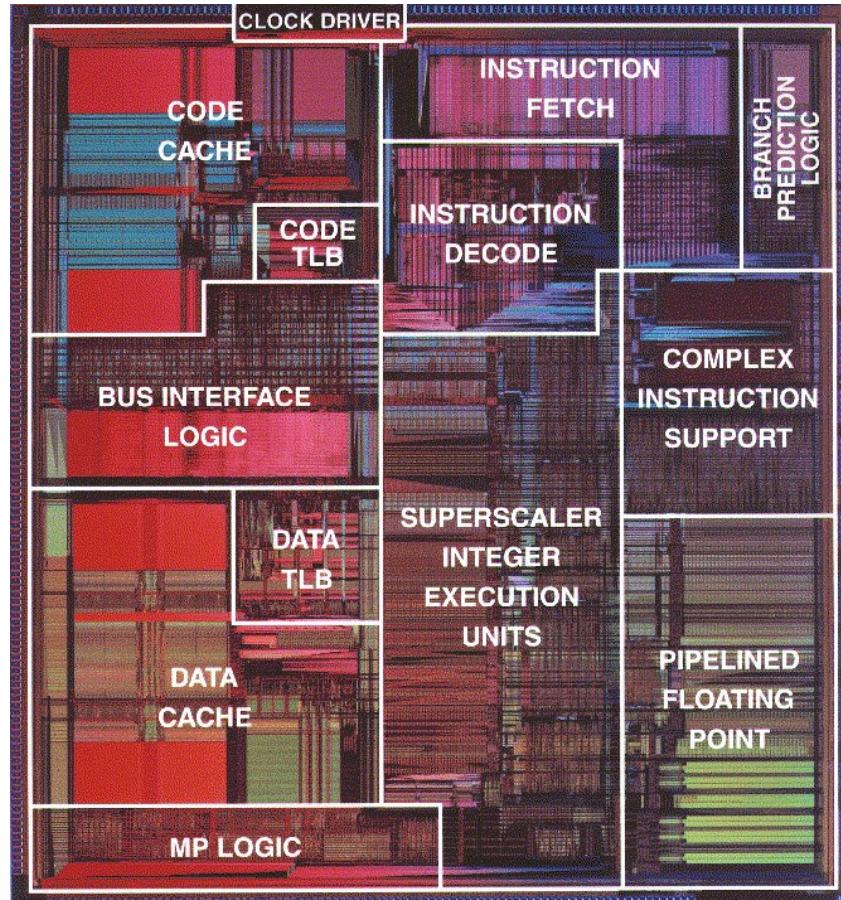


Apple M1 – 16×10^9 transistor 5nm technology

Progettazione layout



Intel 4004 (1972)
2300 transistors
Tecnologia 10 µm



Pentium (1995)
3.100.000 transistors
Tecnologia 0.25 µm

Dispositivi elettronici a stato solido

Tabella 2.1

Classificazione in base alla resistività dei materiali a stato solido

Materiale	Resistività ($\Omega \cdot \text{cm}$)
Isolanti	$10^5 < \rho$
Semiconduttori	$10^{-3} < \rho < 10^5$
Conduttori	$\rho < 10^{-3}$

Tabella 2.2 Sezione della tavola periodica in cui vengono mostrati i semiconduttori elementari più importanti (riquadri ombreggiati)

	IIIA	IVA	VA	VIA
5	10.811 B Boro	12.01115 C Carbonio	14.0067 N Azoto	18.9994 O Ossigeno
13	26.9815 Al Alluminio	28.086 Si Silicio	30.9738 P Fosforo	32.064 S Zolfo
30	65.37 Zn Zinco	69.72 Ga Gallo	72.59 Ge Germanio	74.922 As Arsenico
48	112.40 Cd Cadmio	114.82 In Indio	118.69 Sn Stagno	121.75 Sb Antimonio
80	200.59 Hg Mercurio	204.37 Ti Talio	207.19 Pb Piombo	208.980 Bi Bismuto
				(210) Po Polonio



Dispositivi elettronici a stato solido

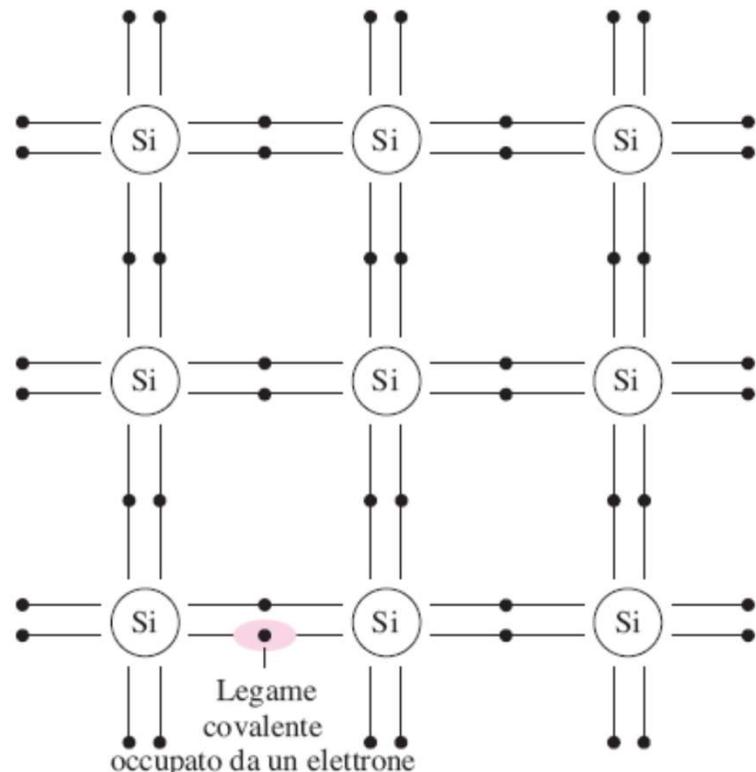


Figura 2.2 Rappresentazione bidimensionale del reticolo cristallino del silicio e dei legami covalenti. Per temperature prossime a 0 K tutti i legami sono soddisfatti, e gli orbitali più esterni sono completi.

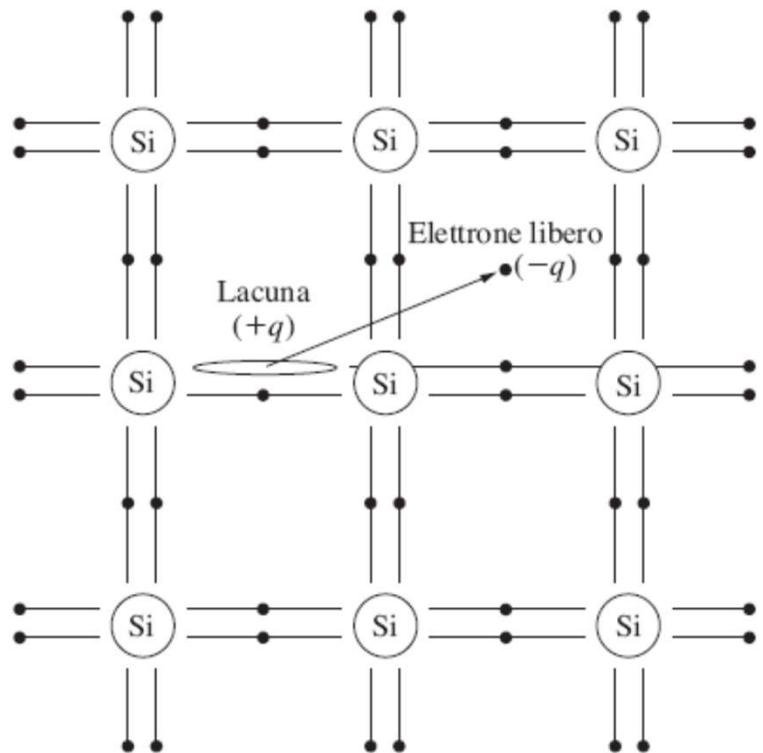


Figura 2.3 Formazione di una coppia elettrone-lacuna in seguito alla rottura di un legame covalente.



Dispositivi elettronici a stato solido

Numero di elettroni liberi $n \rightarrow$ concentrazione intrinseca n_i

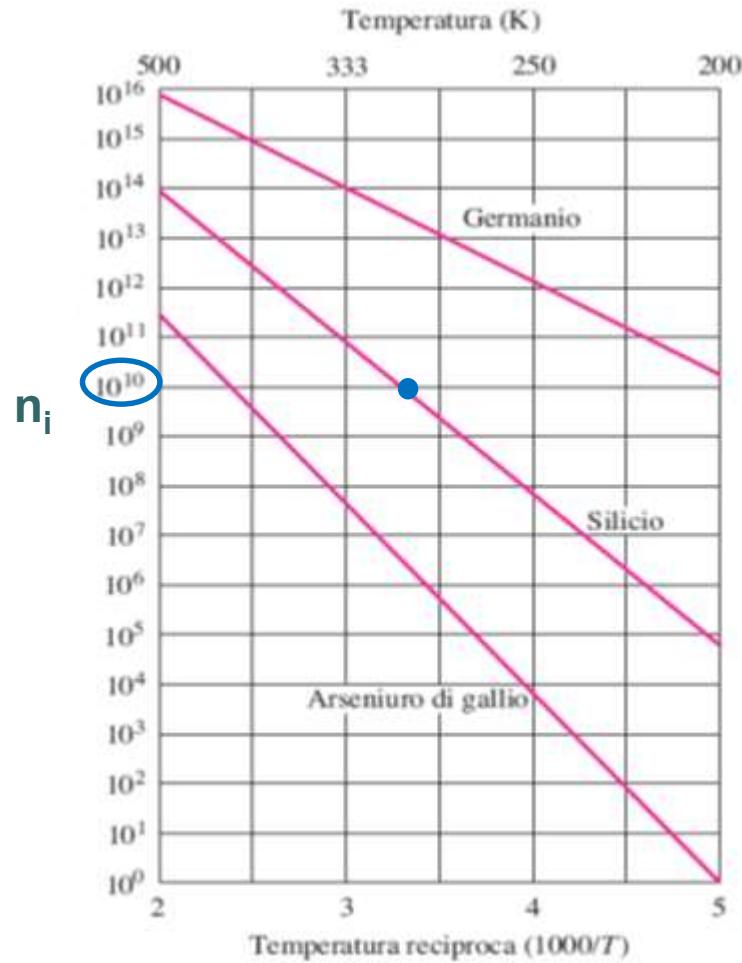
$$n_i^2 = B T^3 \exp(-E_G/kT)$$

Semiconduttore intrinseco : $n = n_i = p$

$$\rightarrow p \cdot n = n_i^2$$



Dispositivi elettronici a stato solido



Silicio @ 300K : $n_i \approx 10^{10} \text{ [cm}^{-3}]$

$\rightarrow p = n = n_i \approx 10^{10} \text{ [cm}^{-3}]$

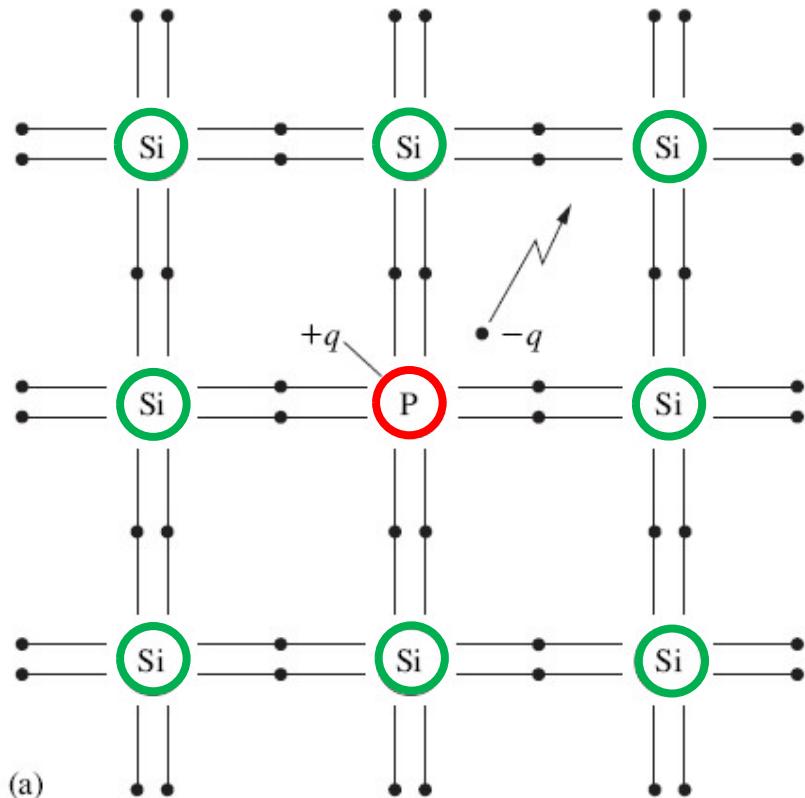
$$\rho = 3.3 \cdot 10^5 \text{ } \Omega \cdot \text{cm}$$

$$(n_i^2 \approx 10^{20} \text{ [cm}^{-6}])$$

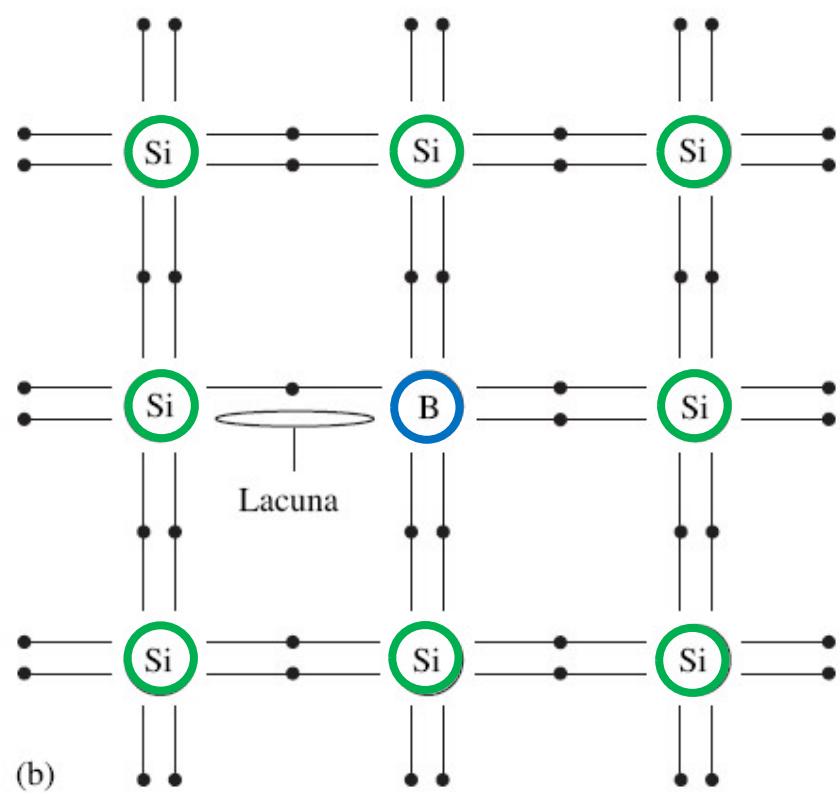
Dispositivi elettronici a stato solido

Tabella 2.2 Sezione della tavola periodica in cui vengono mostrati i semiconduttori elementari più importanti (riquadri ombreggiati)

IIIA	IVA	VA	VIA
10.811 Boro	12.01115 Carbonio	5 N	8 O
13 Aluminio	26.9815 Silicio	14 Silicio	16 Zolfo
	28.086 Fosforo	15 Fosforo	
30 Zinco	69.72 Gallo	33 Germanio	34 Selenio
48 Cadmio	114.82 Indio	50 Stagno	52 Tellurio
80 Mercurio	200.99 Talio	82 Piombo	84 Polonio
	204.37 Mercurio	207.19 Piombo	(210) Bismuto



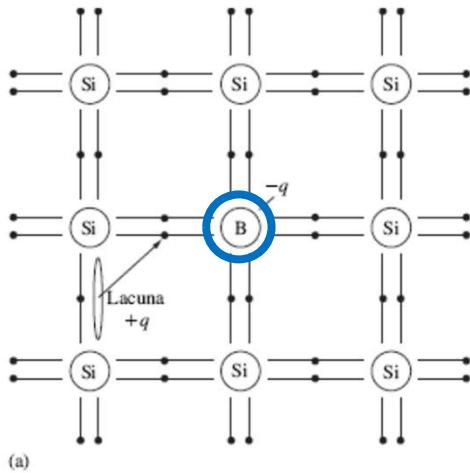
N_D atomi di fosforo



N_A atomi di boro

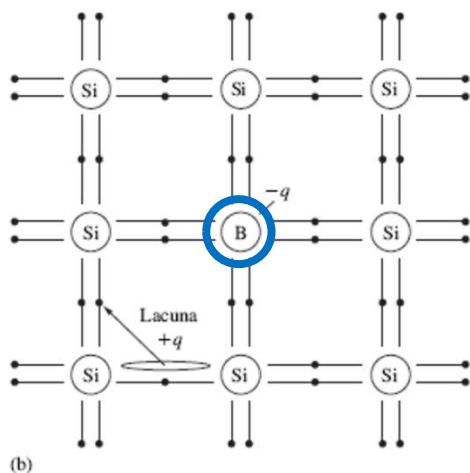


Dispositivi elettronici a stato solido



(a)

Moto di una lacuna



(b)

Figura 2.7 (a) Formazione di una lacuna in seguito al passaggio di un elettrone da un atomo di silicio a uno di accettore (boro). (b) Moto della lacuna nel reticolo cristallino del silicio.



Dispositivi elettronici a stato solido

Semiconduttore drogato con $N_D > N_A$ (tipo n):

$$\left. \begin{array}{l} p \cdot n = n_i^2 \\ n \approx N_D - N_A \end{array} \right\} \rightarrow p = n_i^2 / (N_D - N_A)$$

Esempio: se $N_D = 10^{18} \text{ [cm}^{-3}\text{]}$ e $N_A = 10^{14} \text{ [cm}^{-3}\text{]}$

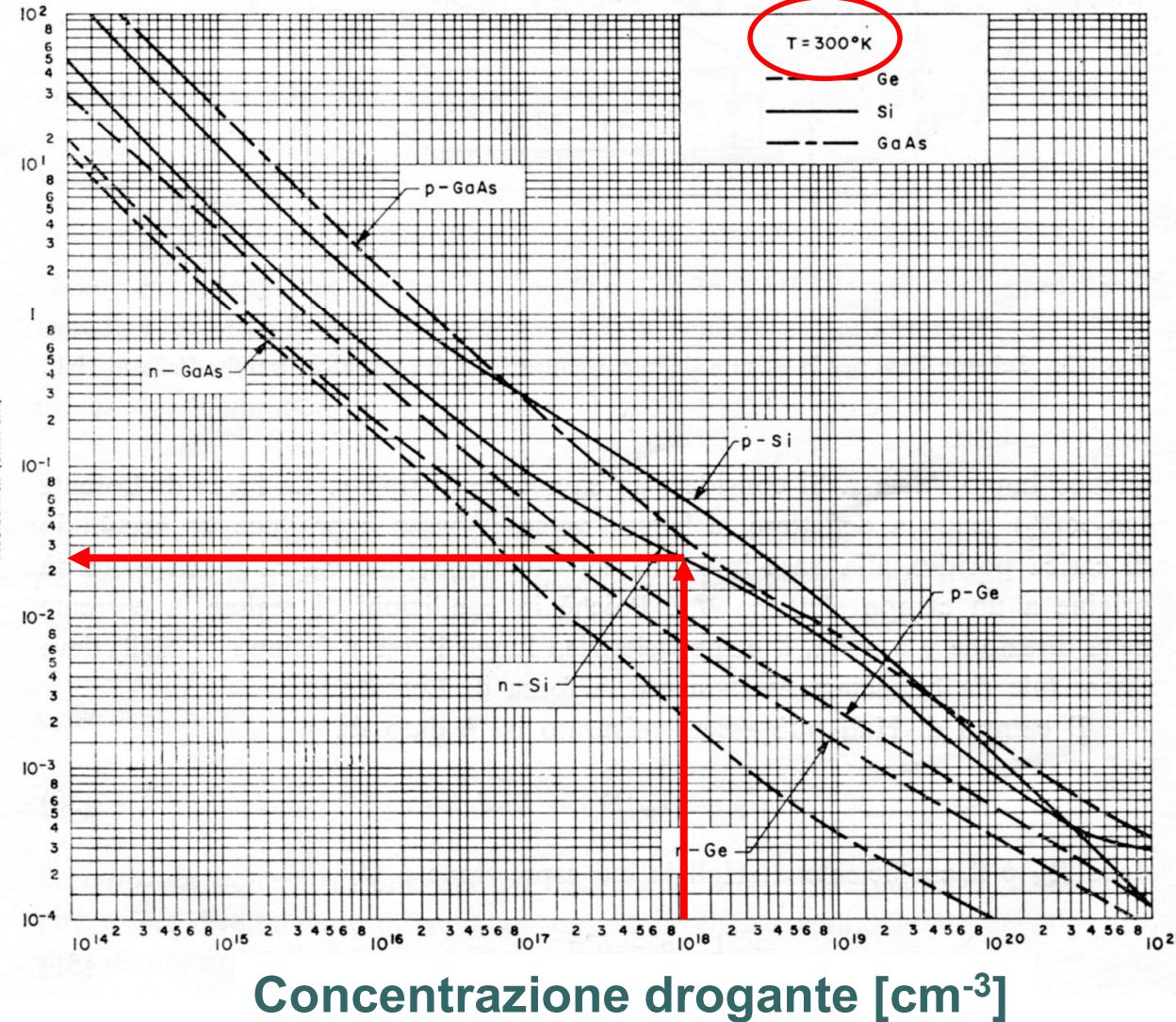


allora $n \approx 10^{18} \text{ [cm}^{-3}\text{]}$ e $p \approx 10^2 \text{ [cm}^{-3}\text{]}$ $\rightarrow p + n \approx 10^{18} \text{ [cm}^{-3}\text{]}$



Dispositivi elettronici a stato solido

Resistività [Ohm·cm]



Esempio:

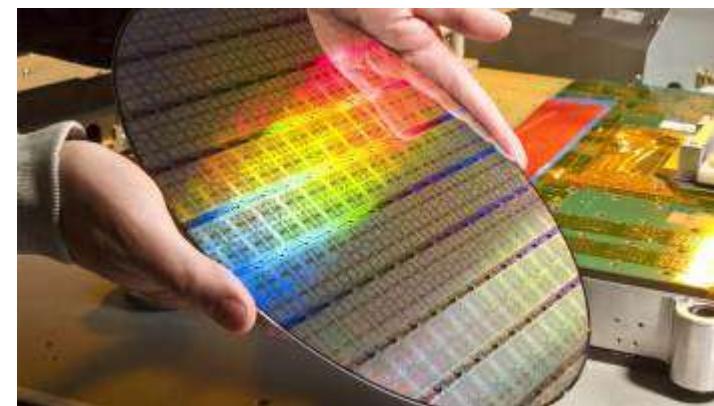
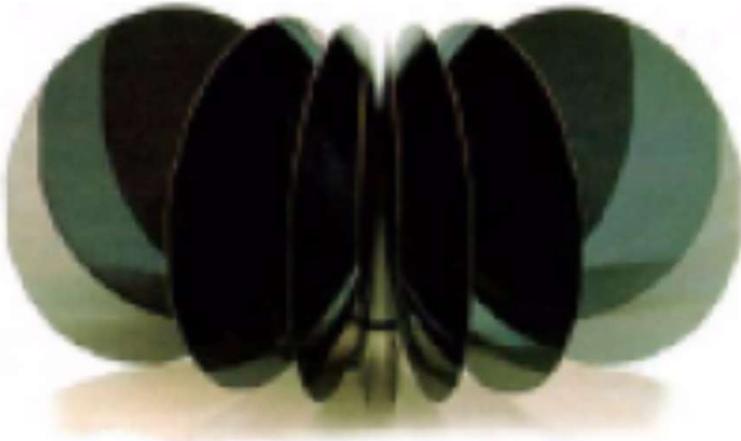
$n\text{-Si } N_D = 10^{18}$



$$\rho \approx 2 \times 10^{-2} \Omega \cdot \text{cm}$$

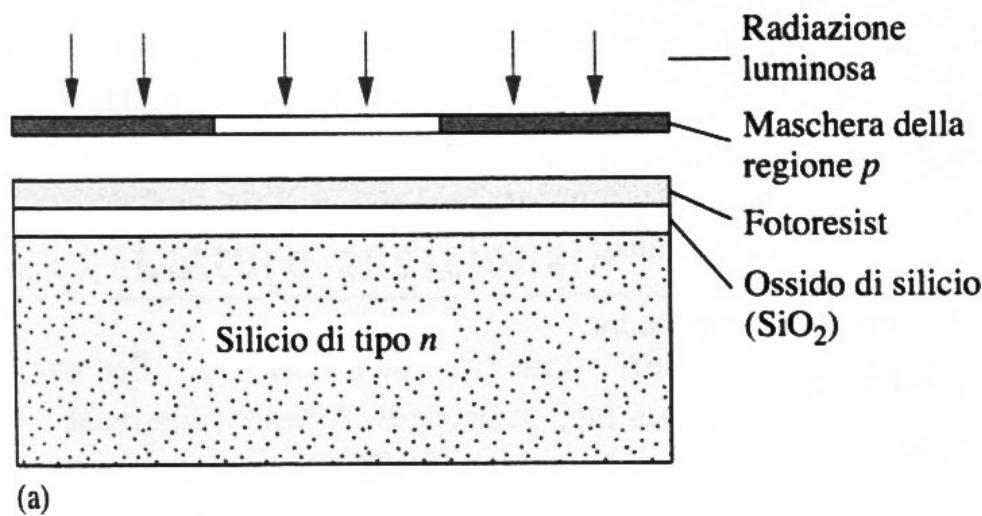


Tecnologia planare

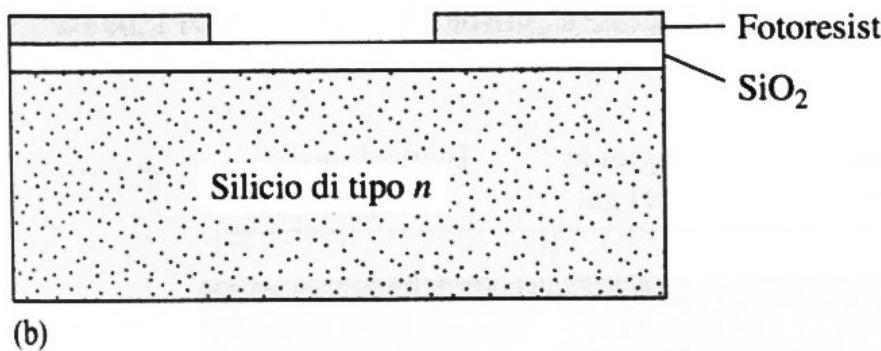




Giunzione p-n (silicio)



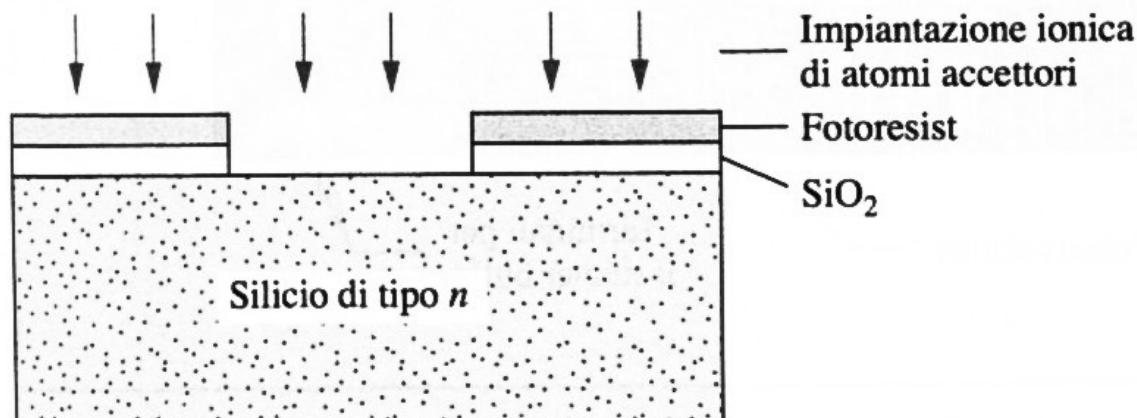
(a)



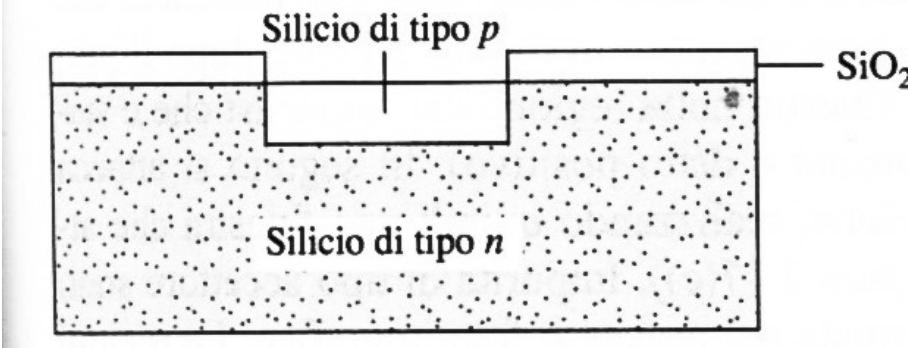
(b)



Giunzione p-n (silicio)



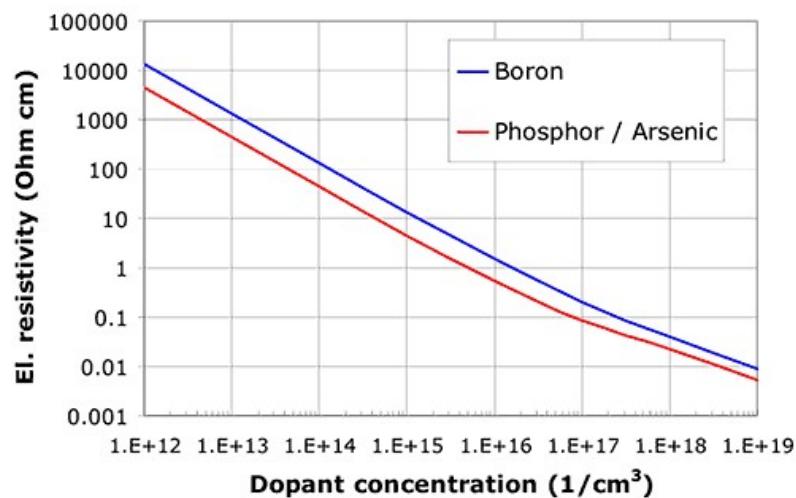
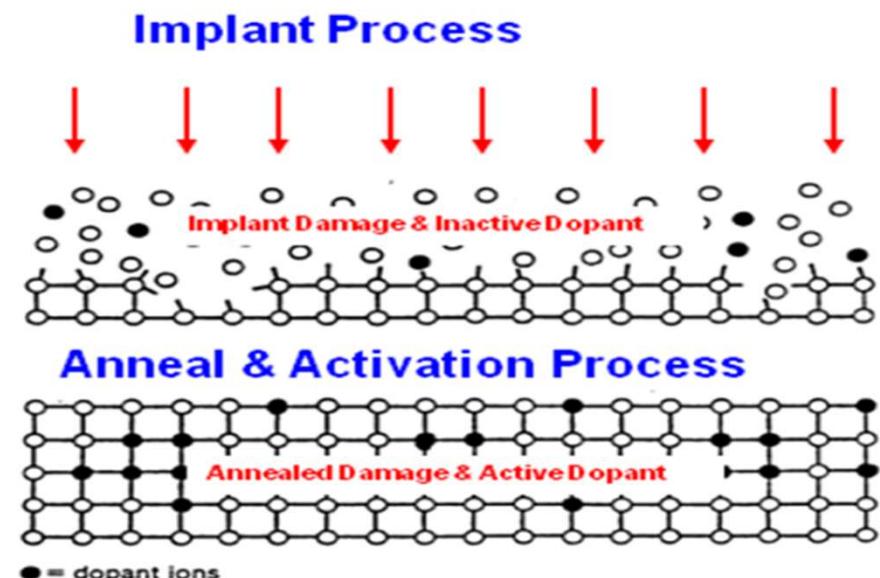
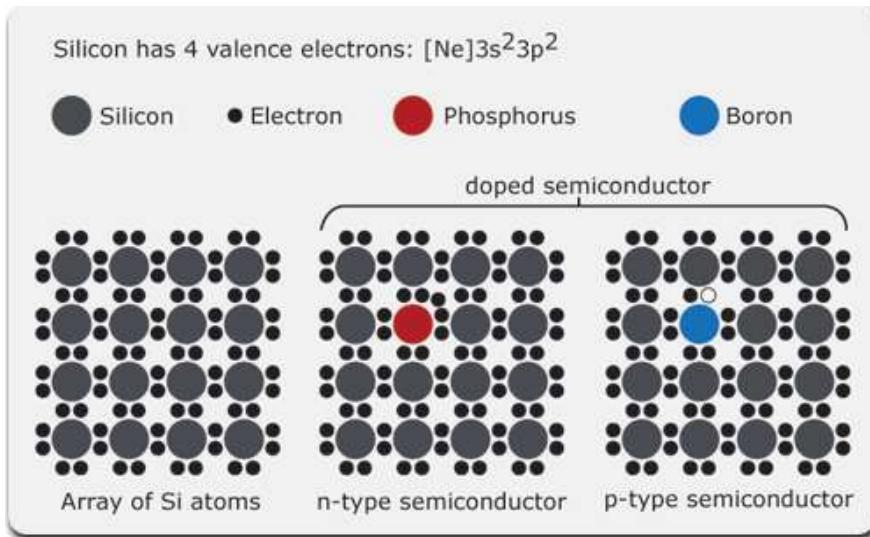
(c)



(d)

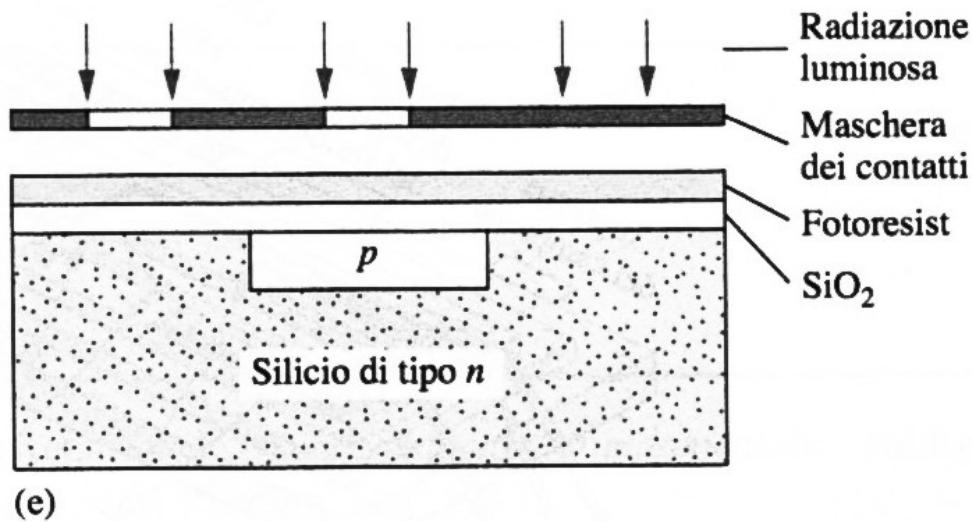


Giunzione p-n (silicio)



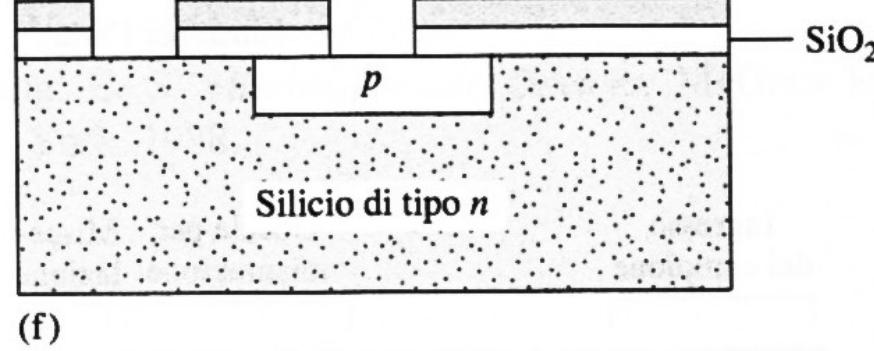
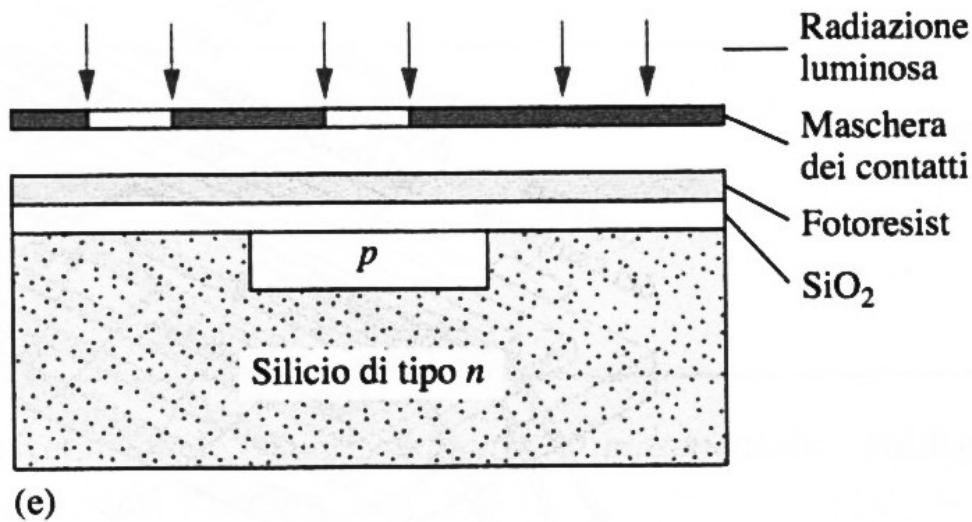


Giunzione p-n (silicio)



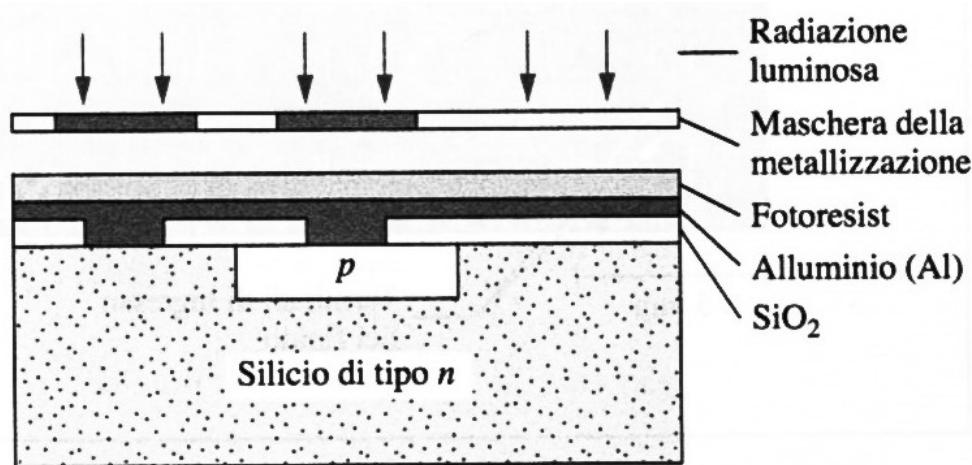


Giunzione p-n (silicio)

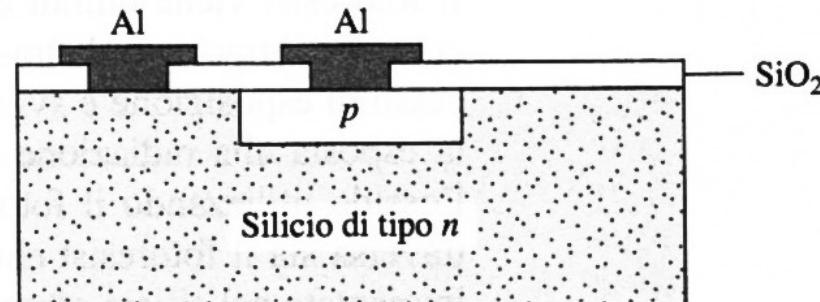




Giunzione p-n (silicio)



(g)

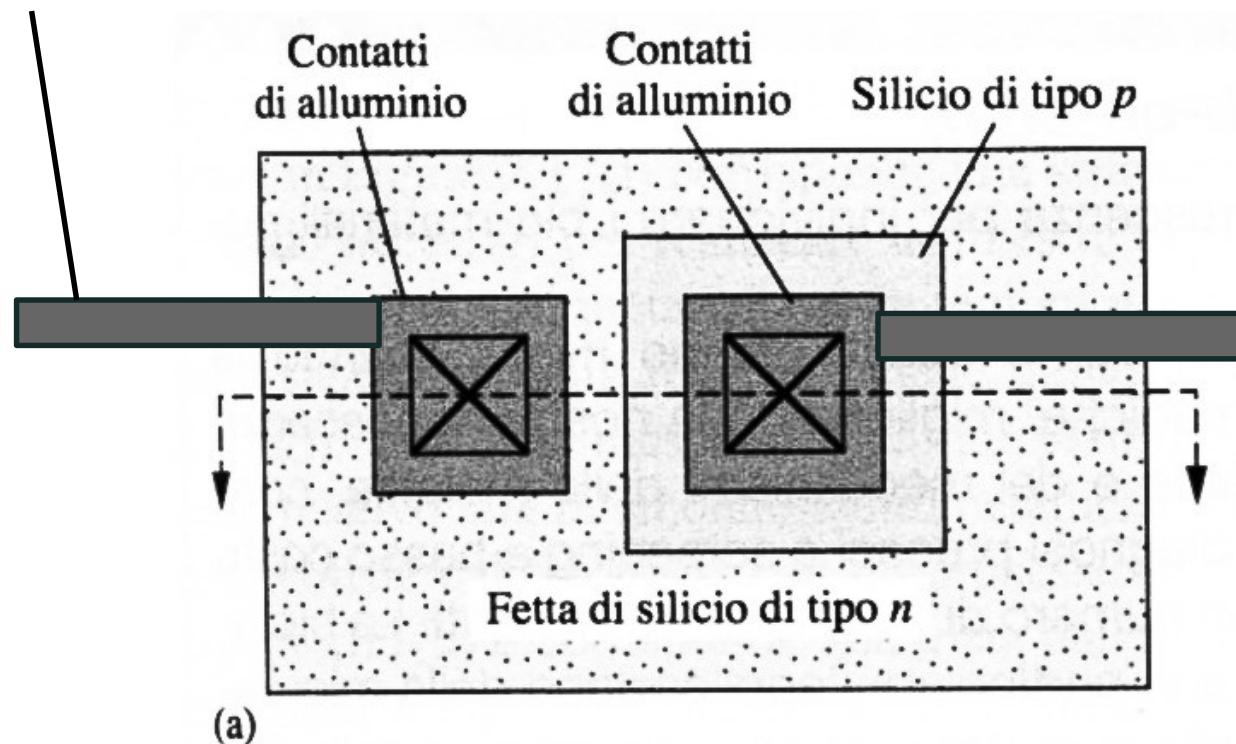


(h)



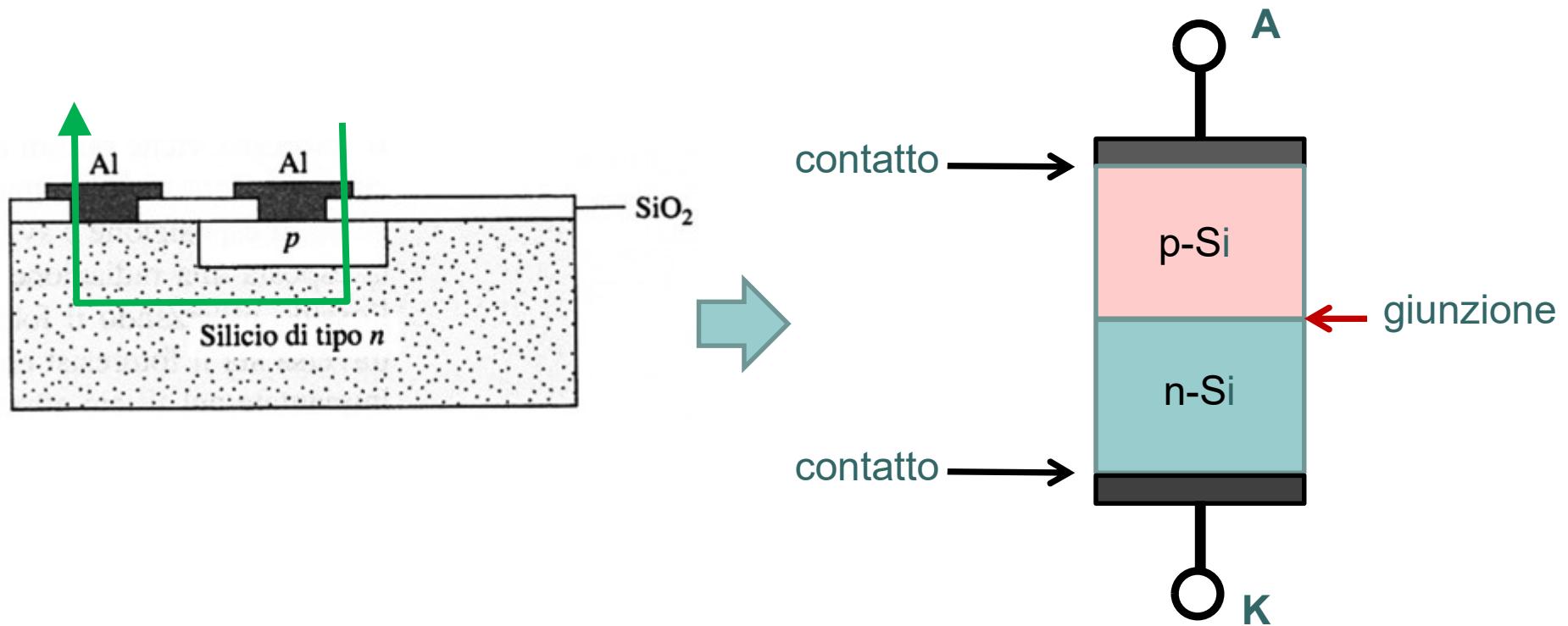
Giunzione p-n (silicio)

Pista in alluminio



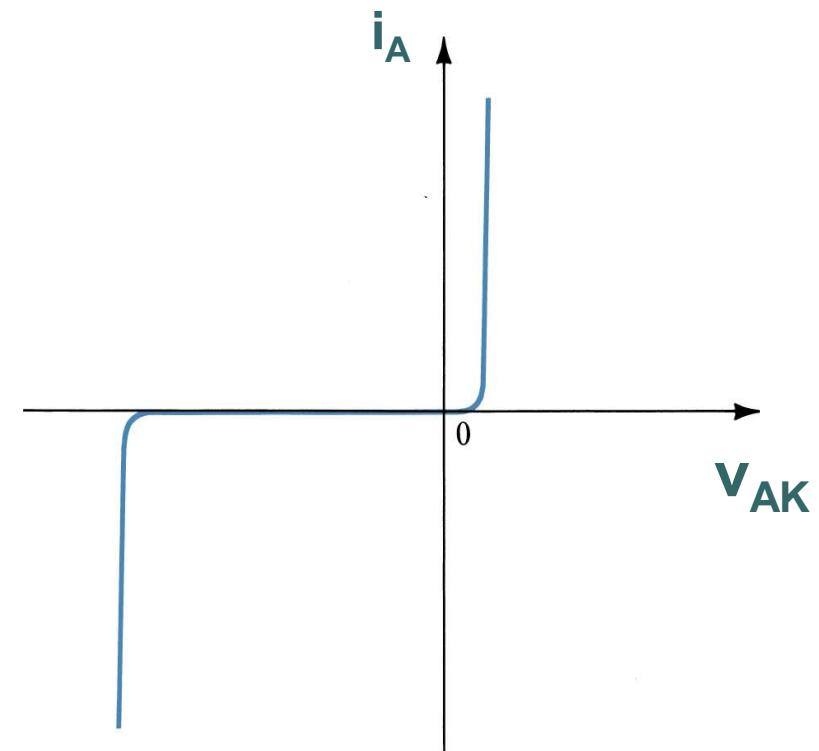
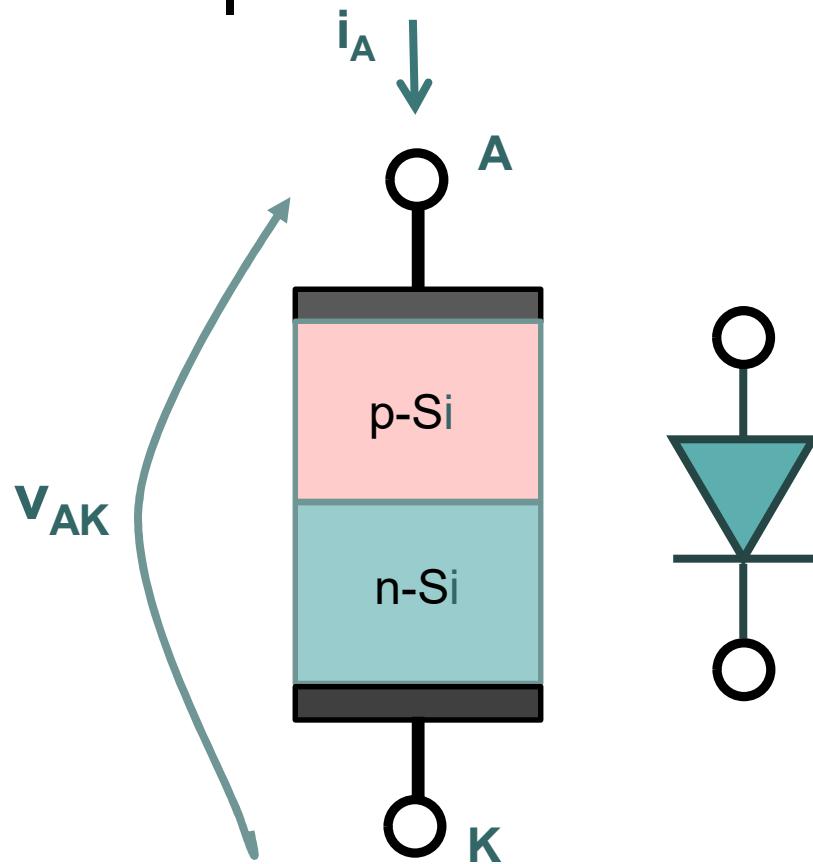


Giunzione p-n (silicio)



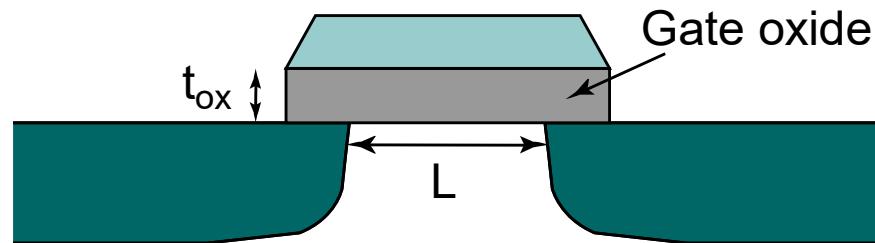
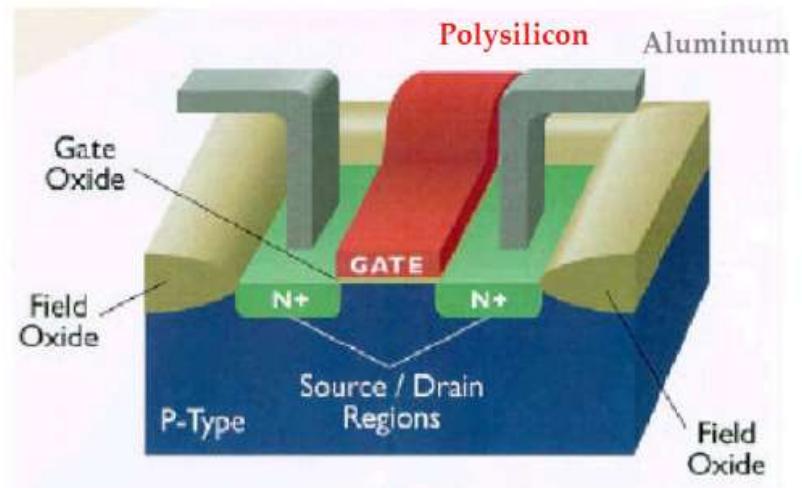
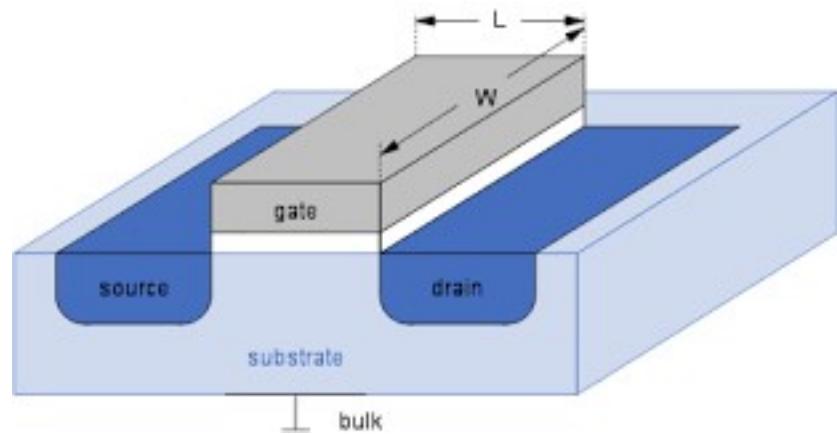


Giunzione p-n: il diodo a semiconduttore





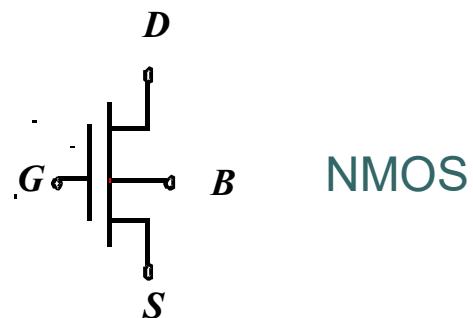
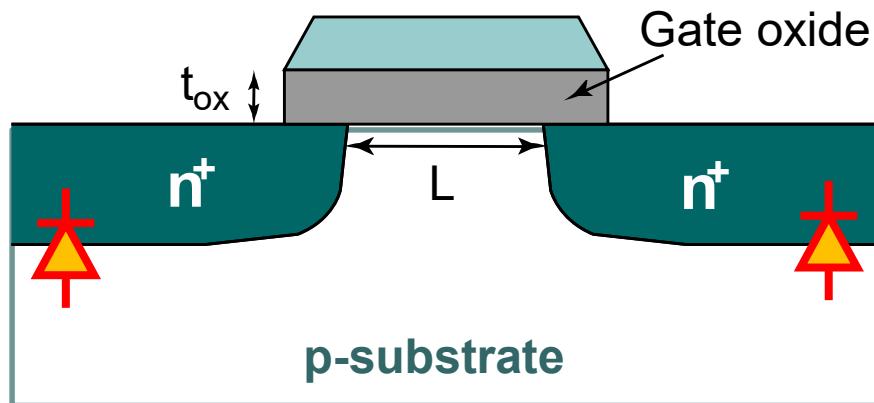
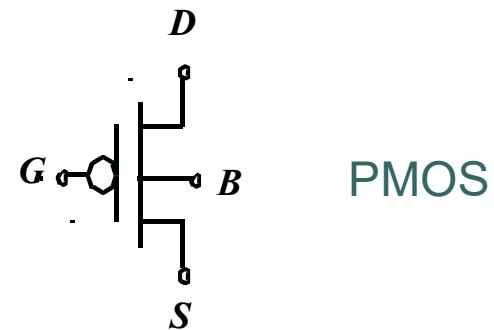
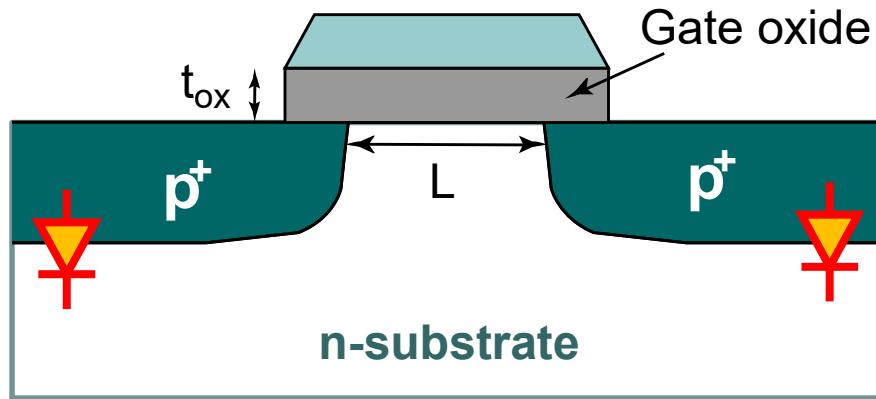
MOS transistor



Cross section

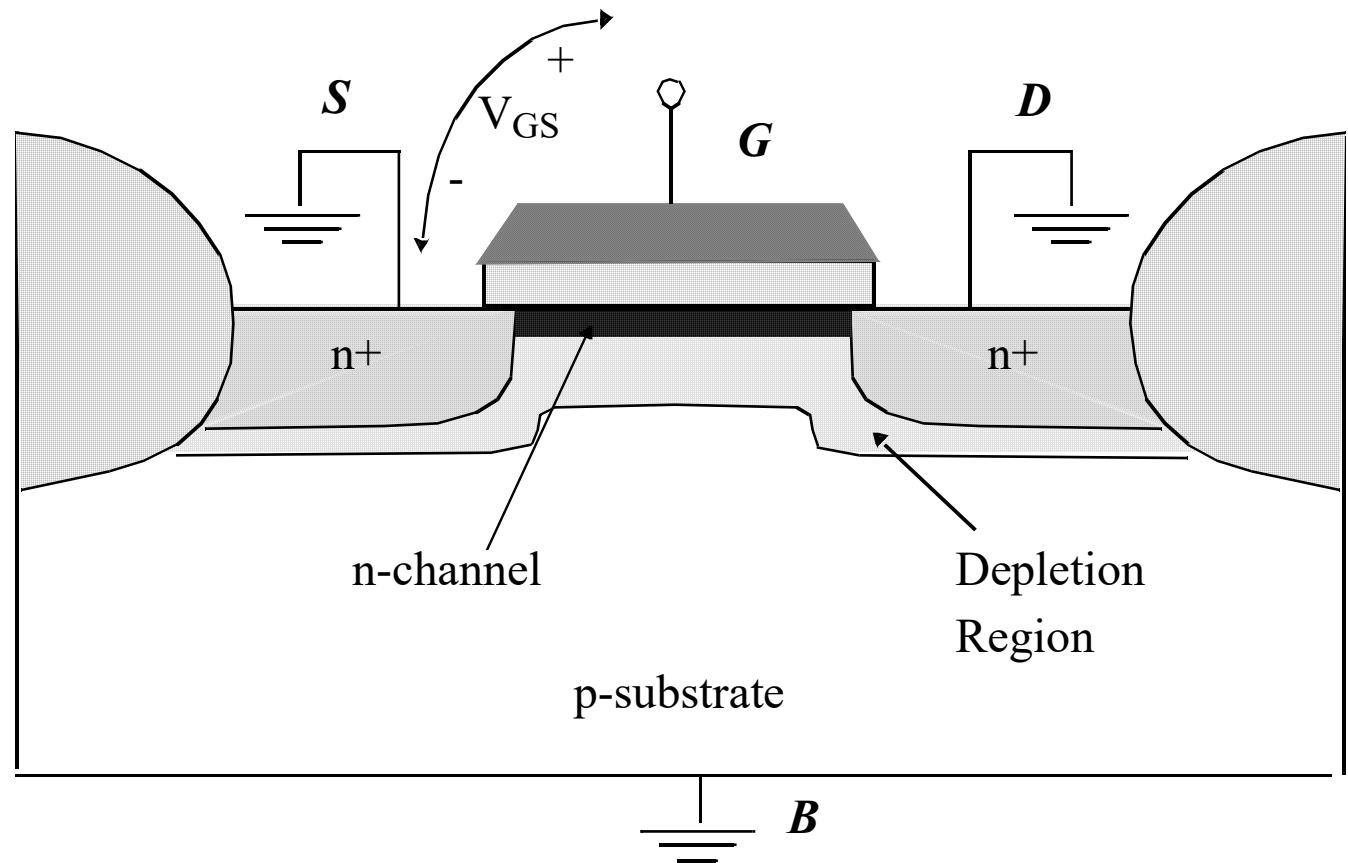
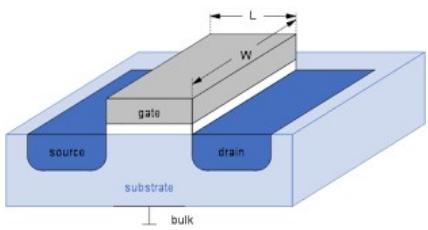


MOS transistor



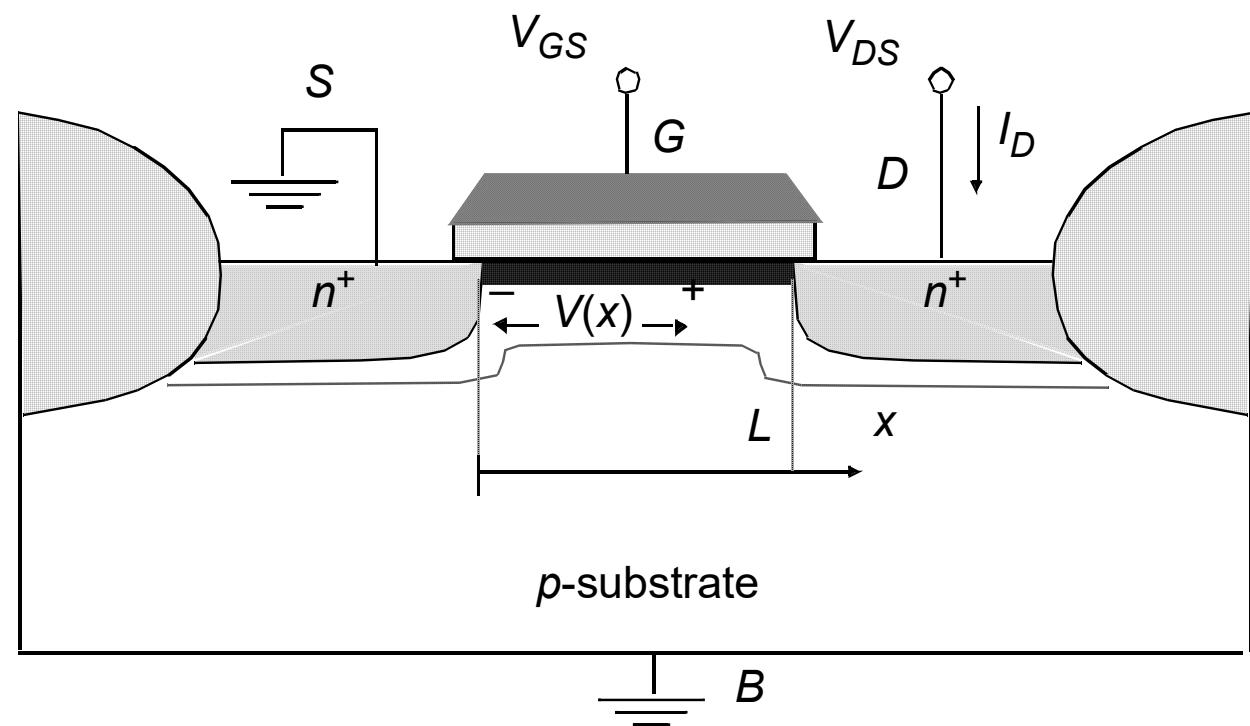
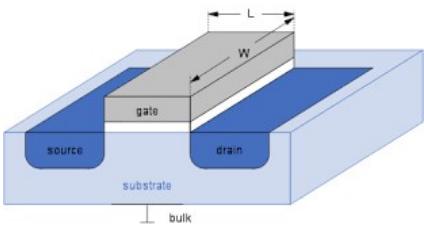


Transistor NMOS:il concetto di soglia





Transistor NMOS : corrente I_{DS}

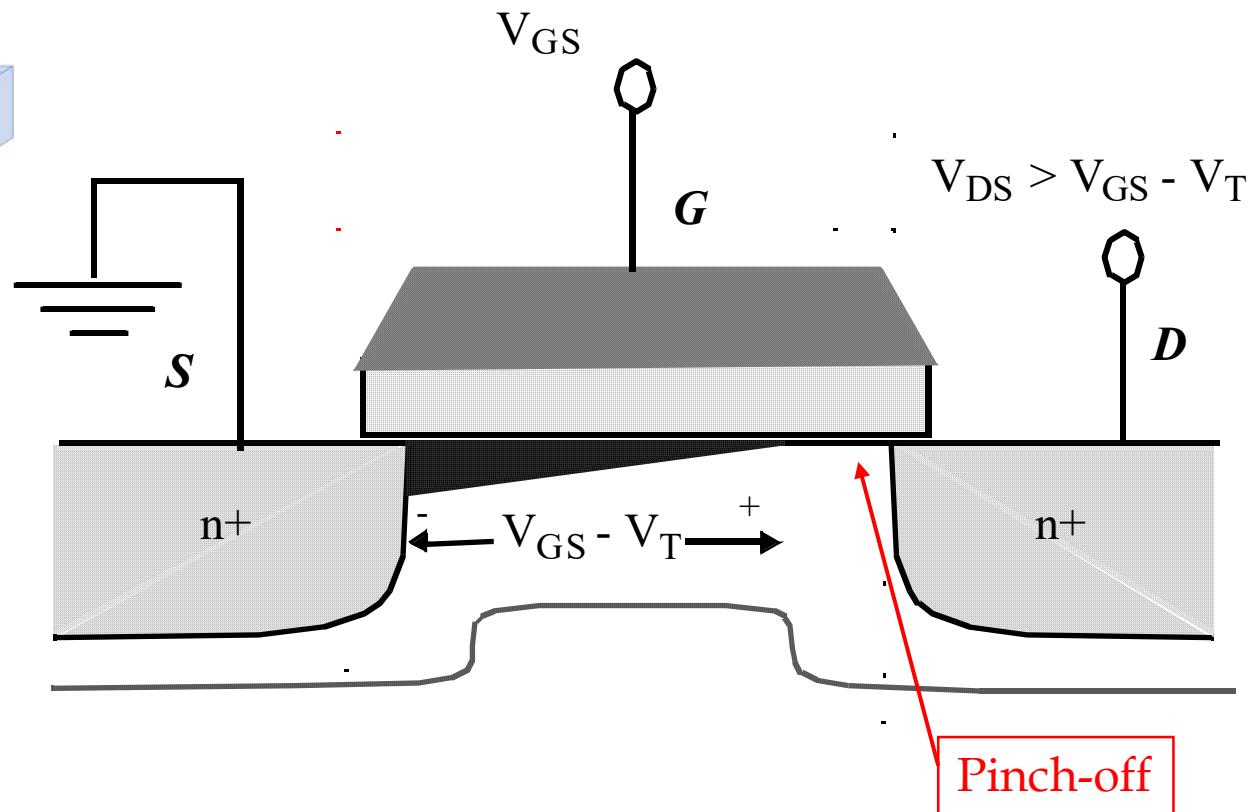
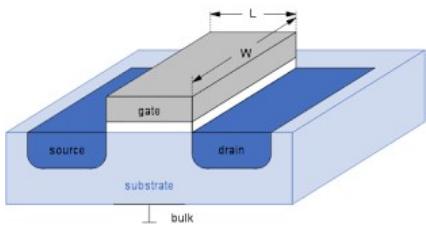


$$\begin{aligned}V_{GS} &> V_{TH} \\V_{DS} &> 0\end{aligned}$$

MOS transistor and its bias conditions

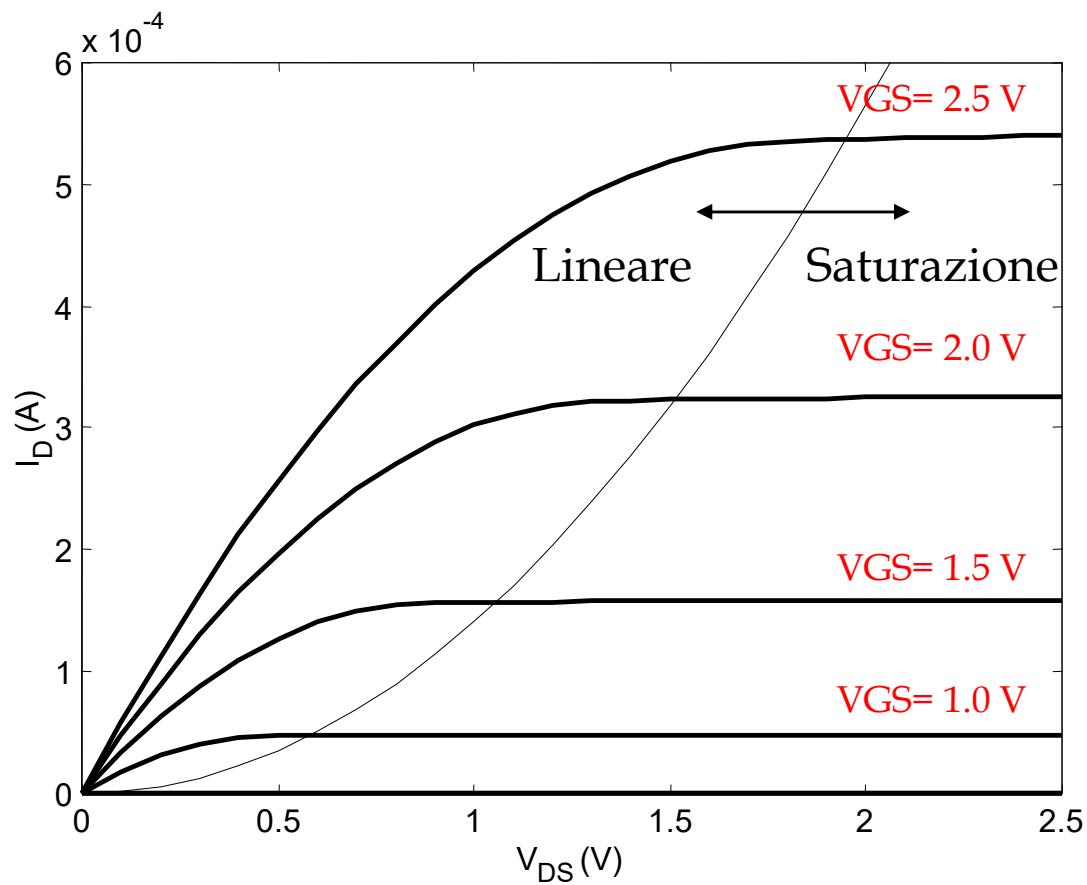


Transistor NMOS : Saturazione



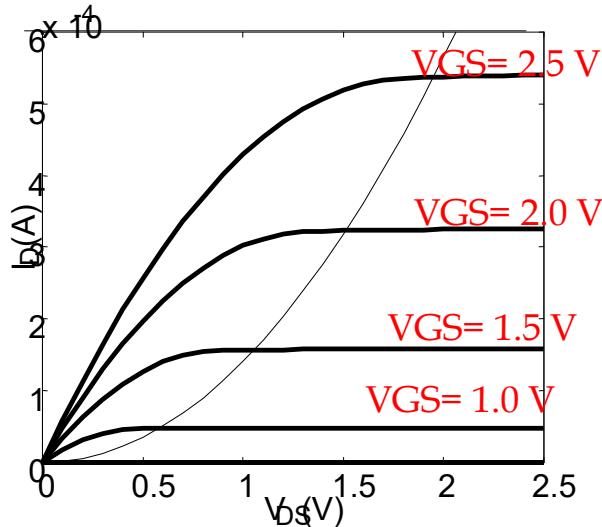


Transistor NMOS: Caratteristica I_{DS} - V_{DS}





Transistor NMOS: Modello



Linear Region: $V_{DS} \leq V_{GS} - V_T$

$$I_D = k'_n \frac{W}{L} \left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right)$$

with

$$k'_n = \mu_n C_{ox} = \frac{\mu_n \epsilon_{ox}}{t_{ox}}$$

Process Transconductance Parameter

Saturation Mode: $V_{DS} \geq V_{GS} - V_T$

$$I_D = \frac{k'_n W}{2 L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

\downarrow
Channel Length Modulation

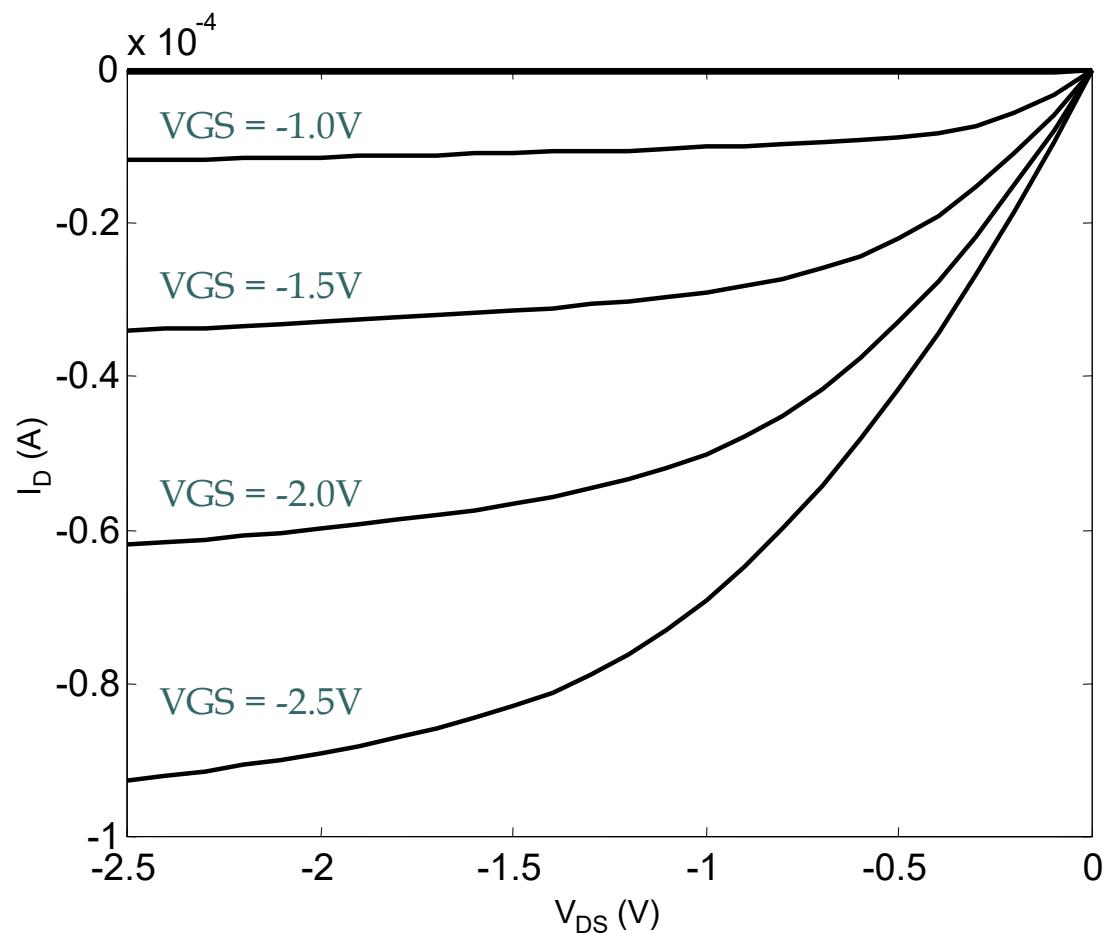
k' = transconduttanza (processo)

W/L = fattore di forma (transistor)

$k = k' \cdot W/L =$ fattore di guadagno [A/V^2] (transistor)



Transistor PMOS: Caratteristica I_{DS} - V_{DS}



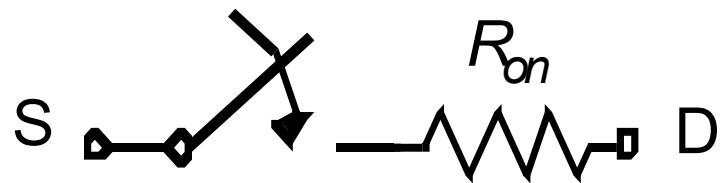
Assume all variables
negative!

N.B $V_{TH} < 0\text{V}$!

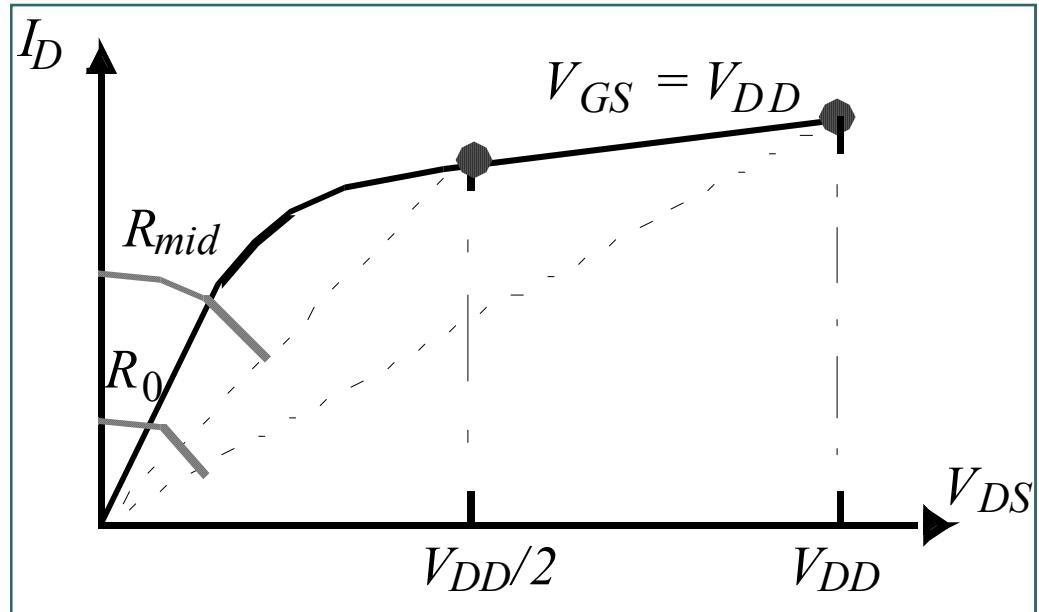


Il transistore MOS come interruttore

$$V_{GS} \geq V_T$$



NMOS





Inverter: dalla porta logica al circuito logico

Porta Logica

Ingresso	Uscita
falso	vero
vero	falso

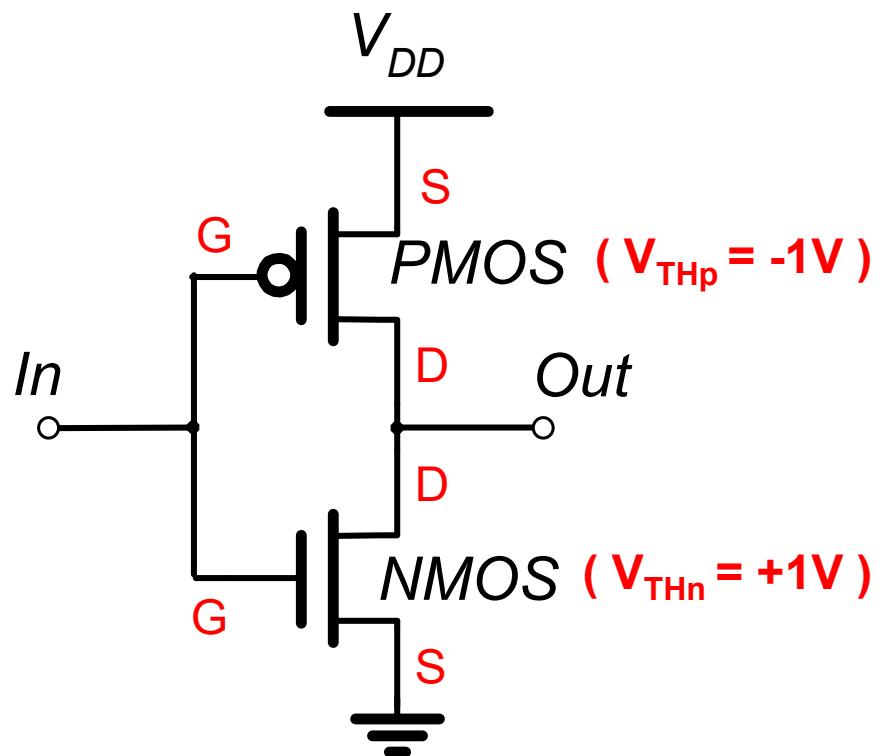


Circuito Logico

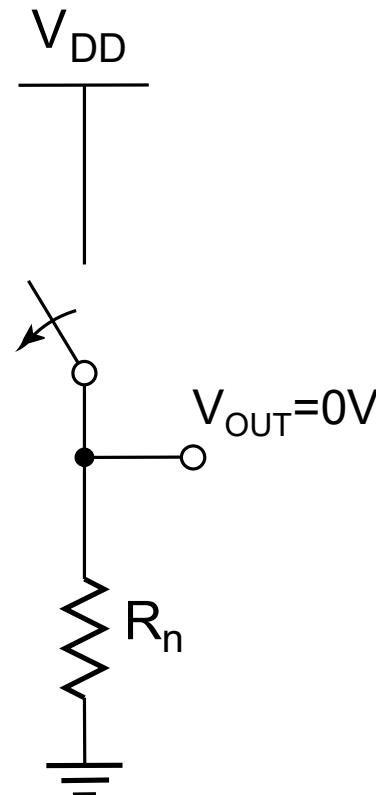
Ingresso	Uscita
0V	V_{DD}
V_{DD}	0V



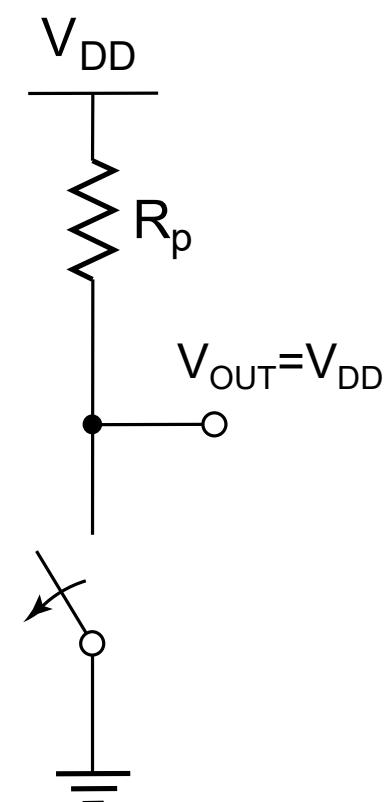
L' inverter CMOS



N.B. $V_{DD} > |V_{TH}|$



$$V_{in} = V_{DD}$$

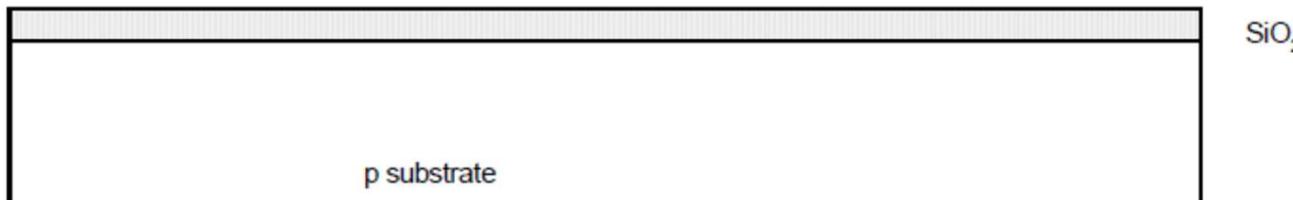


$$V_{in} = 0V$$

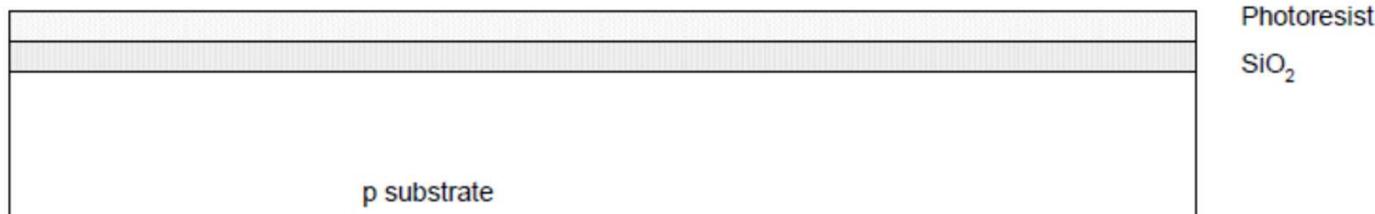


CMOS fabrication process

Blank wafer covered with a layer of SiO_2 using oxidation



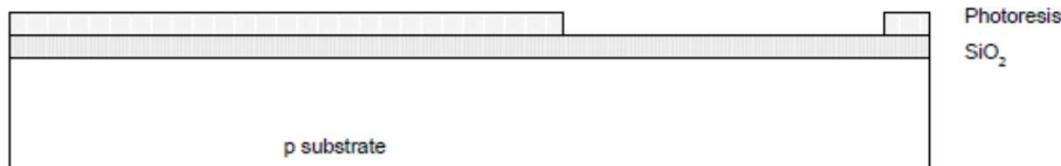
Spin on the photoresist. Exposed to UV light using the n-well mask. (Photolithography)



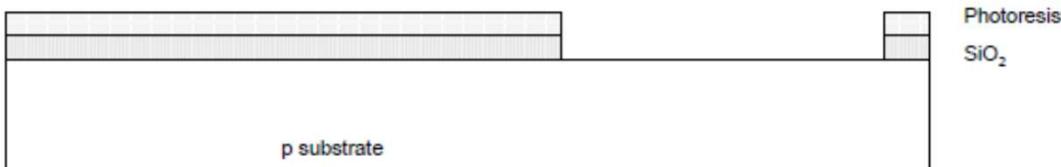


CMOS fabrication process

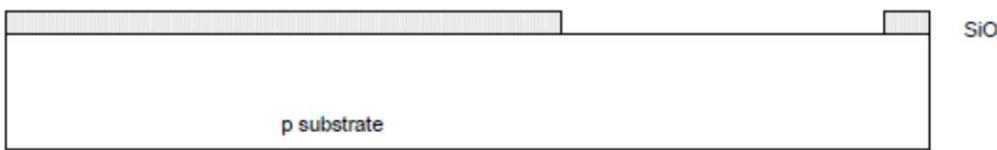
Strip off the exposed photoresist using organic solvents



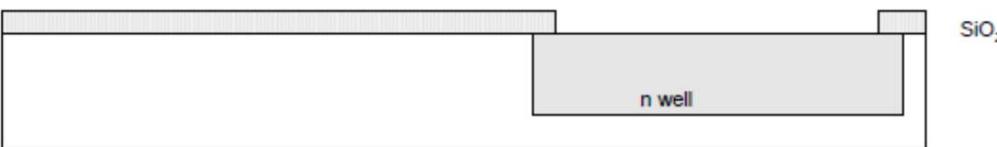
Etch the uncovered oxide using HF (Hydroflouric acid)



Etch the remaining photoresist using a mixture of acids



n-well is formed using either diffusion or ion implantation



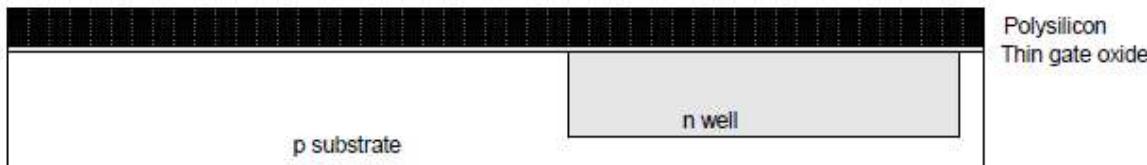


CMOS fabrication process

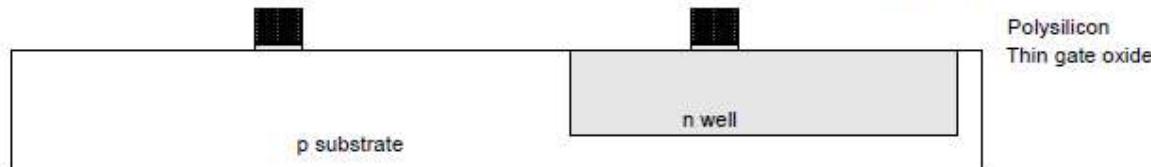
Strip off remaining oxide using HF. Subsequent steps use the same photolithography process



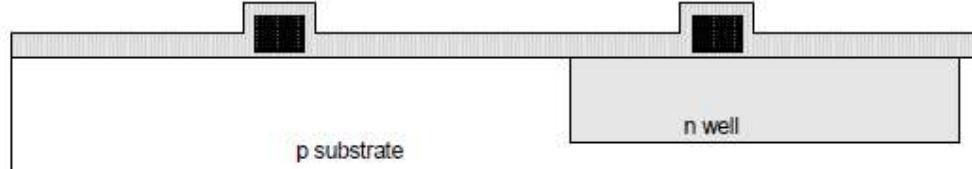
Deposit thin layer of oxide. Use CVD to form poly and dope heavily to increase conductivity



Pattern poly using the previously discussed photolithography process



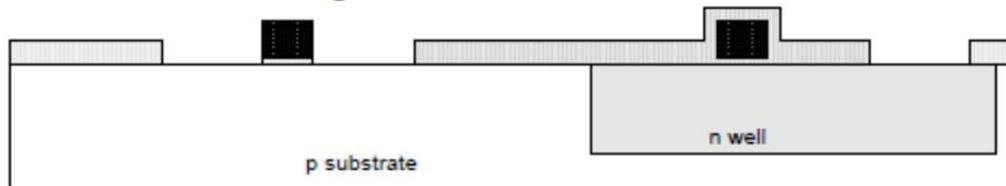
Cover with oxide to define n diffusion regions



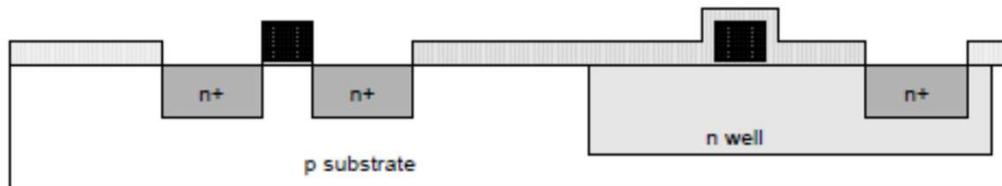


CMOS fabrication process

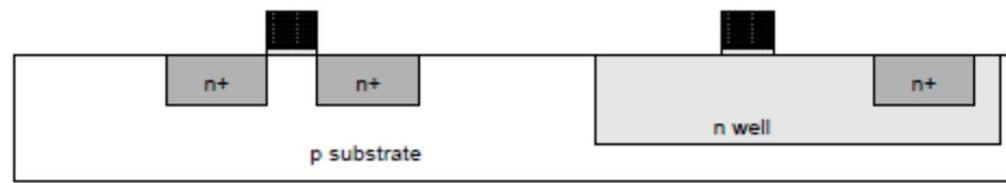
Pattern oxide using n+ active mask to define n diffusion regions



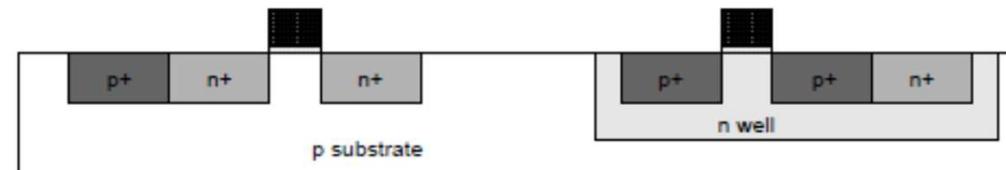
Diffusion or ion implantation used to create n diffusion regions



Strip off the oxide to complete patterning step

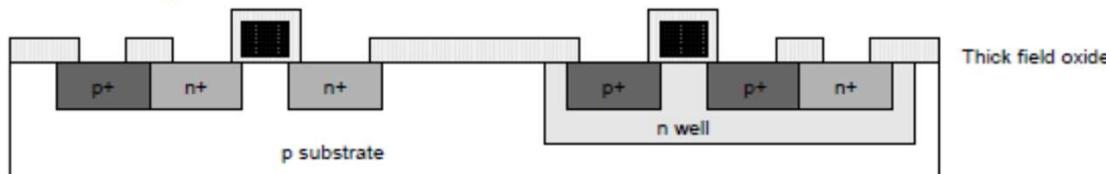


Similar steps used to create p diffusion regions

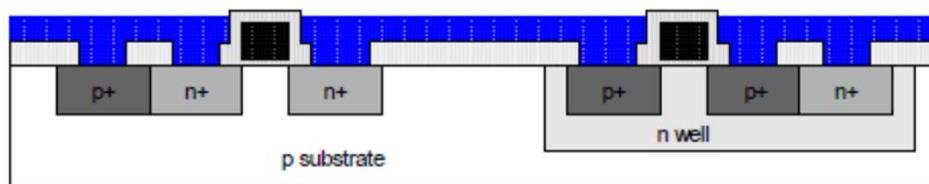


CMOS fabrication process

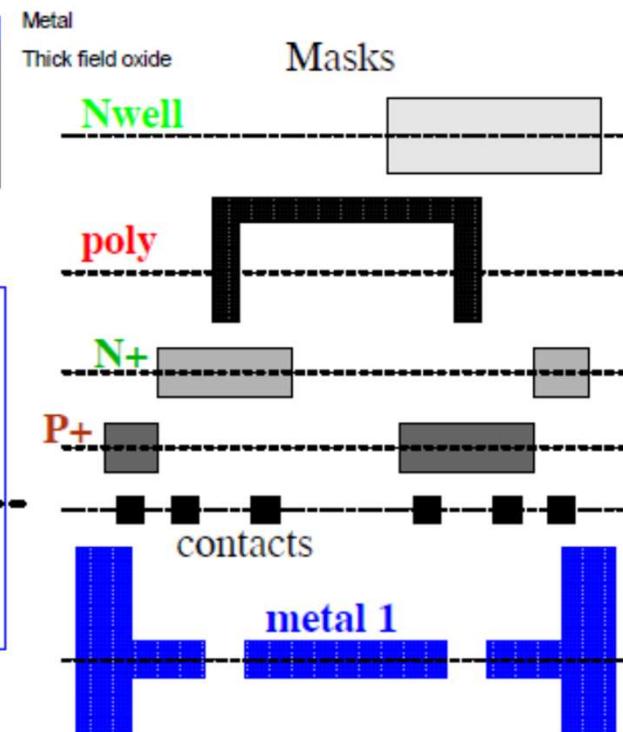
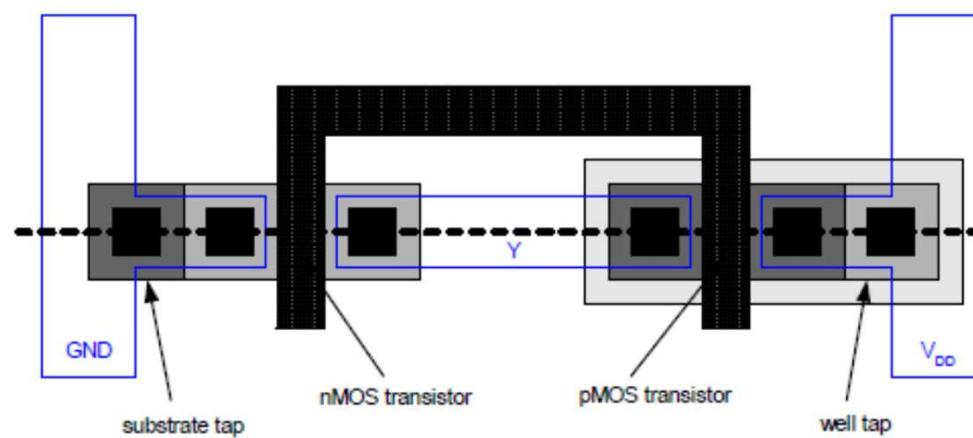
Cover chip with thick field oxide and etch oxide where contact cuts are needed



Remove excess metal leaving wires

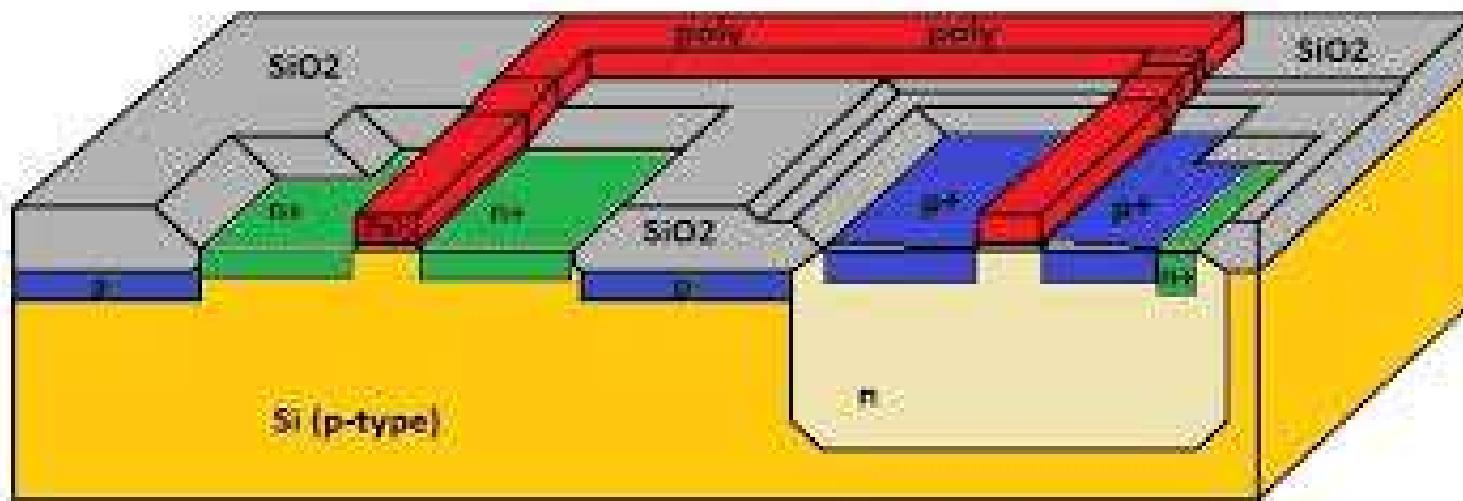


Layout (mask) view of the inverter.



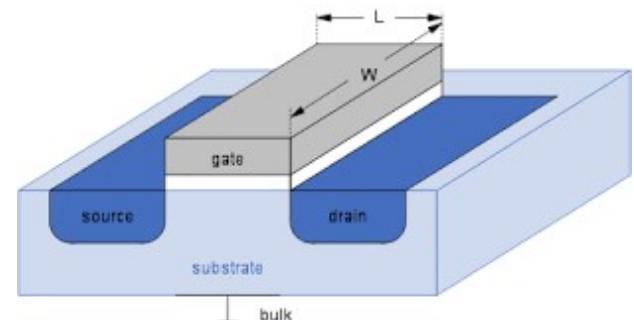


CMOS inverter



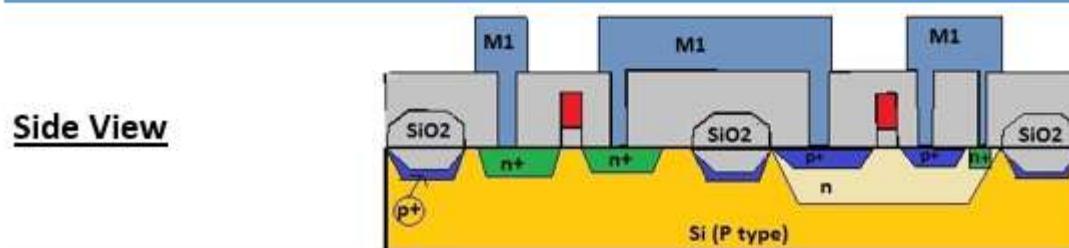
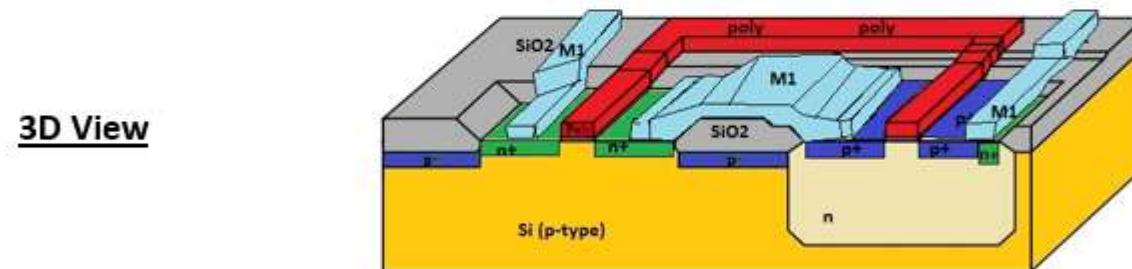
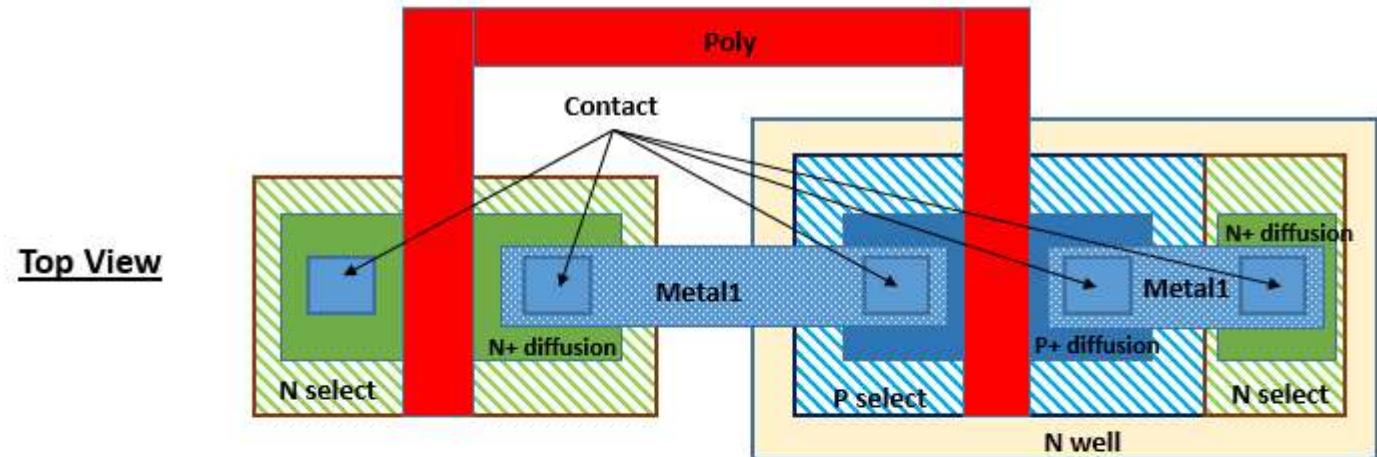
3D view of silicon wafer. Now we have PMOS and NMOS Device.

NB: NO metal layer



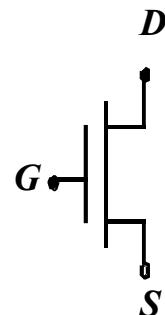


CMOS Inverter

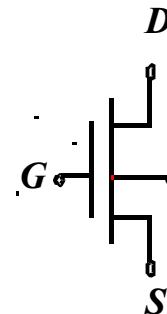




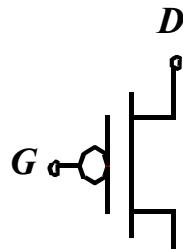
Electrical Symbols



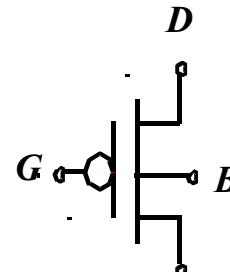
NMOS Enhancement



NMOS with
Bulk Contact



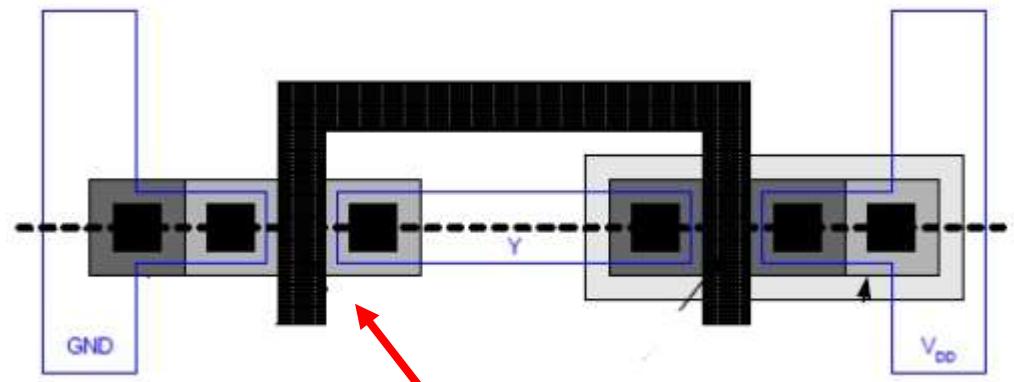
PMOS Enhancement



PMOS
Bulk Contact



Scaling



Linear Region: $V_{DS} \leq V_{GS} - V_T$

$$I_D = k'_n \frac{W}{L} \left((V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

with

$$k'_n = \mu_n C_{ox} = \frac{\mu_n \epsilon_{ox}}{t_{ox}}$$

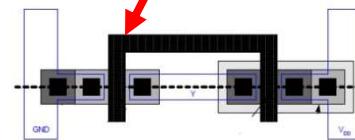
Process Transconductance Parameter

Saturation Mode: $V_{DS} \geq V_{GS} - V_T$

$$I_D = \frac{k'_n W}{2 L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

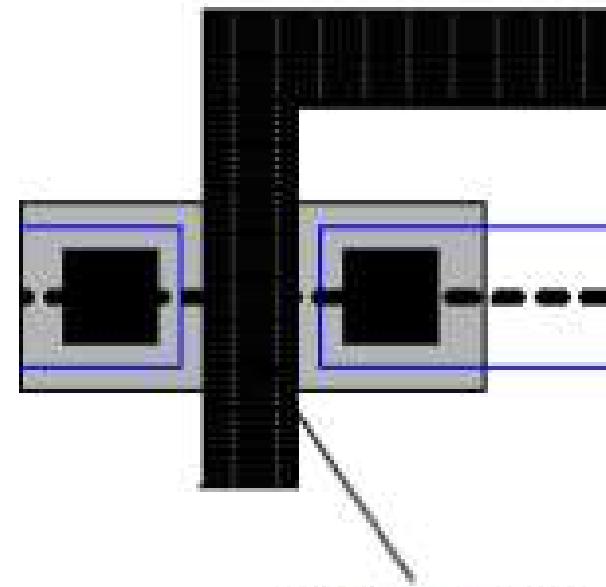
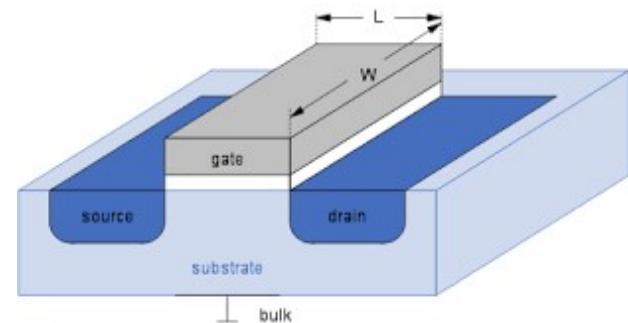
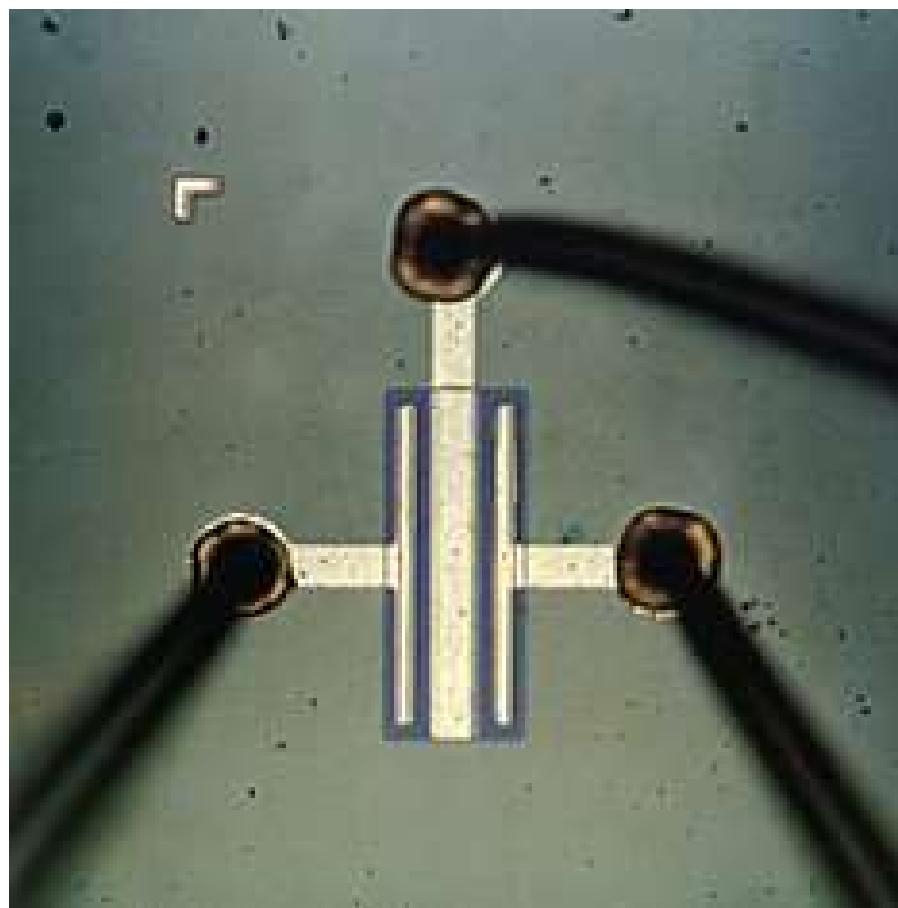
↙
Channel Length Modulation

Stesso W/L !





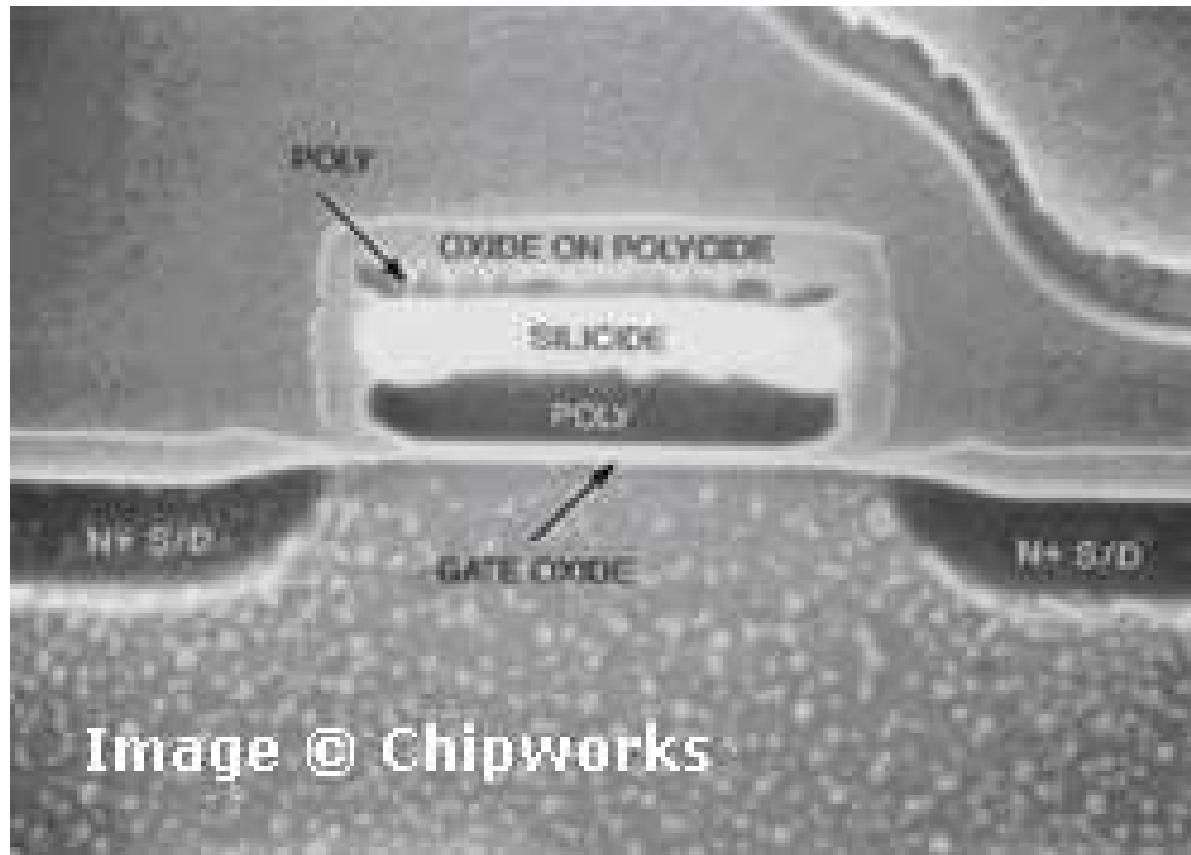
FI 100 (Fairchild 1964)



nMOS transistor



CMOS transistor: SEM image





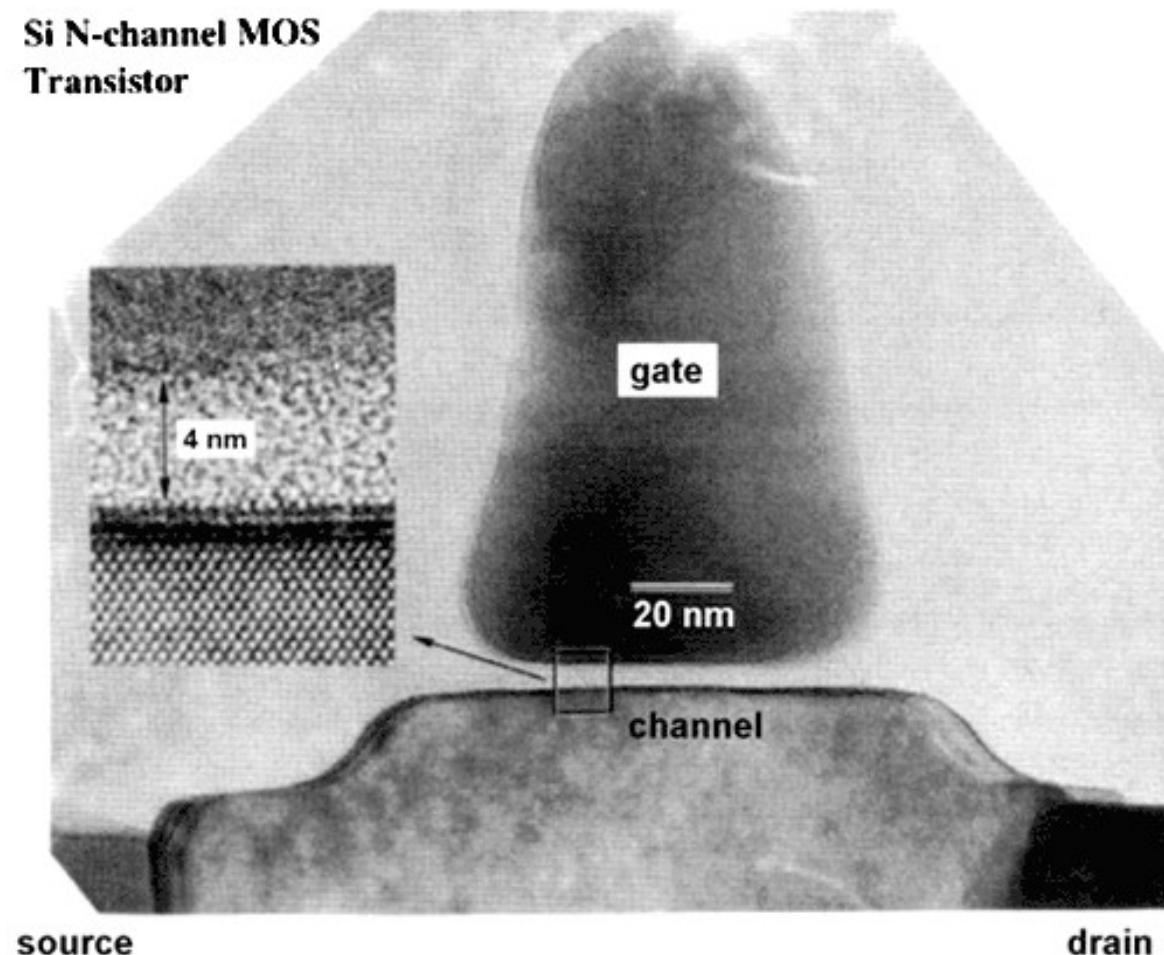
CMOS transistors: TEM image



Apple A4
45 nm MOS transistors

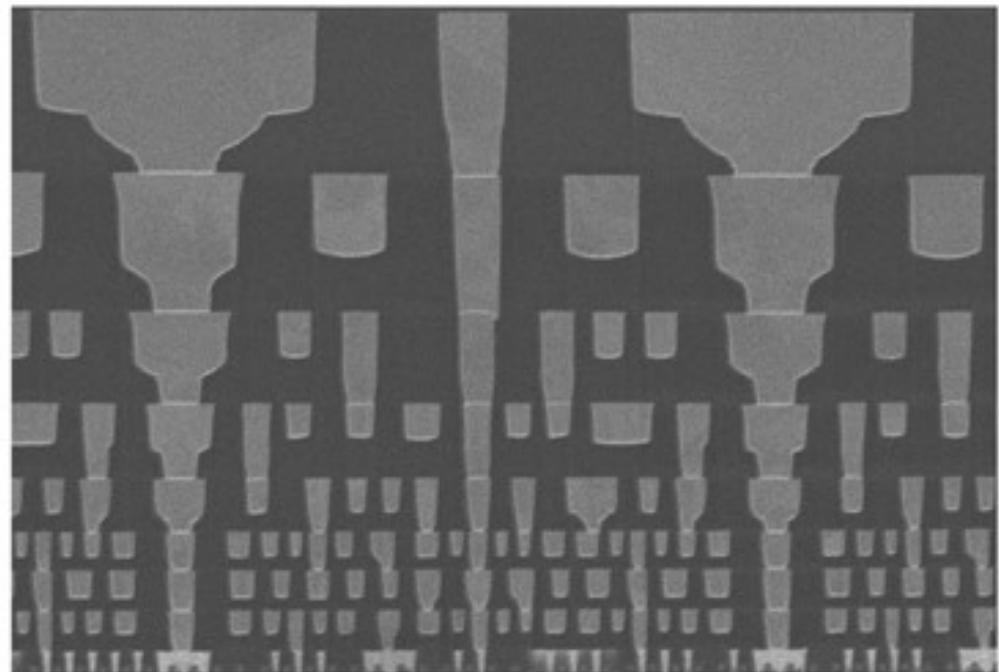
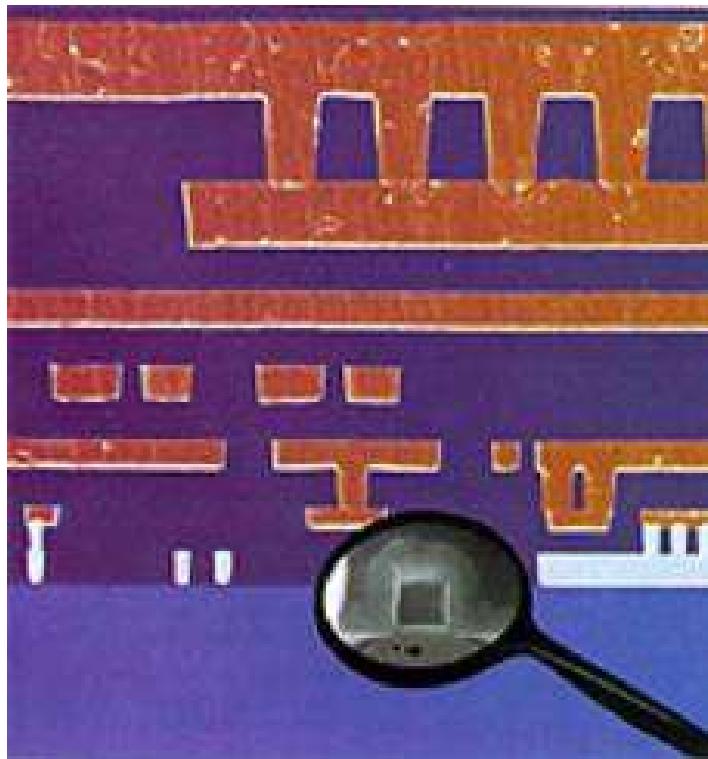


CMOS transistor: TEM image



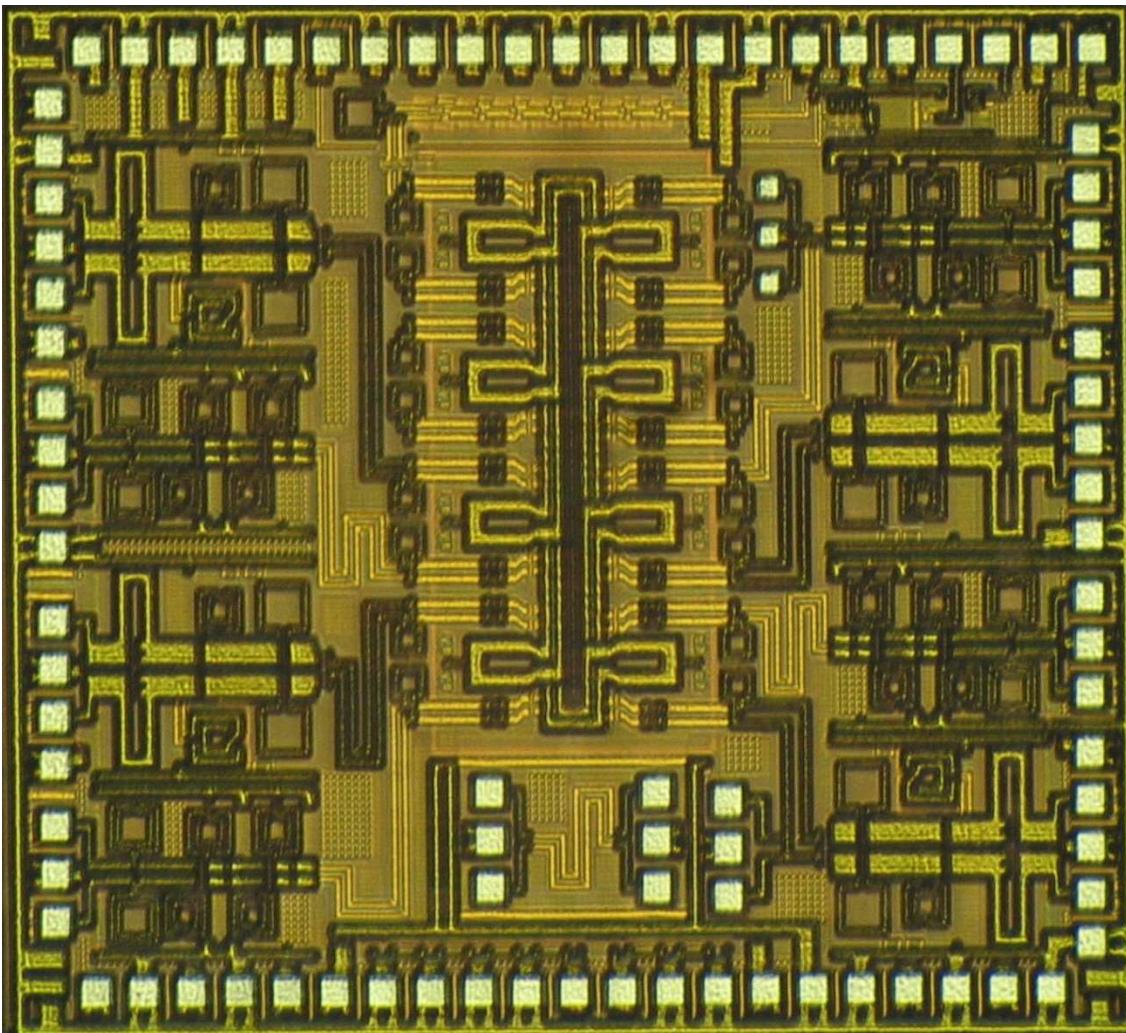


CMOS fabrication process



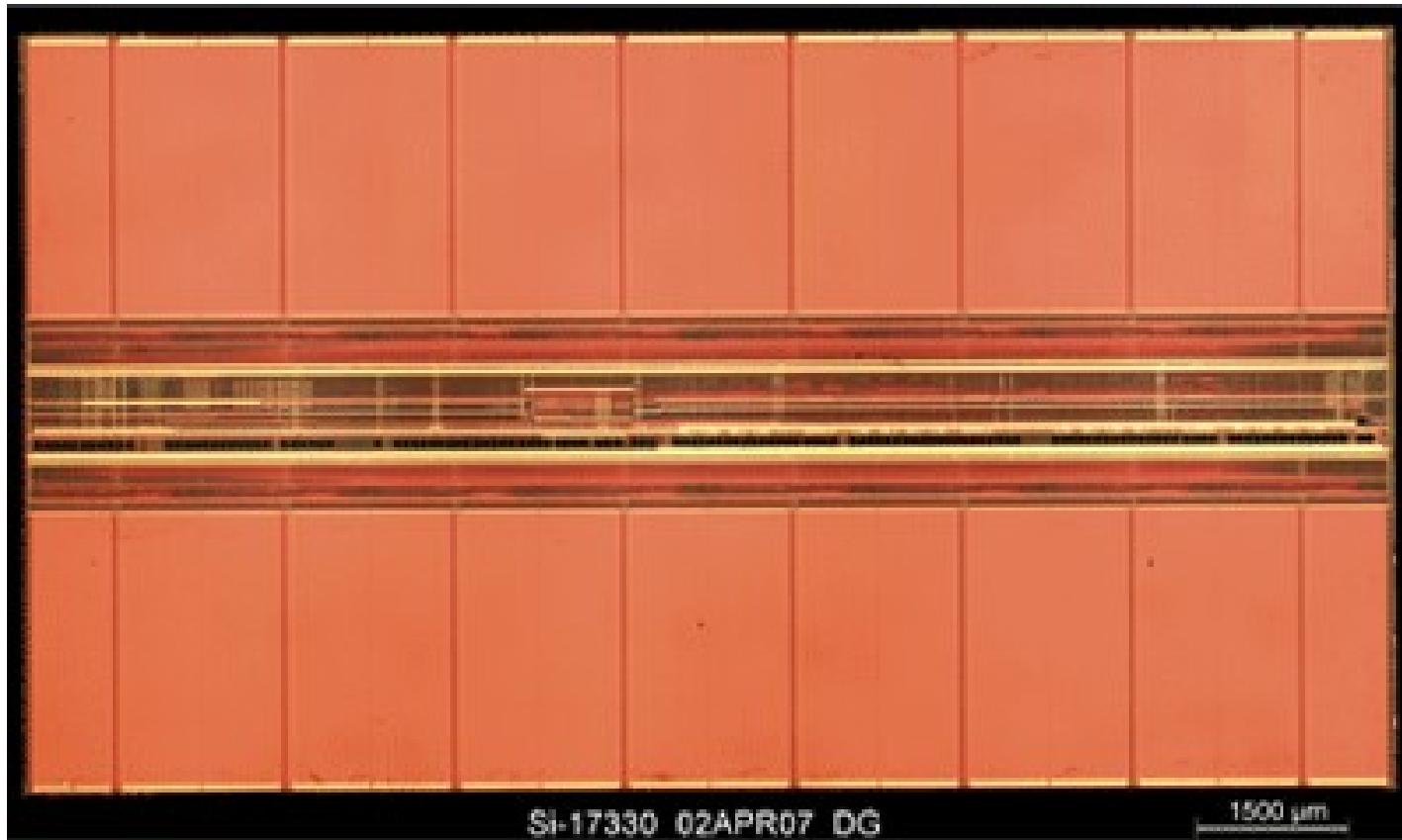


Integrated circuits





Integrated circuits



Micron
1 Gbit DRAM
Today



Figure di merito di un IC

- **Costo**
- Affidabilità
- Scalabilità
- Velocità (delay, frequenza operativa)
- Dissipazione di potenza
- Energia necessaria per ogni operazione



Costo

- Costi fissi

- Costo del progetto e delle maschere
- Tuning del processo
- Marketing
- Mantenimento infrastruttura ecc.

- Costi variabili

- Fabbricazione delle fette
- Testing
- packaging



Costo

$$\text{Costo per IC} = \text{costo variabile per IC} + \frac{\text{costo fisso}}{\text{volume}}$$

costo variabile = costo del die + costo del test + costo del packaging

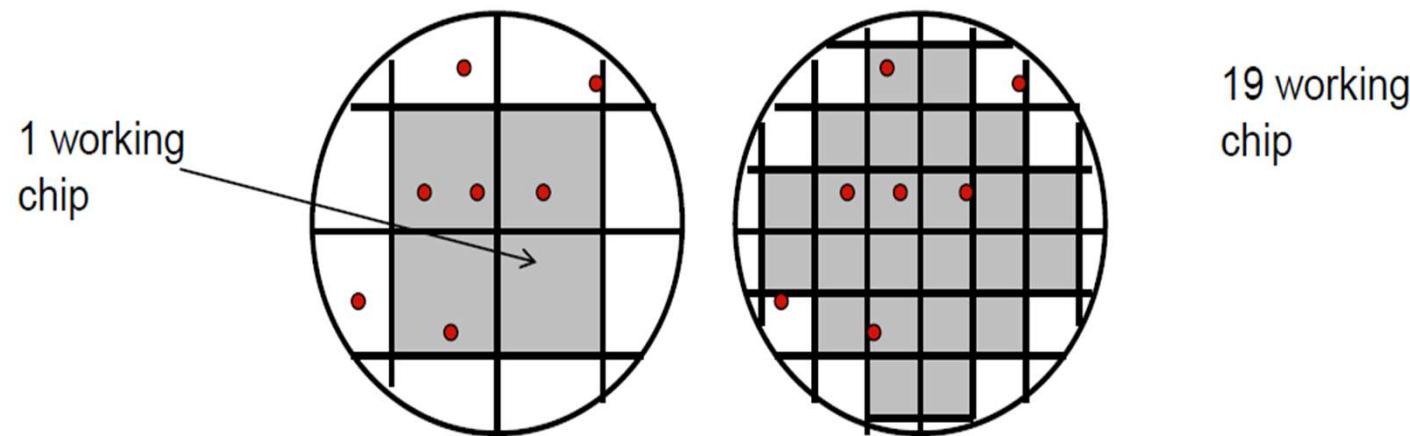
$$\text{Costo del die} = \frac{\text{costo del wafer}}{\text{numero die} \times \text{resa}}$$

$$\text{Resa} = \left(1 + \frac{\text{difetti per unità di area} \times \text{area del die}}{\alpha} \right)^{-\alpha}$$

(valori tipici $\alpha=3$, densità di difetti 1 difetto/cm²)



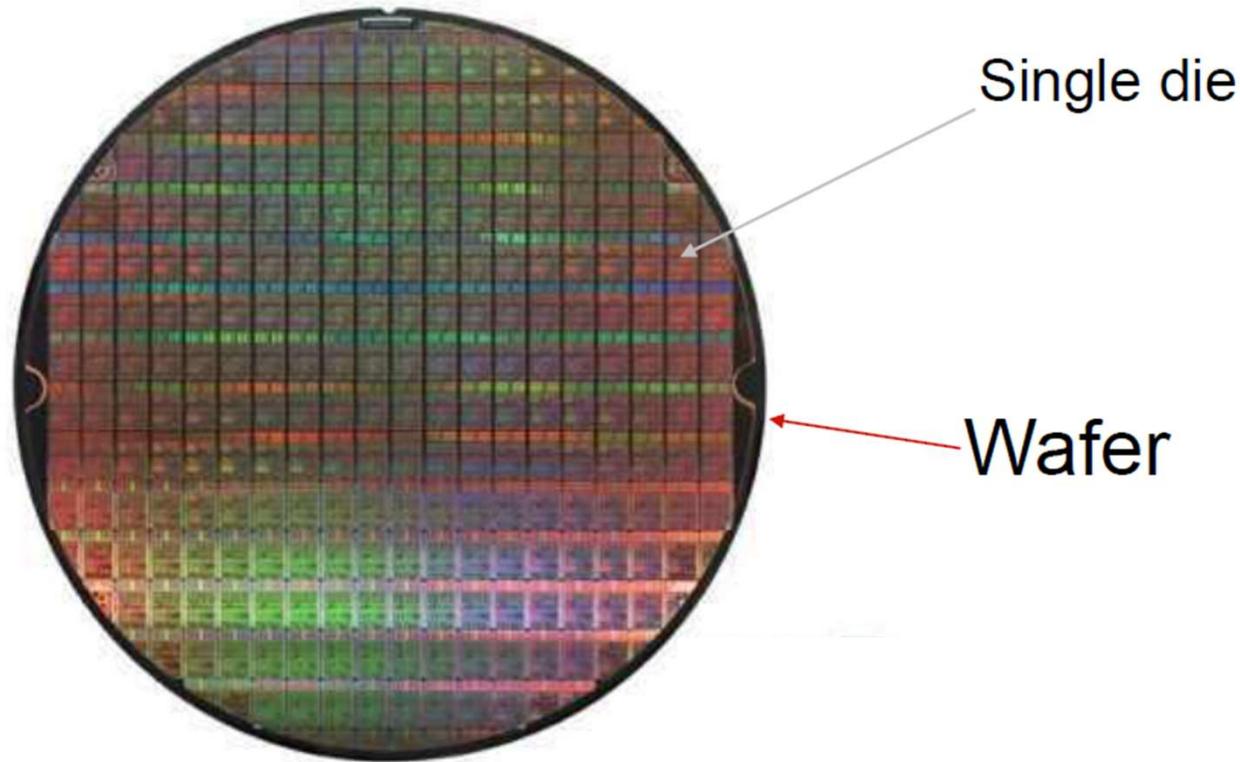
Resa



$$\text{Die Cost} = f(\text{Die Area})^4$$

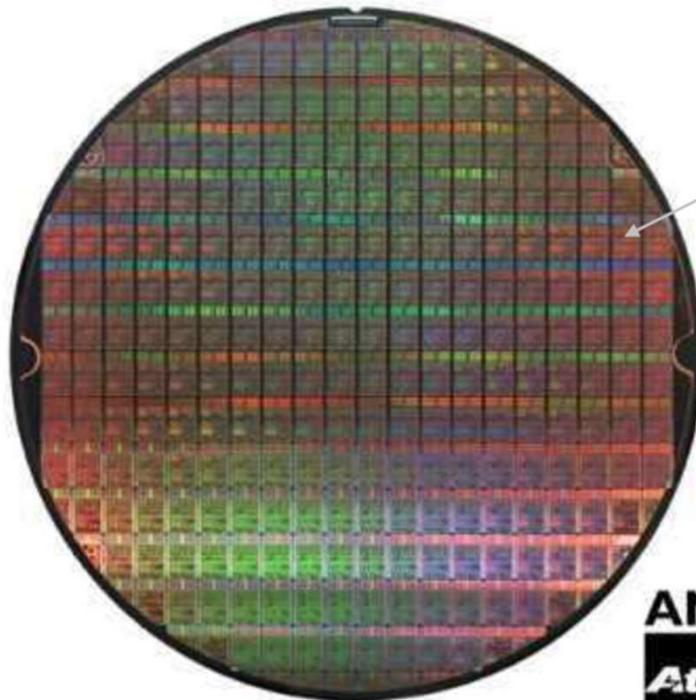


Die e Wafer





Die e Wafer



Going up to 12" (30cm)



Velocità

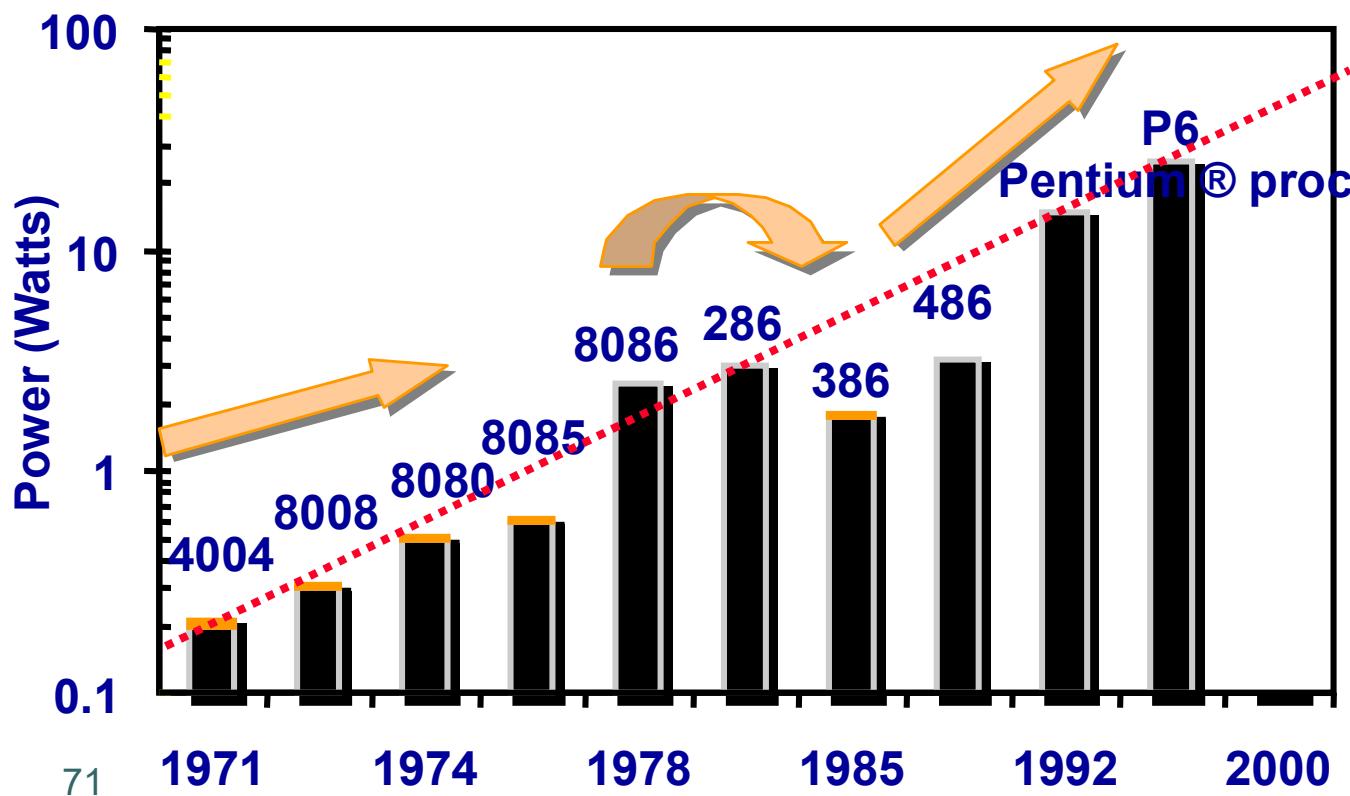
- Lo scaling ha permesso il continuo aumento della velocità dei processori





Dissipazione di potenza

- All' aumentare della complessità la dissipazione di potenza nei microprocessori aumenta nonostante lo scaling





Dissipazione di potenza

- L'aumento della potenza unito al non pari aumento delle dimensioni del die tende a rendere proibitivo il livello di densità di potenza

