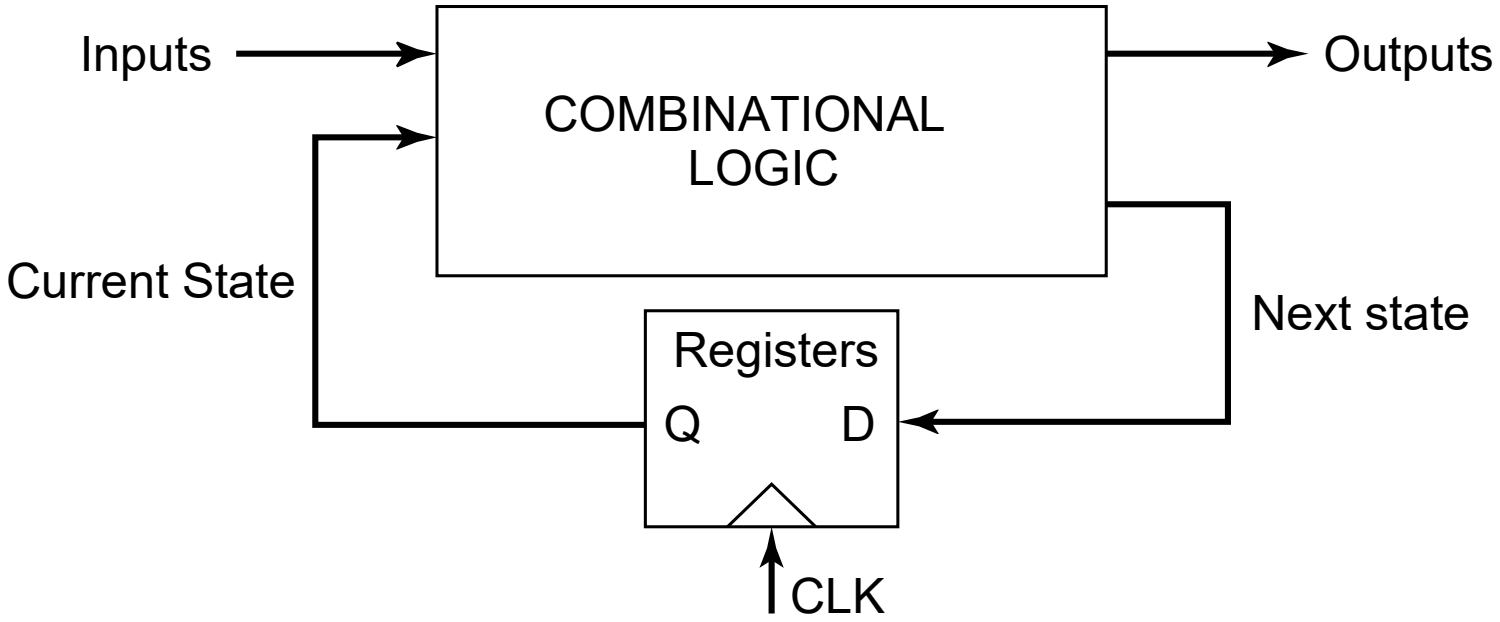
Memorie

- **Memoria locale :** registi o banchi di registri. Realizzano la memoria di stato delle reti sequanziali.

- **Memoria globale :** array organizzati di elementi di memorizzazione. Permettono la memorizzazione di dati e programmi. Possono essere di vario tipo e a vari livelli.

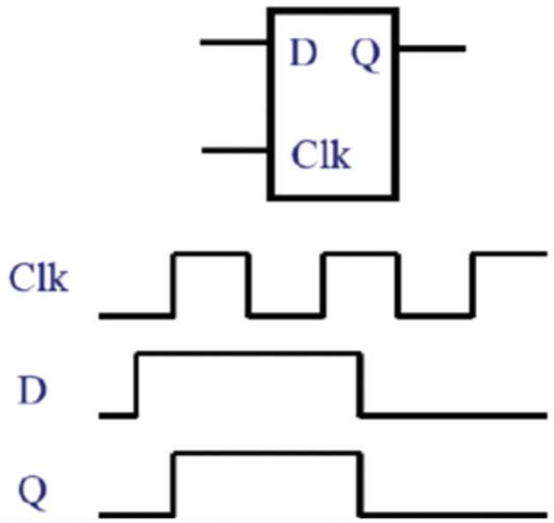
Logica sequenziale

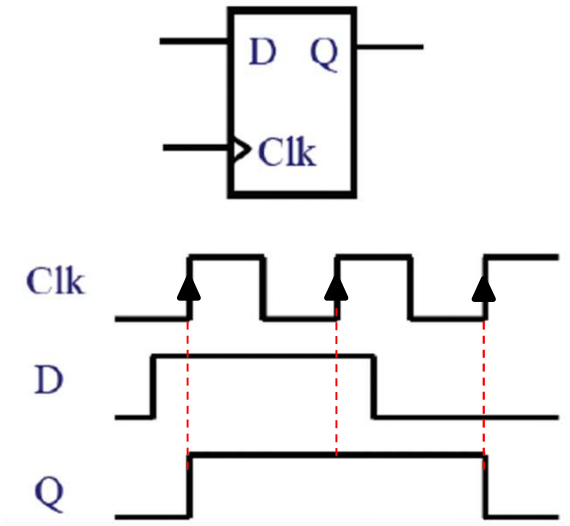
- Nelle logiche sequenziali le uscite dipendono non solo dal valore ***presente*** degli ingressi ma anche da quello ***passato***
- La ***memoria*** del passato viene mantenuta in ***registri*** che, assieme al valore presente degli ingressi rappresentano lo ***stato*** della rete.



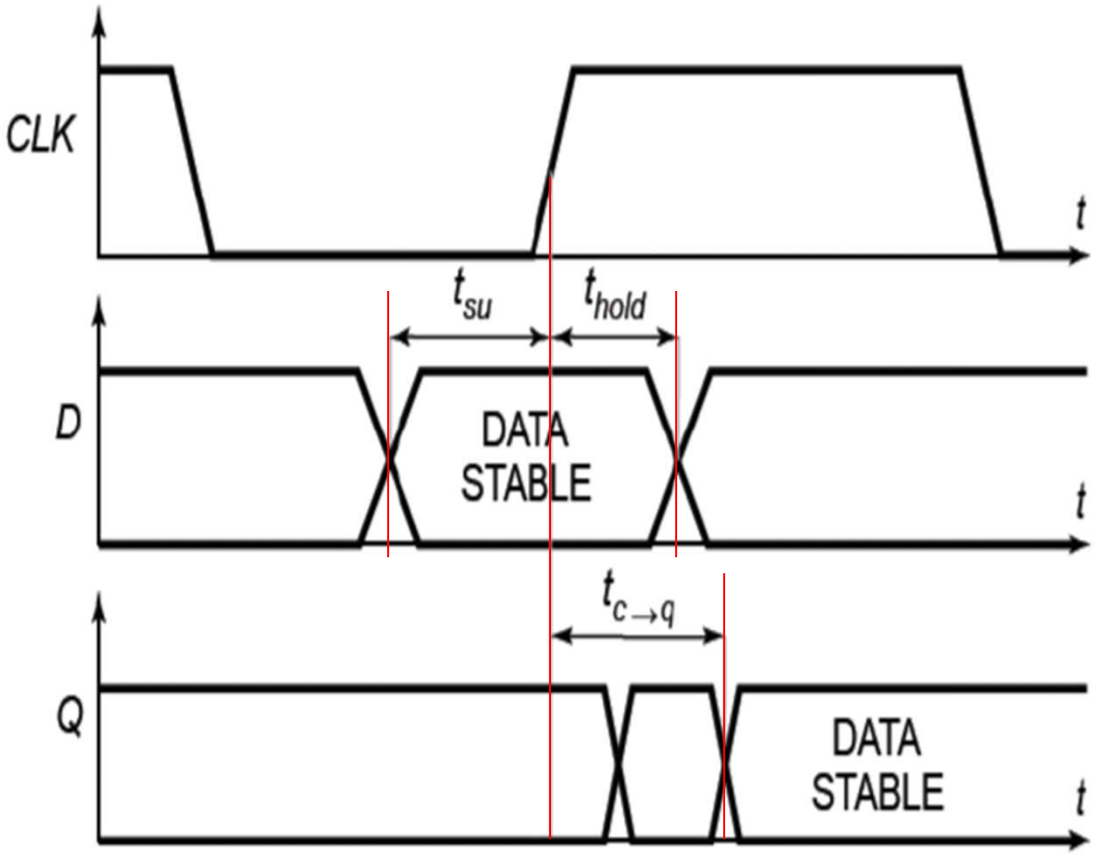
Tipi di registri

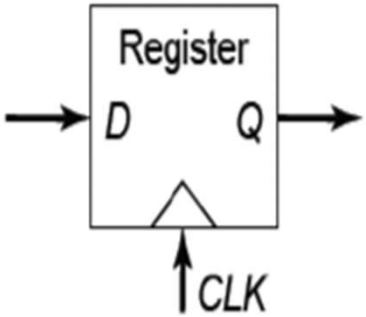
- Esitono due tipi di registri:
  - **Latch** – Level-sensitive
    il clock basso: la modalità di attesa
    alto: trasparente
  - **Register** – Edge-triggered
    memorizza i dati sul fronte di salita o discesa del clock (positive o negative edge triggered)





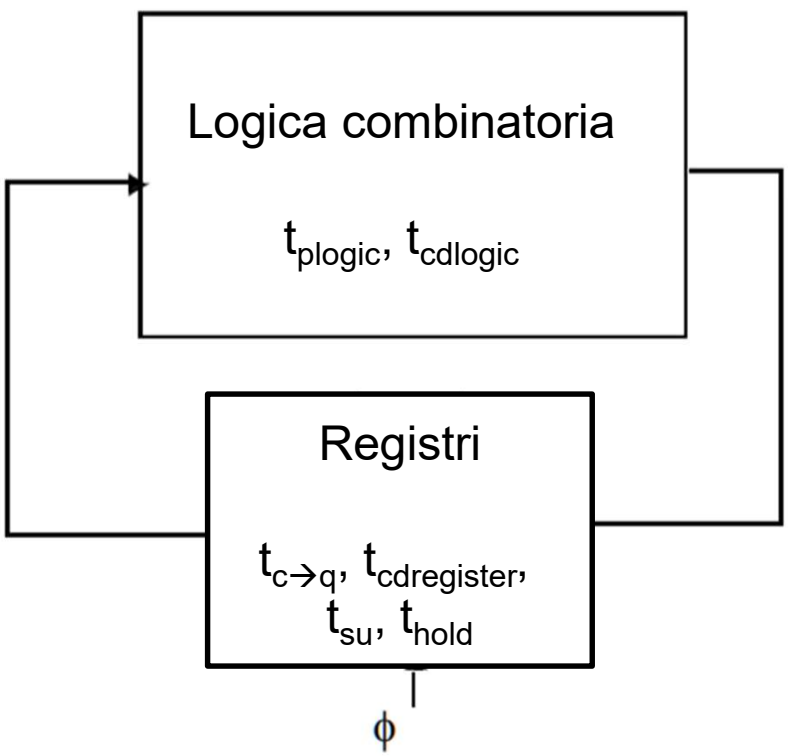
Register: Definizione Del Tempo





t_{su} : setup time
t_{hold}: hold time
$t_{c \rightarrow q}$: propagation time

Massima frequenza di clock



Deve essere:

$$T \geq t_{c\rightarrow q} + t_{plogic} + t_{su}$$

dove:

$t_{c\rightarrow q}$ è il tempo massimo di propagazione del registro

t_{plogic} è il tempo massimo di propagazione della logica combinatoria

Ed inoltre:

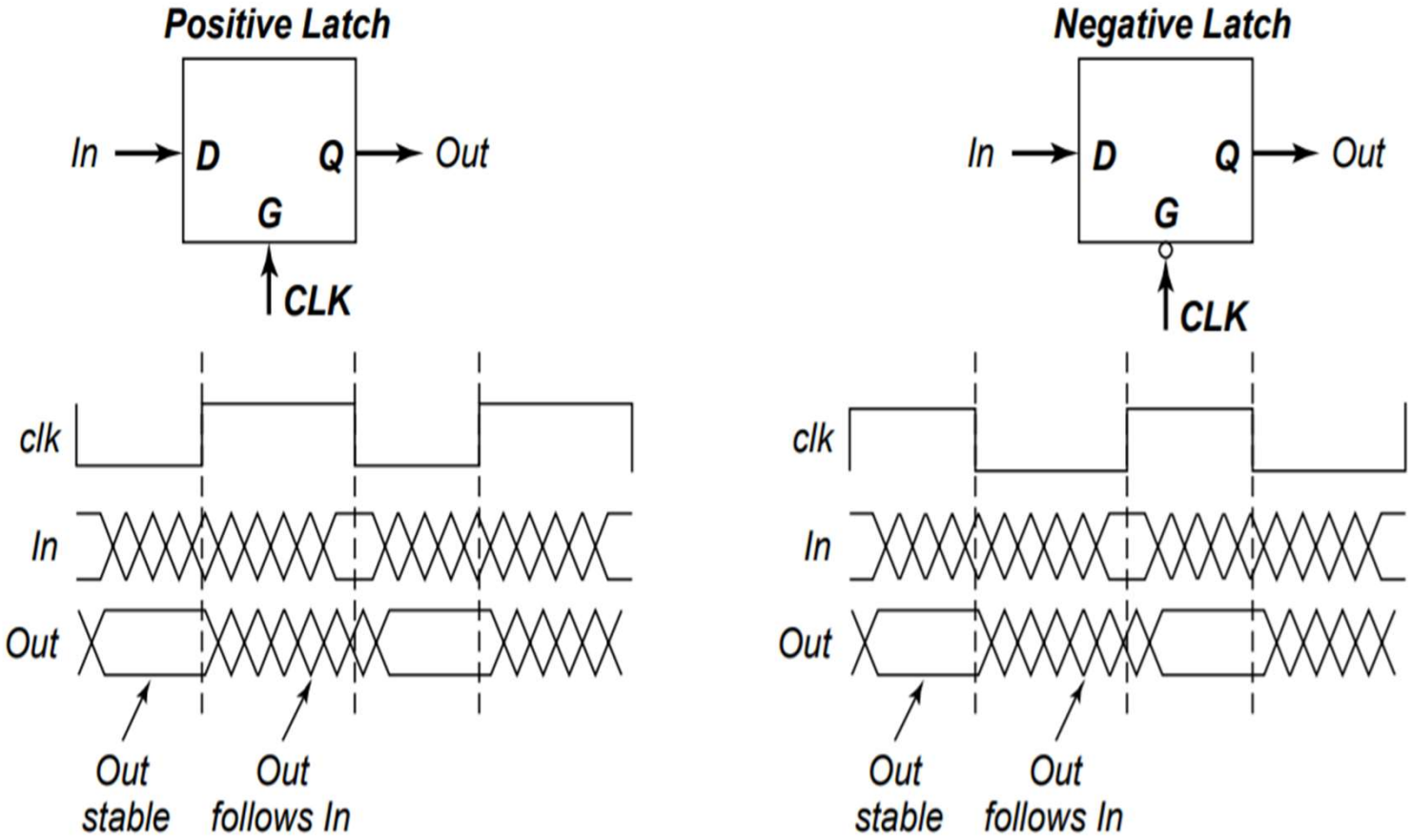
$$t_{cdregister} + t_{cdplogic} \geq t_{hold}$$

dove:

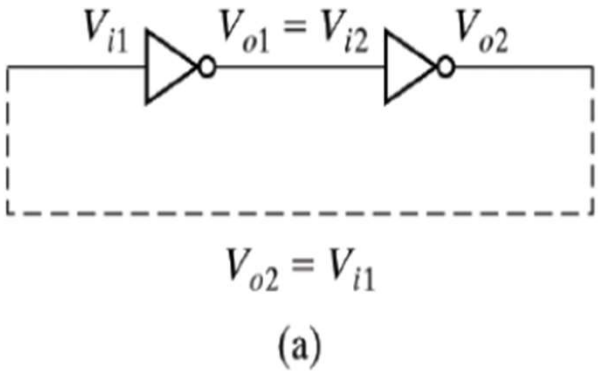
$t_{cdregister}$ è il tempo minimo di propagazione del registro

$t_{cdlogic}$ è il tempo minimo di propagazione della logica (tempo di contaminazione)

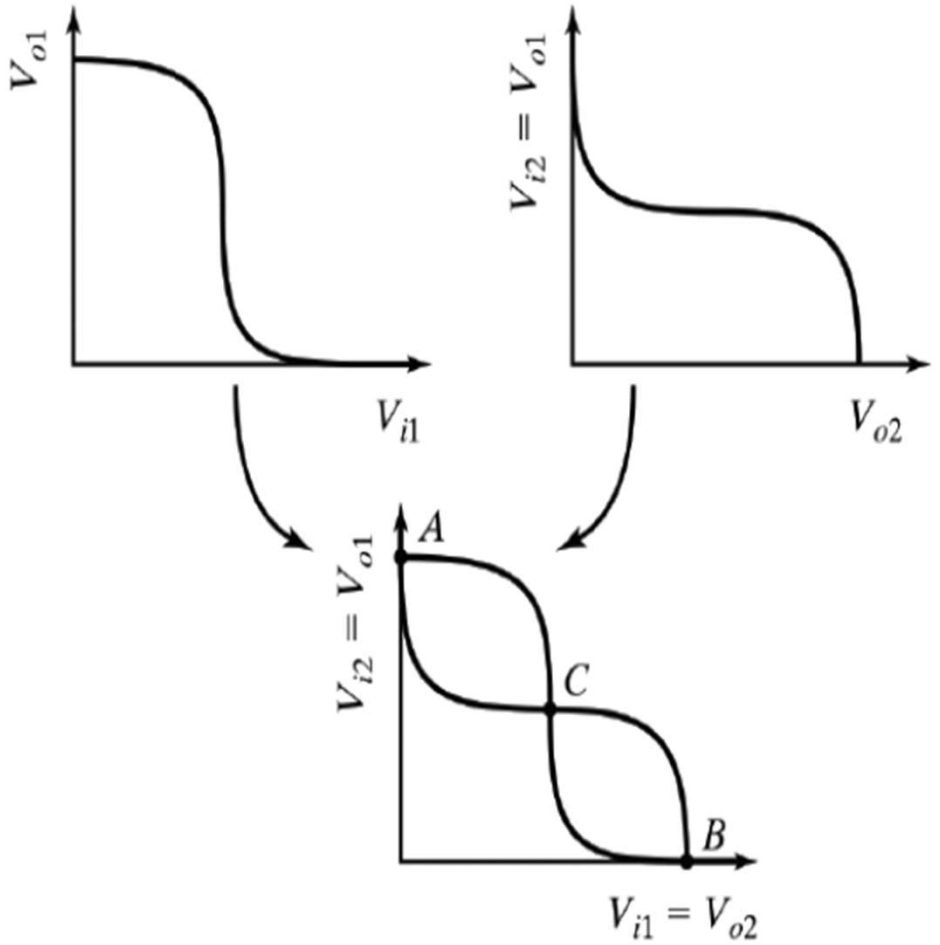
l Latches


Positive Latch
In
D
Q
Out
G
CLK
clk
In
Out
Out stable
Out follows In
Negative Latch
In
D
Q
Out
G
CLK
clk
In
Out
Out stable
Out follows In

Principio di Bistabilità: flip-flop

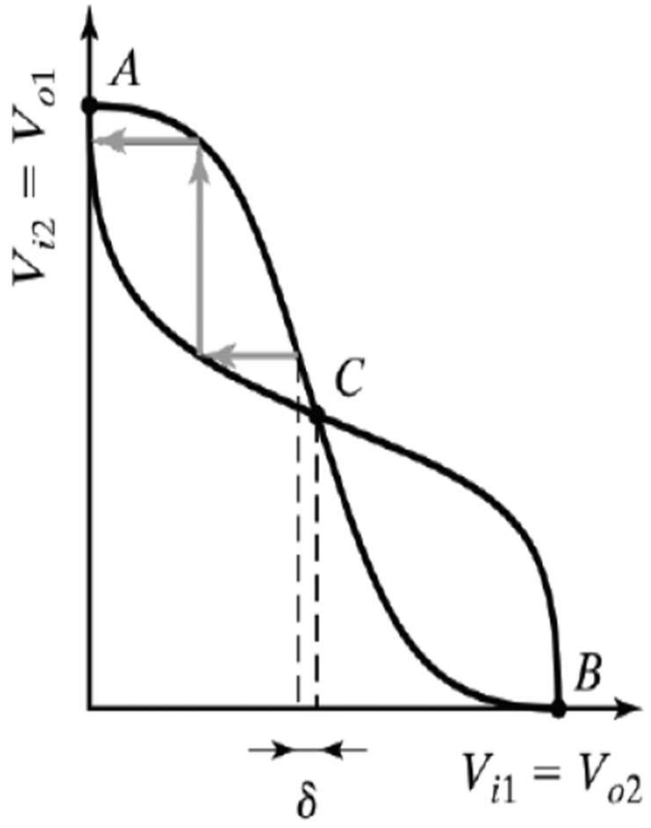


(a)

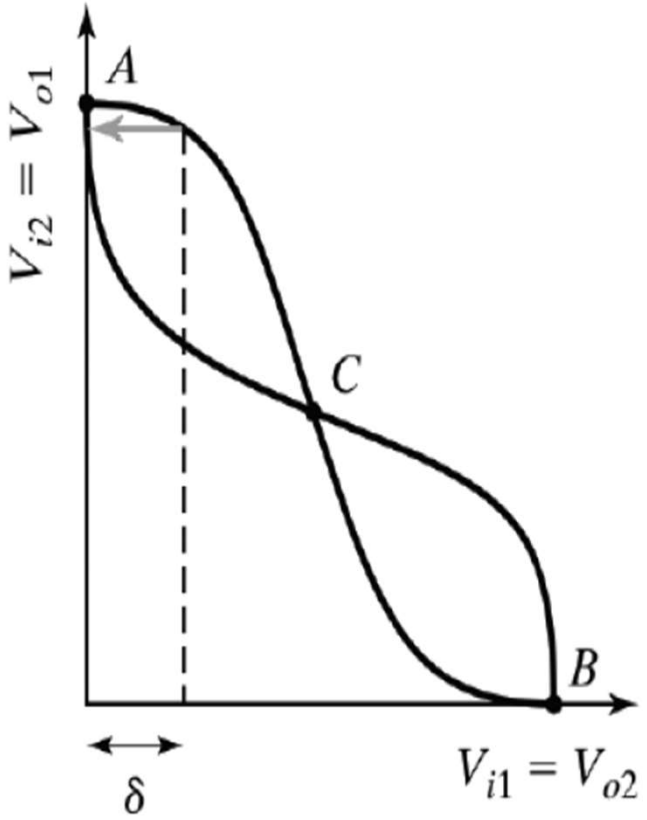


(b)

Metastabilità

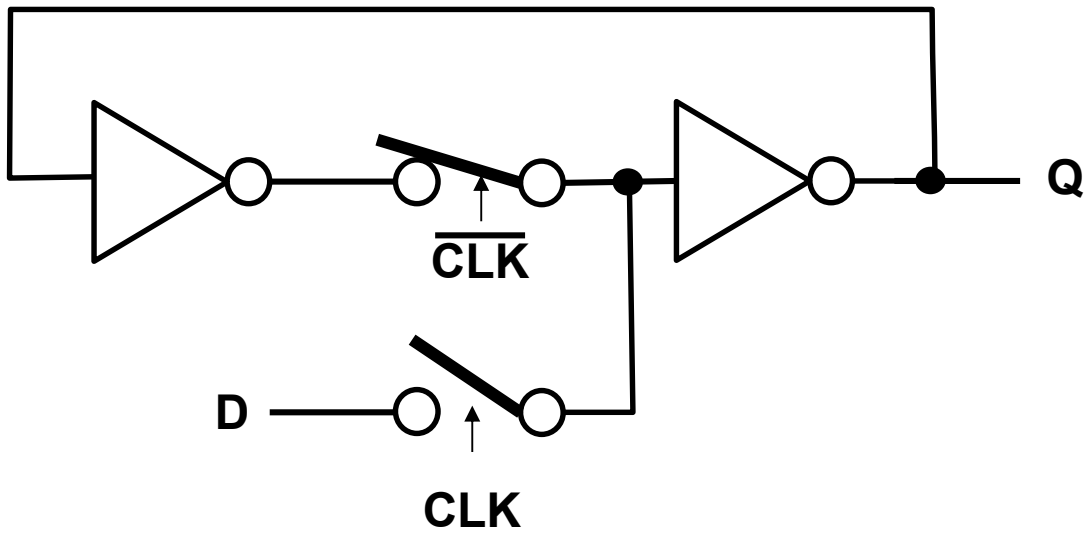


(a)



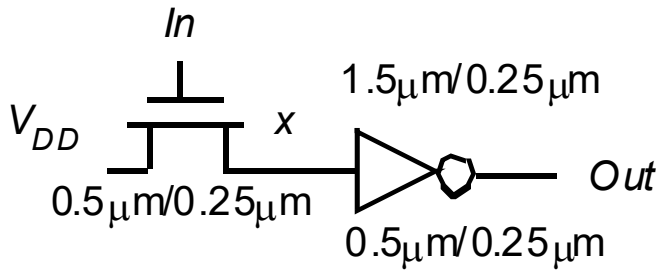
(b)

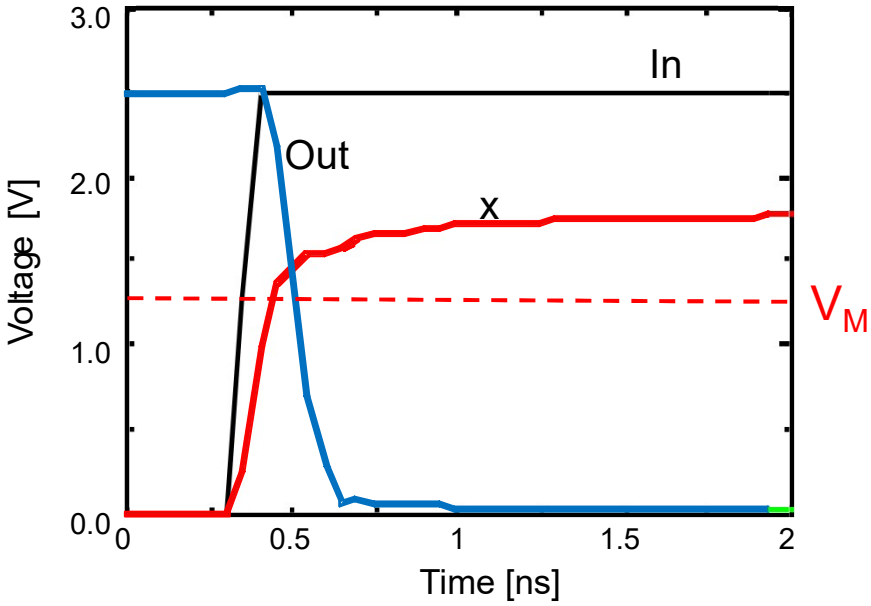
Dal flip-flop al (positive) latch



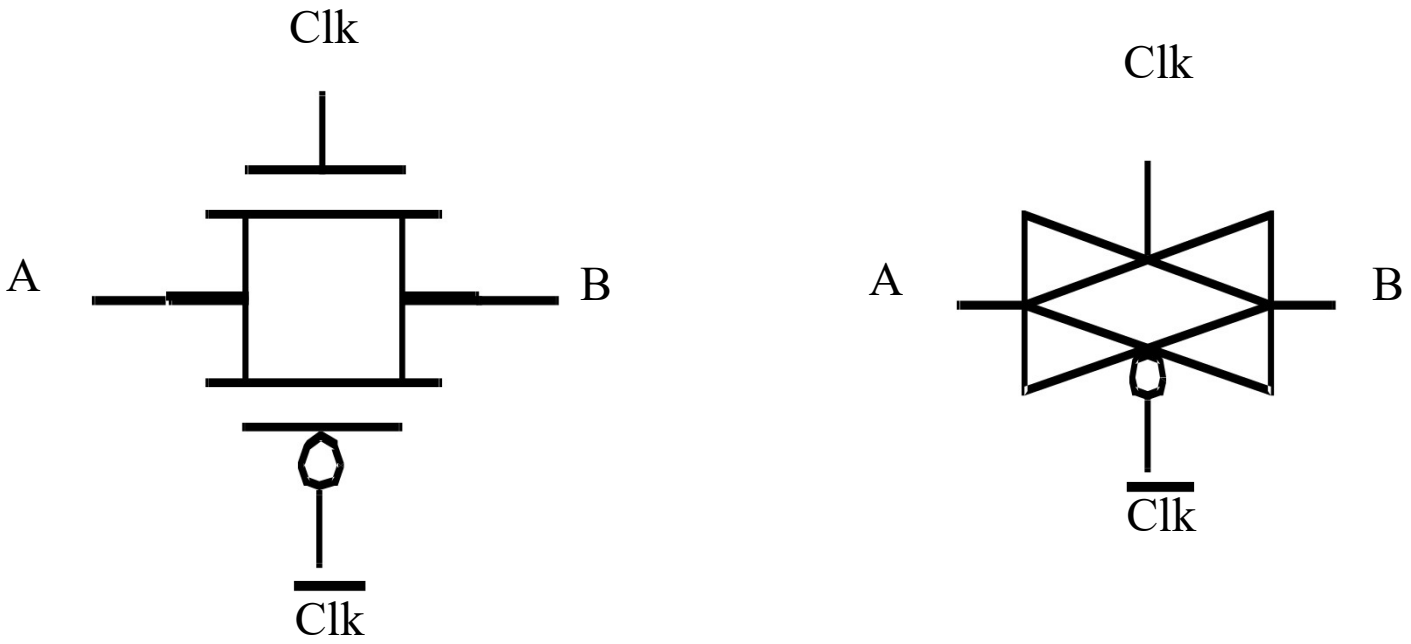
$$Q = \overline{Clk} \cdot Q + Clk \cdot D$$

Transmission gate – NMOS only





Transmission gate – CMOS

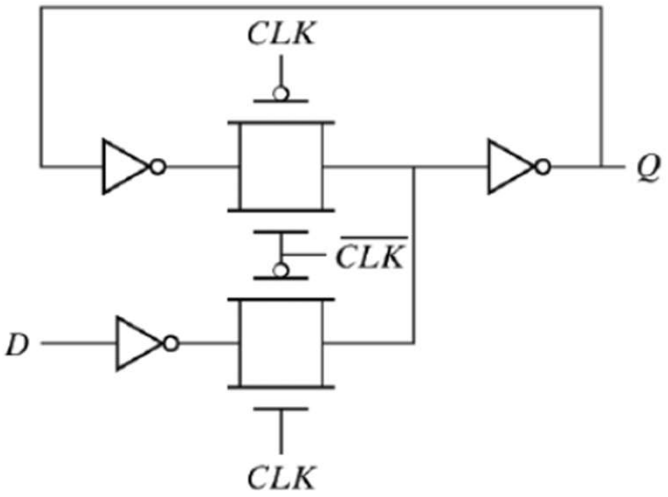


Quando Clk=1 allora $V_A=V_B$

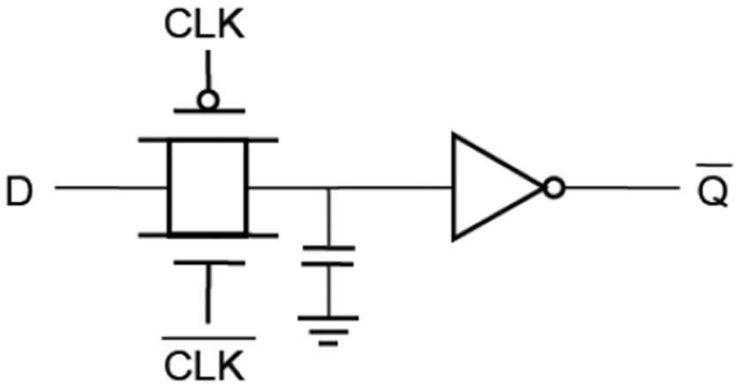
Latch a multiplexer

- Utilizzare il clock come segnale di disaccoppiamento, che distingue tra gli stati trasparenti e opachi
- Due transmission gate fungono da multiplexer

Static



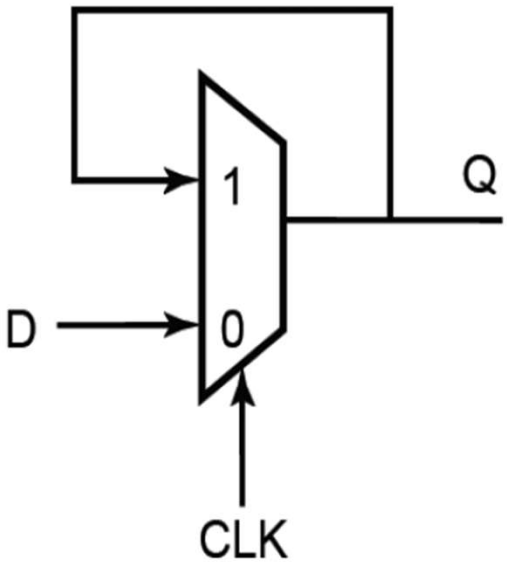
Dynamic



$$Q = \overline{Clk} \cdot Q + Clk \cdot D$$

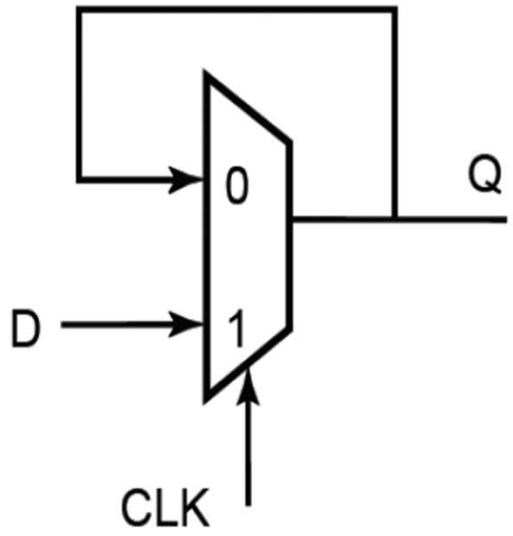
Latch Positivo e Negativo

Negative latch
(transparent when CLK= 0)



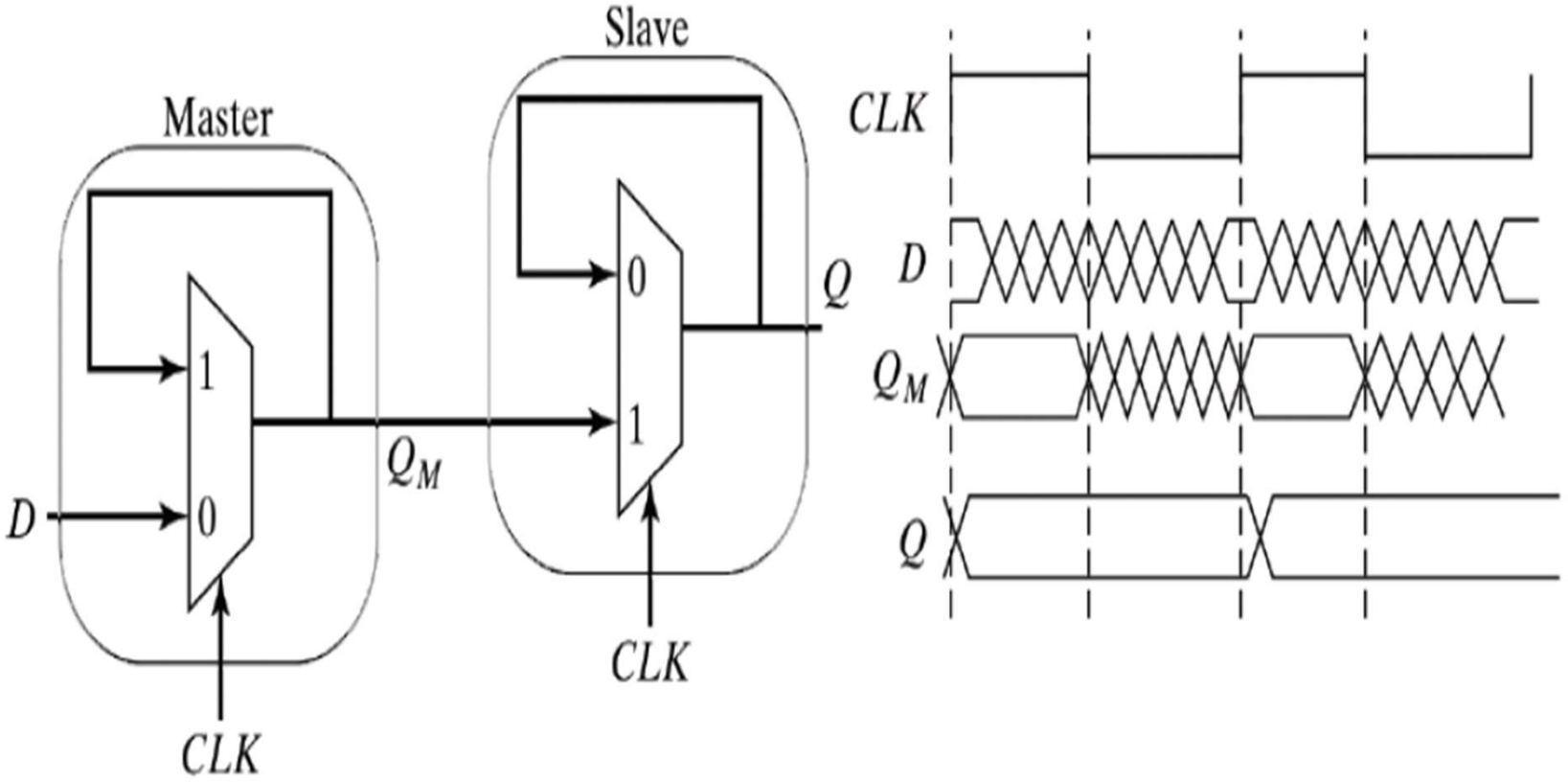
$$Q = Clk \cdot Q + \overline{Clk} \cdot D$$

Positive latch
(transparent when CLK= 1)

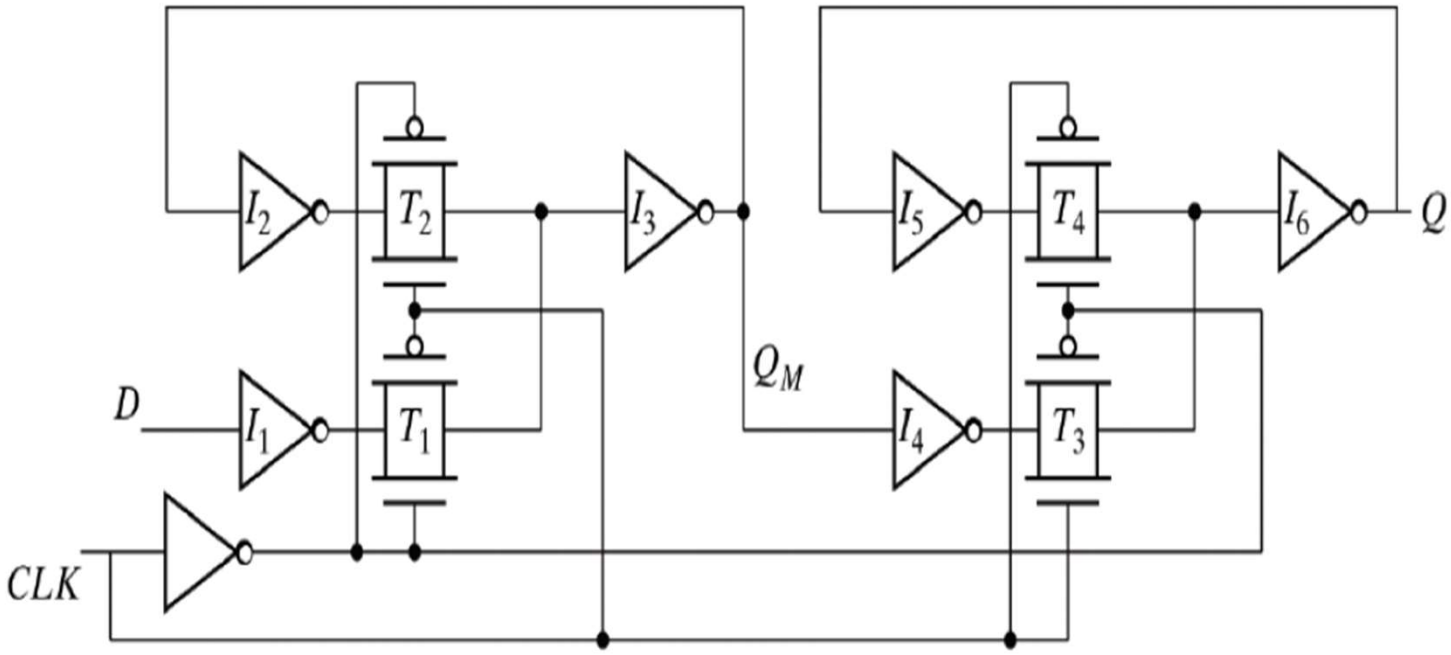


$$Q = \overline{Clk} \cdot Q + Clk \cdot D$$

Master–Slave Register (Edge-Triggered)

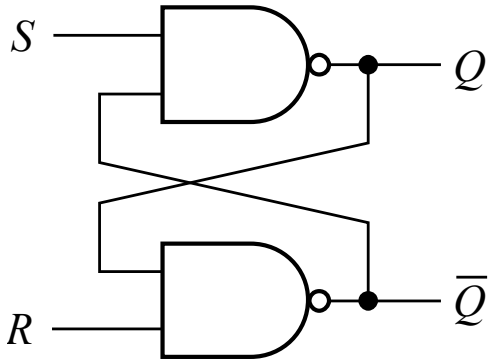


Master–Slave Register (Edge-Triggered)

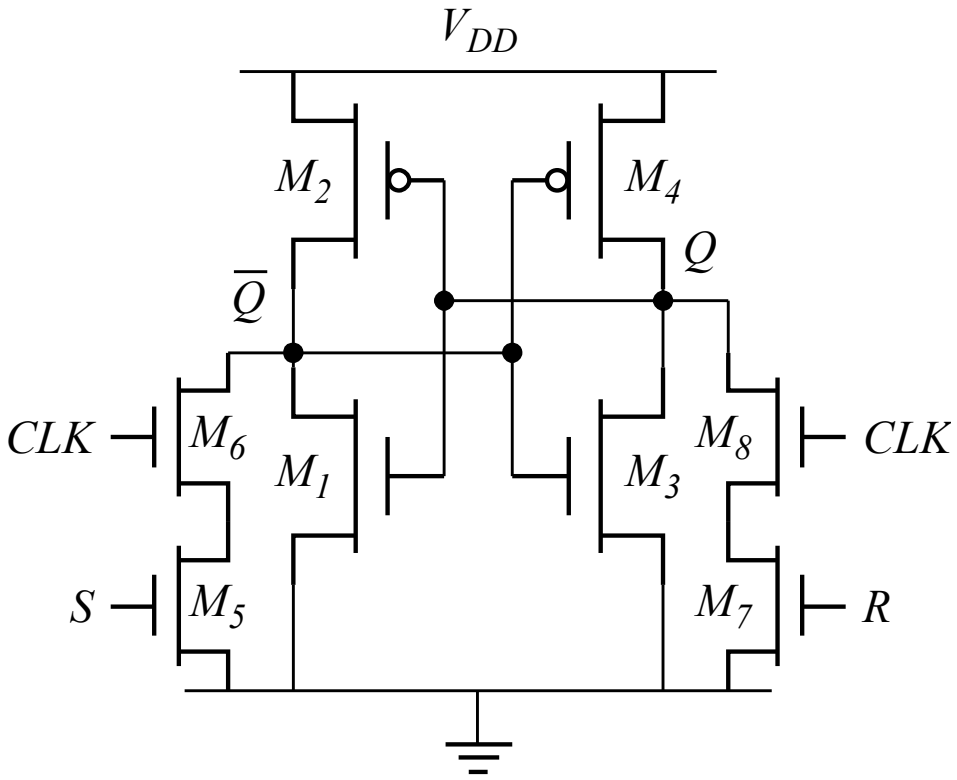


Flip-Flop SR - NAND

Cross-coupled NANDs



Added clock



This is not used in datapaths any more, but is a basic building memory cell