CSEE223

Name: _____

Flip-Flops Quiz 1

Date: _____

1. The truth table for an S-R flip-flop has how many VALID entries?
a) 1
b) 2
c) 3
d) 4

2. A basic S-R flip-flop can be constructed by cross-coupling of which basic logic gates?
a) AND or OR gates
b) XOR or XNOR gates
c) NOR or NAND gates
d) AND or NOR gates
.
3. The logic circuits whose outputs at any instant of time depends only on the present input but also on the past outputs are called
a) Combinational circuits
b) Sequential circuits
c) Latches
d) Flip-flops

4. Whose operations are more faster among the following?
a) Combinational circuits
b) Sequential circuits
c) Latches
d) Flip-flops

5. How many types of sequential circuits are?
a) 2
b) 3
c) 4
d) 5

6. The sequential circuit is also called _____
a) Flip-flop
b) Latch
c) Strobe
d) Adder

7. The basic latch consists of _____
a) Two inverters
b) Two comparators

c) Two amplifiers
d) Two adders

8. The output of latches will remain in set/reset until _____
a) The trigger pulse is given to change the state
b) Any pulse given to go into previous state
c) They don't get any pulse more
d) The pulse is edge-triggered

9. In a NAND based S-R latch, if S=1 & R=1 then the state of the latch is _____
a) No change
b) Set
c) Reset
d) Forbidden.

10. One major difference between a NAND based S'-R' latch & a NOR based S-R latch is _____
a) The inputs of NOR latch are 0 but 1 for NAND latch
b) The inputs of NOR latch are 1 but 0 for NAND latch
c) The output of NAND latch becomes set if S'=0 & R'=1 and vice versa for NOR latch
d) The output of NOR latch is 1 but 0 for NAND latch

11. The Gated S-R flip flop consist of _____
a) 4 AND gates
b) Two additional AND gates
c) An additional clock input
d) 3 AND gates

12. What is one disadvantage of an S-R flip-flop?
a) It has no Enable input
b) It has a RACE condition
c) It has no clock input
d) Invalid State

13. If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____
a) SET
b) RESET
c) Clear
d) Invalid

14. A latch is an example of a _____
a) Monostable multivibrator
b) Astable multivibrator
c) Bistable multivibrator
d) 555 timer

.
15. Latch is a device with _____
a) One stable state
b) Two stable state
c) Three stable state
d) Infinite stable states
.
16. Why latches are called a memory devices?
a) It has capability to stare 8 bits of data
b) It has internal memory of 4 bit
c) It can store one bit of data
d) It can store infinite amount of data
.
17. Two stable states of latches are _____
a) Astable & Monostable
b) Low input & high output
c) High output & low output
d) Low output & high input

18. The full form of SR is _____
a) System rated
b) Set reset
c) Set ready
d) Set Rated
.
19. The SR latch consists of _____
a) 1 input
b) 2 inputs
c) 3 inputs
d) 4 inputs

20. The outputs of SR latch are _____
a) x and y
b) a and b
c) s and r
d) q and q’

.
21. The NAND latch works when both inputs are _____
a) 1
b) 0
c) Inverted
d) Don’t cares
22. The first step of analysis procedure of SR latch is to _____
a) label inputs
b) label outputs

c) label states
d) label tables
.
23. The inputs of SR latch are _____
a) x and y
b) a and b
c) s and r
d) j and k

24. When a high is applied to the Set line of an SR latch, then _____
a) Q output goes high
b) Q’ output goes high
c) Q output goes low
d) Both Q and Q’ go high

25. When both inputs of SR latches are low, the latch _____
a) Q output goes high
b) Q’ output goes high
c) It remains in its previously set or reset state
d) it goes to its next set or reset state