CSEE223 Lab

Name: _____

Logic Gates

Date: _____

Reading
Lecture on the Logic Gates

Objectives
After performing this experiment, you will be able to
1. Construct a basic logic gate circuit using Multisim 2001.
2. Construct a basic logic gate circuit using a breadboard.
3. Understand the function of the 7 basic logic gates.
4. Maintain an engineering notebook during lab activities..

Materials Needed
1 – Windows PC with Multisim 2001
1 – 7408 (2-input AND gate) (OPTIONAL)
1 – 7432 (2-input OR gate) (OPTIONAL)
1 – 7400 (2-input NAND gate) (OPTIONAL)
1 – 7402 (2-input NOR gate) (OPTIONAL)
1 – 7404 (Inverter) (OPTIONAL)
1 – resistor 100Ω (OPTIONAL)
1 – dip switch (OPTIONAL)
3 – LEDs (OPTIONAL)

Summary of Theory and Operation
Lecture on the Logic Gates

Procedures

1. Prelab: Complete “Logic” columns for Table1 through Table 7.

2. Use the Data Sheets and illustrations provided in pages 13 through 15 to breadboard each circuit.

3. Using Multisim/Breadboard construct the following AND Gate circuit:

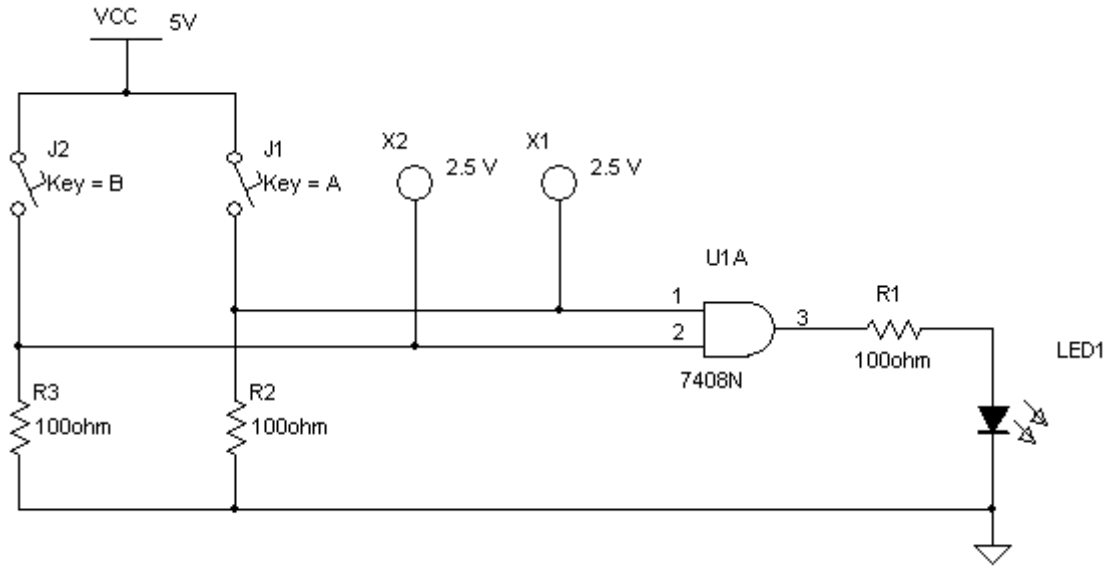


FIG 1

4. Using the A and B keys set each key to the appropriate input setting. Record the condition of the LED for each input combination. Record the logical binary equivalent at each output.

TABLE 1					
INPUTS				OUTPUT (*Y*)	
A		*B*			
X1 Lamp	Logic	X2 Lamp	Logic	LED1 (On/Off)	Logic
OFF (0V)		OFF (0V)			
OFF (0V)		ON (5V)			
ON (5V)		OFF (0V)			
ON (5V)		ON (5V)			

Prelab Signoff: _____

Breadboard Signoff: _____

Notebook Entry Signoff: _____

5. Using Multisim/Breadboard construct the following OR Gate circuit:

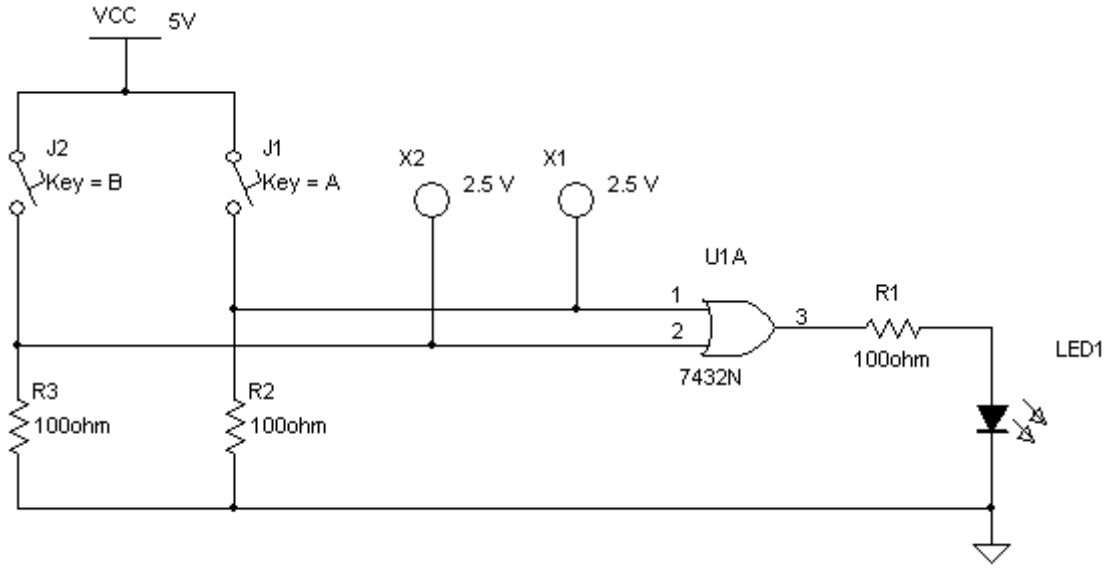


FIG 2

6. Using the A and B keys set each key to the appropriate input setting. Record the condition of the LED for each input combination. Record the logical binary equivalent at each output.

TABLE 2					
INPUTS				OUTPUT (*Y*)	
A		*B*			
X1 Lamp	Logic	X2 Lamp	Logic	LED1 (On/Off)	Logic
OFF (0V)		OFF (0V)			
OFF (0V)		ON (5V)			
ON (5V)		OFF (0V)			
ON (5V)		ON (5V)			

Prelab Signoff: _____

Breadboard Signoff: _____

Notebook Entry Signoff: _____

7. Using Multisim/Breadboard construct the following NAND Gate circuit:

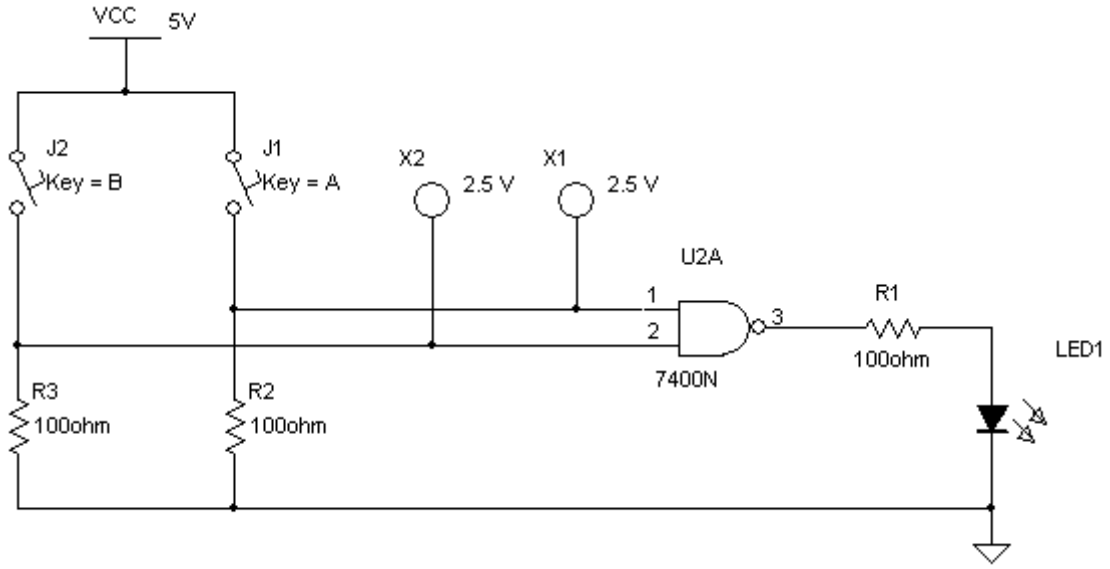


FIG 3

8. Using the A and B keys set each key to the appropriate input setting. Record the condition of the LED for each input combination. Record the logical binary equivalent at each output.

TABLE 3					
INPUTS				OUTPUT (*Y*)	
A		*B*			
X1 Lamp	Logic	X2 Lamp	Logic	LED1 (On/Off)	Logic
OFF (0V)		OFF (0V)			
OFF (0V)		ON (5V)			
ON (5V)		OFF (0V)			
ON (5V)		ON (5V)			

Prelab Signoff: _____

Breadboard Signoff: _____

Notebook Entry Signoff: _____

9. Using Multisim/Breadboard construct the following NOR Gate circuit:

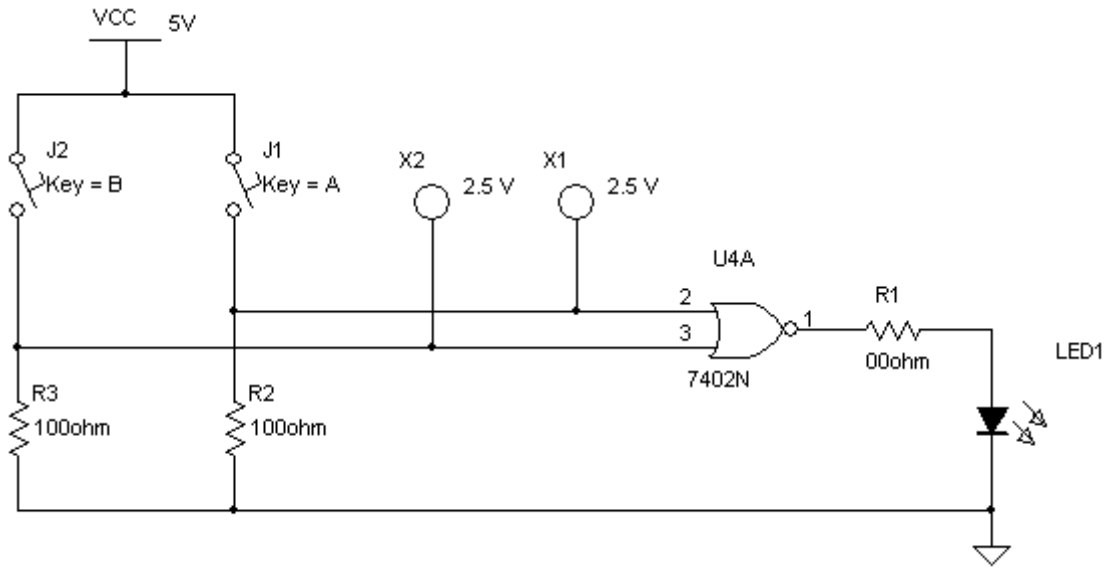


FIG 4

10. Using the A and B keys set each key to the appropriate input setting. Record the condition of the LED for each input combination. Record the logical binary equivalent at each output.

TABLE 4					
INPUTS				OUTPUT (*Y*)	
A		*B*			
X1 Lamp	Logic	X2 Lamp	Logic	LED1 (On/Off)	Logic
OFF (0V)		OFF (0V)			
OFF (0V)		ON (5V)			
ON (5V)		OFF (0V)			
ON (5V)		ON (5V)			

Prelab Signoff: _____

Breadboard Signoff: _____

Notebook Entry Signoff: _____

11. Using Multisim/Breadboard construct the following XOR Gate circuit:

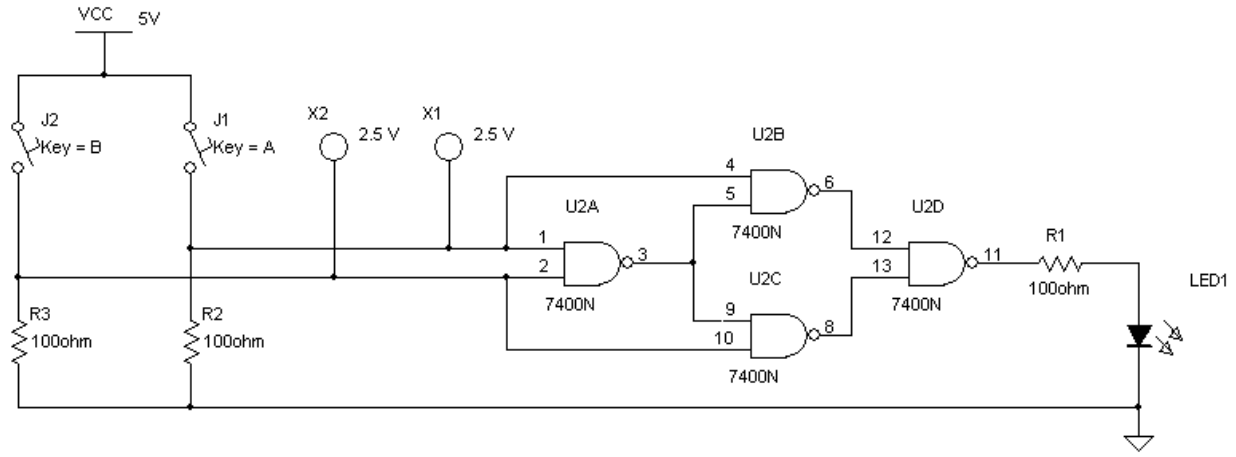


FIG 5

12. Using the A and B keys set each key to the appropriate input setting. Record the condition of the LED for each input combination. Record the logical binary equivalent at each output.

TABLE 5					
INPUTS				OUTPUT (*Y*)	
A		*B*			
X1 Lamp	Logic	X2 Lamp	Logic	LED1 (On/Off)	Logic
OFF (0V)		OFF (0V)			
OFF (0V)		ON (5V)			
ON (5V)		OFF (0V)			
ON (5V)		ON (5V)			

Prelab Signoff: _____

Breadboard Signoff: _____

Notebook Entry Signoff: _____

13. Using Multisim/Breadboard construct the following XNOR Gate circuit:

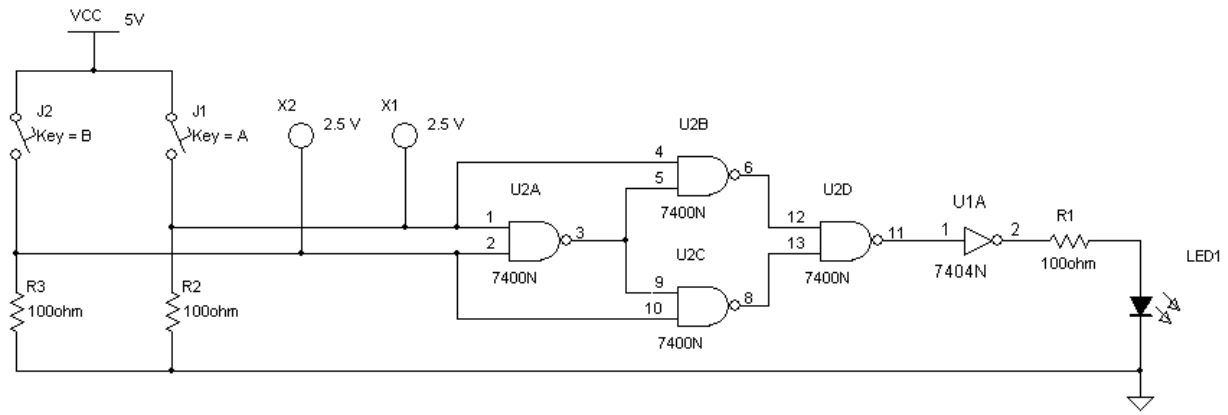


FIG 6

14. Using the A and B keys set each key to the appropriate input setting. Record the condition of the LED for each input combination. Record the logical binary equivalent at each output.

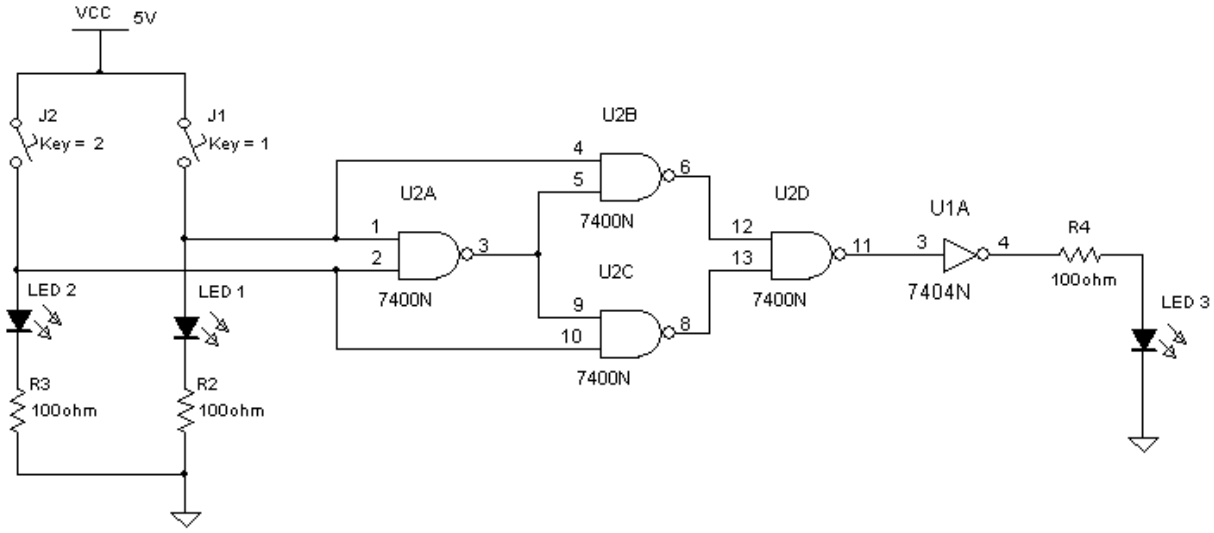
TABLE 6					
INPUTS				OUTPUT (*Y*)	
A		*B*			
X1 Lamp	Logic	X2 Lamp	Logic	LED1 (On/Off)	Logic
OFF (0V)		OFF (0V)			
OFF (0V)		ON (5V)			
ON (5V)		OFF (0V)			
ON (5V)		ON (5V)			

Prelab Signoff: _____

Breadboard Signoff: _____

Notebook Entry Signoff: _____

15. Using the data sheets for the 7400 NAND gate IC and 7404 Invert gate IC, construct the circuit below. Connect your dip switches to the inputs of the logic and demonstrate its operation for a sign-off.



16. Using the A and B keys set each key to the appropriate input setting. Record the condition of the LED for each input combination. Record the logical binary equivalent at each output.

TABLE 7					
INPUTS				OUTPUT (*Y*)	
A		*B*			
X1 Lamp	Logic	X2 Lamp	Logic	LED1 (On/Off)	Logic
OFF (0V)		OFF (0V)			
OFF (0V)		ON (5V)			
ON (5V)		OFF (0V)			
ON (5V)		ON (5V)			

Prelab Signoff: _____

Breadboard Signoff: _____

Notebook Entry Signoff: _____

Questions

1. The AND gate is referred to as the “ALL or Nothing Gate”.

    a. True
    b. False

2. The XOR gate is referred to as the “Some but Not ALL” gate.

    a. True
    b. False

3. LOW voltage (0V) represents a

    a. Logical 0
    b. Logical 1

4. HIGH voltage (5V) represents a

    a. Logical 0
    b. Logical 1

5. A NOR gate can be constructed with an OR gate and an Inverter.

    a. True
    b. False

6. Write the Boolean expression for

    a. 2-input AND gate _____
    b. 2-input NAND gate _____
    c. 2-input OR gate _____
    d. 2-input NOR gate _____

7. The OR gate is referred to as the “Any or ALL” gate.

    a. True
    b. False

8. The NOT gate inverts or compliments the input.

    a. True
    b. False

9. Draw the Truth Table for a 3-input OR gate suing 1's and 0's.

INPUTS			OUTPUT
A	B	C	Y

10. The NAND gate is called the Universal gate because it can be used in conjunction with any other gate to create any logic function..

    a. True
    b. False

Data Sheets

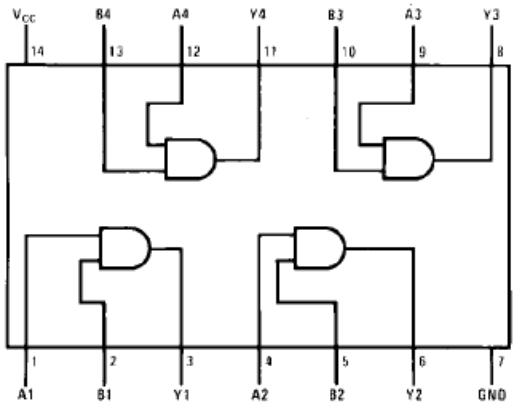
FAIRCHILD
SEMICONDUCTOR™

DM74LS08
Quad 2-Input AND Gates

General Description

This device contains four independent gates each of which performs the logic AND function.

Connection Diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SN5432, SN54LS32, SN54S32, SN7432, SN74LS32, SN74S32
QUADRUPLE 2-INPUT POSITIVE-OR GATES

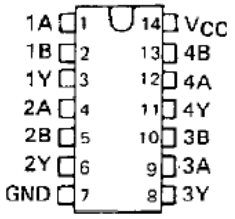
DECEMBER 1983 – REVISED MARCH 1988

description

These devices contain four independent 2-input OR gates.

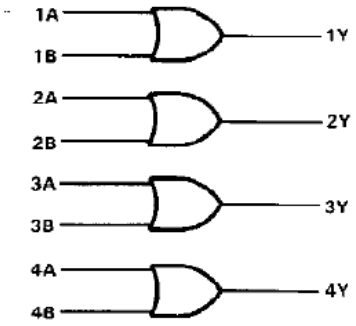
The SN5432, SN54LS32 and SN54S32 are characterized for operation over the full military range of −55°C to 125°C. The SN7432, SN74LS32 and SN74S32 are characterized for operation from 0°C to 70°C.

SN5432, SN54LS32, SN54S32 . . . J OR W PACKAGE
SN7432 . . . N PACKAGE
SN74LS32, SN74S32 . . . D OR N PACKAGE
(TOP VIEW)



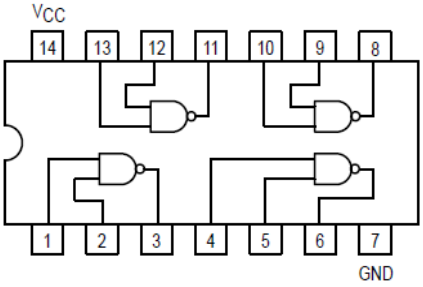
SN54LS32, SN54S32 . . . FK PACKAGE
(TOP VIEW)

logic diagram



MOTOROLA

QUAD 2-INPUT NAND GATE



SN54/74LS00
74HC00 / 74HCT00

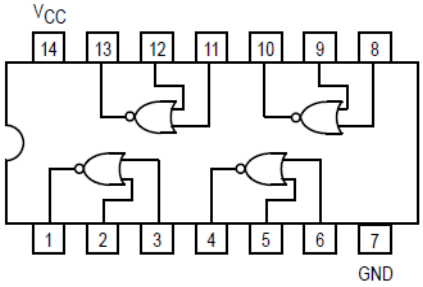
DESCRIPTION

QUAD 2-INPUT NAND GATE

LOW POWER SCHOTTKY
OR
HIGH SPEED CMOS

MOTOROLA

QUAD 2-INPUT NOR GATE



SN54/74LS02

QUAD 2-INPUT NOR GATE

LOW POWER SCHOTTKY

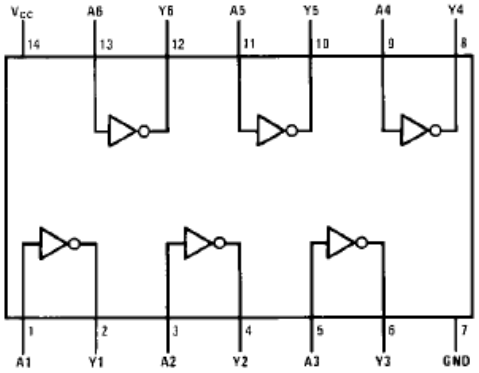
FAIRCHILD
SEMICONDUCTOR TM

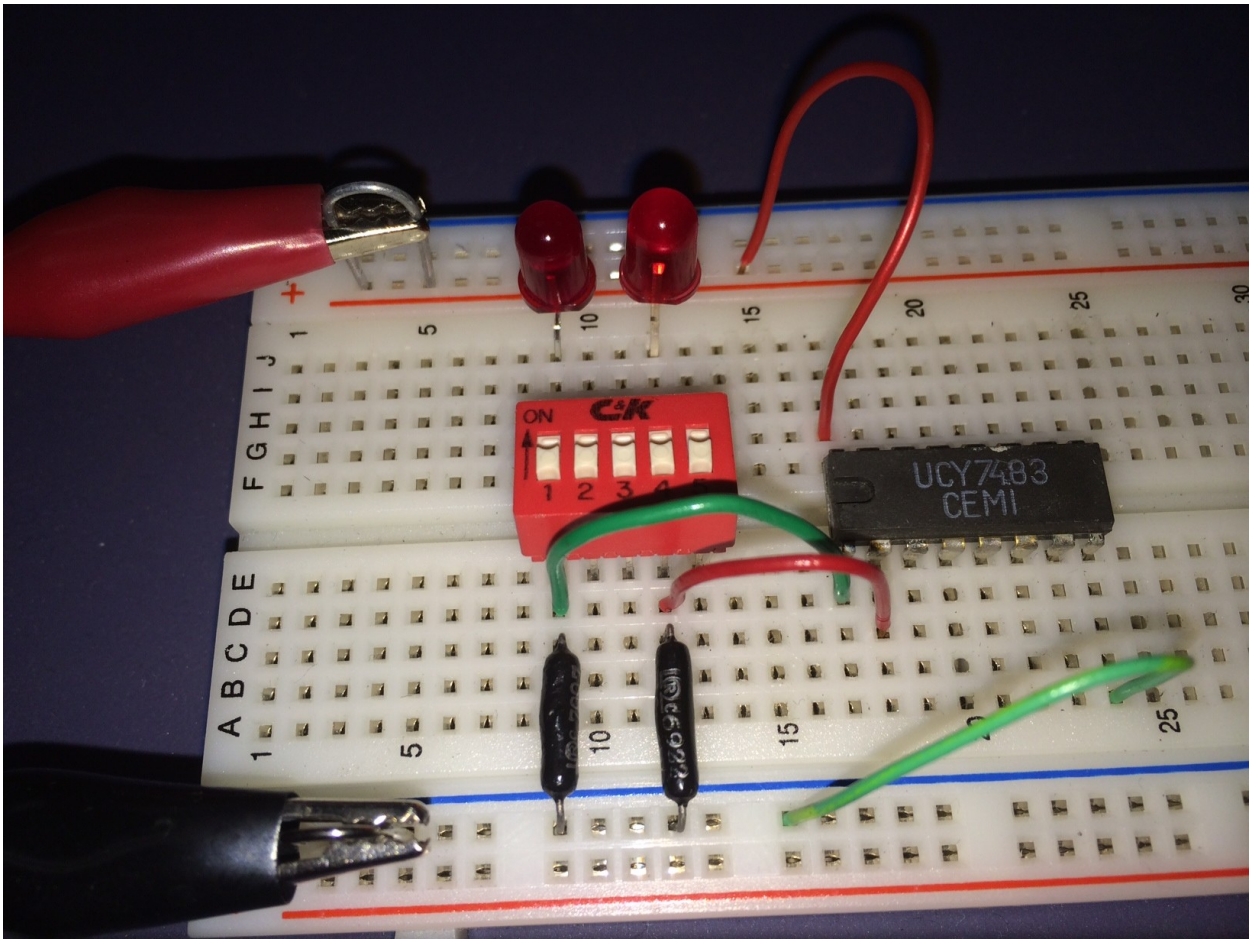
DM74LS04
Hex Inverting Gates

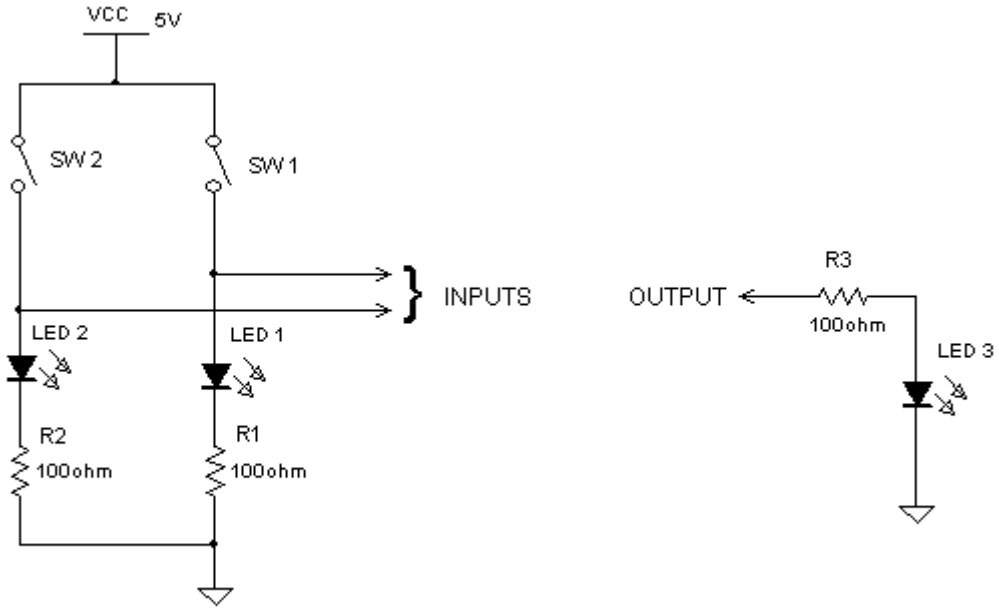
General Description

This device contains six independent gates each of which performs the logic INVERT function.

Connection Diagram




ON
C&K
1 2 3 4
UCY7483
CEMI


VCC
5V
SW 2
SW 1
INPUTS
LED 2
LED 1
R2
100ohm
R1
100ohm
OUTPUT
R3
100ohm
LED 3