CSEE223 Lab

Name: _____

Flip Flops

Date: _____

Reading
Lecture on the Flip-Flops

Objectives
After performing this experiment, you will be able to construct and understand the function of basic Flip Flops.

Materials Needed
1 – 7476 (J-K Flip Flop)
1 – 7474 (D Flip Flop)
1 – 7400 (2-input NAND gate)
1 – 7402 (2-input NOR gate)
1 – 7404 (Inverter)
5 – resistors 100Ω
1 – dip switch

Summary of Theory and Operation

A **flip-flop** or **latch** is a circuit that has two stable states and can be used to store state information. A flip-flop is a *bistable multivibrator*. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs. It is the basic storage element in sequential logic. Flip-flops and latches are a fundamental building block of digital electronics systems used in computers, communications, and many other types of systems.

Flip-flops and latches are used as data storage elements. Such data storage can be used for storage of *state*, and such a circuit is described as *sequential logic*. When used in a finite-state machine, the output and next state depend not only on its current input, but also on its current state (and hence, previous inputs). It can also be used for counting of pulses, and for synchronizing variably-timed input signals to some reference timing signal.

Flip-flops can be either *simple* (transparent or opaque) or *clocked* (synchronous or edge-triggered); the simple ones are commonly called latches. The word *latch* is mainly used for storage elements, while clocked devices are described as *flip-flops*.

Procedure

1. Using Multisim, construct the SR NOR Latch circuit below.

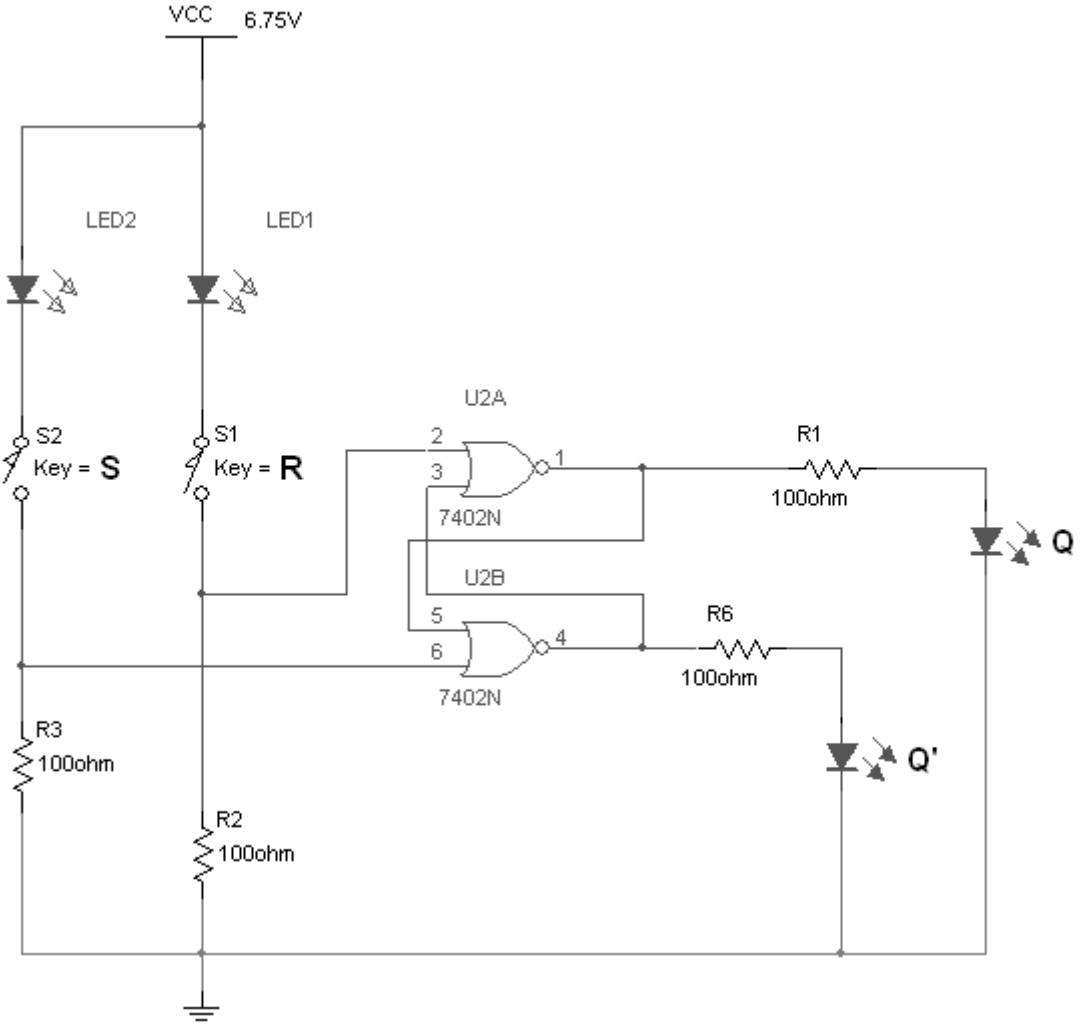

FIG 1

2. Using the switches set each switch to the appropriate input setting for ***S*** and ***R***. Record the binary condition (1 or 0) of the LED at for each input combination. Record the name of the condition (hold, reset, set, prohibited) at the ***Q*** and ***Q'*** outputs.

INPUTS		**OUTPUTS**		
S	*R*	*Q*	*Q'*	**Mode of Operation**
0	0			
0	1			
1	0			
1	1			

Notes:

- 1 = ON = Hi = ↑
- 0 = OFF = Lo = ↓
- Q’ = the compliment of Q
- Hold = Previous state or condition or no change

Demo and Signoff: _____

3. Using Multisim, construct the Gated SR NOR Latch circuit below

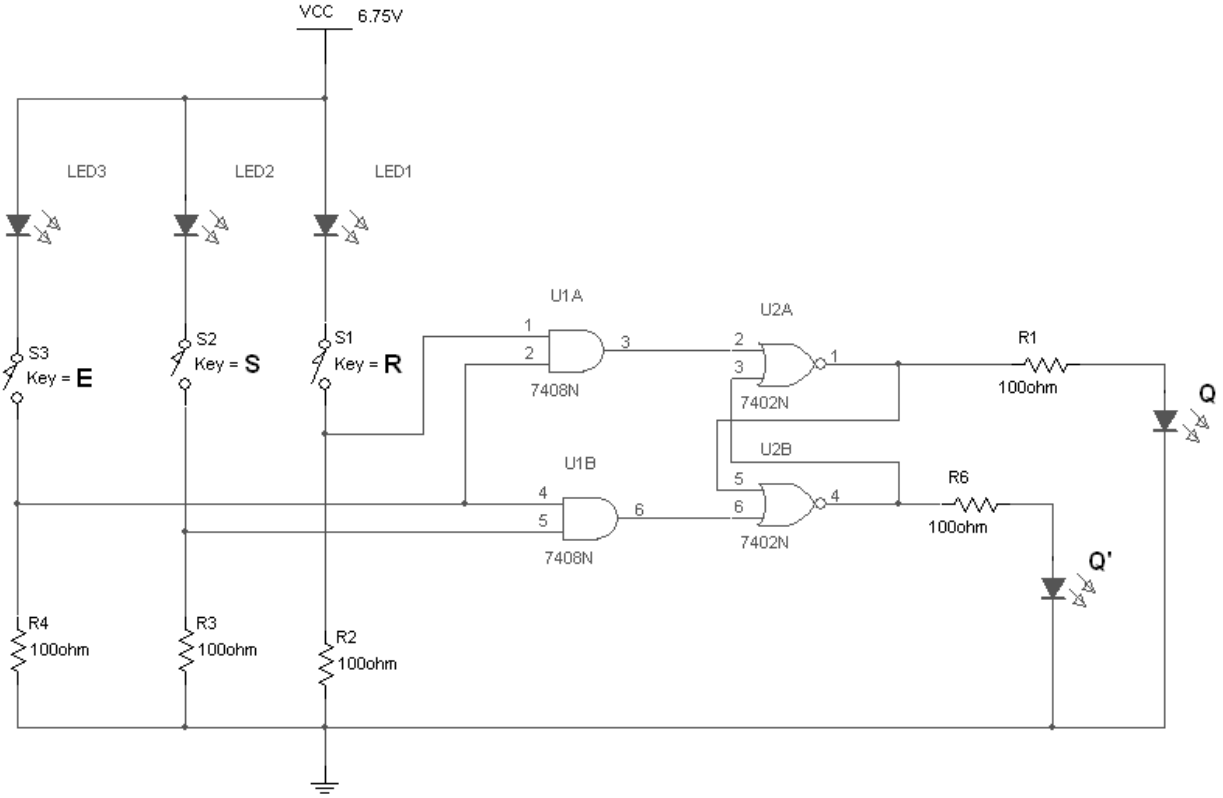

FIG 2

4. Using the dip switches set each switch to the appropriate setting for ***S, R,*** and ***E*** inputs. Record the binary condition (1 or 0) of the LED at for each input combination. Record the name of the condition (hold, reset, set, prohibited) at the ***Q*** and ***Q'*** outputs.

Mode of operation	**INPUTS**			**OUTPUTS**		
	E	*S*	*R*	*Q*	*Q'*	**Mode of Operation**
Hold	⎍	0	0			
Reset	⎍	0	1			
Set	⎍	1	0			
Prohibited	⎍	1	1			

Notes:

- 1 = ON = Hi = ↑
- 0 = OFF = Lo = ↓
- Q' = the compliment of Q
- Hold = previous state or condition or no change
- Prohibited = state or condition that is not allowed

Demo and Signoff: _____

5. Using the data sheets for the 7474 D Flip-Flop IC, construct the circuit below. Connect your dip switches to the ***D***, ***CLK***, ***PR***, and ***CLR*** inputs.

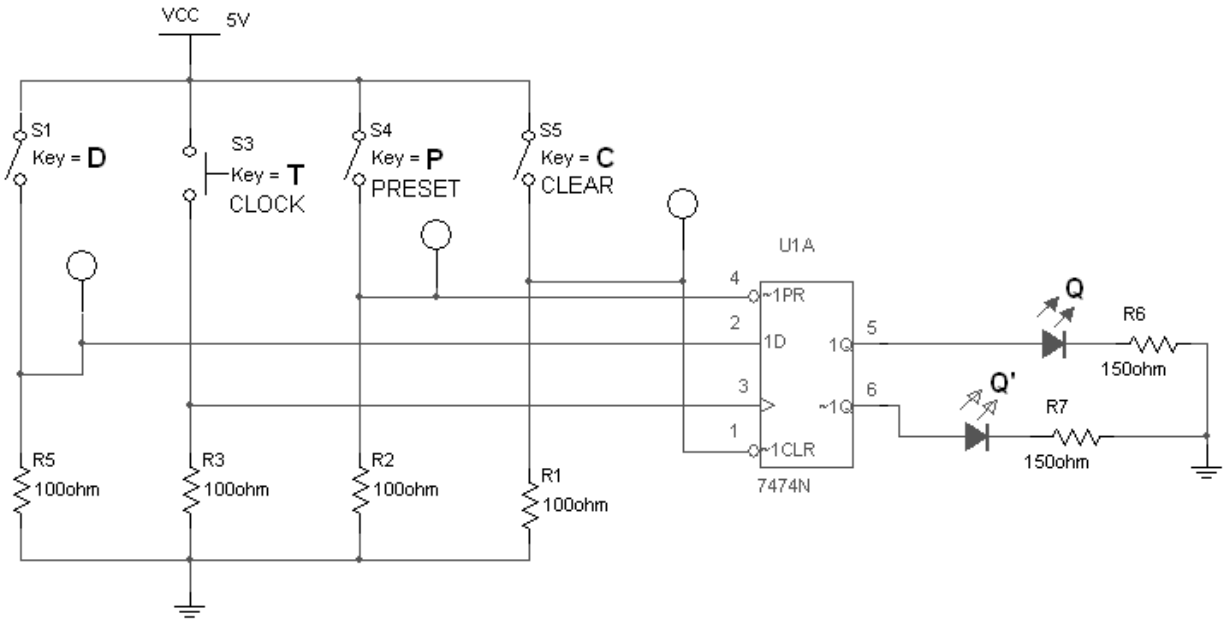

FIG 3

6. Using the dip switches set each switch to the appropriate setting for ***D***, ***CLK***, ***PR***, and ***CLR*** inputs. Record the binary condition (1 or 0) of the LED at for each input combination. Record the name of the binary condition (1 or 0) at the ***Q*** and ***Q'*** outputs.

Mode of operation	**INPUTS**				**OUTPUTS**	
	PS	*CLR*	*CLK*	*D*	*Q*	*Q'*
Asynchronous set	0	1	X	X		
Asynchronous reset	1	0	X	X		
Prohibited	0	0	X	X	X	X
Set	1	1	⎍	1		
Reset	1	1	⎍	0		

Notes:

- 1 = ON = Hi
- 0 = OFF = Lo
- X = irrelevant or don't care
- ⎍ = either high-low or low-high transition of clock pulse

Demo and Signoff: _____

7. Using the data sheets for the 7476 JK Flip-Flop IC, construct the circuit below. Connect your dip switches to the ***J***, ***K***, ***CLK***, ***PR***, and ***CLR*** inputs.

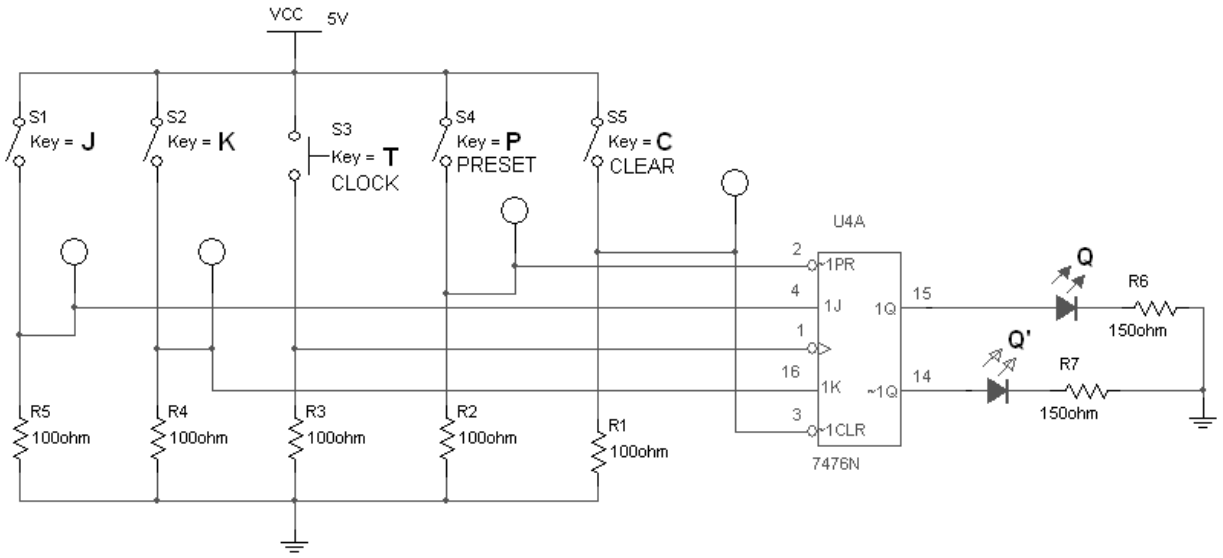

FIG 4

8. Using the switches set each switch to the appropriate setting for ***J***, ***K***, ***CLK***, ***PR***, and ***CLR*** inputs. Record the binary condition (1 or 0) of the LED at for each input combination. Record the name of the binary condition (1 or 0) at the ***Q*** and ***Q'*** outputs.

Mode of operation	INPUTS					OUTPUTS	
	Asynchronous		Synchronous				
	PS	*CLR*	*CLK*	*J*	*K*	*Q*	*Q'*
Asynchronous set	0	1	X	X	X		
Asynchronous reset	1	0	X	X	X		
Prohibited	0	0	X	X	X	X	X
Hold	1	1	⎍	0	0	X	X
Reset	1	1	⎍	0	1		
Set	1	1	⎍	1	0		
Toggle	1	1	⎍	1	1	X	X

Notes:

- 1 = ON = Hi
- 0 = OFF = Lo
- X = irrelevant or don't care
- ⎍ = either high-low or low-high transition of clock pulse

Demo and Signoff: _____

Questions

1. What are the inputs to an RS flip-flop?

2. What are the input states for *SET* mode on a RS flip-flop?

   S = _____

   R = _____

3. What controls the operation of the gated RS flip-flop?

4. What are the input states for *Asynchronous* RESET on a D flip-flop?

   PS = _____

   CLR = _____

   D = _____

   CLK = _____

5. What are the input states for *Synchronous* SET mode on a JK flip-flop?

   K = _____

   J = _____

   PS = _____

   CLR = _____

   CLK = _____

6. What is the difference between *SYNCHRONOUS* and *ASYNCHRONOUS* mode?

7. What is the purpose of the *CLK* line on a JK and D flip-flop?

8. Depending on the type of flip-flop, triggering can be either on the positive or negative edge of the CLOCK pulse.

   a. True
   b. False