# CSEE223

**Name: _____**

## Flip-Flops Quiz 2

**Date: _____**

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# Multiple Choices:

1. Which circuit is generated from D flip-flop due to addition of an inverter by causing reduction in the number of inputs?
a) Gated JK-latch
b) Gated SR-latch
c) Gated T-latch
d) Gated D-latch

2. The characteristic of J-K flip-flop is similar to _____
a) S-R flip-flop
b) D flip-flop
c) T flip-flop
d) Gated T flip-flop

3. A J-K flip-flop can be obtained from the clocked S-R flip-flop by augmenting _____
a) Two AND gates
b) Two NAND gates
c) Two NOT gates
d) Two OR gates.

4. How is a J-K flip-flop made to toggle?
a) J = 0, K = 0
b) J = 1, K = 0
c) J = 0, K = 1
d) J = 1, K = 1

5. In J-K flip-flop, “no change” condition appears when _____
a) J = 1, K = 1

b) J = 1, K = 0
c) J = 0, K = 1
d) J = 0, K = 0

6. A J-K flip-flop with J = 1 and K = 1 has a 20 kHz clock input. The Q output is _____
a) Constantly LOW
b) Constantly HIGH
c) A 20 kHz square wave
d) A 10 kHz square wave

7. On a J-K flip-flop, when is the flip-flop in a hold condition?
a) J = 0, K = 0
b) J = 1, K = 0
c) J = 0, K = 1
d) J = 1, K = 1

8. How many flip-flops are in the 7475 IC?
a) 2
b) 1
c) 4
d) 8

9. In D flip-flop, D stands for _____
a) Distant
b) Data
c) Desired
d) Delay

10. The D flip-flop has _____ input.
a) 1
b) 2
c) 3

d) 4

11. The D flip-flop has _____ output/outputs.
a) 2
b) 3
c) 4
d) 1

12. A D flip-flop can be constructed from an _____ flip-flop.
a) S-R
b) J-K
c) T
d) S-K

13. In D flip-flop, if clock input is LOW, the D input _____
a) Has no effect
b) Goes high
c) Goes low
d) Has effect

14. In D flip-flop, if clock input is HIGH & D=1, then output is _____
a) 0
b) 1
c) Forbidden
d) Toggle

15. Which statement describes the BEST operation of a negative-edge-triggered D flip-flop?
a) The logic level at the D input is transferred to Q on NGT of CLK
b) The Q output is ALWAYS identical to the CLK input if the D input is HIGH
c) The Q output is ALWAYS identical to the D input when CLK = PGT
d) The Q output is ALWAYS identical to the D input

16. Which of the following is correct for a gated D flip-flop?
a) The output toggles if one of the inputs is held HIGH
b) Only one of the inputs can be HIGH at a time
c) The output complement follows the input when enabled
d) Q output follows the input D when the enable is HIGH

17. With regard to a D latch _____
a) The Q output follows the D input when EN is LOW
b) The Q output is opposite the D input when EN is LOW
c) The Q output follows the D input when EN is HIGH
d) The Q output is HIGH regardless of EN's input state

18. Which of the following is correct for a D latch?
a) The output toggles if one of the inputs is held HIGH
b) Q output follows the input D when the enable is HIGH
c) Only one of the inputs can be HIGH at a time
d) The output complement follows the input when enabled

19. Which of the following describes the operation of a positive edge-triggered D flip-flop?
a) If both inputs are HIGH, the output will toggle
b) The output will follow the input on the leading edge of the clock
c) When both inputs are LOW, an invalid state exists
d) The input is toggled into the flip-flop on the leading edge of the clock and is passed to the output on the trailing edge of the clock

20. What does the half circle on the clock input of a J-K flip-flop mean?
a) Level enabled
b) Positive edge triggered
c) negative edge triggered
d) Level triggered

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21. A J-K flip-flop with J = 1 and K = 1 has a 20 kHz clock input. The Q output is _____
a) Constantly LOW
b) Constantly HIGH
c) A 20 kHz square wave
d) A 10 kHz square wave

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22. On a positive edge-triggered S-R flip-flop, the outputs reflect the input condition when ___
a) The clock pulse is LOW
b) The clock pulse is HIGH
c) The clock pulse transitions from LOW to HIGH
d) The clock pulse transitions from HIGH to LOW

23. The asynchronous input can be used to set the flip-flop to the _____
a) 1 state
b) 0 state
c) either 1 or 0 state
d) forbidden State

24. Input clock of RS flip-flop is given to _____
a) Input
b) Pulser
c) Output
d) Master slave flip-flop

25. D flip-flop is a circuit having _____
a) 2 NAND gates
b) 3 NAND gates
c) 4 NAND gates
d) 5 NAND gates

26. Master slave flip flop is also referred to as?
a) Level triggered flip flop

b) Pulse triggered flip flop
c) Edge triggered flip flop
d) Edge-Level triggered flip flop

27. In a positive edge triggered JK flip flop, a low J and low K produces?
a) High state
b) Low state
c) Toggle state
d) No Change State

28. If one wants to design a binary counter, the preferred type of flip-flop is _____
a) D type
b) S-R type
c) Latch
d) J-K type

29. S-R type flip-flop can be converted into D type flip-flop if S is connected to R through ____
a) OR Gate
b) AND Gate
c) Inverter
d) Full Adder

30. Which of the following is the Universal Flip-flop?
a) S-R flip-flop
b) J-K flip-flop
c) Master slave flip-flop
d) D Flip-flop

31. How many types of triggering takes place in a flip flops?
a) 3
b) 2
c) 4

d) 5

32. Flip-flops are _____
a) Stable devices
b) Astable devices
c) Bistable devices
d) Monostable devices

33. The term synchronous means _____
a) The output changes state only when any of the input is triggered
b) The output changes state only when the clock input is triggered
c) The output changes state only when the input is reversed
d) The output changes state only when the input follows it

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34. The S-R, J-K and D inputs are called _____
a) Asynchronous inputs
b) Synchronous inputs
c) Bidirectional inputs
d) Unidirectional inputs

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**35) In delay flip-flop, _____ after the propagation delay.**

**a.** Input follows input
**b.** Input follows output
**c.** Output follows input
**d.** Output follows output

36. What is a trigger pulse?
a) A pulse that starts a cycle of operation
b) A pulse that reverses the cycle of operation
c) A pulse that prevents a cycle of operation

d) A pulse that enhances a cycle of operation

37. The circuits of NOR based S-R latch classified as asynchronous sequential circuits, why?
a) Because of inverted outputs
b) Because of triggering functionality
c) Because of cross-coupled connection
d) Because of inverted outputs & triggering functionality

38. The difference between a flip-flop & latch is _____
a) Both are same
b) Flip-flop consist of an extra output
c) Latches has one input but flip-flop has two
d) Latch has two inputs but flip-flop has one

39. How many types of flip-flops are?
a) 2
b) 3
c) 4
d) 5

40. On a positive edge-triggered S-R flip-flop, the outputs reflect the input condition when _____
a) The clock pulse is LOW
b) The clock pulse is HIGH
c) The clock pulse transitions from LOW to HIGH
d) The clock pulse transitions from HIGH to LOW