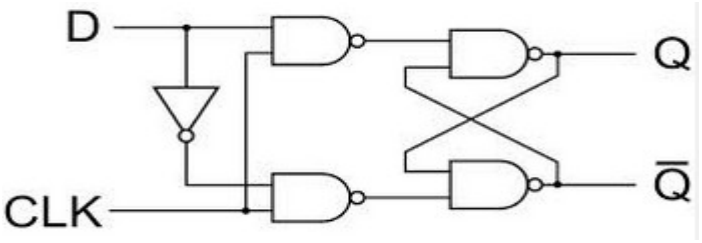
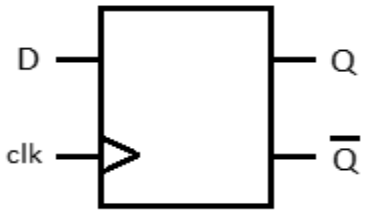
D Flip-Flop

The D flip-flop shown is a modification of the clocked SR flip-flop. By simply inverting the input S to a NAND gate input so always S&R are opposite to each other, so we overcome the problem that S&R be high (1,1) or low (0,0).The D input goes directly into the S input and the complement of the D input goes to the R input.

The D input is sampled during the occurrence of a clock pulse. If it is 1, the flip-flop is switched to the set state (unless it was already set). If it is 0, the flip-flop switches to the clear state.

It's a 1-bit memory device, Capture and store on bit (1,0), D stands for data. By the truth table of D flip flop, we can observe that Q always depends on D. Hence, for every negative trigger pulse, the logic at input D is shifted to Output Q



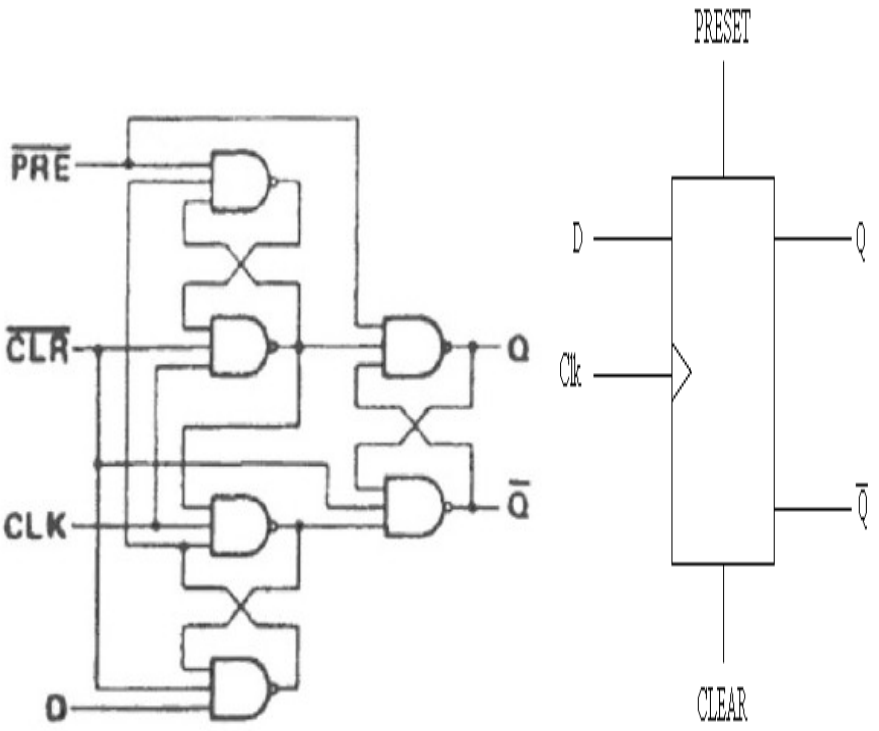


clk	D	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	Q	$\overline{Q}$
1	0	0	1
1	1	1	0

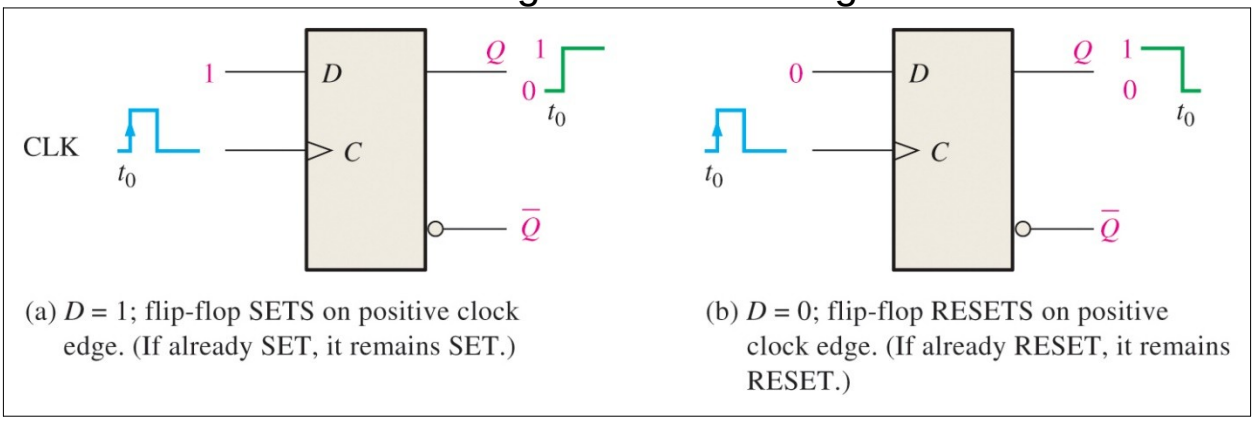
When D input is HIGH and the EN is HIGH the latch will SET (1)

D Input is LOW and the EN is HIGH the latch will RESET (0)

D Flip-Flop with Preset and Clear



The data bit at the D-input is transferred to the component output on the edge of the clock signal



(a) $D = 1$; flip-flop SETS on positive clock edge. (If already SET, it remains SET.)

(b) $D = 0$; flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)

Once triggered, the output (Q) equals the last value at the D input until a new value is triggered in.

Mode of Operation	Inputs				Outputs	
	PS	CLR	CLK	D	Q	Q′
Asynchronous set	0	1	X	X	1	0
Asynchronous reset	1	0	X	X	0	1
Prohibited	1	1	X	X	1	1
Set	1	1	^	1	1	0
Reset	1	1	^	0	0	1

X = irrelevant
^ = L-to-H transition of the clock pulse

Flip-flop Asynchronous Inputs

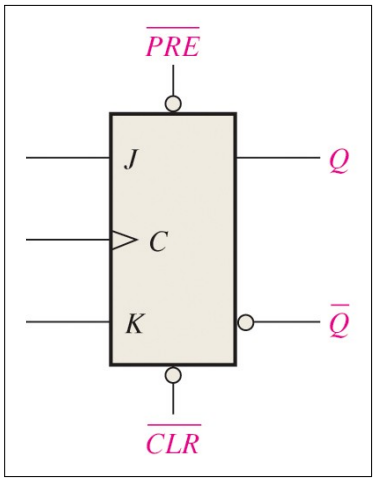
Synchronous (clocked) inputs are transferred on the triggering edge of the clock.

Synchronous inputs mean data of the inputs are transferred to the o/p **only** on the triggering edge of the clock pulse.

Most flip-flops have other inputs that are **asynchronous**, meaning they operate independently of the clock.

Asynchronous inputs mean that inputs affect the state of the flip flop independent of the clock and normally called **preset (PRE**) and **clear (CLR)** and usually active low.

There are 4 flip flops used in 7475 IC and those are D flip-flops



Asynchronous flip-flop inputs are normally labeled preset (*PRE*) and clear (*CLR*). These inputs are usually active LOW
A J-K flip flop with active LOW preset and CLR is shown.
Note that the asynchronous inputs always override
the synchronous inputs

Flip-flops

Flip flops are bistable devices. The o/p changes state only at a specified point A flip-flop differs from a latch in the manner it changes states.

A flip-flop is a **clocked device**, in which only the **clock edge** determines when a new bit is entered.

There are 4 types of flip-flops , S-R,J-K,D and T. D flip flop is an advanced version of S-R flip-flop,while T flip- flop is an advanced version of J-K flip flop.

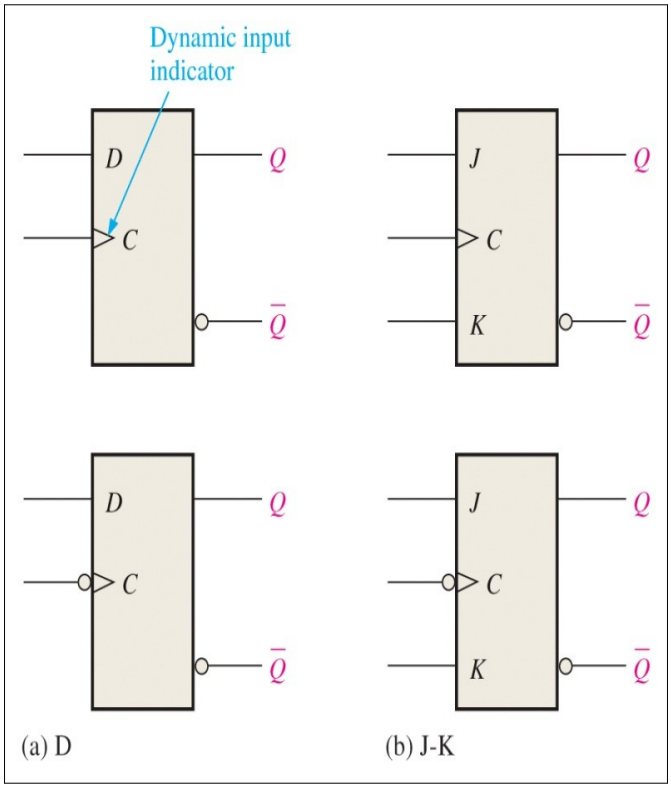
The flip flop is sensitive only to the positive or negative edge of the clock pulse. So, the flip-flop toggles whenever the clock is falling/rising at edge. This triggering of flip-flop during the transition state, is known as Edge-triggered flip-flop. Thus, the output curve has a time period twice that of the clock.

Frequency is inversely related to time period and hence frequency gets halved

The active edge can be positive or negative

The output from an edge-triggered flip-flop changes on the positive-going or negative-going edge of its clock signal.

A bubble on the clock input indicates that it is a negative edge triggered flip-flop.

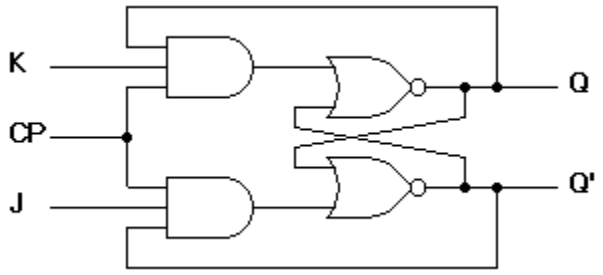


JK Flip-Flop

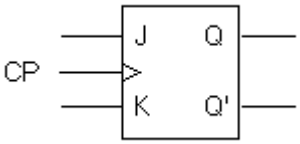
A JK flip-flop is a refinement of the SR flip-flop in that the indeterminate state of the SR type is defined in the JK type. Inputs J and K behave like inputs S and R to set and clear the flip-flop (note that in a JK flip-flop, the letter J is for set and the letter K is for clear). Whenlogic 1 inputs are applied to both J and K simultaneously, the flipflopswitches to its complement state, i.e.., if Q=1, it switches to Q=0 and vice versa.

A clocked JK flip-flop is shown in Figure 6. Output Q is ANDed with K and CP inputs so that the flip-flop is cleared during a clock pulse only if Q was previously 1. Similarly, output Q' is ANDed with J and CP inputs so that the flip-flop is set with a clock pulse only if Q' was previously 1.

Note that because of the feedback connection in the JK flip-flop, a CP signal which remains a 1 (while J=K=1) after the outputs have been complemented once will cause repeated and continuous transitions of the outputs. To avoid this, the clock pulses must have a time duration less than the propagation delay through the flip-flop. The restriction on the pulse width can be eliminated with a master-slave or edge-triggered construction. The same reasoning also applies to the T flip-flop presented next.



(a) Logic diagram

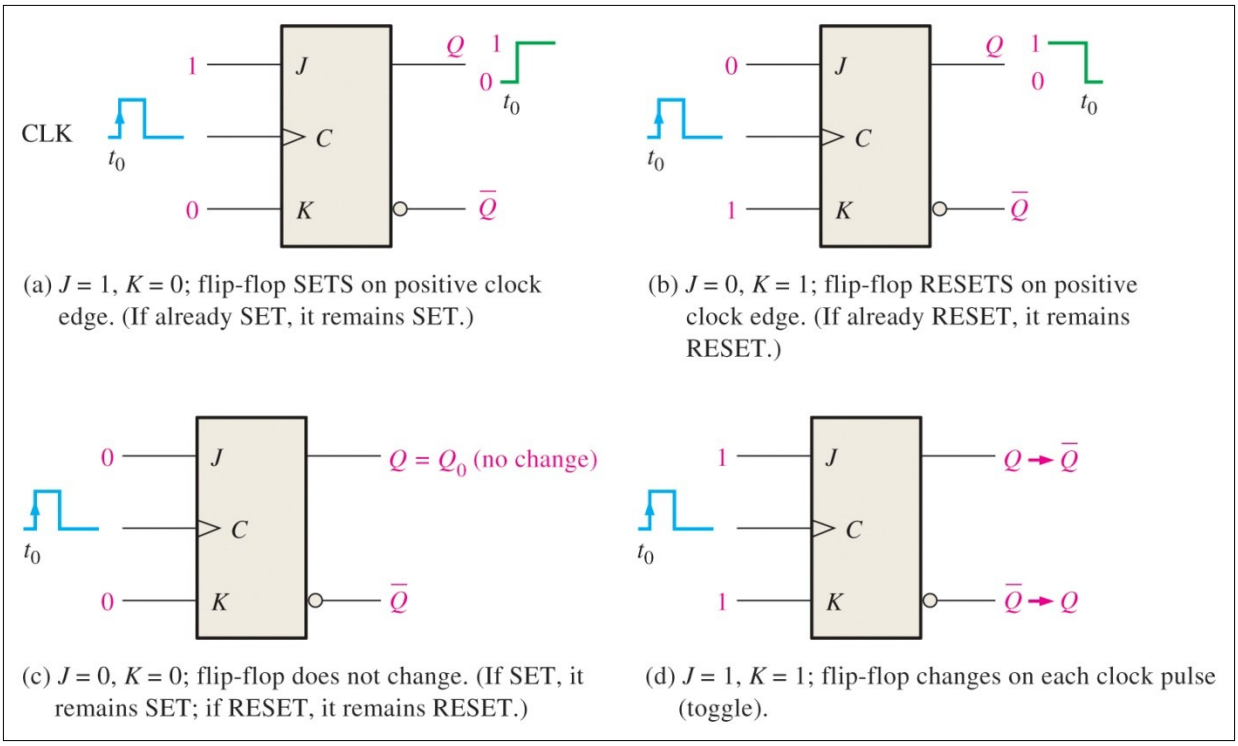


(b) Graphical symbol

There are lots of flip-flops can be prepared by using J-K flip flop .So , the name is a universal flip-flop . Also, the JK flip-flop resolves the forbidden state.

There are three types of triggering in a flip-flop, level triggering, edge triggering and pulse triggering.

The values at the J and K inputs to a J-K flip-flop determine its output state. The results of the four possible combinations of J and K are shown.



CLK	J	K	Q	Q’
↑	0	0	hold	
↑	0	1	0	1
↑	1	0	1	0
↑	1	1	toggle	

Toggle means changes states of the triggering edge of the clock.

Triggering of Flip-flops

The state of a flip-flop is changed by a momentary change in the input signal. This change is called a trigger and the transition it causes is said to trigger the flip-flop. The basic circuits of Figure 2 and Figure 3 (In the previous Handouts) require an input trigger defined by a change in signal level. The Flip flop cannot change state except on the triggering edge of the clock pulse .

The operation for the a negative edge triggered are the same as the positive edge except that the falling edge of the clock pulse.

This level must be returned to its initial level before a second trigger is applied. Clocked flip-flops are triggered by pulses.

The feedback path between the combinational circuit and memory elements in Figure 1 can produce instability if the outputs of the memory elements (flip-flops) are changing while the outputs of the combinational circuit that go to the flip-flop inputs are being sampled by the clock pulse.

A way to solve the feedback timing problem is to make the flip-flop sensitive to the pulse transition rather than the pulse duration.

The clock pulse goes through two signal transitions: from 0 to 1 and the return from 1 to 0. As shown in Figure 8 the positive transition is defined as the positive edge and the negative transition as the negative edge.

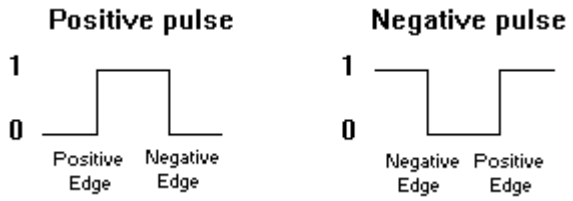
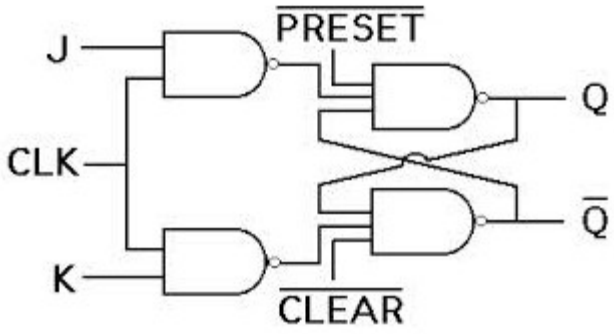


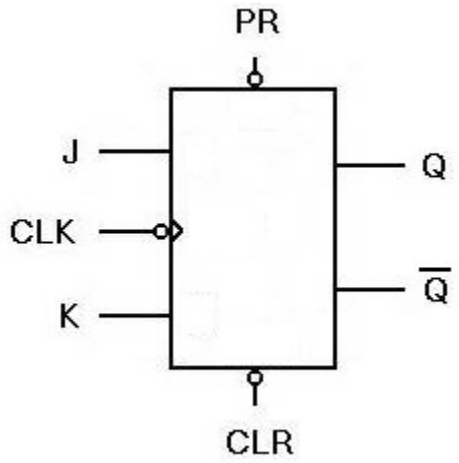
Figure 8. Definition of clock pulse transition

Edge triggered device will follow the input condition when there is a transition. It is said to be positive edge triggered when transition occurs from LOW to HIGH. While it is said to be negative edge triggered when a transition occurs from HIGH to LOW

The clocked flip-flops already introduced are triggered during the positive edge of the pulse, and the state transition starts as soon as the pulse reaches the logic-1 level. If the other inputs change while the clock is still 1, a new output state may occur. If the flip-flop is made to respond to the positive (or negative) edge transition only, instead of the entire pulse duration, then the multiple-transition problem can be eliminated.

J-K Flip-Flop with Preset and Clear





Mode of Operation	Inputs					Outputs	
	PS	Clr	Clk	J	K	Q	Q′
Asynchronous set	0	1	x	x	x	1	0
Asynchronous reset	1	0	x	x	x	0	1
Prohibited	0	0	x	x	x	1	1
Hold	1	1	^	0	0	no change	
Reset	1	1	^	0	1	0	1
Set	1	1	^	1	0	1	0
Toggle	1	1	^	1	1	opposite	

x = Irrelevant
^ = H-to-L transition of clock pulse

Master-Slave Flip-Flop

A master-slave flip-flop is constructed from two separate flip-flops. One circuit serves as a master and the other as a slave. The logic diagram of an SR flip-flop is shown in Figure 9. The master flip-flop is enabled on the positive edge of the **clock pulse CP** and the slave flip-flop is disabled by the inverter. The information at the external R and S inputs

is transmitted to the master flip-flop. When the pulse returns to 0, the master flip-flop is disabled, and the slave flip-flop is enabled. The slave flip-flop then goes to the same state as the master flip-flop.

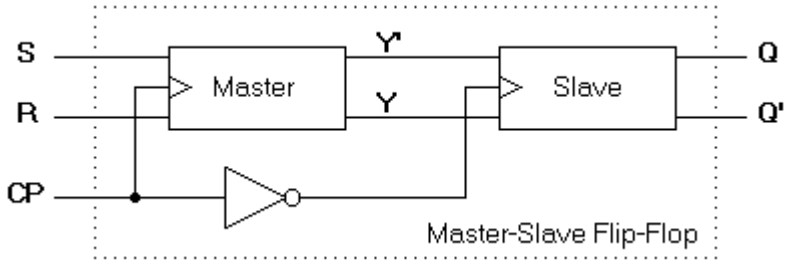


Figure 9. Logic diagram of a master-slave flip-flop

The timing relationship is shown in Figure 10 and is assumed that the flip-flop is in the clear state prior to the occurrence of the clock pulse. The output state of the master-slave flip-flop occurs on the negative transition of the clock pulse. Some master-slave flip-flops change output state on the positive transition of the clock pulse by having an additional inverter between the CP terminal and the input of the master.

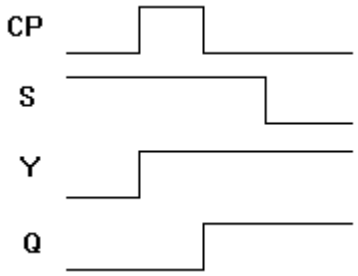


Figure 10. Timing relationship in a master slave flip-flop

The term pulse triggered means the data is entered on the rising edge of the clock pulse, but the output does not reflect the change until the falling edge of the clock pulse.

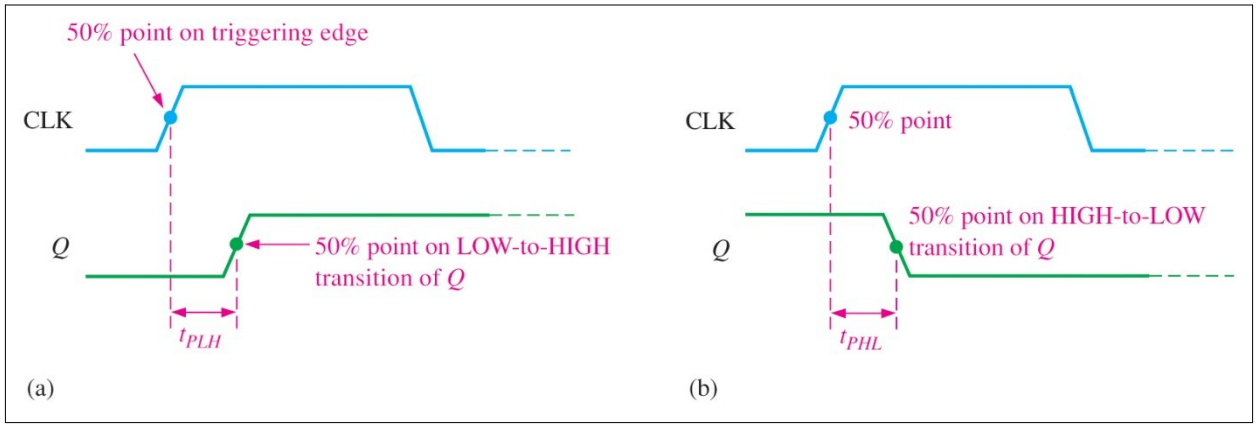
If one wants to design a binary counter, the preferred type of flip-flop is J-K type because it has capability to recover from

toggle condition. SR flip-flop is not suitable as it produces the "Invalid State

Flip-Flop Propagation Delay

Propagation delay time is specified for the rising and falling outputs. It is measured between the 50% level of the clock to the 50% level of the output transition

Propagation delay (t_{PLH}) (Propagation time low to high) is measured as shown in (a).
Propagation delay (t_{PHL})(Propagation time high to low) is measured as shown in (b)



Multivibrator

A **multivibrator** is an electronic circuit used to implement a variety of simple two-state devices such as relaxation oscillators, timers and flip-flops.

- **ASTABLE MULTIVIBRATOR** - In simple words, it produces square waves. As it has no stable state, it keeps oscillating between two values which produce a square wave

- **MONOSTABLE MULTIVIBRATOR** - Mono means one so this type of multivibrator produces an output that has only one state. If you give external trigger then the circuit will change the state temporarily and after some time output will return back to the original state.
- **BISTABLE MULTIVIBRATORS** - BI means two so this will produce output that has two stable states. So if you give external trigger the output will change the state permanently. Let's say it is now 5 volts. Now it will remain in that state. To change the state of output again we have to again give an external trigger. Then it will change state from 5v to let's say -5 volts. Thus it has two stable states 5 and -5.