



## LP3990 150-mA Linear Voltage Regulator for Digital Applications

### 1 Features

- 1% Voltage Accuracy at Room Temperature
- Stable with Ceramic Capacitor
- Logic Controlled Enable
- No Noise Bypass Capacitor Required
- Thermal-Overload and Short-Circuit Protection
- Input Voltage Range, 2 V to 6 V
- Output Voltage Range, 0.8 V to 3.3 V
- Output Current, 150 mA
- Output Stable - Capacitors, 1  $\mu$ F
- Virtually Zero  $I_Q$  (Disabled), < 10 nA
- Very Low  $I_Q$  (Enabled), 43  $\mu$ A
- Low Output Noise, 150  $\mu$ V<sub>RMS</sub>
- PSRR, 55 dB at 1 kHz
- Fast Start-Up, 105  $\mu$ s

### 2 Applications

- Cellular Handsets
- Hand-Held Information Appliances

### 3 Description

The LP3990 regulator is designed to meet the requirements of portable, battery-powered systems providing an accurate output voltage, low-noise, and low-quiescent current. The LP3990 will provide a 0.8-V output from the low input voltage of 2 V at up to a 150-mA load current. When switched into shutdown mode via a logic signal at the enable pin (EN), the power consumption is reduced to virtually zero.

The LP3990 is designed to be stable with space-saving ceramic capacitors with values as low as 1  $\mu$ F.

Performance is specified for a  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  junction temperature range.

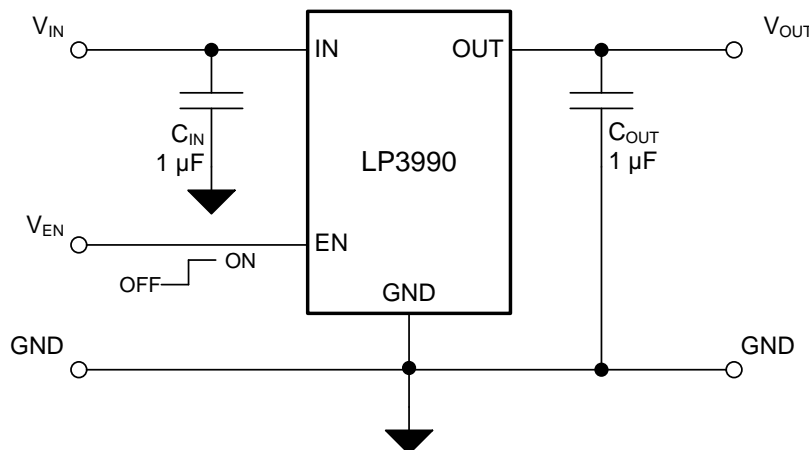
For output voltages other than 0.8 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V, 2.5 V, 2.8 V, or 3.3 V, please contact the Texas Instruments sales office.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP3990	DSBGA (4)	1.324 mm x 1.045 mm (MAX)
	WSON (6)	2.90 mm x 1.60 mm
	SOT-23 (5)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

#### Simplified Schematic



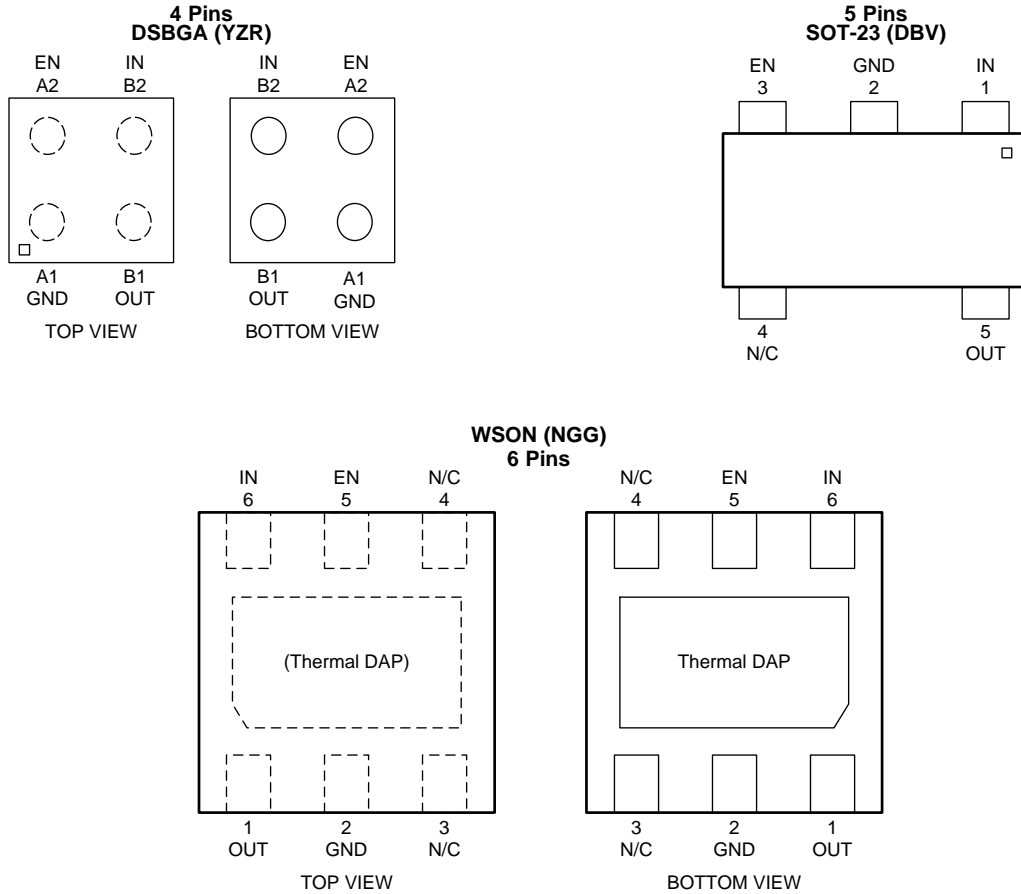
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## 4 Revision History

Changes from Revision I (May 2013) to Revision J	Page
<ul style="list-style-type: none"> <li>Added <i>Device Information</i> and <i>Handling Rating</i> tables, <i>Feature Description</i>, <i>Device Functional Modes</i>, <i>Application and Implementation</i>, <i>Power Supply Recommendations</i>, <i>Layout</i>, <i>Device and Documentation Support</i>, and <i>Mechanical, Packaging, and Orderable Information</i> sections; moved some curves to <i>Application Curves</i> section .....</li> </ul>	<b>1</b>

## 5 Pin Configuration and Functions



### Pin Functions

NAME	PIN			I/O	DESCRIPTION
	DSBGA YZR	SOT-23 DBV	WSN NGG		
GND	A1	2	2	—	Common Ground.
EN	A2	3	5	I	Enable Input; Enables the Regulator when $\geq 0.95$ V. Disables the Regulator when $\leq 0.4$ V. Enable Input has 1-M $\Omega$ (typical) pull-down resistor to GND.
OUT	B1	5	1	O	Voltage output. A 1- $\mu$ F Low ESR Capacitor should be connected to this Pin. Connect this output to the load circuit.
IN	B2	1	6	I	Voltage supply Input. A 1- $\mu$ F capacitor should be connected at this input.
N/C	N/A	4	3	I	No internal connection.
N/C		N/A	4	I	No internal connection.
N/C			Pad	—	Thermal pad. Connect to Pin 2.

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)(2)(3)</sup>

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Input voltage	–0.3	6.5	V
Output voltage	–0.3	Note <sup>(4)</sup>	
ENABLE input voltage	–0.3	6.5	
Continuous power dissipation internally limited	Note <sup>(5)</sup>		

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
- (3) All voltages are with respect to the potential at the GND pin.
- (4) The lower of  $V_{IN} + 0.3\text{ V}$  or  $6.5\text{ V}$ .
- (5) Internal thermal shutdown circuitry protects the device from permanent damage.

### 6.2 Handling Ratings

			MIN	MAX	UNIT
T <sub>stg</sub>	Storage temperature range		−65	150	°C
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	−2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	250	1500	
		Machine model	−200	200	

- (1) JEDEC document JEP155 states that 2000-V HBM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Input voltage, $V_{IN}$	2		6	V
Enable input voltage, $V_{EN}$	0.0		$V_{IN}$	
Junction temperature, $T_J$ <sup>(1)</sup>	–40		125	°C

- (1)  $T_{J(max)} = (T_{A(max)} + (R_{\theta JA} \times P_{D(max)}))$

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LP3990			UNIT
		YZR (DSBGA)	DBV (SOT-23)	NGG (WSON)	
		4 PINS	5 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	188.9	165.2	53.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.0	69.9	51.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	105.3	27.3	28.2	
$\Psi_{JT}$	Junction-to-top characterization parameter	0.7	1.8	0.6	
$\Psi_{JB}$	Junction-to-board characterization parameter	105.2	26.8	28.3	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	8.1	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics<sup>(1)(2)</sup>

Unless otherwise noted,  $V_{EN} = 950 \text{ mV}$ ,  $V_{IN} = V_{OUT} + 1 \text{ V}$  or  $V_{IN} = 2 \text{ V}$ , whichever is higher.  $C_{IN} = 1 \mu\text{F}$ ,  $I_{OUT} = 1 \text{ mA}$ ,  $C_{OUT} = 0.47 \mu\text{F}$ .

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{IN}$	Input voltage	Note <sup>(3)</sup> , $T_J = 25^\circ\text{C}$		2		6	V
$\Delta V_{OUT}$	Output voltage tolerance	$I_{LOAD} = 1 \text{ mA}$ $T_J = 25^\circ\text{C}$	DSBGA	–1		1%	
			WQFN	–1.5%		1.5%	
			SOT-23	–1.5%		1.5%	
		Over full line and load regulation	DSBGA	–2.5%		2.5%	
			WQFN	–3%		3%	
			SOT-23	–4%		4%	
	Line regulation error	$V_{IN} = (V_{OUT(NOM)} + 1 \text{ V})$ to 6 V		0.1	0.02	0.1	%/V
	Load regulation error	$I_{OUT} = 1 \text{ mA}$ to 150 mA	$V_{OUT} = 0.8 \text{ V to } 1.95 \text{ V}$ DSBGA	–0.005	0.002	0.005	%mA
			$V_{OUT} = 0.8 \text{ V to } 1.95 \text{ V}$ WQFN, SOT-23	–0.008	0.003	0.008	
			$V_{OUT} = 2 \text{ V to } 3.3 \text{ V}$ DSBGA	–0.002	0.0005	0.002	
			$V_{OUT} = 2 \text{ V to } 3.3 \text{ V}$ WQFN, SOT-23	–0.005	0.002	0.005	
$V_{DO}$	Dropout voltage	$I_{OUT} = 150 \text{ mA}$ <sup>(4)</sup> <sup>(5)</sup>			120	200	mV
$I_{LOAD}$	Load current	Note <sup>(5)(6)</sup> , $T_J = 25^\circ\text{C}$		0			$\mu\text{A}$
$I_Q$	Quiescent current	$V_{EN} = 950 \text{ mV}$ , $I_{OUT} = 0 \text{ mA}$			43	80	$\mu\text{A}$
		$V_{EN} = 950 \text{ mV}$ , $I_{OUT} = 150 \text{ mA}$			65	120	
		$V_{EN} = 0.4 \text{ V}$ (output disabled), $T_J = 25^\circ\text{C}$			0.002	0.2	
$I_{SC}$	Short circuit current limit	Note <sup>(7)</sup>			550	1000	mA
$I_{OUT}$	Maximum output current			150			
PSRR	Power Supply Rejection Ratio	$f = 1 \text{ kHz}$ , $I_{OUT} = 1 \text{ mA to } 150 \text{ mA}$			55		dB
		$f = 10 \text{ kHz}$ , $I_{OUT} = 150 \text{ mA}$			35		
$e_n$	Output noise voltage <sup>(5)</sup>	BW = 10 Hz to 100 kHz	$V_{OUT} = 0.8 \text{ V}$		60		$\mu\text{V}_{RMS}$
			$V_{OUT} = 1.5 \text{ V}$		125		
			$V_{OUT} = 3.3 \text{ V}$		180		
$T_{SHUTDOWN}$	Thermal shutdown junction temperature	Junction temperature ( $T_J$ ) rising until the output is disabled			155		$^\circ\text{C}$
		Hysteresis			15		

- (1) All voltages are with respect to the device GND terminal, unless otherwise stated.
- (2) Minimum and Maximum limits are ensured through test, design, or statistical correlation over the operating junction temperature range ( $T_J$ ) of  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ , unless otherwise stated. Typical values represent the most likely parametric norm at  $T_J = 25^\circ\text{C}$ , and are provided for reference purposes only.
- (3)  $V_{IN(MIN)} = V_{OUT(NOM)} + 0.5 \text{ V}$ , or  $2 \text{ V}$ , whichever is higher.
- (4) Dropout voltage is voltage difference between input and output at which the output voltage drops to 100 mV below its nominal value. This parameter applies only for output voltages above 2 V.
- (5) This electrical specification is verified by design.
- (6) The device maintains the regulated output voltage without the load.
- (7) Short-circuit current is measured with  $V_{OUT}$  pulled to 0 V and  $V_{IN}$  worst case = 6 V.

## Electrical Characteristics<sup>(1)(2)</sup> (continued)

Unless otherwise noted,  $V_{EN} = 950 \text{ mV}$ ,  $V_{IN} = V_{OUT} + 1 \text{ V}$  or  $V_{IN} = 2 \text{ V}$ , whichever is higher.  $C_{IN} = 1 \text{ }\mu\text{F}$ ,  $I_{OUT} = 1 \text{ mA}$ ,  $C_{OUT} = 0.47 \text{ }\mu\text{F}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ENABLE CONTROL CHARACTERISTICS</b>						
$I_{EN}^{(8)}$	Maximum input current at EN pin	$V_{EN} = 0 \text{ V}$ (Output is disabled) $T_J = 25^\circ\text{C}$		0.001	0.1	$\mu\text{A}$
		$V_{EN} = 6 \text{ V}$	2.5	6	10	
$V_{IL}$	Low input threshold	$V_{IN} = 2 \text{ V}$ to $6 \text{ V}$ $V_{EN}$ falling from $\geq V_{IH}$ until the output is disabled			0.4	V
$V_{IH}$	High input threshold	$V_{IN} = 2 \text{ V}$ to $6 \text{ V}$ $V_{EN}$ rising from $\leq V_{IL}$ until the output is enabled	0.95			

(8) ENABLE Pin has 1-M $\Omega$  (typical) resistor connected to GND.

## 6.6 Output Capacitor, Recommended Specifications<sup>(1)</sup>

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{OUT}$	Output capacitance	Capacitance <sup>(2)</sup>	0.7 <sup>(3)</sup>	1	500	$\mu\text{F}$
		ESR	5			m $\Omega$

(1) Unless otherwise specified, values and limits apply for  $T_J = 25^\circ\text{C}$ .

(2) The full operating conditions for the application should be considered when selecting a suitable capacitor to ensure that the minimum value of capacitance is always met. Recommended capacitor type is X7R. However, dependent on application, X5R, Y5V, and Z5U can also be used. (See [Detailed Design Procedure](#).)

(3) Limit applies over the full operating junction temperature range ( $T_J$ ) of  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ .

## 6.7 Timing Requirements

				MIN	NOM <sup>(1)</sup>	MAX <sup>(2)</sup>	UNIT
$T_{ON}$	Turnon time <sup>(3)</sup>	From $V_{EN} \uparrow V_{IH}$ to $V_{OUT}$ 95% level ( $V_{IN(MIN)}$ to $6 \text{ V}$ )	$V_{OUT} = 0.8 \text{ V}$		80	150	$\mu\text{s}$
			$V_{OUT} = 1.5 \text{ V}$		105	200	
			$V_{OUT} = 3.3 \text{ V}$		175	250	
Transient response	Line transient response ( $\Delta V_{OUT}$ )	$T_{rise} = T_{fall} = 30 \text{ }\mu\text{s}^{(3)}$ , $\Delta V_{IN} = 600 \text{ mV}$			8	16	mV (pk-pk)
	Load transient response ( $\Delta V_{OUT}$ )	$T_{rise} = T_{fall} = 1 \text{ }\mu\text{s}^{(3)}$ , $I_{OUT} = 1 \text{ mA}$ to $150 \text{ mA}$ $C_{OUT} = 1 \text{ }\mu\text{F}$			55	100	mV

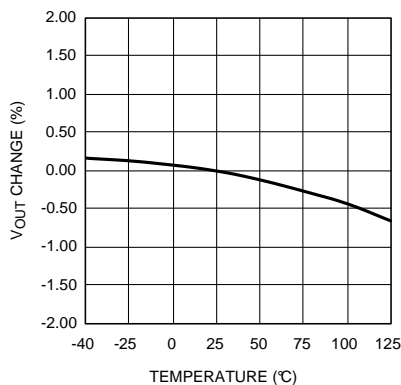
(1) Nom values apply for  $T_J = 25^\circ\text{C}$ .

(2) Maximum limits apply over the full operating junction temperature ( $T_J$ ) range of  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ .

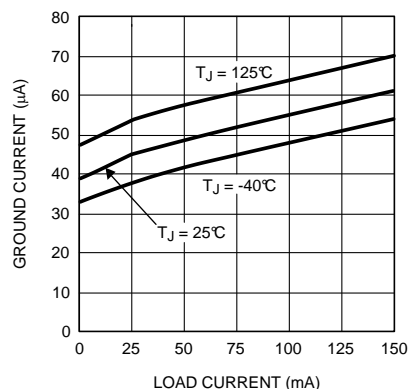
(3) This electrical specification is verified by design.

## 6.8 Typical Performance Characteristics

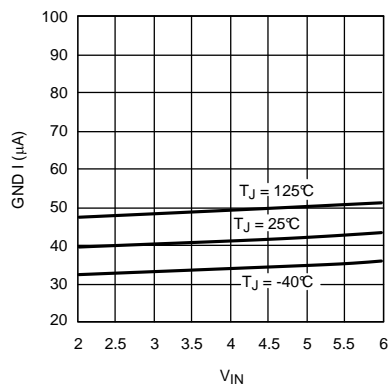
Unless otherwise specified,  $C_{IN} = 1\ \mu\text{F}$  ceramic,  $C_{OUT} = 0.47\ \mu\text{F}$  ceramic,  $V_{IN} = V_{OUT(NOM)} + 1\ \text{V}$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{OUT(NOM)} = 1.5\ \text{V}$ ;  $V_{EN} = V_{IN}$ .



**Figure 1. Output Voltage Change vs Temperature**

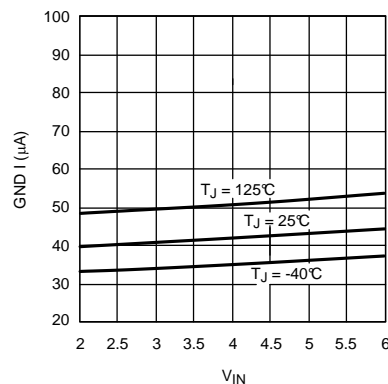


**Figure 2. Ground Current vs Load Current**



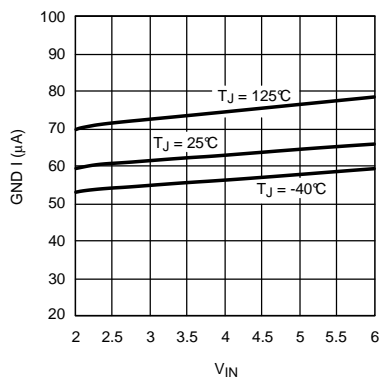
$I_{LOAD} = 0\ \text{mA}$

**Figure 3. Ground Current vs  $V_{IN}$**



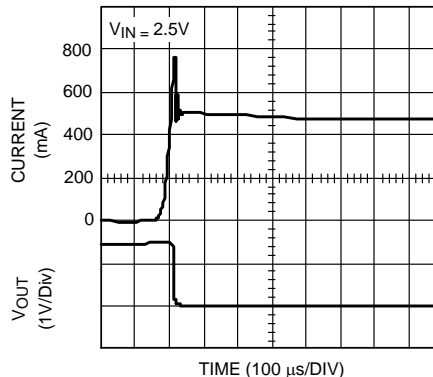
$I_{LOAD} = 1\ \text{mA}$

**Figure 4. Ground Current vs  $V_{IN}$**



$I_{LOAD} = 150\ \text{mA}$

**Figure 5. Ground Current vs  $V_{IN}$**



**Figure 6. Short Circuit Current**

## Typical Performance Characteristics (continued)

Unless otherwise specified,  $C_{IN} = 1 \mu\text{F}$  ceramic,  $C_{OUT} = 0.47 \mu\text{F}$  ceramic,  $V_{IN} = V_{OUT(NOM)} + 1 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{OUT(NOM)} = 1.5 \text{ V}$ ;  $V_{EN} = V_{IN}$ .

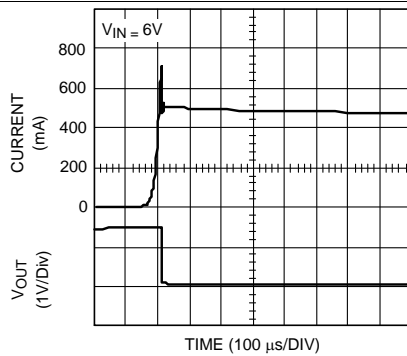


Figure 7. Short Circuit Current

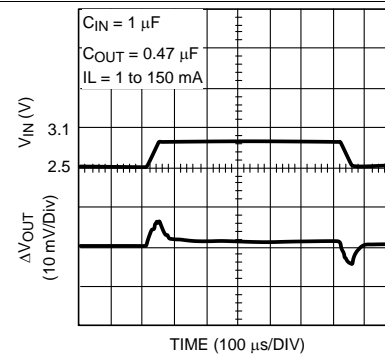


Figure 8. Line Transient

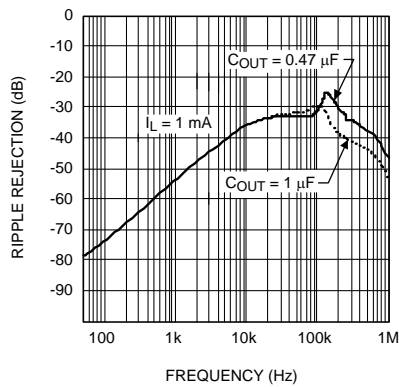


Figure 9. Power Supply Rejection Ratio

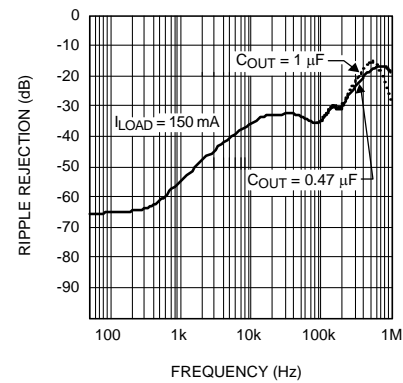


Figure 10. Power Supply Rejection Ratio

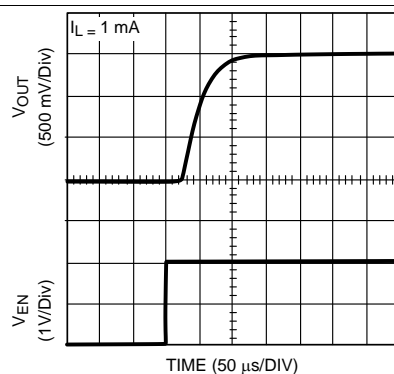


Figure 11. Enable Start-Up Time

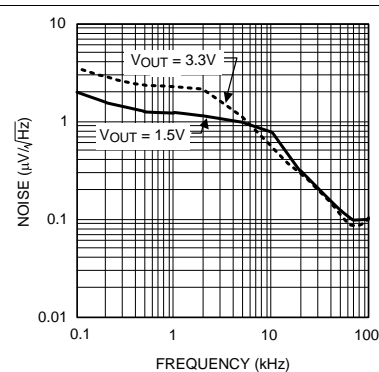


Figure 12. Noise Density



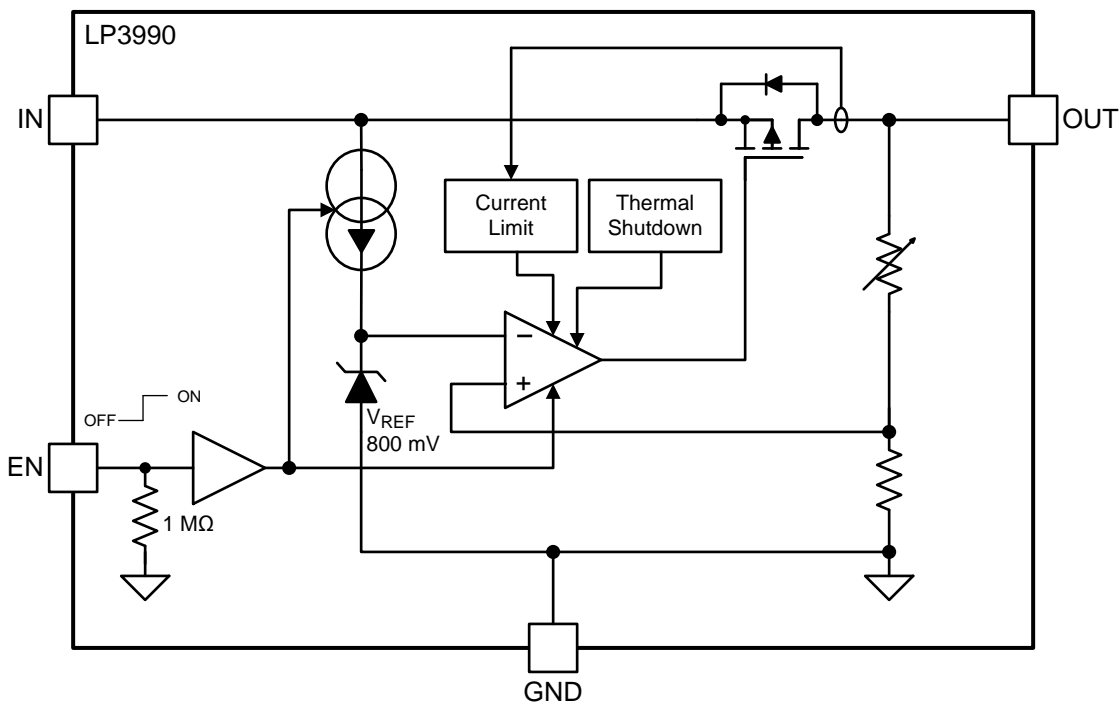
## 7 Detailed Description

### 7.1 Overview

Designed meet the requirements of portable, battery-powered digital systems providing an accurate output voltage with fast start-up. When disabled via a low logic signal at the enable pin (EN), the power consumption is reduced to virtually zero

The LP3990 is designed to perform with a single 1- $\mu$ F input capacitor and a single 1- $\mu$ F ceramic output capacitor.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Enable (EN)

The LP3990 Enable (EN) pin is internally held low by a 1-M $\Omega$  resistor to GND. The EN pin voltage must be higher than the  $V_{IH}$  threshold to ensure that the device is fully enabled under all operating conditions. The EN pin voltage must be lower than the  $V_{IL}$  threshold to ensure that the device is fully disabled. If the EN pin is left open the LP3990 output will be disabled.

#### 7.3.2 Thermal Overload Protection ( $T_{SD}$ )

Thermal Shutdown disables the output when the junction temperature rises to approximately 155°C which allows the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

The Thermal Shutdown circuitry of the LP3990 has been designed to protect against temporary thermal overload conditions. The Thermal Shutdown circuitry was not intended to replace proper heat-sinking. Continuously running the LP3990 device into thermal shutdown may degrade device reliability.

## 7.4 Device Functional Modes

### 7.4.1 Enable (EN)

The LP3990 EN pin is internally held low by a 1-M $\Omega$  resistor to GND. The EN pin voltage must be higher than the  $V_{IH}$  threshold to ensure that the device is fully enabled under all operating conditions.

### 7.4.2 Minimum Operating Input Voltage ( $V_{IN}$ )

The LP3990 does not include any dedicated UVLO circuitry. The LP3990 internal circuitry is not fully functional until  $V_{IN}$  is at least 2 V. The output voltage is not regulated until  $V_{IN} \geq (V_{OUT} + V_{DO})$ , or 2 V, whichever is higher.

## 8 Application and Implementation

### NOTE

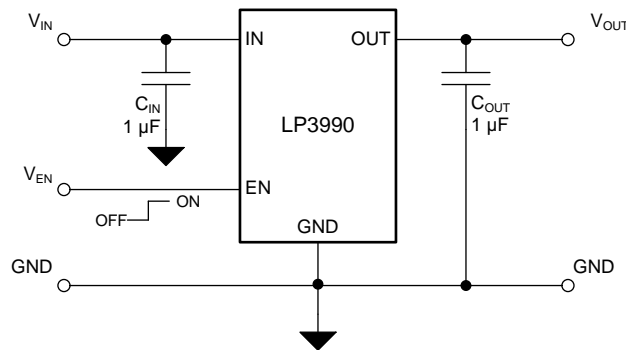
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The LP3990 is a linear voltage regulator for digital applications designed to be stable with space-saving ceramic capacitors as small as 1  $\mu$ F.

### 8.2 Typical Application

Figure 13 shows the typical application circuit for the LP3990. The input and output capacitances may need to be increased above the 1  $\mu$ F shown for some applications.



**Figure 13. LP3990 Typical Application**

#### 8.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2 V to 6 V
Output voltage	1.8 V
Output current	100 mA
Output capacitor range	1 $\mu$ F
Input/output capacitor ESR range	5 m $\Omega$ to 500 m $\Omega$

#### 8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Available input voltage range
- Output voltage needed
- Output current needed
- Input and output capacitors

##### 8.2.2.1 Power Dissipation and Device Operation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus, the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The maximum allowable power dissipation for the device in a given package can be calculated using [Equation 1](#):

$$P_{D-MAX} = ((T_{J-MAX} - T_A) / R_{\theta JA}) \quad (1)$$

The actual power being dissipated in the device can be represented by [Equation 2](#):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

These two equations establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application.

In applications where lower power dissipation ( $P_D$ ) and/or excellent package thermal resistance ( $R_{\theta JA}$ ) is present, the maximum ambient temperature ( $T_{A-MAX}$ ) may be increased.

In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature ( $T_{A-MAX}$ ) may have to be derated.  $T_{A-MAX}$  is dependent on the maximum operating junction temperature ( $T_{J-MAX-OP} = 125^\circ\text{C}$ ), the maximum allowable power dissipation in the device package in the application ( $P_{D-MAX}$ ), and the junction-to ambient thermal resistance of the part/package in the application ( $R_{\theta JA}$ ), as given by [Equation 3](#):

$$T_{A-MAX} = (T_{J-MAX-OP} - (R_{\theta JA} \times P_{D-MAX})) \quad (3)$$

Alternately, if  $T_{A-MAX}$  can not be derated, the  $P_D$  value must be reduced. This can be accomplished by reducing  $V_{IN}$  in the ' $V_{IN}-V_{OUT}$ ' term as long as the minimum  $V_{IN}$  is met, or by reducing the  $I_{OUT}$  term, or by some combination of the two.

### 8.2.2.2 External Capacitors

In common with most regulators, the LP3990 requires external capacitors for regulator stability. The LP3990 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

### 8.2.2.3 Input Capacitor

An input capacitor is required for stability. It is recommended that a 1- $\mu\text{F}$  capacitor be connected between the LP3990 IN pin and GND pin (this capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1 cm from the IN pin and returned to a clean analogue ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

**Important:** To ensure stable operation it is essential that good PCB design practices are employed to minimize ground impedance and keep input inductance low. If these conditions cannot be met, or if long leads are used to connect the battery or other power source to the LP3990, then it is recommended that the input capacitor is increased. Also, tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be ensured by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR (Equivalent Series Resistance) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain approximately 1  $\mu\text{F}$  over the entire operating temperature range.

### 8.2.2.4 Output Capacitor

The LP3990 is designed specifically to work with very small ceramic output capacitors. A 1- $\mu\text{F}$  ceramic capacitor (temperature types Z5U, Y5V or X7R/X5R) with ESR between 5 m $\Omega$  to 500 m $\Omega$ , is suitable in the LP3990 application circuit.

For this device the output capacitor should be connected between the OUT pin and GND pin.

It is also possible to use tantalum or film capacitors at the device output, but these are not as attractive for reasons of size and cost (see [Capacitor Characteristics](#)).

The output capacitor must meet the requirement for the minimum value of capacitance and also have an ESR value that is within the range 5 m $\Omega$  to 500 m $\Omega$  for stability.

### 8.2.2.5 No-Load Stability

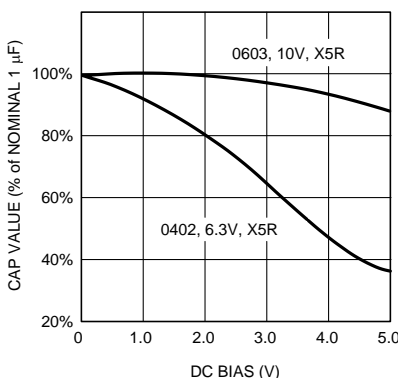
The LP3990 will remain stable and in regulation with no external load. This is an important consideration in some circuits, for example CMOS RAM keep-alive applications.

### 8.2.2.6 Capacitor Characteristics

The LP3990 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer. For capacitance values in the range of 0.47  $\mu\text{F}$  to 4.7  $\mu\text{F}$ , ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1- $\mu\text{F}$  ceramic capacitor is in the range of 20 m $\Omega$  to 40 m $\Omega$ , which easily meets the ESR requirement for stability for the LP3990.

For both input and output capacitors, careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly, depending on the operating conditions and capacitor type.

In particular, the output capacitor selection should take account of all the capacitor parameters, to ensure that the specification is met within the application. The capacitance can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values will also show some decrease over time due to aging. The capacitor parameters are also dependant on the particular case size, with smaller sizes giving poorer performance figures in general. As an example, Figure 14 shows a typical graph comparing different capacitor case sizes in a Capacitance vs. DC Bias plot. As shown in the graph, increasing the DC Bias condition can result in the capacitance value falling below the minimum value given in the recommended capacitor specifications table (0.7  $\mu\text{F}$  in this case). Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions, as some capacitor sizes (for example, 0402) may not be suitable in the actual application.



**Figure 14. Graph Showing A Typical Variation In Capacitance vs DC Bias**

The ceramic capacitor's capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ , will only vary the capacitance to within  $\pm 15\%$ . The capacitor type X5R has a similar tolerance over a reduced temperature range of  $-55^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . Many large value ceramic capacitors, larger than 1  $\mu\text{F}$  are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from  $25^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . Therefore, X7R and X5R types are recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below  $25^{\circ}\text{C}$ .

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 0.47- $\mu\text{F}$  to 4.7- $\mu\text{F}$  range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from  $25^{\circ}\text{C}$  down to  $-40^{\circ}\text{C}$ , so some guard band must be allowed.

### 8.2.2.7 Enable Control

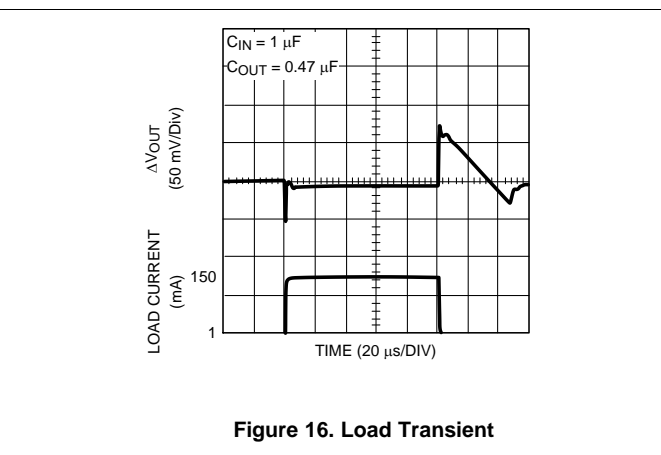
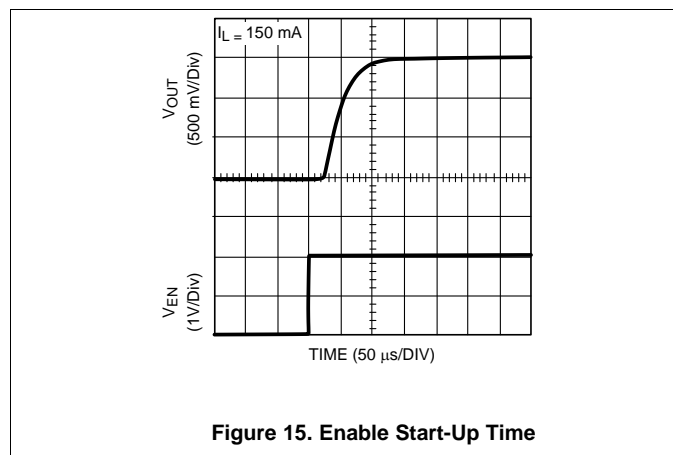
The LP3990 features an active high Enable pin, EN, which turns the device on when pulled high. When not enabled the regulator output is off and the device typically consumes 2 nA.

If the application does not require the Enable switching feature, the EN pin should be tied to  $V_{\text{IN}}$  to keep the regulator output permanently on.

To ensure proper operation, the signal source used to drive the EN input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the [Electrical Characteristics](#) section under  $V_{IL}$  and  $V_{IH}$ .

An internal 1-M $\Omega$  pull-down resistor ties the EN input to ground, ensuring that the device remains off if the EN pin is left open circuit.

## 8.2.3 Application Curves



## 9 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 2 V to 6 V. The input supply should be well regulated and free of spurious noise. To ensure that the LP3990 output voltage is well regulated, the input supply should be at least  $V_{OUT} + 0.5$  V, or 2 V, whichever is higher. A minimum capacitor value of 1- $\mu$ F is required to be within 1 cm of the IN pin.

## 10 Layout

### 10.1 Layout Guidelines

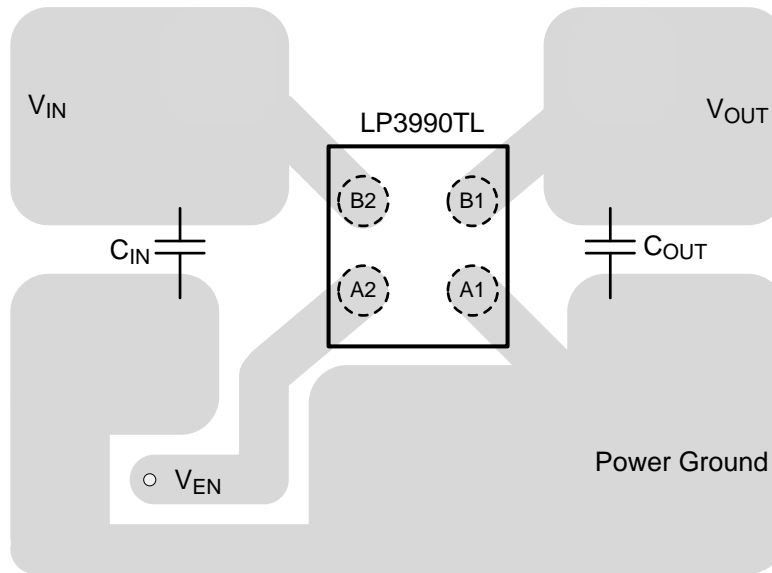
The dynamic performance of the LP3990 is dependant on the layout of the PCB. PCB layout practices that are adequate for typical LDO's may degrade the load regulation, PSRR, noise, or transient performance of the LP3990.

Best performance is achieved by placing  $C_{IN}$  and  $C_{OUT}$  on the same side of the PCB as the LP3990, and as close as is practical to the package. The ground connections for  $C_{IN}$  and  $C_{OUT}$  should be back to the LP3990 ground pin using as wide, and as short, of a copper trace as is practical.

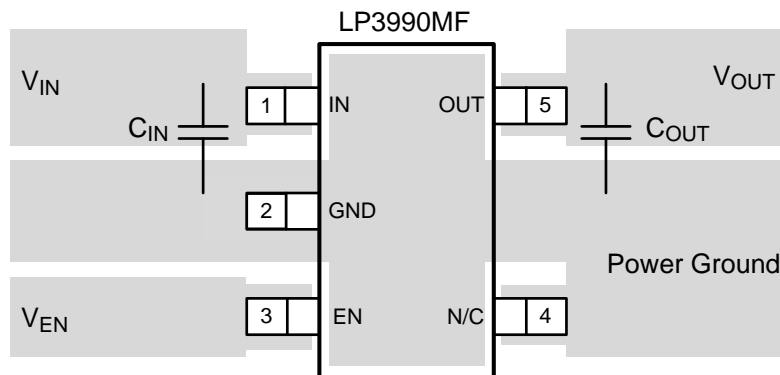
Connections using long trace lengths, narrow trace widths, and/or connections through vias should be avoided. These will add parasitic inductances and resistance that results in inferior performance especially during transient conditions.

A Ground Plane, either on the opposite side of a two-layer PCB, or embedded in a multi-layer PCB, is strongly recommended. This Ground Plane serves two purposes : 1) Provide a circuit reference plane to assure accuracy, and 2) provides a thermal plane to remove heat from the LP3990 WSON package through thermal vias under the package DAP.

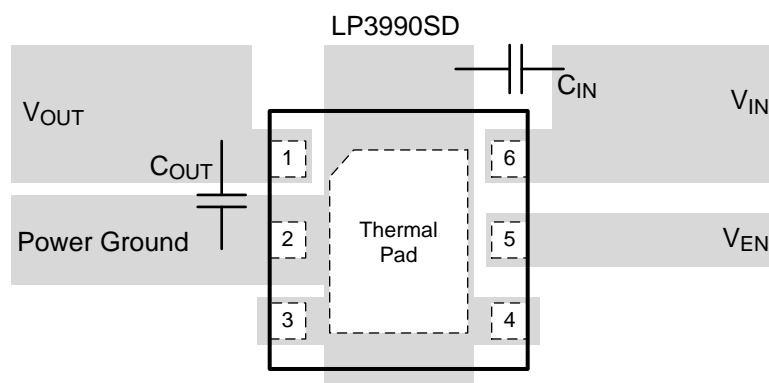
## 10.2 Layout Examples



**Figure 17. LP3990 DSBGA Layout**



**Figure 18. LP3990 SOT-23 Layout**



**Figure 19. LP3990 WSON Layout**

### 10.3 DSBGA Mounting

The DSBGA package requires specific mounting techniques, which are detailed in TI Application Note *DSBGA Wafer Level Chip Scale Package* [SNVA009](#).

For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the DSBGA device.

### 10.4 DSBGA Light Sensitivity

Exposing the DSBGA device to direct light may affect the operation of the device. Light sources, such as halogen lamps, can affect electrical performance, if placed in close proximity to the device.

Light with wavelengths in the infra-red portion of the spectrum is the most detrimental, and so, fluorescent lighting used inside most buildings, has little or no effect on performance.



## 11 Device and Documentation Support

### 11.1 Trademarks

All trademarks are the property of their respective owners.

### 11.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3990MF-1.2/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SCDB	<a href="#">Samples</a>
LP3990MF-1.8	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	SCFB	
LP3990MF-1.8/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SCFB	<a href="#">Samples</a>
LP3990MF-2.5	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	SCJB	
LP3990MF-2.5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SCJB	<a href="#">Samples</a>
LP3990MF-2.8/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SCKB	<a href="#">Samples</a>
LP3990MF-3.3/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SCLB	<a href="#">Samples</a>
LP3990MFX-1.2/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SCDB	<a href="#">Samples</a>
LP3990MFX-1.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SCFB	<a href="#">Samples</a>
LP3990MFX-3.3	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125	SCLB	
LP3990MFX-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SCLB	<a href="#">Samples</a>
LP3990SD-1.2/NOPB	ACTIVE	WSO	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L086B	<a href="#">Samples</a>
LP3990SD-1.5/NOPB	ACTIVE	WSO	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L087B	<a href="#">Samples</a>
LP3990SD-1.8/NOPB	ACTIVE	WSO	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L088B	<a href="#">Samples</a>
LP3990TL-0.8/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		<a href="#">Samples</a>
LP3990TL-1.2/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		<a href="#">Samples</a>
LP3990TL-1.35/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		<a href="#">Samples</a>
LP3990TL-1.5/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3990TL-1.8/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		<a href="#">Samples</a>
LP3990TL-2.5/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		<a href="#">Samples</a>
LP3990TL-2.8/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		<a href="#">Samples</a>
LP3990TLX-0.8/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		<a href="#">Samples</a>
LP3990TLX-1.2/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		<a href="#">Samples</a>
LP3990TLX-1.35/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		<a href="#">Samples</a>
LP3990TLX-1.5/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		<a href="#">Samples</a>
LP3990TLX-1.8/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		<a href="#">Samples</a>
LP3990TLX-2.5/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		<a href="#">Samples</a>
LP3990TLX-2.8/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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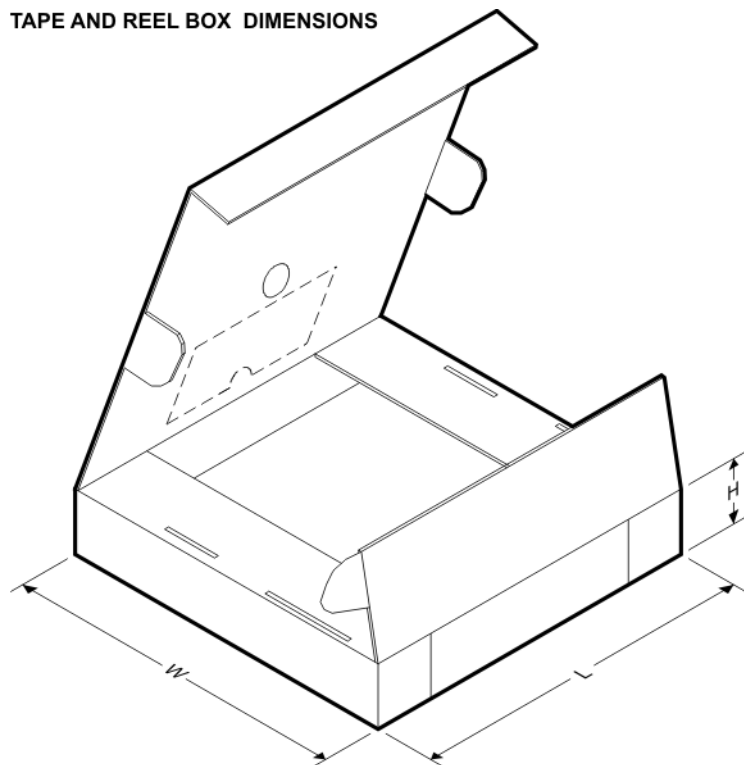
**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3990MF-1.2/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3990MF-1.8	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3990MF-1.8/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3990MF-2.5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3990MF-2.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3990MF-2.8/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3990MF-3.3/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3990MFX-1.2/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3990MFX-1.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3990MFX-3.3	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3990MFX-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3990SD-1.2/NOPB	WSO	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP3990SD-1.5/NOPB	WSO	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP3990SD-1.8/NOPB	WSO	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP3990TL-0.8/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1
LP3990TL-1.2/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1
LP3990TL-1.35/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1
LP3990TL-1.5/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3990TL-1.8/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1
LP3990TL-2.5/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1
LP3990TL-2.8/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1
LP3990TLX-0.8/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1
LP3990TLX-1.2/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1
LP3990TLX-1.35/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1
LP3990TLX-1.5/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1
LP3990TLX-1.8/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1
LP3990TLX-2.5/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1
LP3990TLX-2.8/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.09	1.35	0.76	4.0	8.0	Q1

## TAPE AND REEL BOX DIMENSIONS



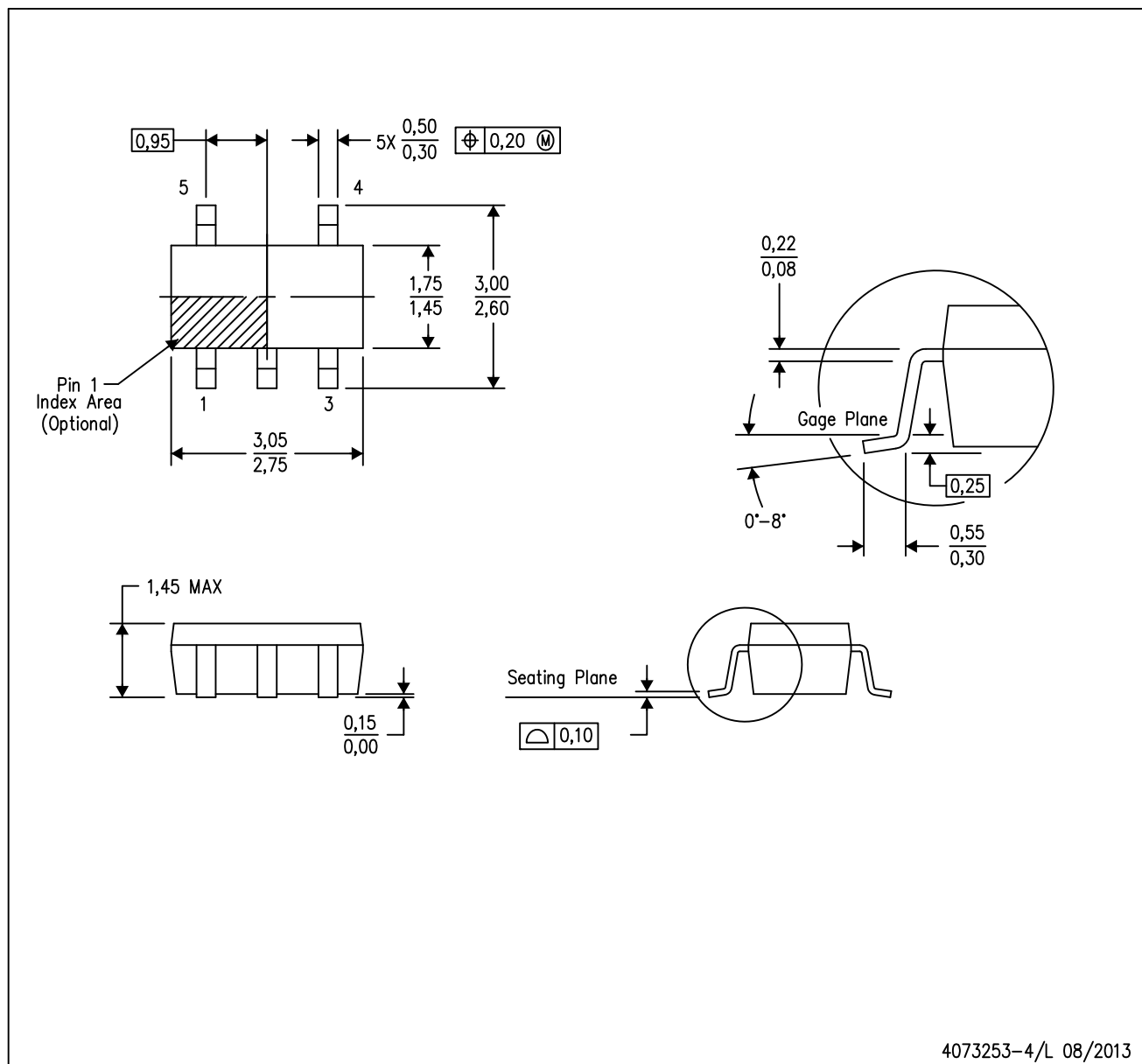
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3990MF-1.2/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3990MF-1.8	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3990MF-1.8/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3990MF-2.5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3990MF-2.5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3990MF-2.8/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3990MF-3.3/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3990MFX-1.2/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3990MFX-1.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3990MFX-3.3	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3990MFX-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3990SD-1.2/NOPB	WSO	NGG	6	1000	210.0	185.0	35.0
LP3990SD-1.5/NOPB	WSO	NGG	6	1000	210.0	185.0	35.0
LP3990SD-1.8/NOPB	WSO	NGG	6	1000	210.0	185.0	35.0
LP3990TL-0.8/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP3990TL-1.2/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP3990TL-1.35/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP3990TL-1.5/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP3990TL-1.8/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP3990TL-2.5/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP3990TL-2.8/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP3990TLX-0.8/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP3990TLX-1.2/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP3990TLX-1.35/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP3990TLX-1.5/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP3990TLX-1.8/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP3990TLX-2.5/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP3990TLX-2.8/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE

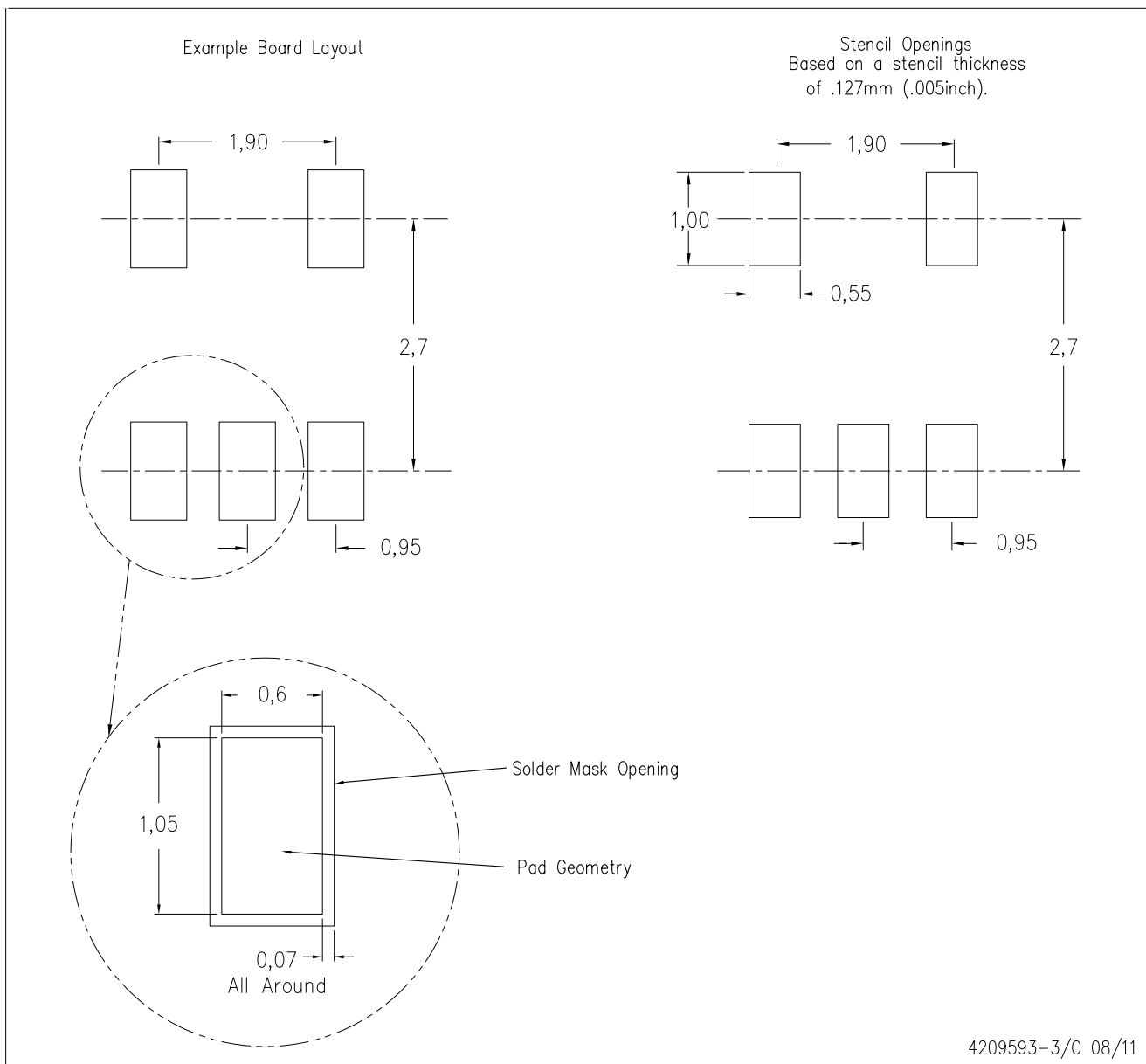


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-178 Variation AA.

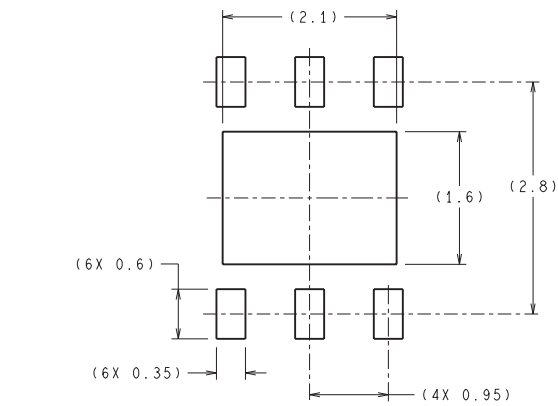


DBV (R-PDSO-G5)

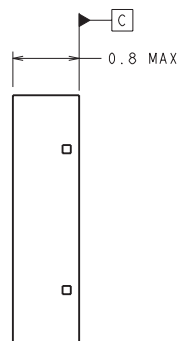
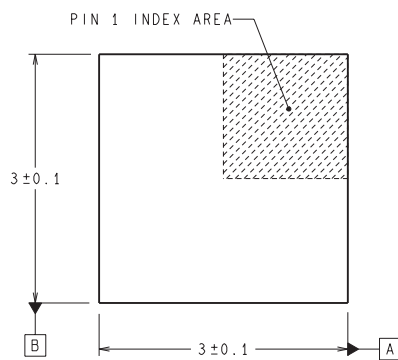
PLASTIC SMALL OUTLINE



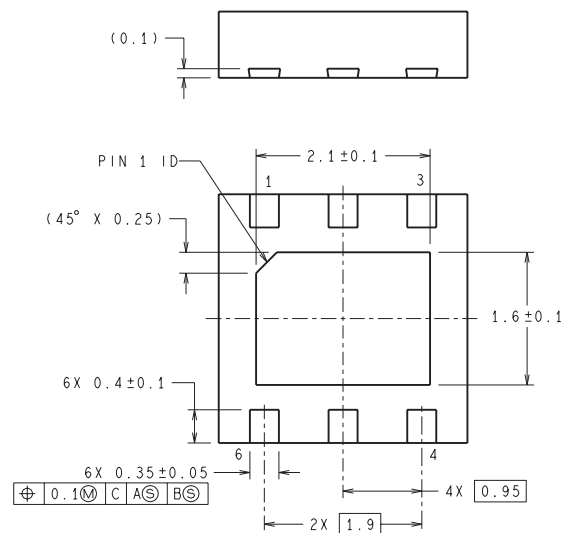
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



## RECOMMENDED LAND PATTERN

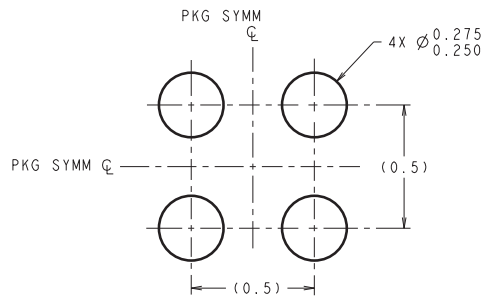


**DIMENSIONS ARE IN MILLIMETERS**  
DIMENSION IN ( ) FOR REFERENCE ONLY

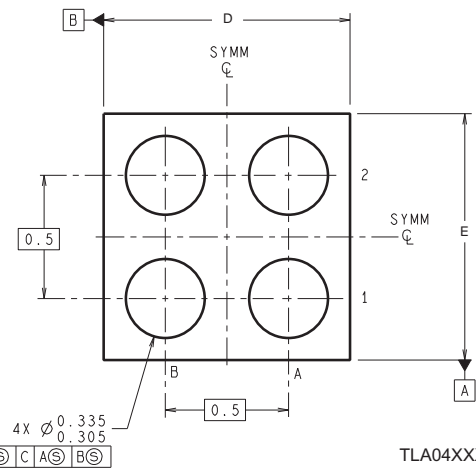
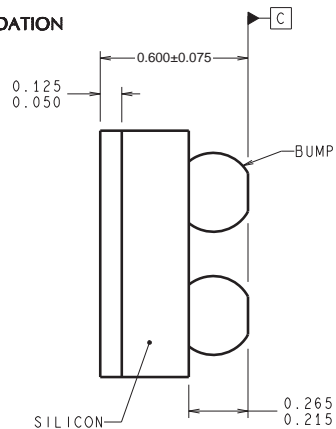
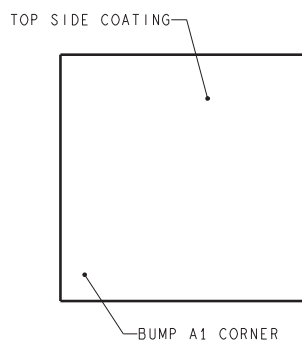


SDE06A (Rev A)

YZR0004



**DIMENSIONS ARE IN MILLIMETERS**  
DIMENSIONS IN ( ) FOR REFERENCE ONLY

**LAND PATTERN RECOMMENDATION**

TLA04XXX (Rev D)

D: Max = 1.324 mm, Min = 1.263 mm

E: Max = 1.045 mm, Min = 0.984 mm

4215042/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.  
B. This drawing is subject to change without notice.

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