4.1.2 Serial Presence Detect (SPD), General Standard

Release Version 7R10

Introduction

New memory technologies are continually being introduced to the industry. As these new technologies are considered, the need for expansion modules becomes evident; consequently, new memory technologies are being incorporated onto existing module form factors. Unfortunately, upon a module's first implementation, the module designer is often unable to predict all of the (as yet unreleased) memory technologies which would eventually be used on the module form factor; hence the parallel Presence Detect method did not allow for these newer technologies. Given that memory modules do not regularly change form factor when a new memory technology is implemented, a Serial Presence Detect (SPD) method should be available and predefined so that it can be considered for new memory modules when needed.

1 Scope

This standard defines the means to implement a Presence Detect (PD) scheme serially. This Serial Presence Detect (SPD) standard is intended for use on any memory module, independent of memory technology or module form factor. At the point of standardization of any given memory module, SPD being defined within this standard, may be easily implemented if so chosen. The body of this standard will depict generally how SPD is implemented; this will be independent of the module's memory technology.

When a specific memory technology is being depicted (e.g., Fast Page Mode DRAM), an annex to this standard will be added describing the characteristics, features, and attributes of that memory technology needed for Presence Detection. The entire address map of the SPD scheme must be presented in each annex.

When a new module form factor implementing SPD is standardized, the (proposed) standard for that module must also include the following information pertinent to the SPD:
- SPD Interface protocol (see 2, herein),
- Acceptable module configurations,
- Legitimate architectures: depth, width, #banks, addressing,
- Acceptable error checking schemes (ECC, Parity...),
- SPD wiring diagram and pinout to module.

Note that all writable memory modules that include a Serial Presence Detect (SPD) feature must also support "Page Write" operations of at least 4 sequential addresses.

2 Interface Protocol

Upon the development/standardization of a new module form factor incorporating SPD, the SPD interface protocol will be defined. As long as that module form factor is used, this protocol must remain constant. Examples of SPD interface protocol include I^2C, Microwire, etc. The physical implementation (pinouts etc.) must also be defined in the standard for the module form factor if it implements SPD.

The interface standard for the SPD used on all JEDEC memory modules is defined for the following device types:
- EE1002 family of EEPROM devices
- TSE2002 family of EEPROM devices with integrated thermal sensor
- TS3000 family of standalone thermal sensors

Though not technically an SPD device, the TS3000 family of sensors are defined to be compatible with modules using SPD devices. In addition, the TSE2002 family of devices is intended to be a superset of the functionality of EE1002 and TS3000 family devices.

3   Data Order and PD Size

This document will present the order in which the PD bytes should follow. It also defines how many bytes must be used to define a given PD; in most cases it will be one byte per PD. The SPD address map is fixed upon selection of any given fundamental technology, this includes all required and optional data; when a fundamental memory technology's PD bits are defined, then the entire address map for those SPDs must also be defined.

4   SPD Data Types

SPD data is stored in a non-volatile serial memory device. The different types of data include, but are not limited to:
- Look Up Table entries
- Binary data
- Optional data (Binary, ASCII, etc.)
- Checksums or Cyclic Redundancy Checks

4.1   Look Up Table (LUT) Entries

Much of the SPD data is organized as a series of table entries. Each table entry contains one or more bytes of information. Each table entry represents one particular characteristic pertinent to the memory module; e.g., fast page mode DRAM will have specific tables for tRAC, tCAC, number of banks, number of row addresses, number of column addresses, error detection/correction, refresh rates, data width, and interface standard. Each table entry corresponds to a position on a lookup table specified within an annex of this standard. The number of bytes (one or more) needed to express a particular aspect of the module is fixed and defined in this standard or in one of its annexes.

4.2   Optional Data

The current JEDEC Standard allows for manufacturers to insert some of their own specific data into the SPD EEROM. This data includes manufacturer ID, manufacturers' module serial numbers, and other ASCII, Binary Coded Decimal, or binary data.

4.3   Checksums and Cyclic Redundancy Checks

In various cases, checksums are required. This procedure applies to all situations where a Checksum is required. Checksum calculation method is as follows:
1. Convert binary information in byte locations 0 to 62 to decimal.
2. Sum all decimal values for locations 0 to 62.
3. Divide "sum" by 256.
4. Convert remainder to binary (will be less than 256).
5. Store result (single byte) in location 63 as 'Checksum'.

Note that the same result can be obtained by summing the binary values in locations 0 to 62, and eliminating all but the low order byte. The low order byte would be the 'checksum'.

4.3   Checksums and Cyclic Redundancy Checks (Cont'd)

Example

SPD Byte Address	Serial PD		Convert to Decimal	
0	0010 0100	=>	36	
1	1111 1110	=>	254	
2	0000 0000	=>	0	
3	0000 0000	=>	0	
-	-	-	-	
-	-	-	-	
-	-	-		
59	0000 0000	=>	0	
60	0000 0000	=>	0	
61	0000 0000	=>	0	
62	0000 0000	=>	0	
			290	(Sum of all decimal values)
			290/256	(Divide by 256) = 1, with a remainder of 34
			34	(Keep remainder)
			0010 0010	(Convert remainder to binary)
63	0010 0010			Store checksum in address location #63

4.3 Checksums and Cyclic Redundancy Checks (Cont'd)

Newer SPDs use a more robust Cyclic Redundancy Check (CRC) algorithm for validating the contents of the SPD EEPROM. The polynomial calculated with this algorithm is $x^{16} + x^{12} + x^5 + 1$. The following algorithm is an example of how to code this polynomial.

```
int Crc16 (char *ptr, int count)
{
    int crc, i;

    crc = 0;
    while (--count >= 0) {
        crc = crc ^ (int)*ptr++ << 8;
        for (i = 0; i < 8; ++i)
            if (crc & 0x8000)
                crc = crc << 1 ^ 0x1021;
            else
                crc = crc << 1;
    }
    return (crc & 0xFFFF);
}

char spdBytes[] = { SPD_byte_0, SPD_byte_1, ..., SPD_byte_N-1 };
int data16;

data16 = Crc16 (spdBytes, sizeof(spdBytes));
SPD_byte_126 = (char) (data16 & 0xFF);
SPD_byte_127 = (char) (data16 >> 8);
```

5   SPD Content, Legacy and Modern Definitions

The legacy SPD definition was traditionally used for memory and module types. As space on the SPD EEPROM ran out, redefinitions of the SPD layout arose for use in subsequent memory and module types. Table 1 summarizes the type of SPD encoding used for various memory types.

Table 1 — Legacy and Modern Definitions

Fundamental Memory Type	SPD Encoding
Fast Page Mode (FPM)	Legacy
Extended Data Out (EDO)	Legacy
SDRAM	Legacy
DDR1 SDRAM	Legacy
DDR2 SDRAM except for FB-DIMM	Legacy
DDR2 FB-DIMM	DDR2 FB-DIMM
DDR3 SDRAM	DDR3 SDRAM

Among all the SPD definitions, Byte 2 (Fundamental Memory Type) is the common Key Byte that is used to differentiate the SPD encoding type.

6   SPD Content, Legacy SPD Definition

The Serial Presence Detect standard calls for various features and items to be defined. Specifically, the definitions listed in Table 2 must be addressed in any SPD implementation.

Table 2 — Legacy SPD Definition

Description	Data Type	Address Map Byte #
SPD size	LUT Entry	0
Total SPD memory size	LUT Entry	1
Fundamental memory type	LUT Entry, Annex A	2
Definition of features specific to the fundamental memory	See pertinent annex	3-XX
(Optional) Superset memory type	See Annex B	XX-60
(Optional) definition of features specific to the superset memory	See pertinent annex	33-61
SPD Revision designator	LUT	62
Checksum for bytes 0-62	Checksum	63
Manufacturer's Jedec ID code per JEP-106	LUT	64-71
Manufacturing location	Supplier Unique	72
Manufacturer's Part Number	Supplier Unique	73-90
Revision Code	Supplier Unique	91-92
Manufacturing date	BCD	93-94
Assembly Serial Number	Supplier Unique	95-98
Manufacturer Specific Data	Supplier Unique	99-125
Reserved	N/A	126-127
Open free-form area	Application Specific	128-255

6.1 Byte 0, Number of Bytes used by Module Manufacturer

This field describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data.

Table 3 — Legacy SPD, Byte 0

Number SPD Bytes	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
...	-	-	-	-	-	-	-	-
128	1	0	0	0	0	0	0	0
...	-	-	-	-	-	-	-	-
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

6.2 Byte 1, Total SPD Memory Size

This field describes the total size of the serial memory (often an EEPROM) used to hold the Serial Presence Detect data. Table 4 describes the possible serial memory densities (in bytes) along with the corresponding descriptor.

Table 4 — Legacy SPD, Byte 1

Serial Memory Density	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	0	0	0	0	0	0	0	0
2 Bytes	0	0	0	0	0	0	0	1
4 Bytes	0	0	0	0	0	0	1	0
8 Bytes	0	0	0	0	0	0	1	1
...	-	-	-	-	-	-	-	-
256 Bytes	0	0	0	0	1	0	0	0
512 Bytes	0	0	0	0	1	0	0	1
1024 Bytes	0	0	0	0	1	0	1	0
2048 Bytes	0	0	0	0	1	0	1	1
4096 Bytes	0	0	0	0	1	1	0	0
8192 Bytes	0	0	0	0	1	1	0	1
16284 Bytes	0	0	0	0	1	1	1	0
...	-	-	-	-	-	-	-	-
-	1	1	1	1	1	1	1	0
-	1	1	1	1	1	1	1	1

6.3   Byte 2, Fundamental Memory Type

This field will identify the fundamental type of memory. The fundamental type of memory may include Fast Page Mode DRAM, EDO DRAM, Masked ROM, EEPROM, Synchronous DRAM, etc. The table listing all the types of Fundamental memory is contained in Annex A. New fundamental types can be added to this table anytime after standardization of a fundamental memory type. Note that if a given new technology is completely backward compatible with pre-existing technology, then it should be considered a Superset technology and so described as detailed in 6.5.

6.4   Bytes 3-31: Descriptions of Module Specific Features

Annexes to this standard detail the tables for the features specific to each of the fundamental memory types as described above. For example, see Annex C for details of SPD features for Fast Page Mode and Extended Data Out DRAM Modules.

6.5   Byte 32: Superset Memory Type

When a new technology is developed that is completely backward compatible to an already specified (fundamental) technology, then it may be considered a 'Superset' technology. The benefits of specifying a technology as a superset are obvious; if a system is capable of operating in a 'fundamental' mode only and a superset module is inserted, then the system can still use the module. The memory superset type or technology is specified in Annex B, which provides the decode of specific superset technologies. It references other annexes where the specific superset PDs are further detailed. As new supersets are created, annexes must also be added. Presence Detects for a superset technology are specified just as for any given fundamental technology except that any and all backward compatible fundamental technologies must be referenced.

6.6   Bytes 33-62: Superset Features

Annexes to this standard detail the tables for the features specific to each of the superset memory types as described above. A new annex must be added to this standard detailing the PDs for that superset technology detailed in Annex B and represented in byte 32. Annex B would identify the superset technology type and would also reference the appropriate annex where the superset is detailed.

6.7   Byte 63

Checksum of Bytes 0 to 62 as defined in 4.3.

6.8   Bytes 64-127

Module manufacturers may include information that is pertinent to their particular modules. This information is detailed below.

6.8.1   Bytes 64-71: Manufacturer's Jedec ID code per EIA/JEP106

Manufacturers of a given module may include their identifier per JEDEC spec EIA/JEP106. 0x00 is not allowed in bytes 64 to 67 (bank 1), and a 0x7F (continuation code) indicates that the manufacturer's code is beyond the limit of this field and will reside in bytes 68 to 71 (bank 2). 0x00 or 0xFF may be used in bytes 68 to 71 if they are unused.

6.8.2   Byte 72: Manufacturing Location

Manufacturers may include an identifier that uniquely defines the manufacturing location of the memory module. While the SPD spec will not attempt to present a decode table for manufacturing sites, the individual manufacturer may keep track of manufacturing location and its appropriate decode represented in this byte.

6.8.3   Bytes 73-90: Manufacturer's Part Number

Manufacturers may include their part number in 6-bit ASCII format within these bytes.

6.8.4   Bytes 91-92: Revision Code

This refers to the module revision code. While the SPD spec will not attempt to define the format for this information, the individual manufacturer may keep track of the revision code and its appropriate decode represented in this byte.

6.8.5   Bytes 93-94: Date of Module Manufacture

The module manufacturer may include a date code for the module. If this is done, then specifically, byte 93 must contain the year in Binary Coded Decimal (BCD) and byte 94 must contain the week in Binary Coded Decimal (BCD).

6.8.6   Bytes 95-98: Module Serial Number

The supplier may include a serial number for module. The supplier may use whatever decode method desired to maintain a unique serial number for each module.

6.8.7   Bytes 99-125: Manufacturers specific data, open area

The module manufacturer may add any additional information desired into the module within these locations.

6.8.8   Bytes 126-127: Reserved

These bytes are reserved and cannot be later allocated.

6.9   Bytes 128-255: System Integrators specific information

The system integrator may choose to use the SPD EEPROM for various items. If so, then bytes 128-255 may be used.

7   SPD Content, FB-DIMM SPD Definition

The Serial Presence Detect standard calls for various features and items to be defined. Specifically, the definitions listed in Table 5 must be addressed in any SPD implementation:

Table 5 — FB-DIMM SPD Definition

Description	Data Type	Address Map Byte #
General Section	-	0-59
Number of Serial PD Bytes Written / SPD Device Size / CRC Coverage	LUT Entry	0
SPD Revision	LUT Entry	1
Key Byte / DRAM Device Type	LUT Entry, Annex A	2
Other entries in General Section	-	3-59
FB-DIMM Specific Section	-	60-116
Manufacturer Specific Section	-	117-175
Module manufacturer JEDEC ID code	LUT Entry, JEP-106	117-118
Manufacturing location	Supplier Unique	119
Manufacturing date	BCD	120-121
Assembly Serial Number	Supplier Unique	122-125
Cyclic Redundancy Check code	Supplier Unique	126-127
Module manufacturer's serial number	Supplier Unique	128-145
Module revision code	Supplier Unique	146-147
SDRAM manufacturer JEDEC ID code per JEP-106	Supplier Unique	148-149

7   SPD Content, FB-DIMM SPD Definition (Cont'd)

Table 5 — FB-DIMM SPD Definition

Description	Data Type	Address Map Byte #
Module manufacturer's specific data	Supplier Unique	150-175
Open free-form area	Application Specific	176-255

7.1   Byte 0: Number of Serial PD Bytes Written / SPD Device Size / CRC Coverage

This byte has three distinct fields, broken down by bit location.

Table 6 — FB-DIMM SPD, Byte 0

Bit 7	Bit 6 ~ 4	Bit 3 ~ Bit 0
CRC Coverage	SPD Bytes Total	SPD Bytes Used

0 = CRC covers bytes 0 ~ 125
1 = CRC covers bytes 0 ~ 116
	Bit [6, 5, 4] :
	   000 = Undefined
	   001 = 256
	   All Others TBD
		Bit [3, 2, 1, 0] :
		   0000 = Undefined
		   0001 = 128
		   0010 = 176
		   0011 = 256
		   All Others TBD

Byte 0 bit 7 determines the coverage of the CRC contained in bytes 126-127, which is either bytes 0 through 125 or bytes 0 through 116.

7.2   Byte 1: SPD Revision

This byte describes the compatibility level of the encoding of the bytes contained in the SPD EEPROM, and the current collection of valid defined bytes. Software should examine the upper nibble (Encoding Level) to determine if it can correctly interpret the contents of the module SPD. The lower nibble (Additions Level) can optionally be used to determine which additional bytes or attribute bits have been defined; however, since any undefined additional byte must be encoded as 0x00 or undefined attribute bit must be defined as 0, software can safely detect additional bytes and use safe defaults if a zero encoding is read for these bytes.

The Additions Level is never reduced even after an increment of the Encoding Level. For example, if the current SPD revision level were 1.2 and a change in Encoding Level were approved, the next revision level would be 2.2. If additions to revision 2.2 were approved, the next revision would be 2.3. Changes in the Encoding Level are extremely rare, however, since they can create incompatibilities with older systems.

The exceptions to the above rule are the SPD revision levels used during development prior to the Revision 1.0 release. Revisions 0.0 through 0.9 are used to indicate sequential pre-production SPD revision levels, however the first production release will be Revision 1.0.

7.3   Byte 2: Fundamental Memory Type

This field identifies the fundamental type of memory used on the assembly. The fundamental type of memory for FB-DIMMs are DDR2 or FB-DIMM Probe (a unique Fundamental Type value to indicate logic analysis probe boards).

7.4   Bytes 3-59: General Section

These bytes describe general features such as DRAM timings and thermal characteristics.

7.5   Bytes 60-116: FB-DIMM Specific Section

These bytes describe features that are specific to a class of FB-DIMM types, such as Advanced Memory Buffer timings and thermal characteristics.

7.6   Bytes 117-118: Module Manufacturer ID

Manufacturers of a given module may include their identifier per JEDEC spec EIA/JEP106. 0x00 is not allowed in bytes 64 to 67 (bank 1) and a 0x7F (continuation code) indicates that the manufacturer's code is beyond the limit of this field and will reside in bytes 68 to 71 (bank 2). 0x00 or 0xFF may be used in bytes 68 to 71 if they are unused.

7.7   Byte 119: Manufacturer Location

The module manufacturer includes an identifier that uniquely defines the manufacturing location of the memory module. While the SPD spec will not attempt to present a decode table for manufacturing sites, the individual manufacturer may keep track of manufacturing location and its appropriate decode represented in this byte.

7.8   Bytes 120-121: Manufacturing Date

The module manufacturer includes a date code for the module. The JEDEC definitions for bytes 120 and 121 are year and week respectively. These bytes must be represented in Binary Coded Decimal (BCD). For example, week 47 in year 2003 would be coded as 03 (0000 0011) in byte 120 and 47 (0100 0111) in byte 121.

7.9   Bytes 122-125: Assembly Serial Number

The supplier must include a unique serial number for the module. The supplier may use whatever decode method desired to maintain a unique serial number for each module.

7.10 Bytes 126-127: Cyclic Redundancy Check

This two-byte field contains the calculated 16-bit CRC-CCITT (polynomial 0x1021) for previous bytes in the SPD. The following algorithm and data structures (shown in C) are to be followed in calculating and checking the code. Bit 7 of Byte 0 indicates which bytes are covered by the CRC. The polynomial calculated with this algorithm is $x^{16} + x^{12} + x^5 + 1$.

7.11 Bytes 128-145: Module Manufacturer's Serial Number

The manufacturer's part number is written in ASCII format within these bytes. Unused digits are coded as ASCII blanks (0x20).

7.12 Bytes 146-147: Module Revision Code

This refers to the module revision code. While the SPD spec will not attempt to define the format for this information, the individual manufacturer may keep track of the revision code and its appropriate decode represented in this byte.

7.13 Bytes 148-149: SDRAM Manufacturer's Code

Manufacturers of a given module may include their identifier per JEDEC spec EIA/JEP106. 0x00 is not allowed in bytes 64 to 67 (bank 1) and a 0x7F (continuation code) indicates that the manufacturer's code is beyond the limit of this field and will reside in bytes 68 to 71 (bank 2). 0x00 or 0xFF may be used in bytes 68 to 71 if they are unused.

7.14 Bytes 150-175: Module Manufacturer's Specific Data

The module manufacturer may include any additional information desired into the module within these locations.

7.15 Bytes 176-255: Open Free-form Area

The system integrator may choose to use the SPD EEPROM for various items. If so, then bytes 176-255 may be used.

8   SPD Content, DDR3 SDRAM SPD Definition

The Serial Presence Detect standard calls for various features and items to be defined. Specifically, the definitions listed in Table 7 must be addressed in any SPD implementation:

Table 7 — DDR3 SDRAM SPD Definition

Description	Data Type	Address Map Byte #
General Section		0-59
Number of Serial PD Bytes Written / SPD Device Size / CRC Coverage	LUT Entry	0
SPD Revision	LUT Entry	1
Key Byte / DRAM Device Type	LUT Entry	2
Key Byte / Module Type	LUT Entry	3
Other entries in General Section	-	4-59
Module Type Specific Section, Indexed by Key Byte 3		60-116
Manufacturer Specific Section	-	117-175
Module ID: Module Manufacturer's JEDEC ID Code	LUT Entry, JEP-106	117-118
Module ID: Module Manufacturing Location	Supplier Unique	119
Module ID: Module Manufacturing Date	BCD	120-121
Module ID: Module Serial Number	Supplier Unique	122-125
Cyclical Redundancy Code	Supplier Unique	126-127
Module Part Number	Supplier Unique	128-145
Module Revision Code	Supplier Unique	146-147
DRAM Manufacturer's JEDEC ID Code	Supplier Unique	148-149
Manufacturer's Specific Data	Supplier Unique	150-175
Open for customer use	Application Specific	176-255

8.1   Byte 0: Number of Serial PD Bytes Written / SPD Device Size / CRC Coverage

The least significant nibble of this byte describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data. Bits 6 ~ 4 describe the total size of the serial memory used to hold the Serial Presence Detect data. Bit 7 indicates whether the unique module identifier (found in bytes 117 ~ 125) is covered by the CRC encoded on bytes 126 and 127.

Table 8 — DDR3 SDRAM SPD, Byte 0

Bit 7	Bits 6 ~ 4	Bits 3 ~ 0
CRC Coverage	SPD Bytes Total	SPD Bytes Used

0 = CRC covers bytes 0 ~ 125
1 = CRC covers bytes 0 ~ 116
	Bit [6, 5, 4] :
	    000 = Undefined
	    001 = 256
	    All others reserved
		Bit [3, 2, 1, 0] :
		    0000 = Undefined
		    0001 = 128
		    0010 = 176
		    0011 = 256
		    All others reserved

8.2   Byte 1: SPD Revision

This byte describes the compatibility level of the encoding of the bytes contained in the SPD EEPROM, and the current collection of valid defined bytes. This byte must be coded as 0x10 for SPDs with revision level 1.0. Software should examine the upper nibble (Encoding Level) to determine if it can correctly interpret the contents of the module SPD. The lower nibble (Additions Level) can optionally be used to determine which additional bytes or attribute bits have been defined; however, since any undefined additional byte must be encoded as 0x00 or undefined attribute bit must be defined as 0, software can safely detect additional bytes and use safe defaults if a zero encoding is read for these bytes.

Table 9 — DDR3 SDRAM SPD, Byte 1

Production Status	SPD Revision	Encoding Level				Additions Level				Hex
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Pre-production	Revision 0.0	0	0	0	0	0	0	0	0	00
	Revision 0.1	0	0	0	0	0	0	0	1	01
	...	.	.	.	.	.	.	.	.	.
	Revision 0.9	0	0	0	0	1	0	0	1	09
Production	Revision 1.0	0	0	0	1	0	0	0	0	10
	Revision 1.1	0	0	0	1	0	0	0	1	11
	...	.	.	.	.	.	.	.	.	...
Undefined	Undefined	1	1	1	1	1	1	1	1	FF

The Additions Level is never reduced even after an increment of the Encoding Level. For example, if the current SPD revision level were 1.2 and a change in Encoding Level were approved, the next revision level would be 2.2. If additions to revision 2.2 were approved, the next revision would be 2.3. Changes in the Encoding Level are extremely rare, however, since they can create incompatibilities with older systems.

The exceptions to the above rule are the SPD revision levels used during development prior to the Revision 1.0 release. Revisions 0.0 through 0.9 are used to indicate sequential pre-production SPD revision levels, however the first production release will be Revision 1.0.

8.3   Byte 2: Key Byte, DRAM Device Type

This byte is the key byte used by the system BIOS to determine how to interpret all other bytes in the SPD EEPROM. The BIOS must check this byte first to ensure that the EEPROM data is interpreted correctly. Any DRAM or Module type that requires significant changes to the SPD format (beyond defining previously undefined bytes or bits) also requires a new entry in the key byte table.

8.4   Byte 3: Key Byte, Module Type

This byte is a Key Byte used to index the module specific section of the SPD from bytes 60 ~ 116. Byte 3 identifies the SDRAM memory module type, which implies the width (D dimension) of the module. Other module physical characteristics, such as height (A dimension) or thickness (E dimension) are documented in the module specific section of the SPD. Refer to the relevant JEDEC JC-11 module outline (MO) documents for dimension definitions.

8.4 Byte 3: Key Byte, Module Type (Cont'd)

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<p align="center">Table 10 — DDR3 SDRAM SPD, Byte 3</p>

Bits 7 ~ 4	Bits 3 ~ 0
Reserved	**Module Type**

	Bit [3, 2, 1, 0] :
	  0000 = Undefined
	  0001 = RDIMM (width = 133.35 mm nom)
	  0010 = UDIMM (width = 133.35 mm nom)
	  0011 = SO-DIMM (width = 67.6 mm nom)
	  0100 = Micro-DIMM (width = TBD mm nom)
	  0101 = Mini-RDIMM (width = TBD mm nom)
	  0110 = Mini-UDIMM (width = TBD mm nom)
	All others reserved

Definitions:
  RDIMM: Registered Dual In-Line Memory Module
  UDIMM: Unbuffered Dual In-Line Memory Module
  SO-DIMM: Small Outline Dual In-Line Memory Module
  Micro-DIMM: Micro Dual In-Line Memory Module
  Mini-RDIMM: Mini Registered Dual In-Line Memory Module
  Mini-UDIMM: Mini Unbuffered Dual In-Line Memory Module	

8.5 Bytes 4-59: General Section

Bytes 4 through 59 describe general characteristics of the module and the DRAMs on the module that apply to all module types.

8.6 Bytes 60-116: Module Type Specific Section, Indexed by Key Byte 3

Bytes 60 through 116 are redefined by the contents of Key Byte 3. Similar module types are grouped into each annex which describes the module specific features for that module type.

<p align="center">Table 11 — DDR3 SDRAM SPD, Bytes 60-116</p>

Appendix	Byte 3 Code	Module Type
Unbuffered DIMMs	02	UDIMM
	03	SO-DIMM
	04	Micro-DIMM
	06	Mini-DIMM
Registered DIMM	01	RDIMM
	05	Mini-RDIMM

8.7 Bytes 117-118: Module ID: Module Manufacturer's JEDEC ID Code

This two-byte field indicates the manufacturer of the module, encoded as follows: the first byte is the number of continuation bytes indicated in JEP-106; the second byte is the last non-zero byte of the manufacturer's ID code, again as indicated in JEP-106.

8.8 Byte 119: Module ID: Module Manufacturing Location

The module manufacturer includes an identifier that uniquely defines the manufacturing location of the memory module. While the SPD spec will not attempt to present a decode table for manufacturing sites, the individual manufacturer may keep track of manufacturing location and its appropriate decode represented in this byte.

8.9   Bytes 120-121: Module ID: Module Manufacturing Date

The module manufacturer includes a date code for the module. The JEDEC definitions for bytes 120 and 121 are year and week respectively. These bytes must be represented in Binary Coded Decimal (BCD). For example, week 47 in year 2003 would be coded as 0x03 (0000 0011) in byte 120 and 0x47 (0100 0111) in byte 121.

8.10 Bytes 122-125: Module ID: Module Serial Number

The supplier must include a unique serial number for the module. The supplier may use whatever decode method desired to maintain a unique serial number for each module. One method of achieving this is by assigning a byte in the field from 122 ~ 125 as a tester ID byte and using the remaining bytes as a sequential serial number. Bytes 117 ~ 125 will then result in a nine-byte unique module identifier. Note that part number is not included in this identifier: the supplier may not give the same value for Bytes 119 ~ 125 to more than one DIMM even if the DIMMs have different part numbers.

8.11 Bytes 126-127: Cyclical Redundancy Code

This two-byte field contains the calculated CRC for previous bytes in the SPD. The following algorithm and data structures (shown in C) are to be followed in calculating and checking the code. Bit 7 of Byte 0 indicates which bytes are covered by the CRC.

8.12 Bytes 128-145: Module Part Number

The manufacturer's part number is written in ASCII format within these bytes. Unused digits are coded as ASCII blanks (0x20).

8.13 Bytes 146-147: Module Revision Code

This refers to the module revision code. While the SPD spec will not attempt to define the format for this information, the individual manufacturer may keep track of the revision code and its appropriate decode represented in this byte.

8.14 Bytes 148-149: DRAM Manufacturer's JEDEC ID Code

This two-byte field indicates the manufacturer of the DRAM on the module, encoded as follows: the first byte is the number of continuation bytes indicated in JEP-106; the second byte is the last non-zero byte of the manufacturer's ID code, again as indicated in JEP-106.

8.15 Bytes 150-175: Manufacturer's Specific Data

The module manufacturer may include any additional information desired into the module within these locations.

8.16 Bytes 176-255: Open for customer use

These bytes are unused by the manufacturer and are open for customer use.

9   SPD Common Landing Pattern

The SPD common landing pattern is shown in Figure 1. The common landing pattern recommendations for the TDFN packaged SPD (EE1002 compatible) or SPD with Thermal Sensor (TSE2002 compatible) are parameterized to allow for routing design constraints. The preferred implementation with wide corner pads enhances device centering during assembly, but two narrower options are defined for modules with tight routing requirements.
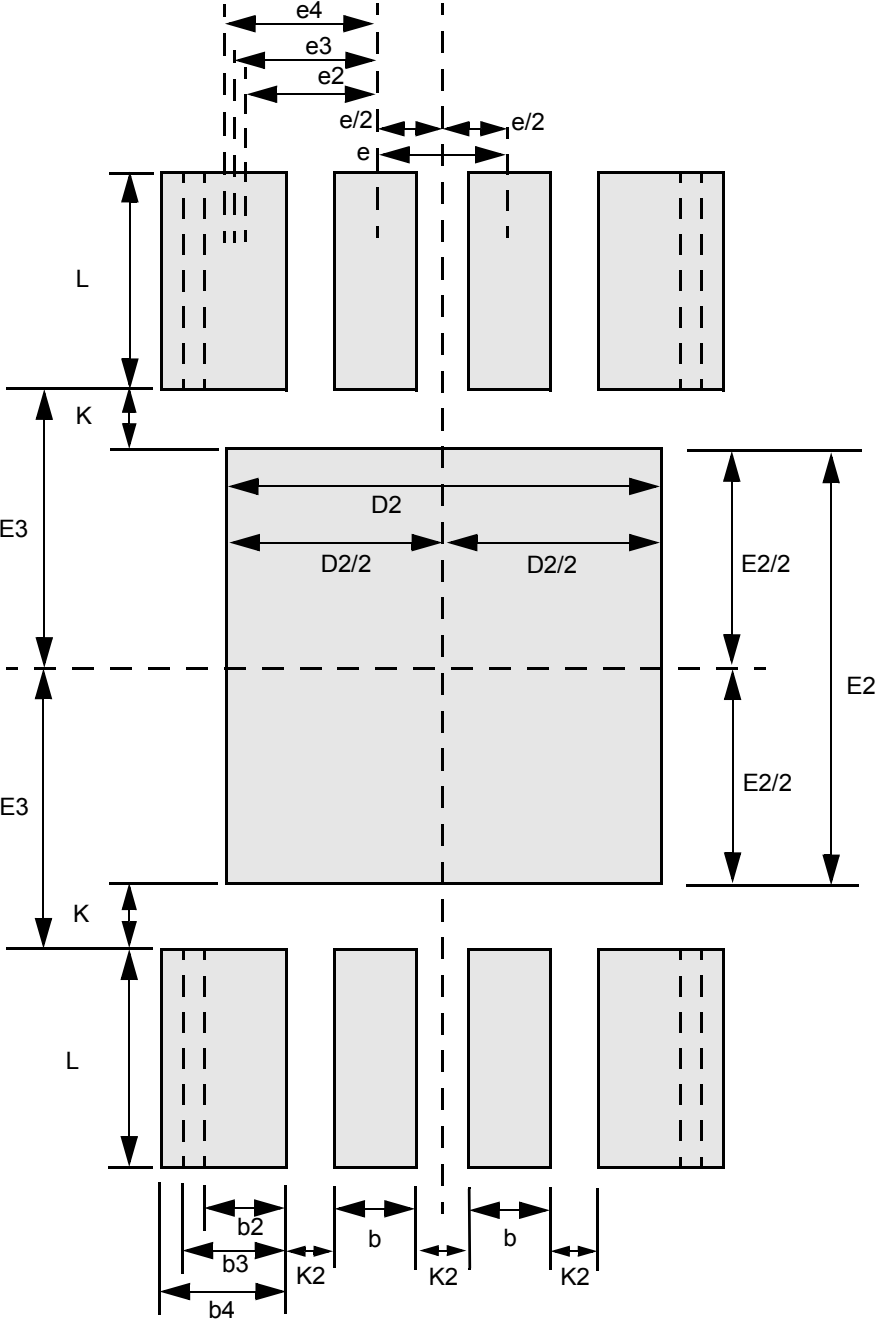
Figure 1 — SPD Common Landing Pattern

9   SPD Common Landing Pattern (Cont'd)

Table 12 lists three variations of landing pattern implementations, ranked as "Preferred", "Intermediate", and "Minimum Acceptable".

Table 12 — Parameters for SPD Common Landing Pattern

Parameter	Description	Dimension			Notes
		Min	Nom	Max	
D2	Heat paddle width	1.40	-	1.60	
E2	Heat paddle height	1.40	-	1.60	
E3	Heat paddle centerline to contact inner locus	1.00	-	1.05	
L	Contact length	0.70	-	0.80	
K	Heat paddle to contact keepout	0.20	-	-	
K2	Contact to contact keepout	0.20	-	-	
e	Contact centerline to contact centerline pitch for inner contacts	-	0.50	-	
b	Contact width for inner contacts	0.25	-	0.30	
e2	Landing pattern centerline to outer contact centerline, "minimum acceptable" option	-	0.50	-	1
b2	Corner contact width, "minimum acceptable" option	0.25	-	0.30	1
e3	Inner contact centerline to outer contact centerline, "intermediate" option	-	0.55	-	2
b3	Corner contact width, "intermediate" option	0.35	-	0.40	2
e4	Landing pattern centerline to outer contact centerline, "preferred" option	-	0.60	-	3
b4	Corner contact width, "preferred" option	0.45	-	0.50	3

NOTE 1   Minimum acceptable option to be used when routing prevents preferred or intermediate width contact.
NOTE 2   Intermediate option to be used when routing prevents preferred width contact.
NOTE 3   Preferred option to be used when possible.