WP2 status
Summary of engineering design review

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Outline

Selected themes from the MOSS FE testing and relation to the MOSAIX FE design

MOSAIX Design Status and Outlook

Summary of Engineering Design Review

MOSS FE TESTING AND RELATION TO MOSAIX

Themes for FE and Biasing from MOSS testing

Temperature dependence of MOSS front-end

Seen in measurements

Reproduced in simulation globally but root cause and possible correction not yet identified

FHR noise analysis

The FHR curves have changes of slope possibly indicating fixed pattern noise. Revisiting the determination of the pixel mask appears needed.

Reports of variations of biasing values with VCASB

Reports of large supply and ground rail voltage differences on one RSU

MOSAIX DESIGN STATUS AND OUTLOOK

New Metal Stack

Received parts of the new PDK for the new metal stack (Friday 7 June)

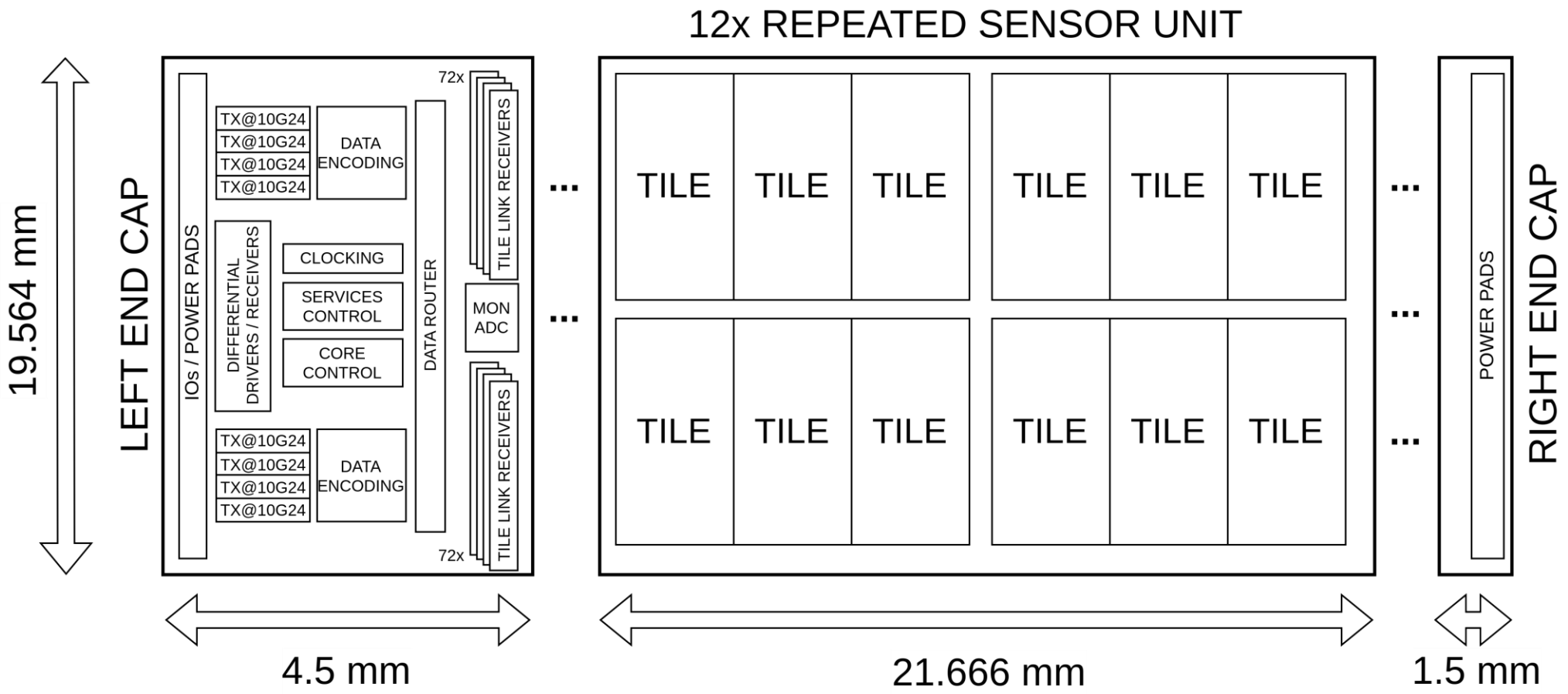
- New design layers and corresponding Design Rules Manual and DRC rules.
- Installed and under test, with pad ring, chiplets and then MOSAIX blocks.
- Some (minor) differences wrt to old PDK for the thin metal layers identified.

Currently: PDK not ready for general usage. Design continues on all blocks with the previous PDK

Missing PEX Parasitic Extraction Rules and DDK Digital Design Kit

- Essential parts
- Foundry replied with the expected release date: end of June

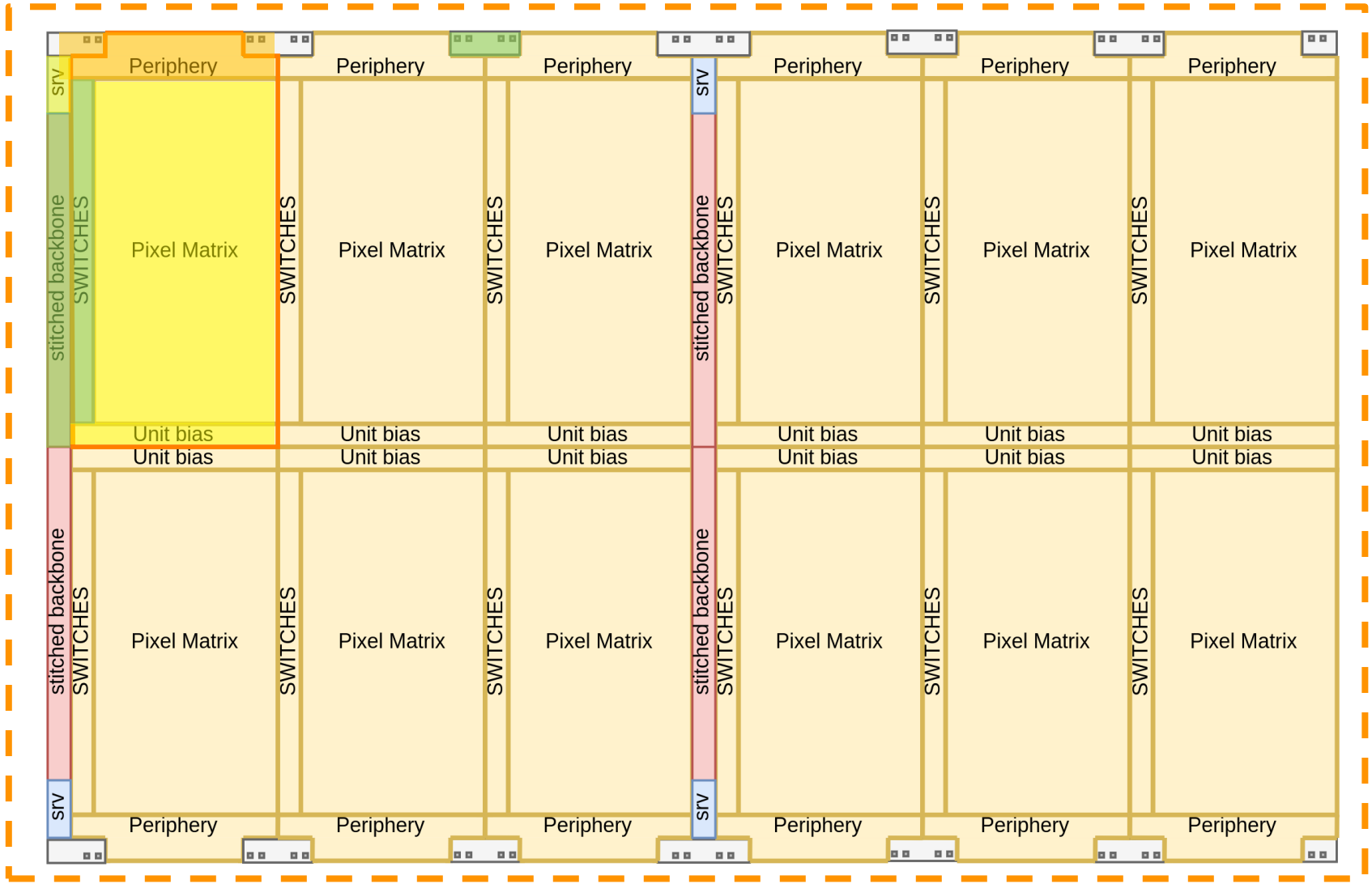
MOSAIX components



RSU

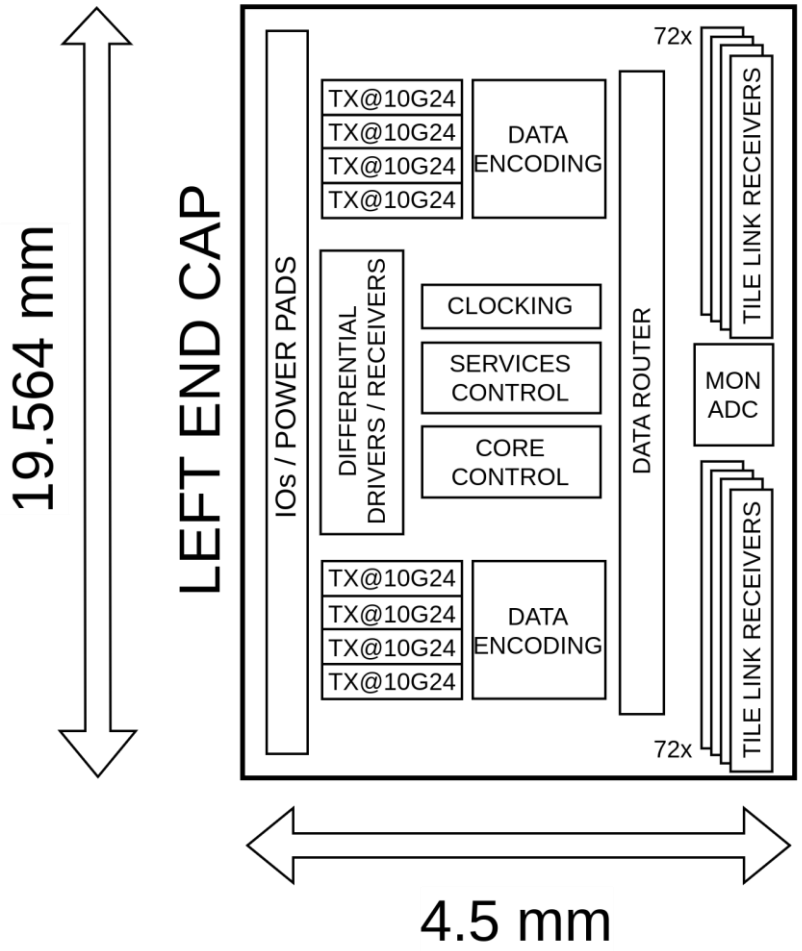
SWITCHES	DONE
BIASING UNIT	DONE
BACKBONE	Layout done. Needs validation with PEX, filling, refinements
MATRIX	Layout submitted 14/06, checking
SBB TILE	Mixed-signal block. Need layout entry of full-custom part. Needs validation with PEX, needs STA and completion.
PERIPHERY	Readout RTL advanced. Control RTL to review. Timing to improve. Implementation flow available
SERVICE NODE	RTL and implementation flow available. Needs final review.
RSU top	Flow Completion Ongoing

RSU TOP INTEGRATION



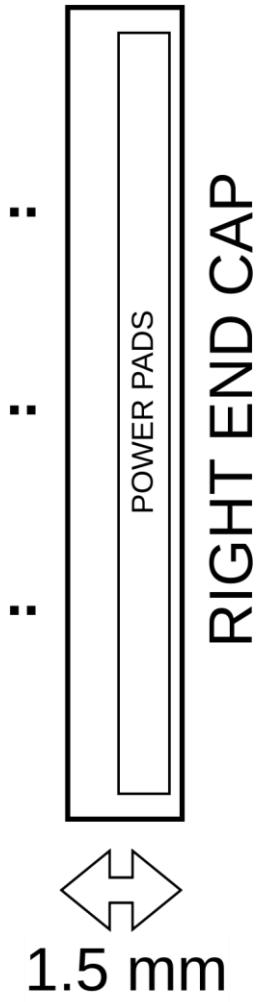
LEC

GWT-PSI	Entry of full custom blocks advancing, completion ETA end of July. Integration on the critical path, unclear ETA of completion.
MONITORING	Design study phase of the analog monitoring part. ADC block port ETA mid July. Full integration ETA unclear.
DIFFERENTIAL I/Os	Unassigned.
PADS	Re-arrangement of pads after specs review was DONE. Missing enlargement.
RECEIVERS	RTL available
ROUTER	RTL available
DATA ENCODING	RTL available
CLOCKING AND SLOW CONTROL	RTL available. Corrections of slow control ongoing. Need refinements and review.
LEC top	Implementation Flow available. Refinements on Floorplan ongoing.



REC

PADS	AVAILABLE
REC	Top Level Implementation ongoing



Design status and work ahead

Significant progress on all components

- Corrections and fixes being already found and applied
- Integration flows made significant progress on various blocks (RSU, LEC, REC, periphery, service node)
- Verification also on the path to complete the environment.

TODO Completion of block level designs

- Target of all blocks completed and available in the new metal stack by end of June won't be reached.
  - My estimate is about 2 months delay on that.
- RSU approaching completion. LEC less mature. GWT-PSI, Analog Monitoring, Differential I/Os are my top concerns.

TODO Port of block designs and integration flow to the new metal stack

- Dependency on full release of PEX and DDK (expected end of June)

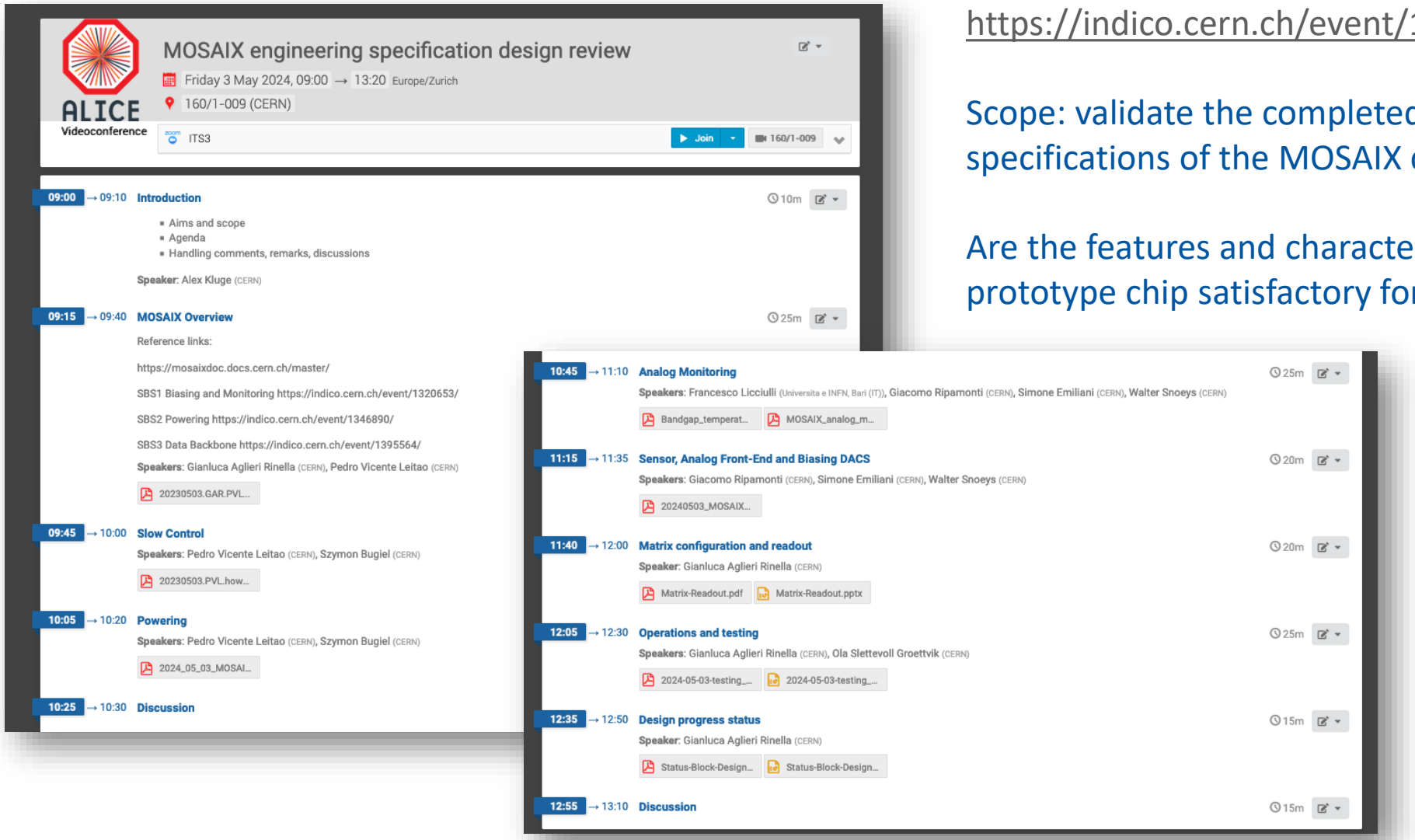
TODO Ramp-up of verification and validation phases of the integrated design

- Functional sims, gate-level annotated models, PEX simulations, Power Integrity, Physical Integrity, …
- Detailed plan to be revamped

Contingency for full completion of the sign-off work and submission end of October exhausted by the delayed completion of block level designs.

SUMMARY OF ENGINEERING DESIGN REVIEW

Summary of Engineering Design Review



https://indico.cern.ch/event/1408655/

Scope: validate the completed and detailed design specifications of the MOSAIX chip.

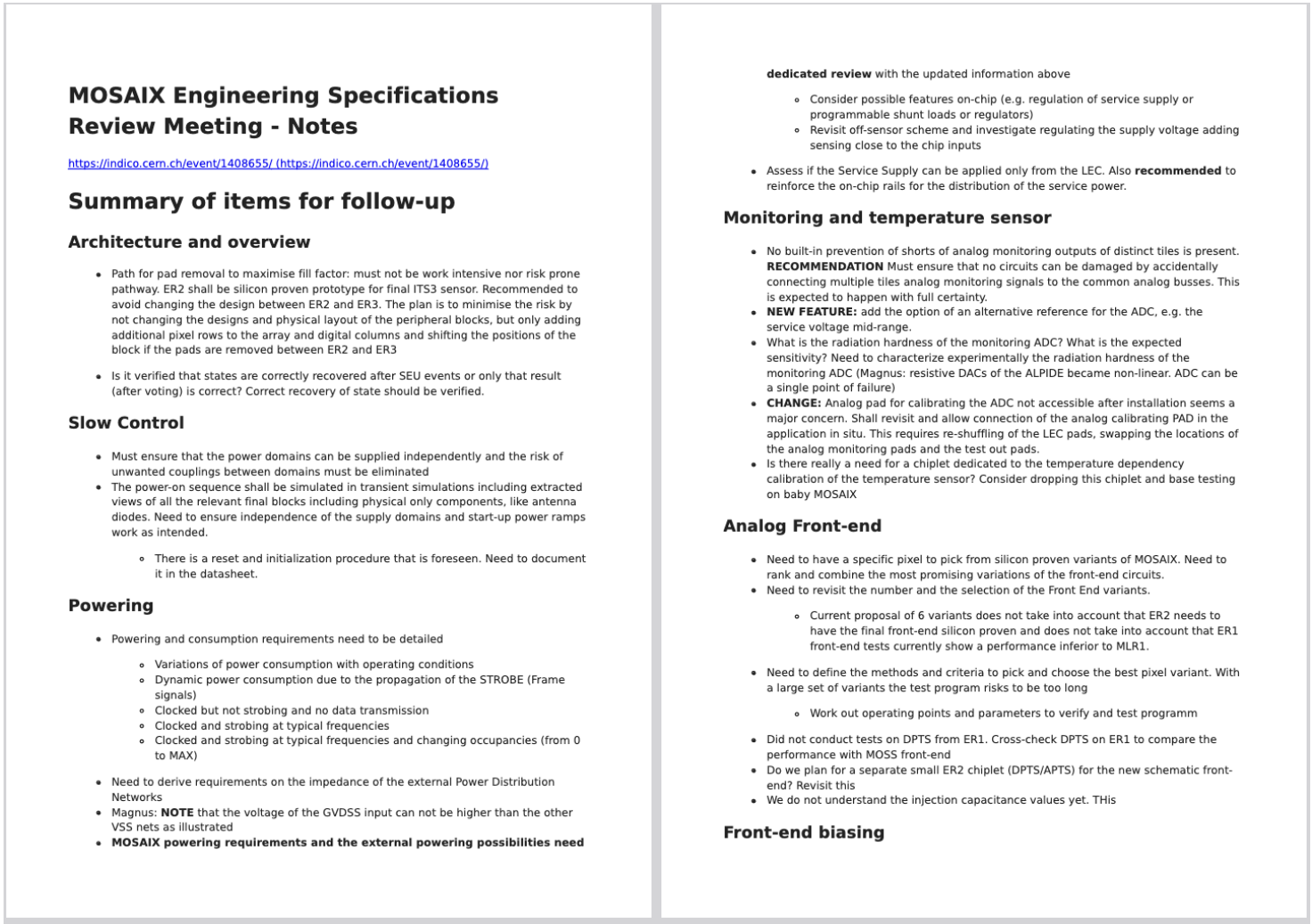
Are the features and characteristics of the MOSAIX prototype chip satisfactory for the ITS3 application?

Review note

Note with questions, answers, discussions, topics, recommendations

12 pages in pdf

2.5 pages summary items



MOSAIX Engineering Specifications Review Meeting - Notes

https://indico.cern.ch/event/1408655/ (https://indico.cern.ch/event/1408655/)

Summary of items for follow-up

Architecture and overview

- Path for pad removal to maximise fill factor: must not be work intensive nor risk prone pathway. ER2 shall be silicon proven prototype for final ITS3 sensor. Recommended to avoid changing the design between ER2 and ER3. The plan is to minimise the risk by not changing the designs and physical layout of the peripheral blocks, but only adding additional pixel rows to the array and digital columns and shifting the positions of the block if the pads are removed between ER2 and ER3
- Is it verified that states are correctly recovered after SEU events or only that result (after voting) is correct? Correct recovery of state should be verified.

Slow Control

- Must ensure that the power domains can be supplied independently and the risk of unwanted couplings between domains must be eliminated
- The power-on sequence shall be simulated in transient simulations including extracted views of all the relevant final blocks including physical only components, like antenna diodes. Need to ensure independence of the supply domains and start-up power ramps work as intended.
    - There is a reset and initialization procedure that is foreseen. Need to document it in the datasheet.

Powering

- Powering and consumption requirements need to be detailed
    - Variations of power consumption with operating conditions
    - Dynamic power consumption due to the propagation of the STROBE (Frame signals)
    - Clocked but not strobing and no data transmission
    - Clocked and strobing at typical frequencies
    - Clocked and strobing at typical frequencies and changing occupancies (from 0 to MAX)
- Need to derive requirements on the impedance of the external Power Distribution Networks
- Magnus: **NOTE** that the voltage of the GVDSS input can not be higher than the other VSS nets as illustrated
- **MOSAIX powering requirements and the external powering possibilities need dedicated review** with the updated information above
    - Consider possible features on-chip (e.g. regulation of service supply or programmable shunt loads or regulators)
    - Revisit off-sensor scheme and investigate regulating the supply voltage adding sensing close to the chip inputs
- Assess if the Service Supply can be applied only from the LEC. Also **recommended** to reinforce the on-chip rails for the distribution of the service power.

Monitoring and temperature sensor

- No built-in prevention of shorts of analog monitoring outputs of distinct tiles is present. **RECOMMENDATION** Must ensure that no circuits can be damaged by accidentally connecting multiple tiles analog monitoring signals to the common analog busses. This is expected to happen with full certainty.
- **NEW FEATURE:** add the option of an alternative reference for the ADC, e.g. the service voltage mid-range.
- What is the radiation hardness of the monitoring ADC? What is the expected sensitivity? Need to characterize experimentally the radiation hardness of the monitoring ADC (Magnus: resistive DACs of the ALPIDE became non-linear. ADC can be a single point of failure)
- **CHANGE:** Analog pad for calibrating the ADC not accessible after installation seems a major concern. Shall revisit and allow connection of the analog calibrating PAD in the application in situ. This requires re-shuffling of the LEC pads, swapping the locations of the analog monitoring pads and the test out pads.
- Is there really a need for a chiplet dedicated to the temperature dependency calibration of the temperature sensor? Consider dropping this chiplet and base testing on baby MOSAIX

Analog Front-end

- Need to have a specific pixel to pick from silicon proven variants of MOSAIX. Need to rank and combine the most promising variations of the front-end circuits.
- Need to revisit the number and the selection of the Front End variants.
    - Current proposal of 6 variants does not take into account that ER2 needs to have the final front-end silicon proven and does not take into account that ER1 front-end tests currently show a performance inferior to MLR1.
- Need to define the methods and criteria to pick and choose the best pixel variant. With a large set of variants the test program risks to be too long
    - Work out operating points and parameters to verify and test programm
- Did not conduct tests on DPTS from ER1. Cross-check DPTS on ER1 to compare the performance with MOSS front-end
- Do we plan for a separate small ER2 chiplet (DPTS/APTS) for the new schematic front-end? Revisit this
- We do not understand the injection capacitance values yet. THis

Front-end biasing

Summary of items for follow-up (1/2)

Challenges of power supply distribution

There are tight requirements on the voltage levels on the supplies. There are significant IR-drops on the flex, on the bonding wires and in the internal pads. Large variations of the supply current are unavoidable.

TODO: modify pads. Improve internal drops + dual bonding per supply pad.

Analog monitoring needed in situ

Direct analog monitoring in the ITS3 application added as system requirement.

DONE: revise locations of analog monitoring pads to enable their connection to the flex.

Variants of pixels and front-end

Intense debate. Up to 12 variants possible in MOSAIX. Strong recommendation: combine most promising variations. Need to pick one variant for the final chip. Need to define how to pick the best.

See the dedicated contribution

Summary of items for follow-up (2/2)

Prepare for shrinking of periphery height and increase matrix fill factor

MOSAIX design will be prepared such to simplify at maximum the adaptations to the possible removal of the auxiliary pads from the long edge.

DONE: floorplan of MOSAIX periphery as if the pads were removed.

Review data transport over on-chip links and SEE effects

Full TMR of the on-chip links unfeasible. Risk of residual SEE effects on data links.

TODO: revisit design sensitivity by simulations and assess the addition of a coding protection layer.

Various recommendations for the verification and sign-off of the design

TODO: Will be included in the detailed sign-off plan and considered in a submission readiness review.

Summary

MOSAIX Sensor Design Status

Complete RSU and REC design with the current metal stack in reach for end of June.

Layout entry effort for Front-End variants estimated of the order of few weeks.

Design of LEC advanced but significant components will not be available (Serializer, Monitoring, I/Os).

Porting of the flow to the PDK for the new metal stack expected in July.

No contingency for full completion of the verification and sign-off work for end of October.

MOSS Testing

Seeing very positive effects of the close exchanges between FE designers and sensor characterization experts.

More and more experimental information is becoming knowledge.