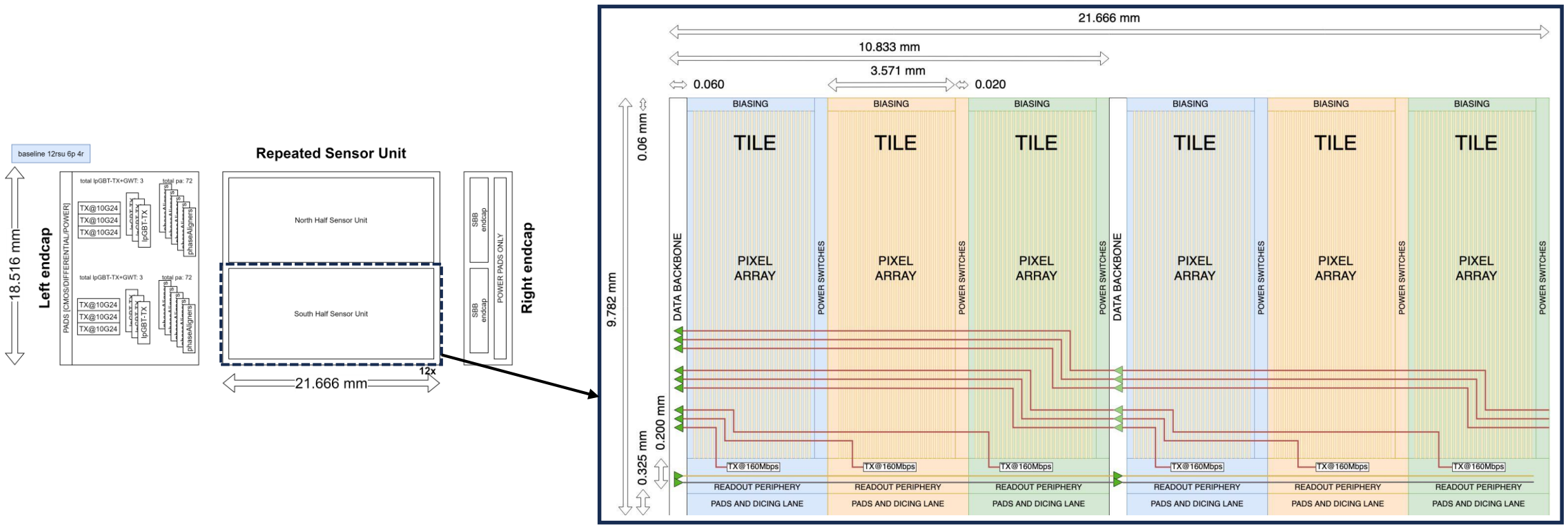
MOSAIX Biasing Unit
Development and Implementation

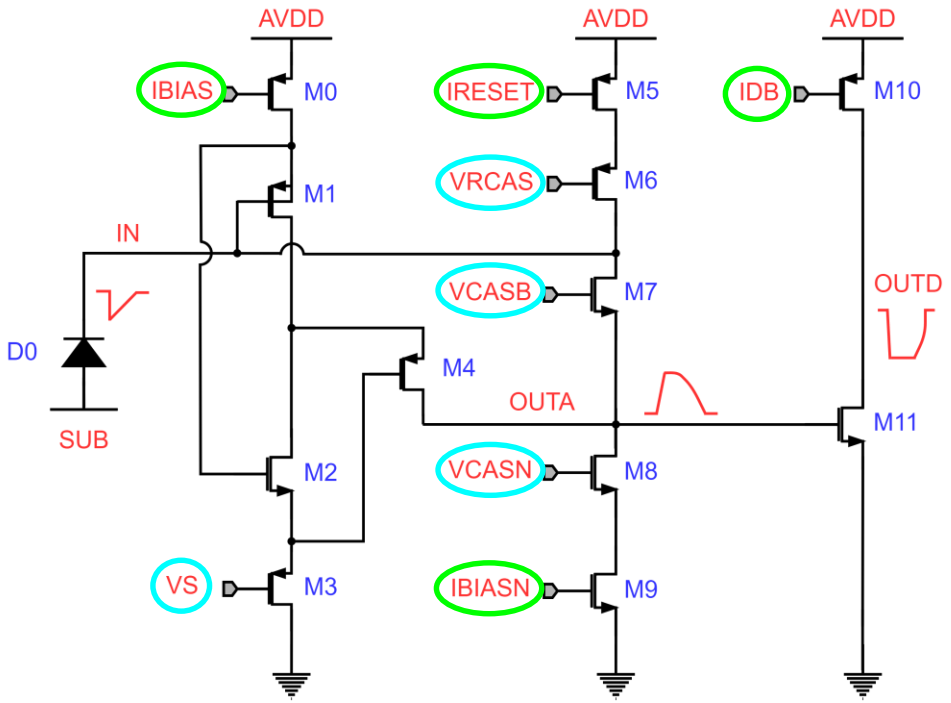
Simone Emiliani, on behalf of the MOSAIX team

18/06/2024

Context - MOSAIX



Overview



FE Current Biases:

- **IBIAS:** first branch bias
- **IRESET:** electrode reset current
- **IDB:** discriminator current
- **IBIASN:** second branch bias

FE Voltage Biases:

- **VS:** tuneable level shifter
- **VRCAS:** cascode of IRESET
- **VCASB:** baseline tuning knob
- **VCASN:** cascode of IBIASN

Pulsing Voltage Biases:

- **VPULSEH:** high level pulsing voltage
- **VPULSEL:** low level pulsing voltage

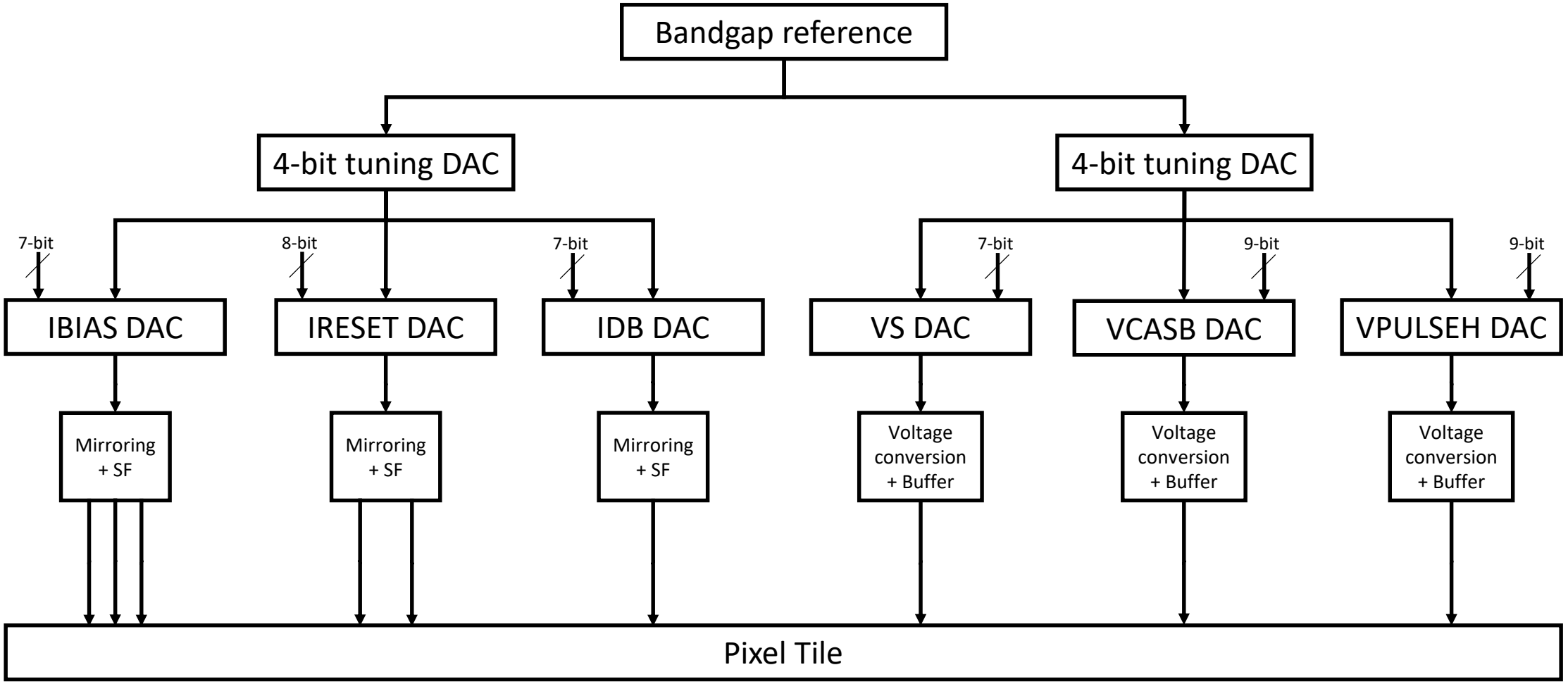
In total, **10** biases lines need to be routed to each pixel
Only **6** DACs are used

Specifications

MOSS specification values are within brackets, where different

	Nominal	Min	Max	LSB	# of bit
IBIAS	25 nA	10 nA	100 nA	0.8 nA [0.4 nA]	7 [8]
IRESET	5 pA	2 pA	127 pA [255 pA] **HighRange** 5 nA [10 nA]	1 pA	7+1 [8+1]
IDB	36 nA	10 nA	250 nA [500 nA]	2 nA	7 [8]
IBIASN	Generated from IBIAS (= IBIAS/10)				
VS	595 mV	10 mV	800 mV	6.25 mV [3.14 mV]	7 [8]
VRCAS	Generated from IRESET				
VCASB	54 mV	10 mV	600 mV	1.17 mV [3.14 mV]	9 [8]
VCASN	Generated from IBIAS				
VPULSEH	-	10 mV	1.2 V	2.34 mV [4.71 mV]	9 [8]
VPULSEL	Tied to LAVSS in the periphery				

General Architecture



Building blocks

- Bandgap (+ Temperature sensor)
  - Evolution of the NIKHEF MLR1/ER1 bandgap developed by Giacomo
  - Auto start-up, improved mismatch, back-bias compatibility, re-layout
  - Temperature sensor added
- 4-bit bandgap tuning DAC
  - Adapted from MOSS to withstand back-bias
- Biasing DACs (7 and 9 bits)
  - Developed at IPCH (Andrei, Isabelle, Xiaochao) on the basis of MOSS DACs
- Mirroring stages with source follower for leakage compensation
  - New design to compensate for matrix gate leakage
- Voltage buffer
  - New design (Giacomo, Andrei, Isabelle) to save area and power
- Local monitoring circuitry
  - Designed by Francesco (INFN Bari)
  - All the biases, bandgap outputs and local supplies (analog and digital) can be monitored
  - Read-out by means of an ADC placed in the left endcap

Biasing Unit Development Summary

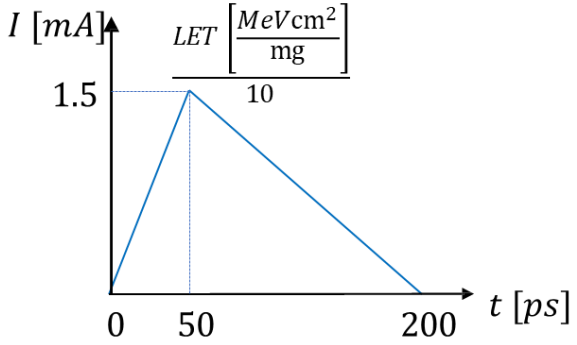
From MOSS to MOSAIX:

- Large reduction of area (from 4050x260 μm^2 to 3500x60 μm^2)
  - To increase sensitive area
- Large reduction of current consumption (from ~700 µA to ~250 µA)
- Removal of PSUB isolation (~30 µm more saved)
  - To increase sensitive area
  - To ease the integration
- Bandgap auto-startup implemented
- Improved VCASB and VPULSEH tunability
  - To ensure better threshold adjustment and characterization of the front-end
- IBIASN and VCASN internally generated, not connected to DACs anymore
  - To reduce the complexity in finding an operating point of the front-end
  - To reduce biasing area
- Temperature and strain monitor included
- Single Event Effects simulated and mitigated with RC filters

Simulation of single event injection

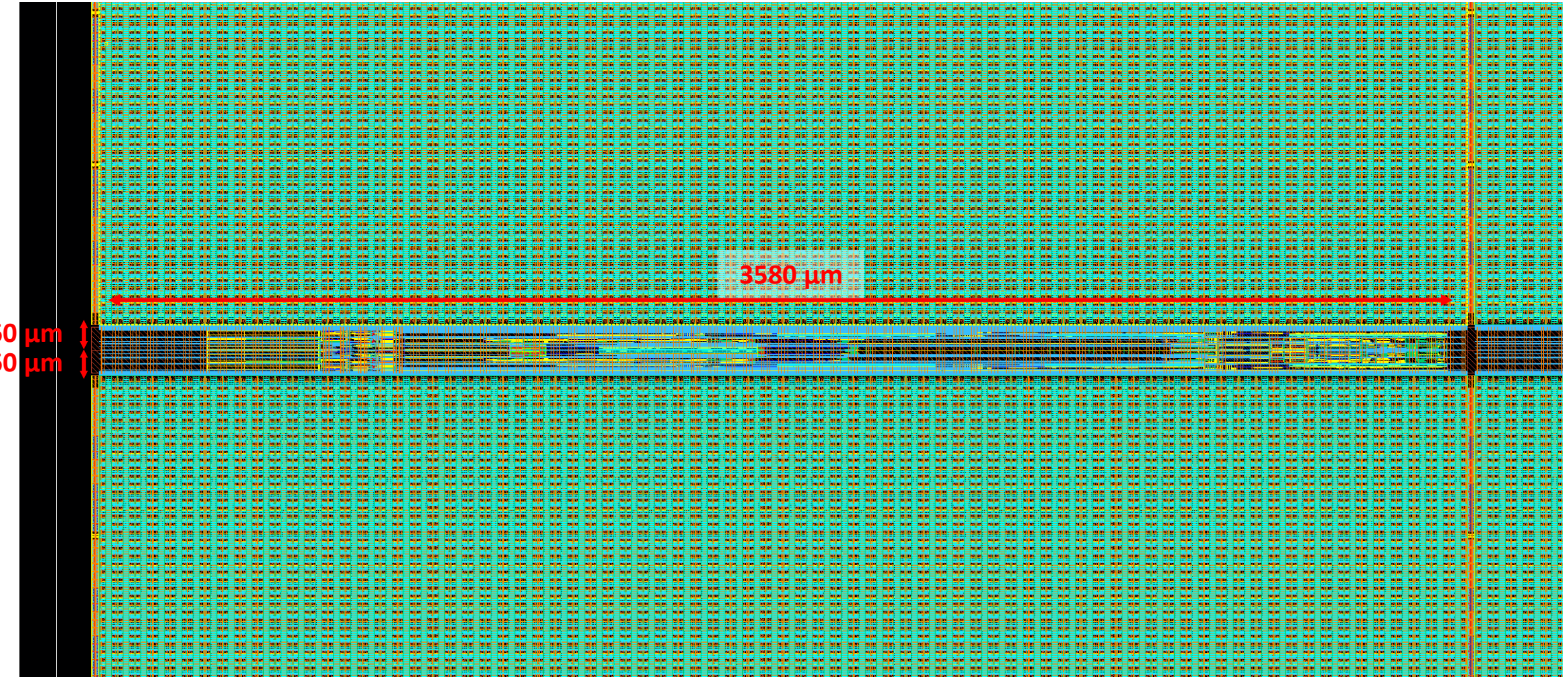
A systematic simulation approach is adopted to improve the robustness of the biasing unit to SEE

- A current pulse is injected in all sensitive nodes (drains of NMOS and PMOS) of the biasing unit, corresponding to $LET = 15 \frac{MeVcm^2}{mg}$ (maximum LET due to recoil of Si ions)



- The used testbench includes the biasing unit and a model of the pixel matrix
- Harmful events are the ones making the full pixel matrix switch
- RC filters are added to the design of the biasing unit (especially on the VS bias) to filter out harmful events

Top view

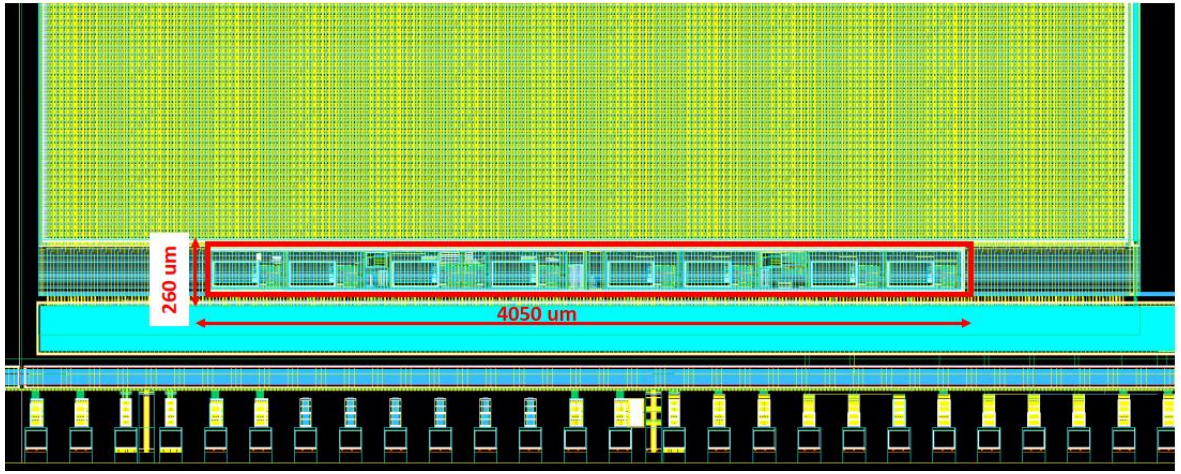


Thank you

BACK-UP

MOSS biasing (F. Loddo)

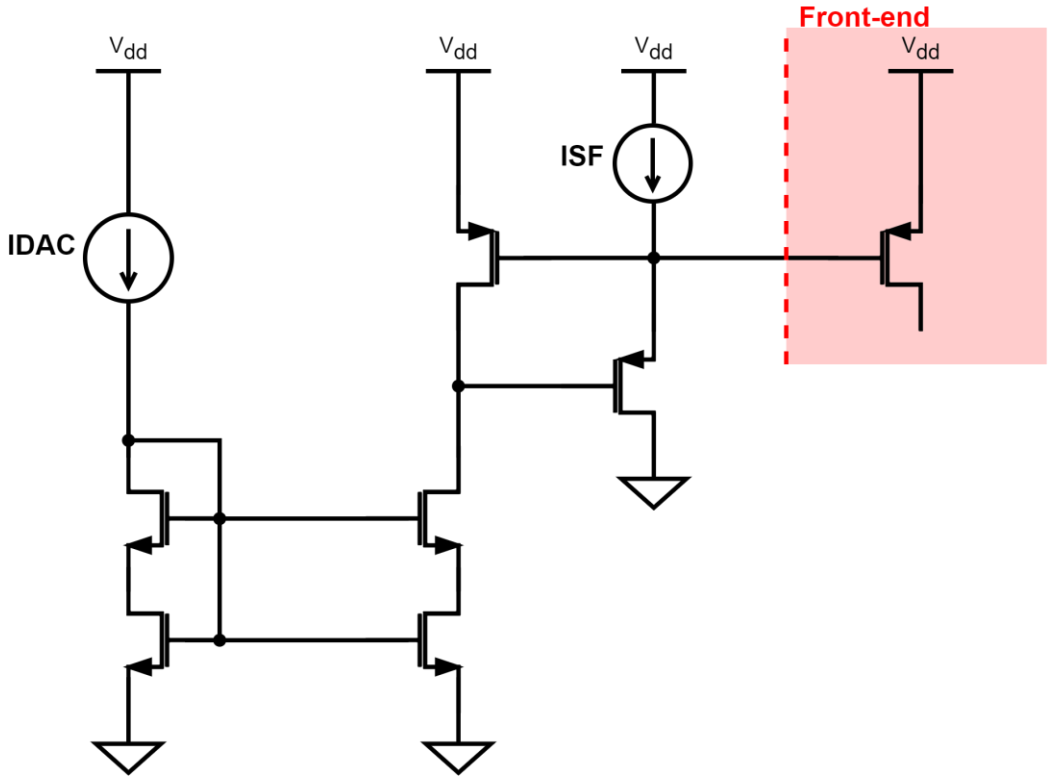
- Designed to be highly programmable and robust
- No constraints in terms of area and power



- Each unit serves one MOSS submatrix, that means 1/4 of half (top or bottom) sensor unit
- It is completely self-standing
- It includes 2 bandgaps, 8 8-bit DACs and 10 R2R buffers
- Current consumption ~700 µA

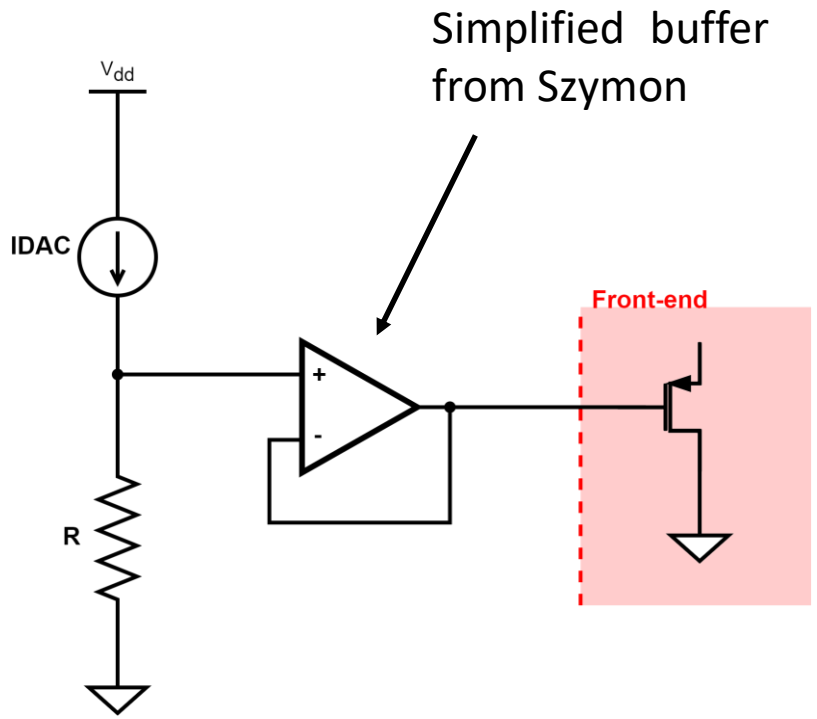
This biasing unit is isolated from the substrate by means of a deep n-well (~30 µm height penalty).

Current mirroring example



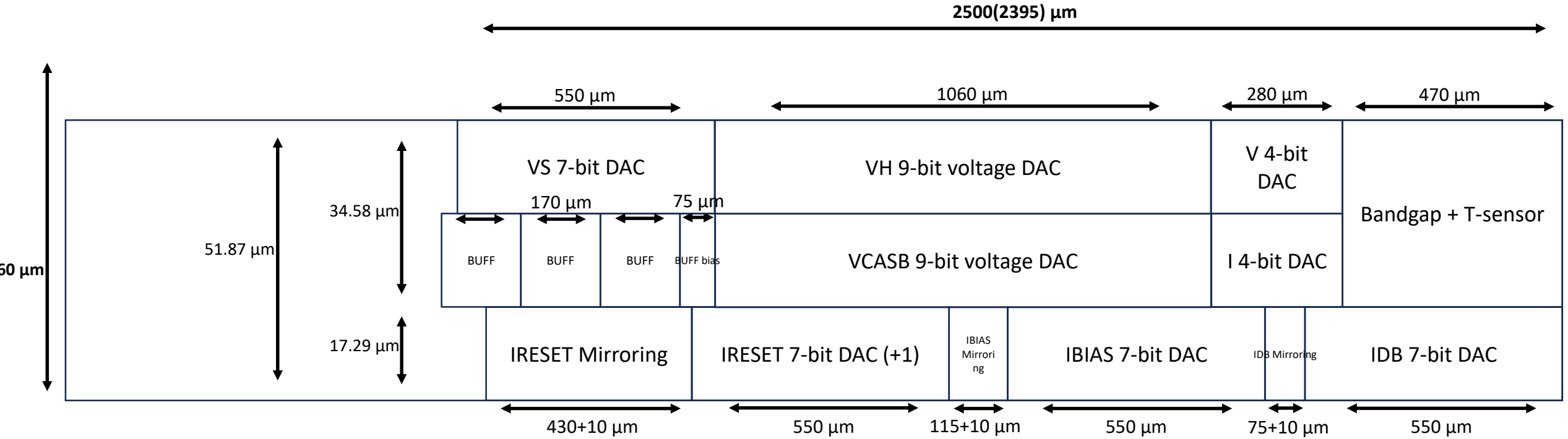
- Scaling factors are:
  - 50 for IBIAS
  - 20 for IDB
  - 40000 for IRESET
- IRESET scheme is slightly different to generate VRCAS and to implement the high range
- The source follower compensates for the gate leakage on the biasing line
- ISF is set at 10 µA, i.e. 10x the worst-case leakage current
- The nMOS loading the DACs have the same dimensions for the three biases
- Transistors are sized to have the performance limited by the last mirror
- Corners simulations were run to check stability of the loops (**phase margin > 57°**)
- It works without substrate isolation

Voltage conversion (Voltage DACs)



- VS
  - Range: 0 – 800 mV
  - 7-bit (~ 6.25 mV resolution)
  - R = 800 mV / 5.08 µA = 157.48 kΩ
- VCASB
  - Range: 0 – 600 mV
  - 9-bit (~ 1.17 mV resolution)
  - R = 600 mV / 20.44 µA = 29.35 kΩ
- VH
  - Range: 0 – 1.2 V
  - 9-bit (~ 2.34 mV resolution)
  - R = 600 mV / 20.44 µA = 29.35 kΩ (implementing **x2** gain)

Floorplan (assuming the matrix at the bottom)

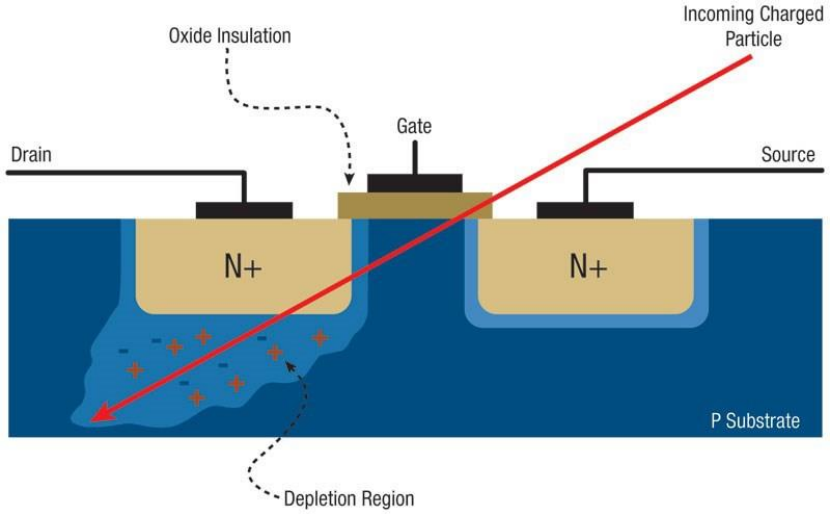


4bit DAC is only ~140µm. 280µm includes the output mirroring

Tile width 3580.8 µm

Courtesy of Giacomo Ripamonti

SEE Physical mechanism



Electron-hole pairs are generated by incoming particles in the depletion region of pn junctions. The single-event-generated charge track can extend the junction electric field away from the junction itself, such that charge deposited some distance from the junction can be collected through drift [1].

Electrons are collected by the node at the higher potential (e.g. by n+ implants in NMOS)

Holes are collected by the node at the lower potential (e.g. by p+ implants in PMOS)

The higher the impedance of the victim node is, the higher is the impact of the injection on the node voltage.

[1] P. E. Dodd, L. W. Massengill, Basic Mechanisms and Modeling of Single-Event Upset in Digital Microelectronics, IEEE Transactions on Nuclear Science, June 2003

Linear Energy Transfer

Linear Energy Transfer (LET) is the amount of energy released by the incoming particle per unit distance. Its value in $\frac{MeV}{cm}$ is often normalized by the target material density (for Silicon, $\rho = 2.33\ \frac{g}{cm^3}$) and expressed in $\frac{MeV \cdot cm^2}{mg}$.

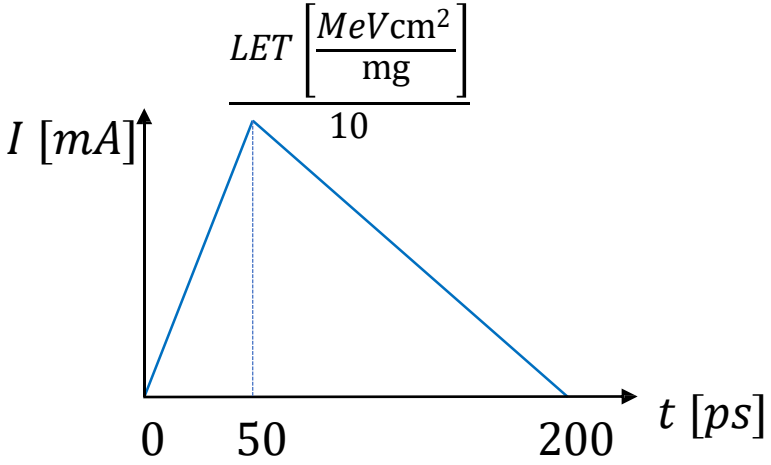
In the LHC detectors, typical recoils of Si ions can produce events with a LET of $\approx 15\ \frac{MeV \cdot cm^2}{mg}$ [2]. The worst-case event (although rarer than Si recoils) can be a recoil of tungsten ions (tungsten is used for the contacts from silicon to M1), producing events with a LET of $\approx 40\ \frac{MeV \cdot cm^2}{mg}$.

[2] F. Faccio, M Huthinen, Computational method to estimate Single Event Upset rates in an accelerator environment, https://lhcb-elec.web.cern.ch/papers/seu_cms.pdf

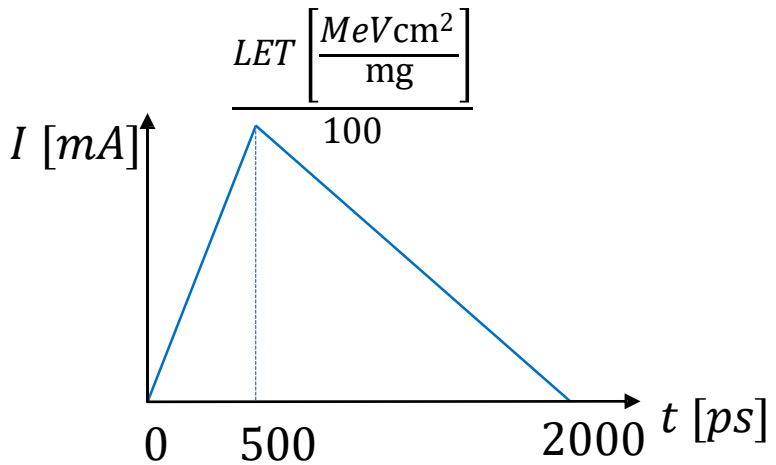
Correspondence between LET and injected charge

Assuming that the charge collected by the victim node is generated not further than 1 μm away from the junction [2], it can be calculated that the total charge collected by the node for a LET of 1 $\frac{MeV \cdot cm^2}{mg}$ is 10 fC.

Such charge can be injected using a current source in simulations. The current profiles that I typically use in simulations are the following:



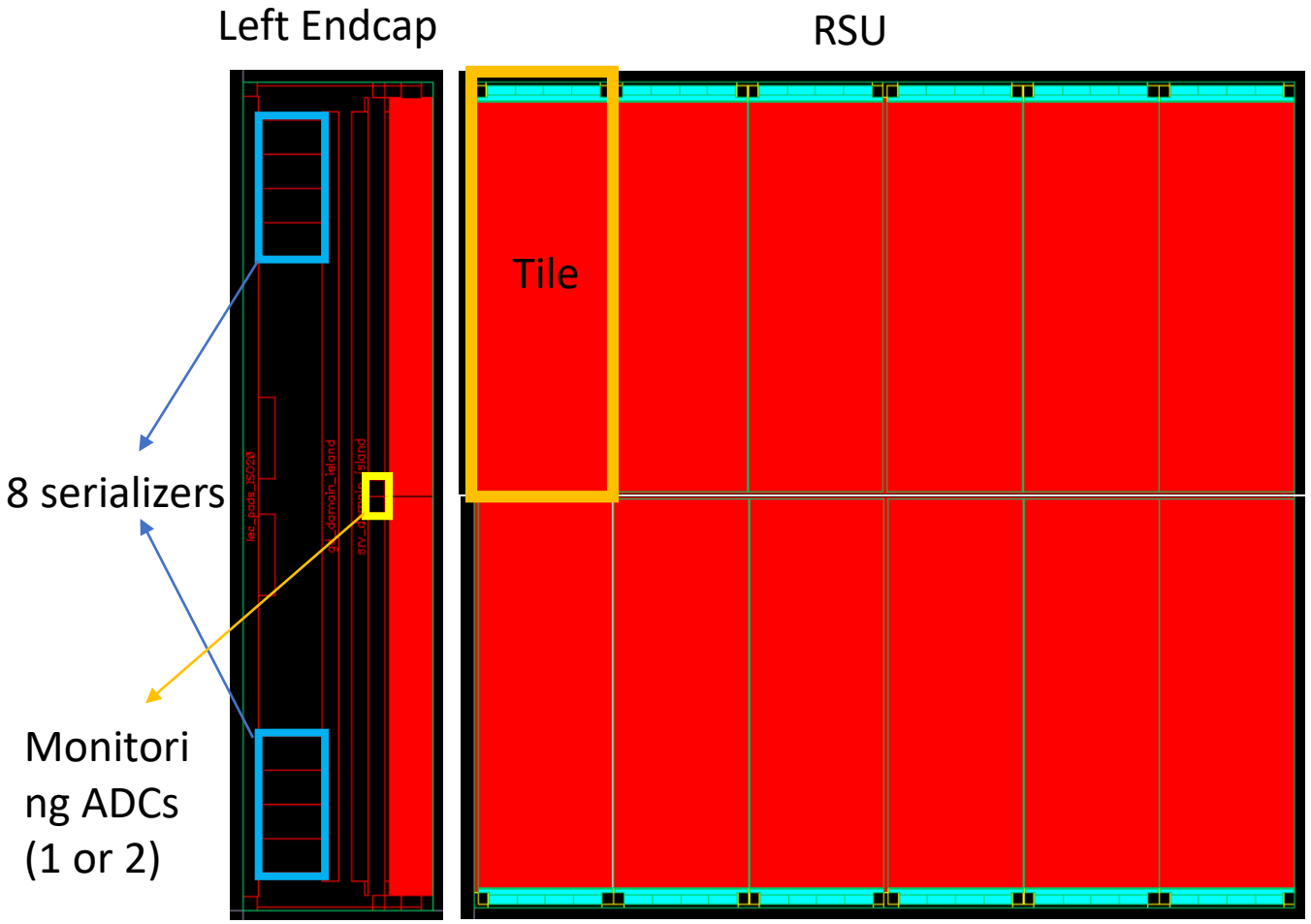
1. “Fast” injection



2. “Slow” injection

[2] F. Faccio, M Huthinen, Computational method to estimate Single Event Upset rates in an accelerator environment, https://lhcb-elec.web.cern.ch/papers/seu_cms.pdf

Bandgap references in MOSAIX



In MOSAIX, bandgap reference circuits will be used:

- In each serializer (8 bandgaps/segment)
- In the monitoring ADC(s) (1 bandgap/segment)
- In each tile (144 bandgaps/segment)

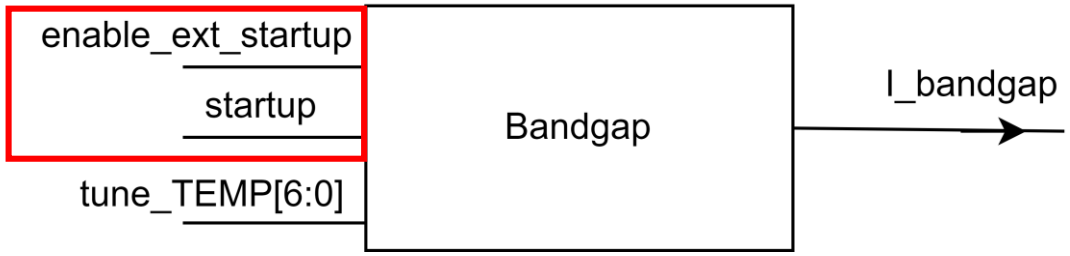
The configuration code to guarantee a temperature-independent output and the startup circuit are the same for all bandgaps.

Bandgap – startup

A dedicated circuit to guarantee the automatic startup of the bandgap has been included in the MOSAIX bandgap (this feature was not present in the MOSS bandgap).

In case of failure of the automatic startup, it is still possible to force the startup using an external pulse. The manual startup procedure is the following:

1. Set the “enable_ext_startup” input of the tile bandgap to 1.
2. Send a pulse on the “startup” input of the tile bandgap (set “startup” to 1 and then to 0, pulse duration specifications as in MOSS).



Bandgap – temperature calibration

The bandgap reference circuit must provide a temperature-independent output voltage/current.

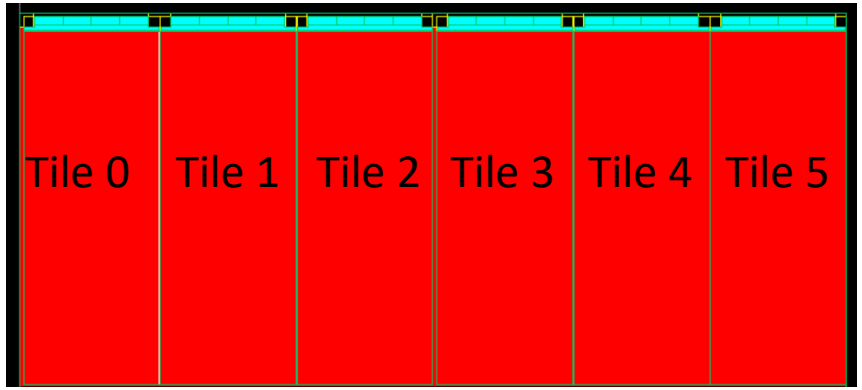
7 calibration bits (tune_TEMP[6:0]) are used to adjust the temperature slope of the bandgap output. The same code for these 7 bits will be provided for all bandgaps.

The default value of these 7 bits is set according to simulation results and to measurements on the MLR1 bandgap test-chip.

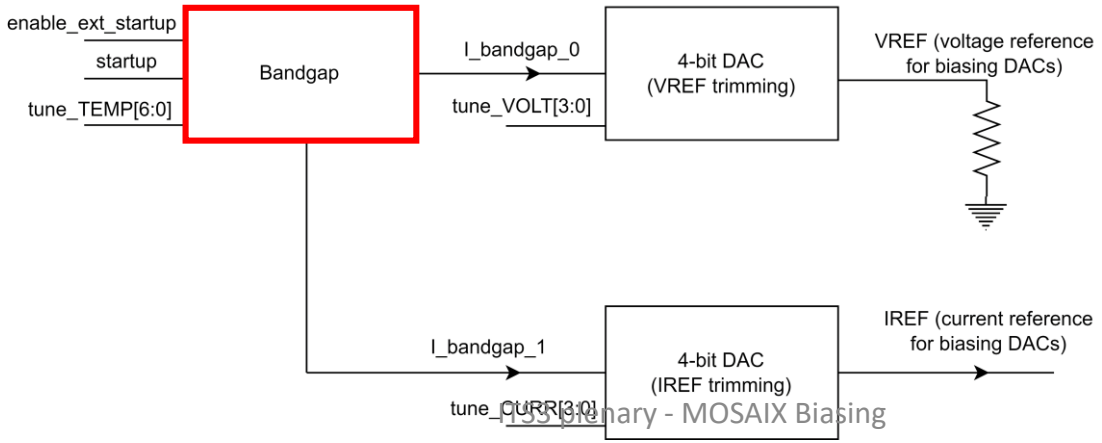
A dedicated test-chip will be designed and measured to characterize the temperature behavior of the MOSAIX bandgap and find the final code for these 7 bits.

Tile bandgap

Half RSU



Each tile hosts a bandgap reference circuit, which provides the reference voltage and current for the biasing DACs.



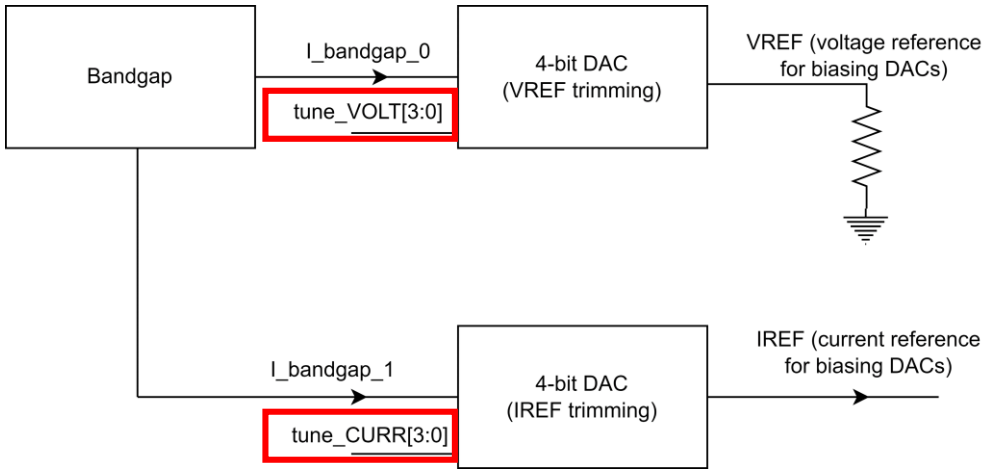
Tile bandgap – offset calibration

Each bandgap will show a different absolute value of its output voltage/current due to mismatch.

Thus, in order to guarantee that the correct resolution and range of the DACs are achieved, the absolute value of the output of each bandgap circuit must be calibrated before exercising any biasing DAC. This calibration must be done tile by tile. As in MOSS, there are two 4-bit trimming DAC to respectively trim the bandgap voltage and the bandgap current.

Calibration procedure for the tile bandgap:

1. Monitor the tile voltage reference VREF and AVSS (local analog VSS), and trim the associated 4-bit voltage trimming DAC (tune_VOLT[3:0] bits) to set VREF-AVSS as close as possible to 188mV
2. Monitor the tile current reference IREF, and trim the associated 4-bit current trimming DAC (tune_CURR[3:0] bits) to set IREF as close as possible to 640nA



Tile temperature sensor

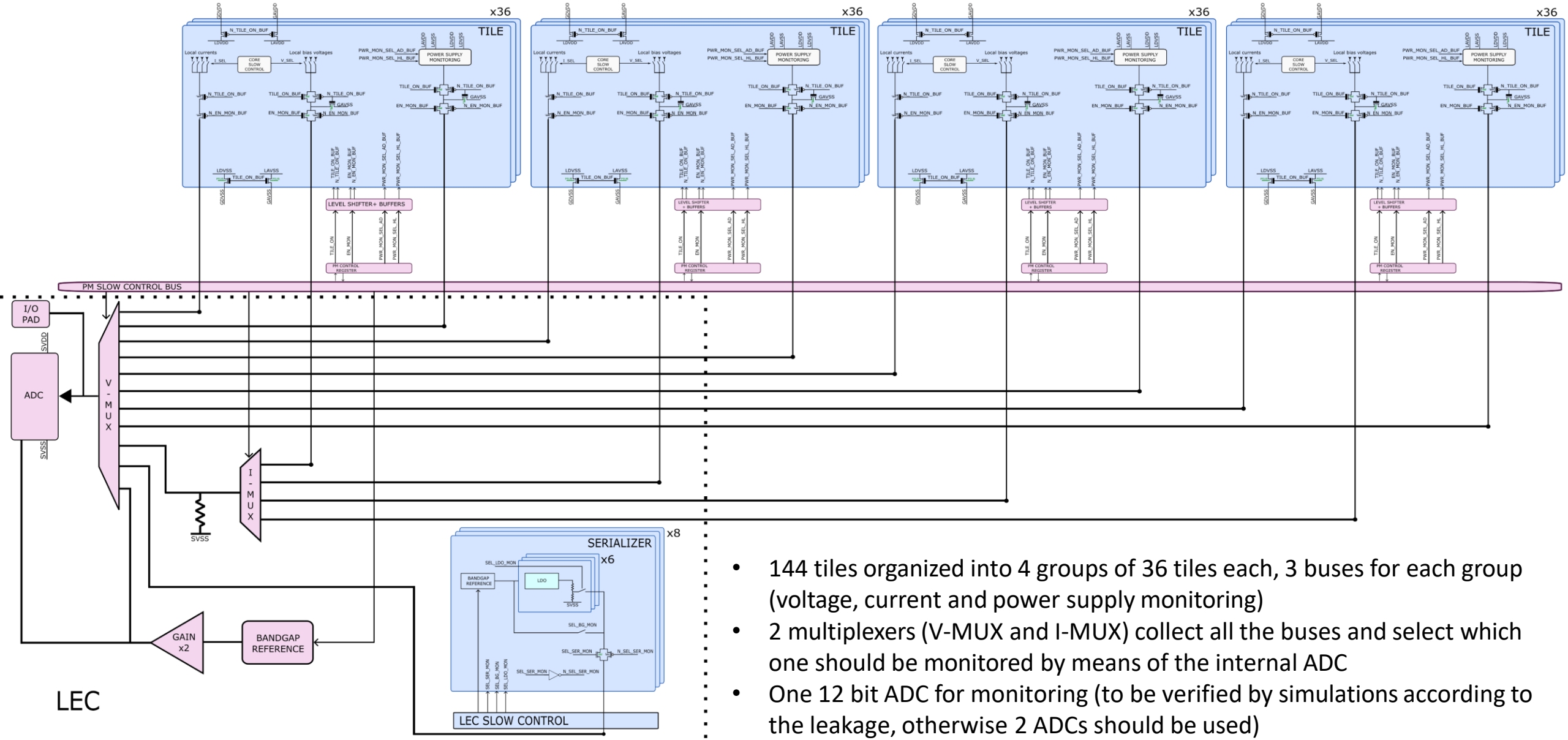
In MOSAIX, each tile will be equipped with a temperature sensor.
The correct functionality of the temperature sensor is guaranteed only after the calibration of the bandgap.

A dedicated test-chip will be designed to characterize the temperature sensor.
4 configuration bits are used to determine the gain (mV/degree) and voltage range of the temperature sensor output. Their final value will be determined after the characterization of the test-chip, and it will be common for all tiles.
With the default values of these bits foreseen for MOSAIX, the simulated gain of the temperature sensor is 4.8 mV/degree.

Mismatch variations will cause each temperature sensor to show a different output voltage for the same temperature. 5 bits can be used to calibrate such offset to equalize the temperature sensor output in all tiles.
Calibration procedure to be done for each tile:
- At room temperature, monitor the temperature sensor output voltage and adjust the 5 offset calibration bits to set the measured output voltage as close as possible to 350mV.

MOSAIX monitoring: architecture

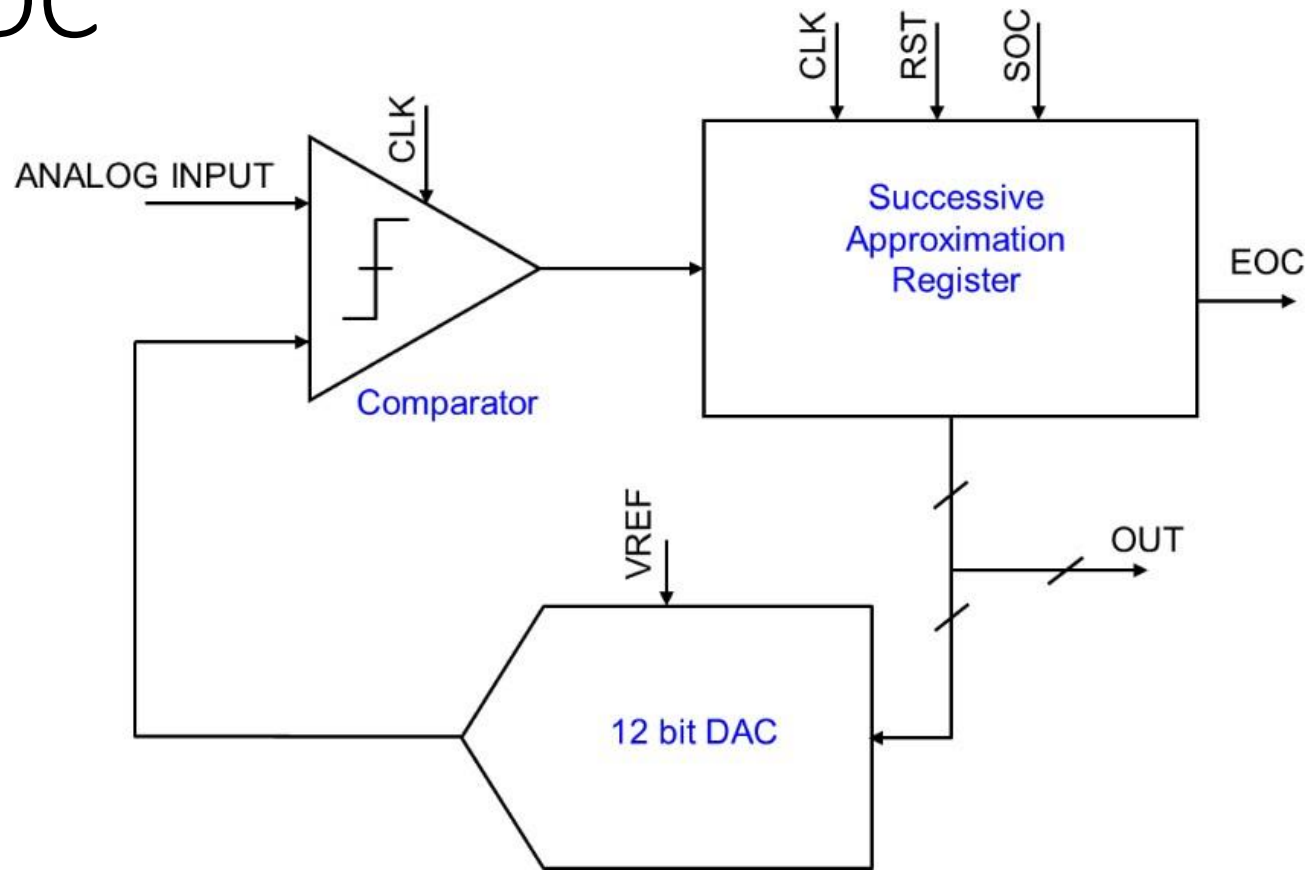
Courtesy of Francesco Licciulli



- 144 tiles organized into 4 groups of 36 tiles each, 3 buses for each group (voltage, current and power supply monitoring)
- 2 multiplexers (V-MUX and I-MUX) collect all the buses and select which one should be monitored by means of the internal ADC
- One 12 bit ADC for monitoring (to be verified by simulations according to the leakage, otherwise 2 ADCs should be used)
- One input pad for ADC calibration and monitoring resistor measurement

MOSAIX monitoring: ADC

Courtesy of Francesco Licciulli



- Resolution: 12 bits
- SAR architecture
- Area about 530 x 240 um2
- Current absorption 20 uA

Analog inputs:

- Input to be converted;
- Vref: 0.9 V generated from bandgap;

Digital Inputs:

- Reset,
- Start of conversion,
- Clock: input clock at 40 MHz, internal scaling factor 1024 -> 39 kHz internal clock,
- 6 bits for calibration (to compensate non linearities due to parasitics in capacitive DAC)

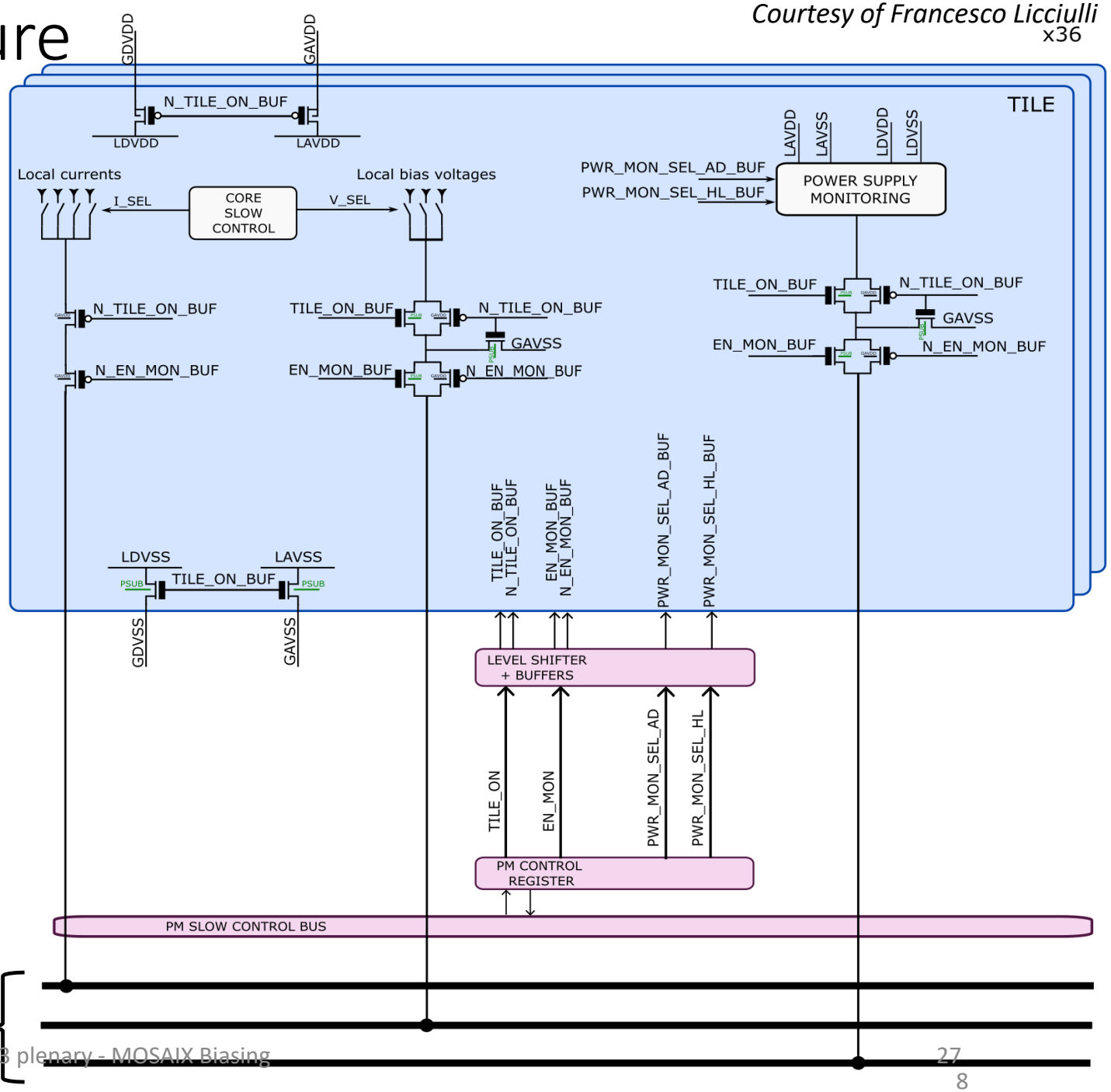
Digital Outputs:

- 12 bit output for conversion
- End of conversion

Tile Monitoring: Architecture

Courtesy of Francesco Licciulli

- 3 common buses for 36 tiles
  - Current monitoring
  - Voltage monitoring
  - Tile power supply monitoring
- One cross-domain switch for each monitoring bus made of two switches in series:
  - Both switches are controlled by the service
  - One switch is controlled by the tile on signal
  - One switch is controlled by the monitoring signal
- Current and voltage monitoring selection is controlled by tile periphery slow control
- Power supply monitoring is controlled by the service, tile power supplies can be monitored also if the periphery does not work



Courtesy of Francesco Licciulli

Tile Monitoring: current and voltage reference list

- **Current references:**
  - IREF: reference current for bias generation
  - IBIAS: pixel bias current (24x scaled copy)
  - IRESET: pixel reset current (20000x scaled copy)
  - IDB: pixel discriminator current (10x scaled copy)
  - ITSENS: temperature sensor current
  - ISTRAIN: strain monitoring current (equal to IBIAS, 24x scaled copy)
- **Voltage references:**
  - VREF: reference voltage for bias generation
  - VCASB: cascode first stage
  - VPULSEH: calibration pulse high level (1 programming bit to choose the monitoring gain 1 or 0.5)
  - VS: electrical NWELL DC shift

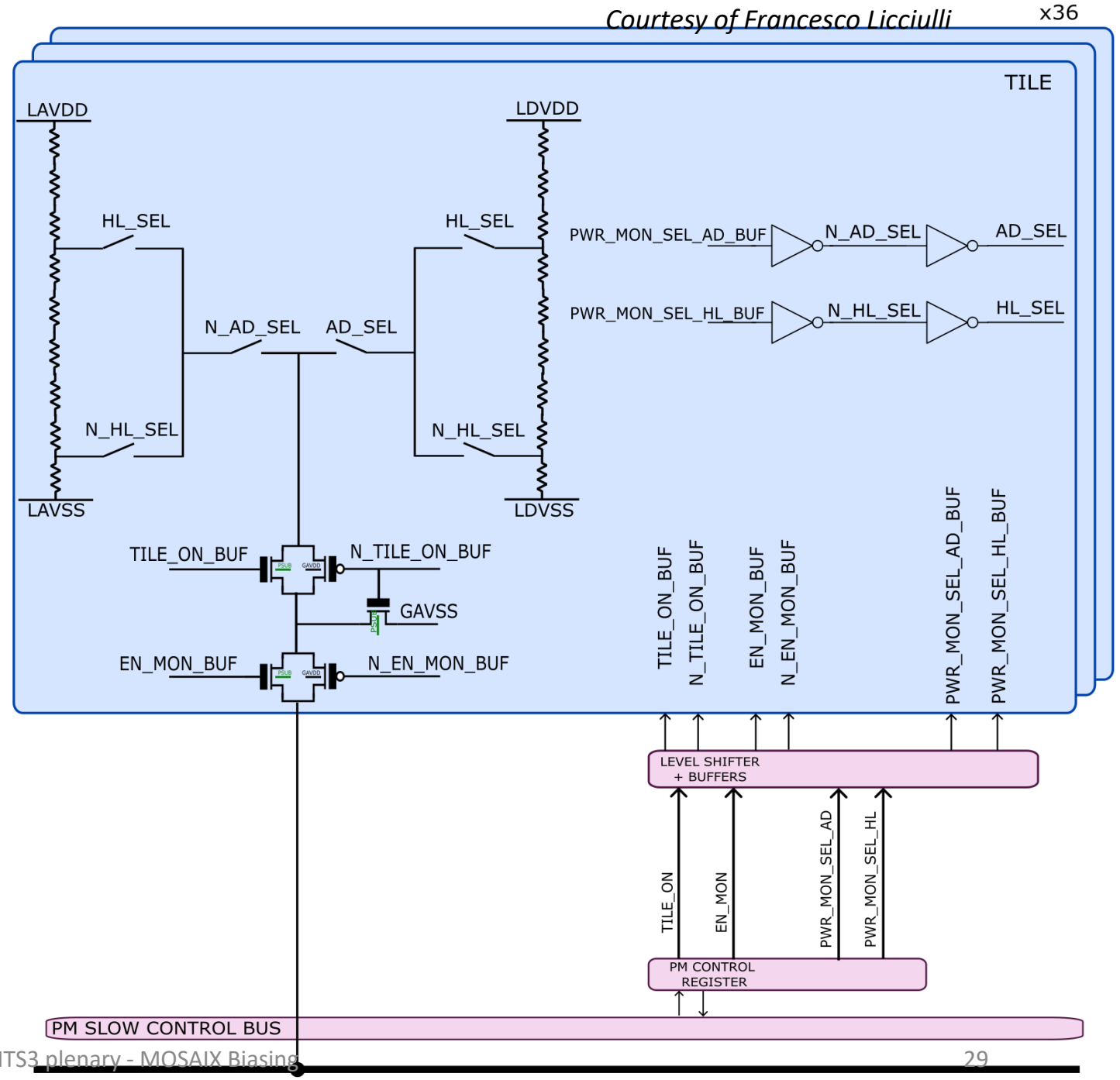
- For each reference a control bit for selection is provided, in total 10 bits for selection + 1 for VPULSEH monitoring gain.

Tile Monitoring: local power supplies

- Two resistor voltage dividers: one for analog domain and one for digital
- Each divider provides two output voltages
- By means of the two output voltages it's possible to indirectly measure VDD and VSS
- Totally controlled by service

Control bits:

- PWR_MON_SEL_AD:
  - 0 -> analog supply
  - 1 -> digital supply
- PWR_MON_SEL_HL:
  - 0 -> low voltage
  - 1 -> high voltage



Tile Monitoring: specs

Courtesy of Francesco Licciulli

	Nominal	Min	Max	LSB	# of bit
IBIAS	25 nA	10 nA	100 nA	0.8 nA	7
IRESET	5 pA	2 pA	127 pA (5 nA)	1 pA	7+1 (high range)
IDB	36 nA	10 nA	250 nA	2 nA	7
IBIASN	Generated from IBIAS (= IBIAS/10)				
VS	600 mV	10 mV	800 mV	7 mV	7
VRCAS	Generated from IRESET				
VCASB	54 mV	10 mV	600 mV	1.2 mV	9
VCASN	Generated from IBIAS				
VPULSEH	-	10 mV	1.2 V	2.4 mV	9
VPULSEL	Tied to AVSS				

ADC specs:

- ADC resolution: 12 bits
- ADC reference = 900 mV
- ADC LSB = 220 uV

Voltage monitoring:

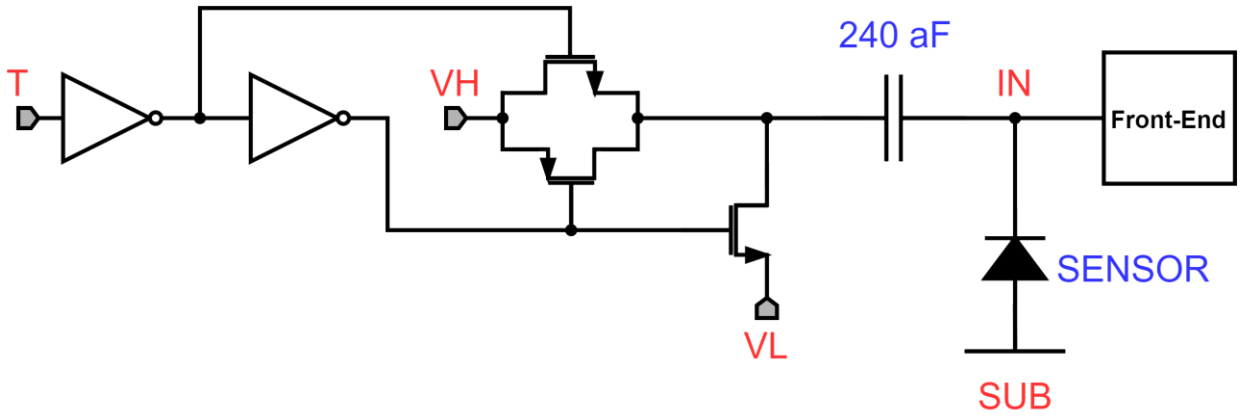
- VS and VCASB monitored without partitioning
- VPULSEH programmable partitioning 1 or ½
- Power supply monitoring: two output voltages 1/9 and 6/9 of VDD - VSS

Current monitoring:

- Current is converted directly on a resistor of 300 kΩ

	Scaling factor	LSB after scaling	Mirror - Max output current	LSB (@ ADC input)	ADC LSB @ bias	Vmax (@ ADC input)
IBIAS	24	19.2 nA	2.4 uA	5.76 mV	30.6 pA	720 mV
ISTRAIN	24	19.2 nA	2.4 uA	5.76 mV	30.6 pA	720 mV
IDB	10	20 nA	2.54 uA	6 mV	69 pA	750 mV
IRESET (low range)	20000	20 nA	2.54 uA	6 mV	35 fA	762 mV
IRESET (high range)	500	20 nA	2.54 uA	6.4 mV	1.4 pA	750 mV
Iref (4 bit DAC)	1	25 nA	825 nA	7.5 mV	73 pA	247.5 mV

Analog Pulsing Schematic



- Injected charge tuneable with (VH-VL) voltage
- Maximum injectable charge is 1.2V x 240aF = 1800e- (to include with some margin the k_α iron peak)
- ΔV = 1mV ⇔ Qinj = 1.5e-

Update 19/01/2024 (version 10 layout on SOS)

- Cinj increased to 280aF to be more conservative wrt VH ($Q_{1.2V}$ = 2100e-, $Q_{1.08V}$ = 1890e-).
- ΔV = 1mV ⇔ Qinj = 1.75e-
- QLSB = 4.2e-