CONTENTS

FULLY SYMMETRICAL OTA DESIGN

The OTA with symmetrical or balanced topology is implemented in bio-potential detection system because of larger transconductance, larger slew rate and larger gain bandwidth (GBW) produced during operation of the OTA. The design of circuit is constructed from several current mirrors which acting as active load to each other. Symmetrical OTA is also called as three current mirrors OTA where the differential input pair consists of two NMOS transistors. There are self-biased inverters and three simple current mirrors adopted to bias the inverters in the circuit.

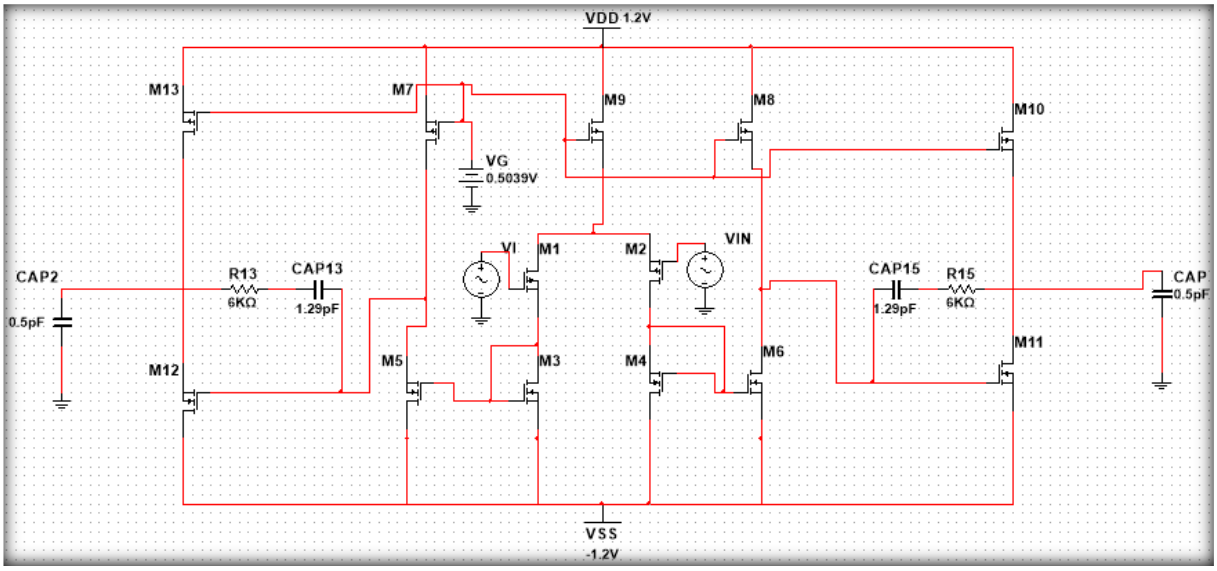
CONDITIONS

Groups-16,18,20,22,24,26,28 Fully Symmetrical OTA Design		
Sample Circuit: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=5533393		
Design Specifications and Constraints		
Technology node: 130nm	DC Gain>80dB	CMRR>100dB
Power Supply: ±1.2V	f_t>20MHz	PSRR>70dB
0.12µm<L<6µm	PM>50°	SR>20µV/s
0.16µm<W<150µm	Power<1500µW	Input Offset<5mV
Current Source: Symmetrical Basic Current Mirror	Area<500μ^2m	C_{load}=0.5pF

RESULTS

GAIN	78.277 dB (Right) 78.277 dB(Left)
PHASE MARGIN	51.713 ° (Right) 54.14 ° (Left)
ft	30.292MHz(Right) 28.893MHz(Left)
Power	1.36 mW
AREA	2,524.82 u^2m
CMRR	41.148 dB
PSRR	39.054 dB
SR	49.197 V/us
Input Offset	0.013 mV

CIRCUIT SHEMATIC



We removed the diode connector to see same value from outputs, connected the above PMOS to each other and gave a common voltage.

First, we simulated one mosfet. Our uncox and upcox values came to 380 uA/V^2 and 80uA/V^2. Using this parameters we basically calculated W/L ratio and current value. The working conditions of the 13 mosfets we used came as it should. In determining the ratio of W and L, we considered the B value.

CODE

```
SAMPLE CİRCUİT*
.INC 130nm.txt
  M9 3 2 1 1     PFET W=48.72u  L=4.5u
  M7 12 2 1 1     PFET W=73.28u    L=4.5u
  M8 8 2 1 1     PFET   W=73.28u    L=4.5u
  M1 6 4 3 3     PFET W=24.36u     L=4.5u
  M2 7 5 3 3     PFET W=24.36u     L=4.5u
  M3 6 6 10 10    NFET W=12.18u   L=4.5u
  M4 7 7 10 10     NFET W=12.18u L=4.5u
  M5 12 6 10 10     NFET W=36.54u   L=4.5u
  M6 8 7 10 10     NFET W=36.54u L=4.5u
  M10 15 2 1 1     PFET   W=73.28u   L=4.5u
  M11  15 8 10 10     NFET W=36.54u    L=4.5u
  M12  13 12 10 10     NFET W=36.54u L=4.5u
  M13  13 2 1 1       PFET  W=73.28u  L=4.5u


VDD 1 GND 1.2
VG 2 GND 0.5039
VIN 4 GND 0 AC 0
VI  GND 5 0 AC 1

R1 16 15 6K
R2 14 13 6K
CAP15 8 16 1.29p
CAP13 12 14 1.29p


CAP 15 GND 0.5p
CAP2 13 GND 0.5p
vss gnd 10 1.2
.tran 1u 1m
.option post
.OP
.ac dec 10 1 3000000000
.END
```

We were unable to provide the area condition to get the best result. In order to prevent oscillation in the circuit, we added external resistor and capacitor.

We have seen that when we increased capacitor value , phase margin increased but bandwidth and gain decreased according to the capacior value.

We have seen that beta values give better results in 3 and 5 value ranges according to our research. We have seen the best results in our circuit with a value of 2.7.

$$B = \frac{(W/L)_5}{(W/L)_3} = \frac{(W/L)_6}{(W/L)_4}$$

LISTING FILE

Node	Voltage
1	1.2
2	0.5039
3	0.693696
4	0
5	0
6	-0.723402
7	-0.723402
8	-0.728551
10	-1.2
12	-0.728551
13	-0.0551679
14	-0.0551679
15	-0.0551679
16	-0.0551679

In order to obtain a healthy result, we tried to make the voltage at the output nodes DC 0. Output nodes are 15 and 13.

Element	VSS	VG	VDD	VIN
volts	1.2000e+000	5.0390e-001	1.2000e+000	0.0000e+000
current	-5.6808e-004	8.7259e-016	-5.6808e-004	-2.9705e-016
power	6.8170e-004	-4.3970e-016	6.8170e-004	0.0000e+000

Power consumption is 1.36 mW.

Element	M4	M9	M3	M1
Model Name	NFET	PFET	NFET	PFET
region	Saturation	Cutoff	Saturation	Cutoff
id	4.0044e-005	-8.0088e-005	4.0044e-005	-4.0044e-005
ibs	0.0000e+000	-0.0000e+000	0.0000e+000	-0.0000e+000
ibd	-1.9451e-016	9.9670e-017	-1.9451e-016	5.0085e-017
vgs	4.7660e-001	-6.9610e-001	4.7660e-001	-6.9370e-001
vds	4.7660e-001	-5.0630e-001	4.7660e-001	-1.4171e+000
vbs	0.0000e+000	0.0000e+000	0.0000e+000	0.0000e+000
vth	2.2450e-001	-2.5964e-001	2.2450e-001	-2.5955e-001
vdsat	2.5129e-001	-3.6324e-001	2.5129e-001	-3.6127e-001
beta	1.2649e-003	1.0192e-003	1.2649e-003	5.0958e-004
gam eff	4.0939e-001	4.6160e-001	4.0939e-001	4.6160e-001
gm	2.7945e-004	3.2941e-004	2.7945e-004	1.6631e-004
gds	2.3044e-006	2.9102e-006	2.3044e-006	3.6737e-007
gmb	3.7341e-005	7.1037e-005	3.7341e-005	3.5844e-005
cdtot	1.1074e-014	6.7287e-014	1.1074e-014	1.9632e-014
cgtot	4.4286e-013	1.8530e-012	4.4286e-013	9.2209e-013
cstot	4.4322e-013	1.8864e-012	4.4322e-013	9.4313e-013
cbtot	9.0925e-014	4.1434e-013	9.0925e-014	2.0331e-013
cgs	4.1103e-013	1.7967e-012	4.1103e-013	8.9759e-013
cgd	4.8493e-015	2.4166e-014	4.8493e-015	7.6354e-015

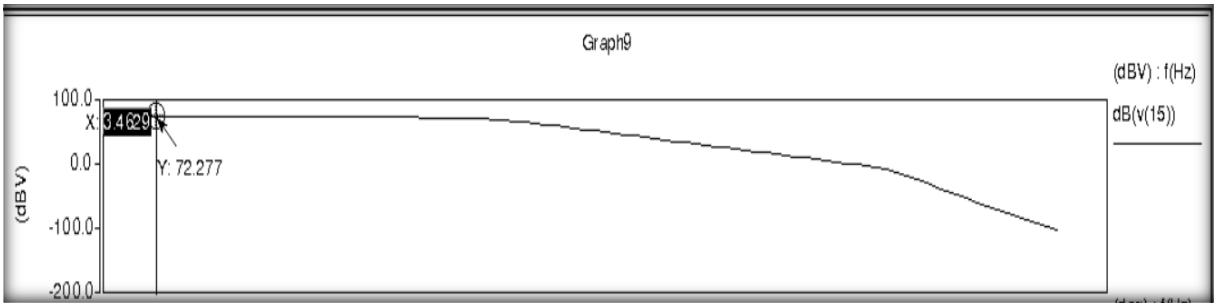
Element	M6	M2	M5	M7
Model Name	NFET	PFET	NFET	PFET
region	Saturation	Cutoff	Saturation	Cutoff
id	1.2238e-004	-4.0044e-005	1.2238e-004	-1.2238e-004
ibs	0.0000e+000	-0.0000e+000	0.0000e+000	-0.0000e+000
ibd	-5.7654e-016	5.0085e-017	-5.7654e-016	1.4966e-016
vgs	4.7660e-001	-6.9370e-001	4.7660e-001	-6.9610e-001
vds	4.7145e-001	-1.4171e+000	4.7145e-001	-1.9286e+000
vbs	0.0000e+000	0.0000e+000	0.0000e+000	0.0000e+000
vth	2.2277e-001	-2.5955e-001	2.2277e-001	-2.5968e-001
vdsat	2.5336e-001	-3.6127e-001	2.5336e-001	-3.6325e-001
beta	3.8094e-003	5.0958e-004	3.8094e-003	1.5335e-003
gam eff	4.0919e-001	4.6160e-001	4.0919e-001	4.6160e-001
gm	8.4846e-004	1.6631e-004	8.4846e-004	5.0516e-004
gds	7.2200e-006	3.6737e-007	7.2200e-006	1.2565e-006
gmb	1.1446e-004	3.5844e-005	1.1446e-004	1.0918e-004
cdtot	3.3676e-014	1.9632e-014	3.3676e-014	5.5193e-014
cgtot	1.3286e-012	9.2209e-013	1.3286e-012	2.7742e-012
cstot	1.3315e-012	9.4313e-013	1.3315e-012	2.8385e-012
cbtot	2.7293e-013	2.0331e-013	2.7293e-013	6.0776e-013
cgs	1.2339e-012	8.9759e-013	1.2339e-012	2.7013e-012
cgd	1.4808e-014	7.6354e-015	1.4808e-014	2.2806e-014

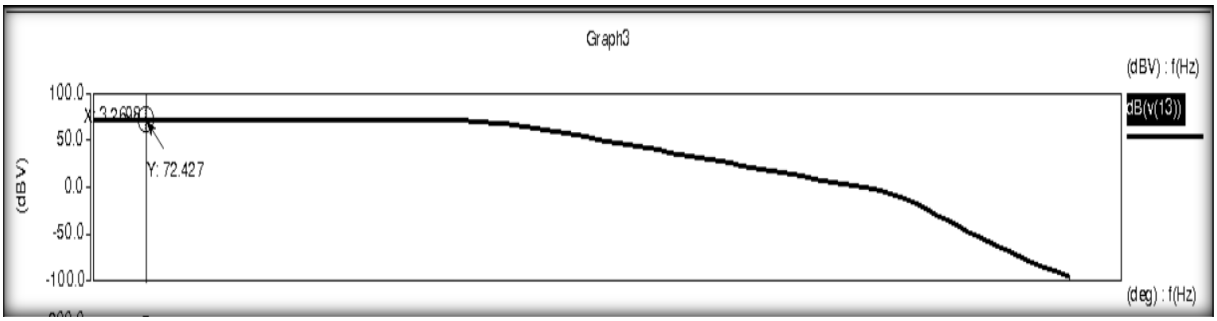
Element	M11	M8	M12	M13
Model Name	NFET	PFET	NFET	PFET
region	Saturation	Cutoff	Saturation	Cutoff
id	1.2161e-004	-1.2238e-004	1.2161e-004	-1.2161e-004
ibs	0.0000e+000	-0.0000e+000	0.0000e+000	-0.0000e+000
ibd	-5.7654e-016	1.4966e-016	-5.7654e-016	1.4966e-016
vgs	4.7145e-001	-6.9610e-001	4.7145e-001	-6.9610e-001
vds	1.1448e+000	-1.9286e+000	1.1448e+000	-1.2552e+000
vbs	0.0000e+000	0.0000e+000	0.0000e+000	0.0000e+000
vth	2.2277e-001	-2.5968e-001	2.2277e-001	-2.5968e-001
vdsat	2.4898e-001	-3.6325e-001	2.4898e-001	-3.6325e-001
beta	3.8155e-003	1.5335e-003	3.8155e-003	1.5335e-003
gam eff	4.0919e-001	4.6160e-001	4.0919e-001	4.6160e-001
gm	8.5911e-004	5.0516e-004	8.5911e-004	5.0240e-004
gds	4.9903e-006	1.2565e-006	4.9903e-006	1.1235e-006
gmb	1.1592e-004	1.0918e-004	1.1592e-004	1.0839e-004
cdtot	2.2578e-014	5.5193e-014	2.2578e-014	6.0650e-014
cgtot	1.3214e-012	2.7742e-012	1.3214e-012	2.7747e-012
cstot	1.3305e-012	2.8385e-012	1.3305e-012	2.8382e-012
cbtot	2.7006e-013	6.0776e-013	2.7006e-013	6.1258e-013
cgs	1.2297e-012	2.7013e-012	1.2297e-012	2.7016e-012
cgd	1.0760e-014	2.2806e-014	1.0760e-014	2.3106e-014

Element	M10
Model Name	PFET
region	Cutoff
id	-1.2161e-004
ibs	-0.0000e+000
ibd	1.4966e-016
vgs	-6.9610e-001
vds	-1.2552e+000
vbs	0.0000e+000
vth	-2.5968e-001
vdsat	-3.6325e-001
beta	1.5335e-003
gam eff	4.6160e-001
gm	5.0240e-004
gds	1.1235e-006
gmb	1.0839e-004
cdtot	6.0650e-014
cgtot	2.7747e-012
cstot	2.8382e-012
cbtot	6.1258e-013
cgs	2.7016e-012
cgd	2.3106e-014

- ✓ We have provided high gm values for current flow of the mosfet in the cascode structure.

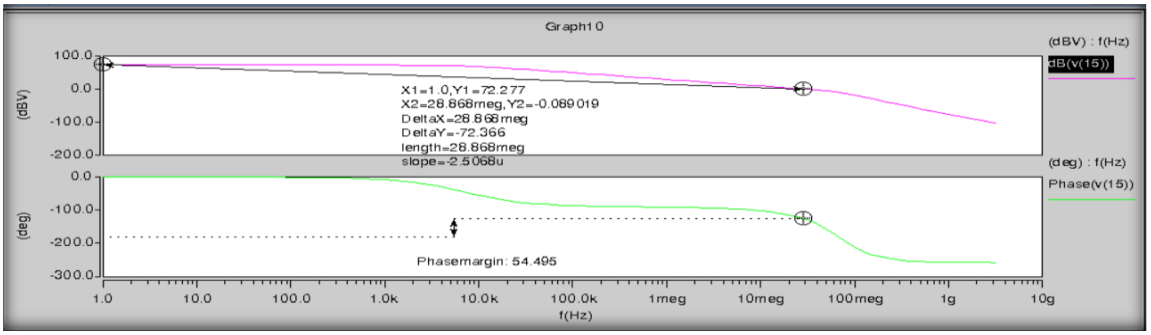
DC GAIN

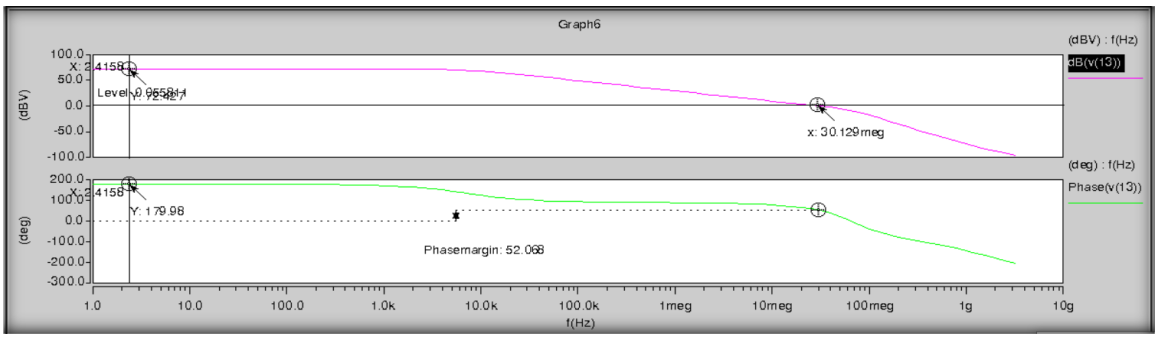




- ✓ To increase DC gain, we have to increase gm value so we increased current value according to W/L ratio.
- ✓ On the other hand, 72.277 dB is pure gain. We should add 6 dB because the circuit reduces both outputs by 6 dB , compared to single-ended measuring .

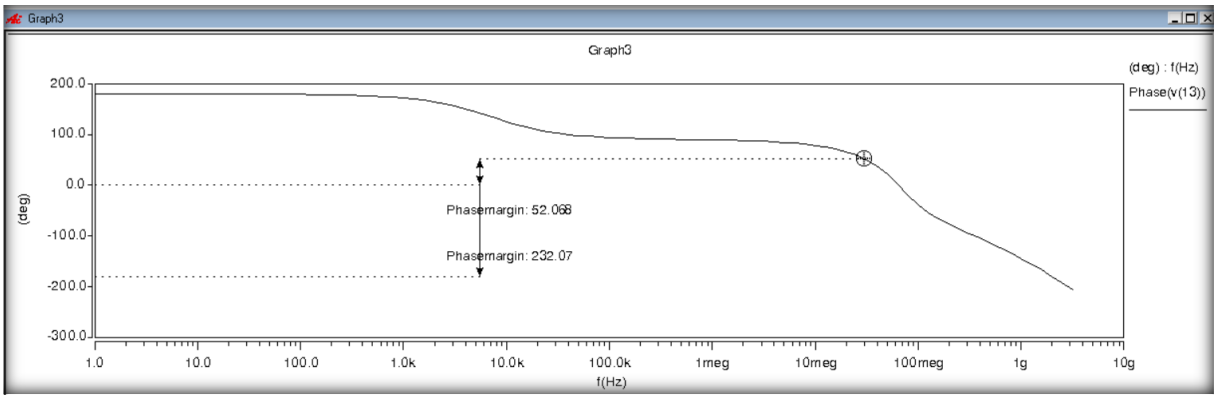
Ft BANDWIDTH

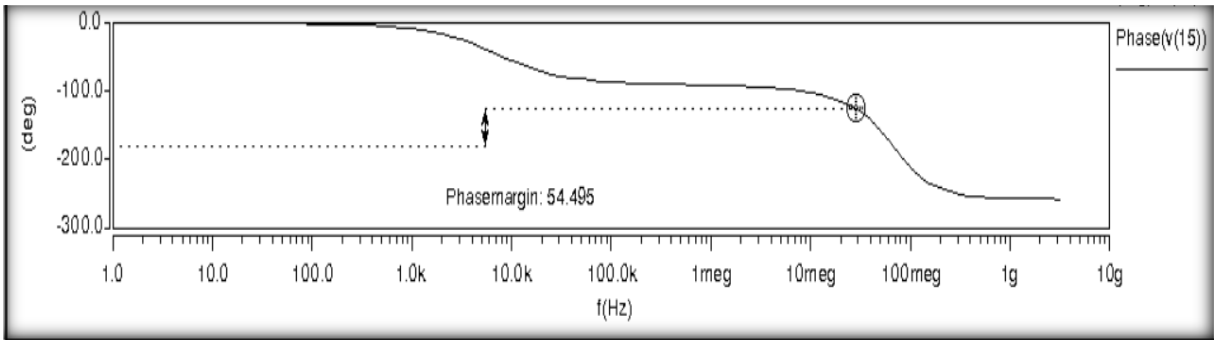




Ft is calculated from the point where the gain falls to zero.

PHASE MARGIN





Phase Margin is calculated distance to 180 degrees from the point where the gain falls to zero.

SLEW RATE

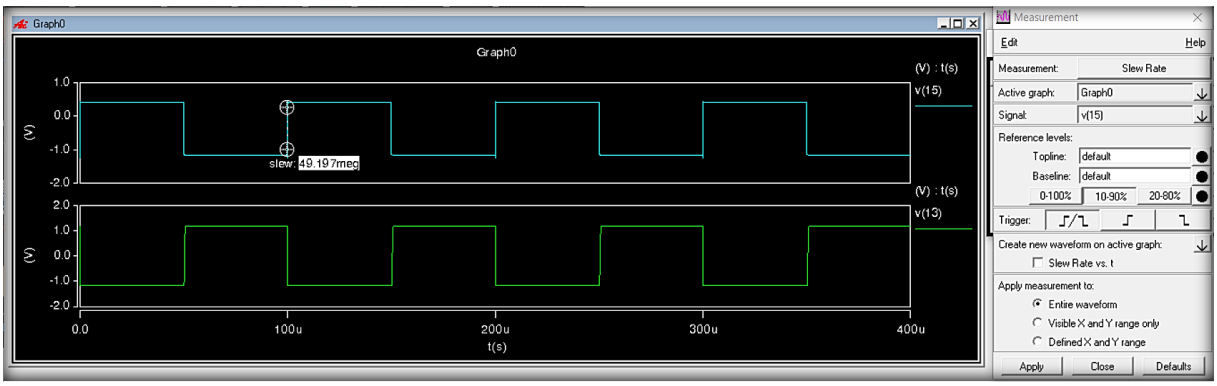
The slew rate of an op amp or any amplifier circuit is the rate of change in the output voltage caused by a step change on the input. It is measured as a voltage change in a given time - typically V / µs or V / ms. A typical general purpose device may have a slew rate of 10 V / microsecond.

```
SAMPLE CİRCUİT*
.INC 130nm.txt
  M9 3 2 1 1      PFET W=48.72u  L=4.5u
  M7 12 2 1 1      PFET W=73.28u    L=4.5u
  M8 8 2 1 1      PFET   W=73.28u    L=4.5u
  M1 6 4 3 3      PFET W=24.36u     L=4.5u
  M2 7 15 3 3      PFET W=24.36u     L=4.5u
  M3 6 6 10 10     NFET W=12.18u   L=4.5u
  M4 7 7 10 10      NFET W=12.18u L=4.5u
  M5 12 6 10 10      NFET W=36.54u   L=4.5u
  M6 8 7 10 10      NFET W=36.54u L=4.5u
  M10 15 2 1 1      PFET   W=73.28u   L=4.5u
  M11  15 8 10 10      NFET W=36.54u    L=4.5u
  M12  13 12 10 10      NFET W=36.54u L=4.5u
  M13  13 2 1 1        PFET  W=73.28u  L=4.5u


VDD 1 GND 1.2
VG 2 GND 0.5039
VIN 4 GND  pulse(-1.2 1.2 0 0.1n 0.1n 50u 100u)
*VI  GND 5 0 AC 1
R1 16 15 6K
R2 14 13 6K
CAP15 8 16 1.29p
CAP13 12 14 1.29p


CAP 15 GND 0.5p
CAP2 13 GND 0.5p
vss gnd 10 1.2
.tran 1u 400u
```

- ✓ We closed negative input than we changed gate of M2 output nodes with 15. After that, we applied pulse at positive input.



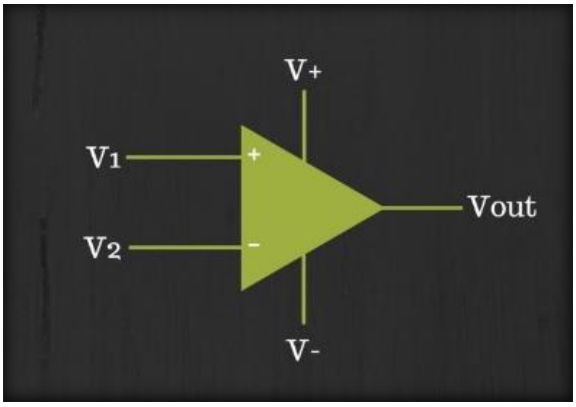
We have seen this graph on transient analysis. SR value is 49.197 V/us.

CMRR (Common Mode Rejection Ratio)

The CMRR in an operational amplifier is a common mode rejection ratio. Generally, the op amp as two input terminals which are positive and negative terminals and the two inputs are applied at the same point. This will give the opposite polarity signals at the output. Hence the positive and the negative voltage of the terminals will cancel out and it will give the resultant output voltage. The ideal op amp will have the infinite CMRR and with the finite differential gain and zero common mode gain.

Theorically; CMRR = 20log|Ad/Ac| dB

CMRR=(Ad-Acm) dB

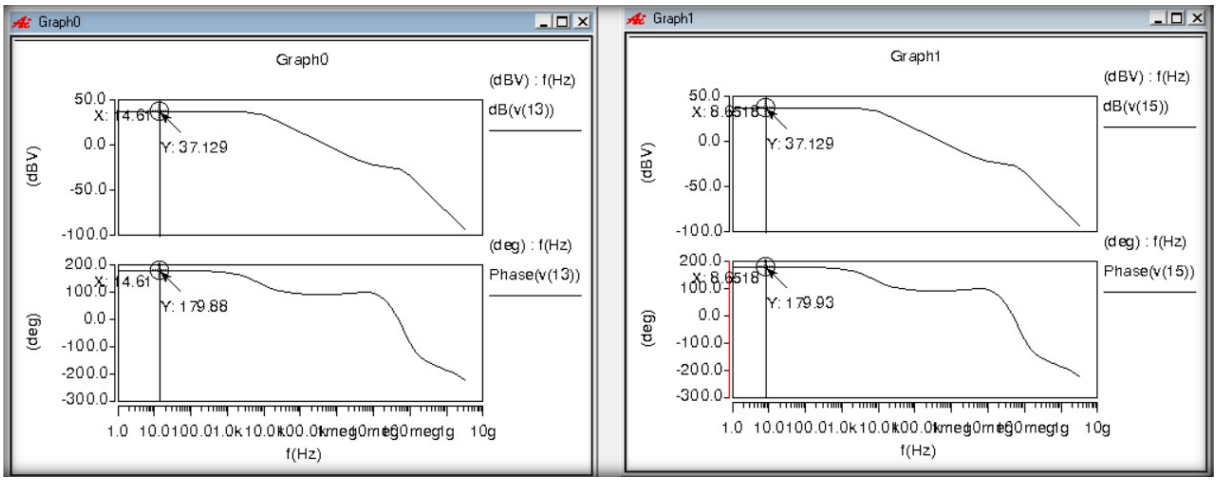


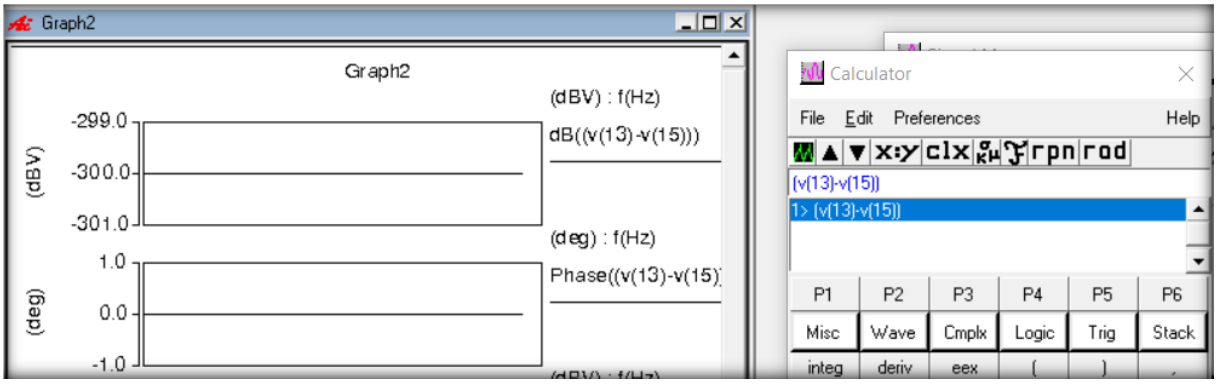

```
VIN   4   GND   AC 1
VI    5   GND  AC 1

*R3 5 17 100K
*R6 15 5 100K
*R4 4 18 100K
*R5 4 GND 100K
```

We have given AC signals to the inputs.

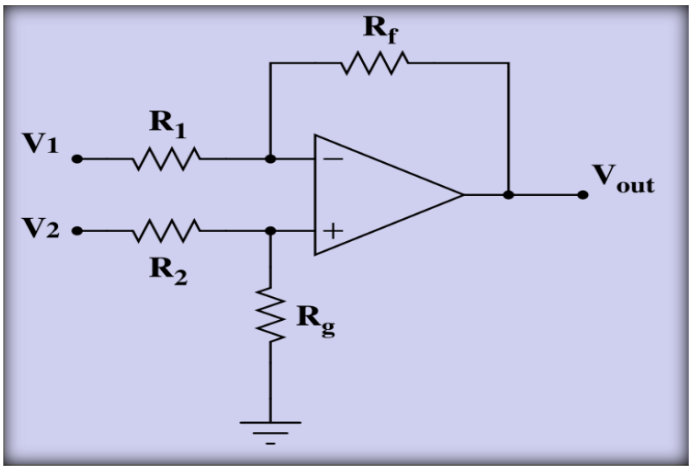
- ✓ We know we have to find negative value for CMRR but we also tried a lot times , we found positive value. There is one way to find negative value that is added resistors. Unfourtunately, lecturer didn't accept. We put it anyway.





We suspected that the circuit is not fully symmetrical so that we calculated V(15)-V(13) and we have seen phase is zero.

To sum up, we have seen CMRR gone infinite according to our circuit.



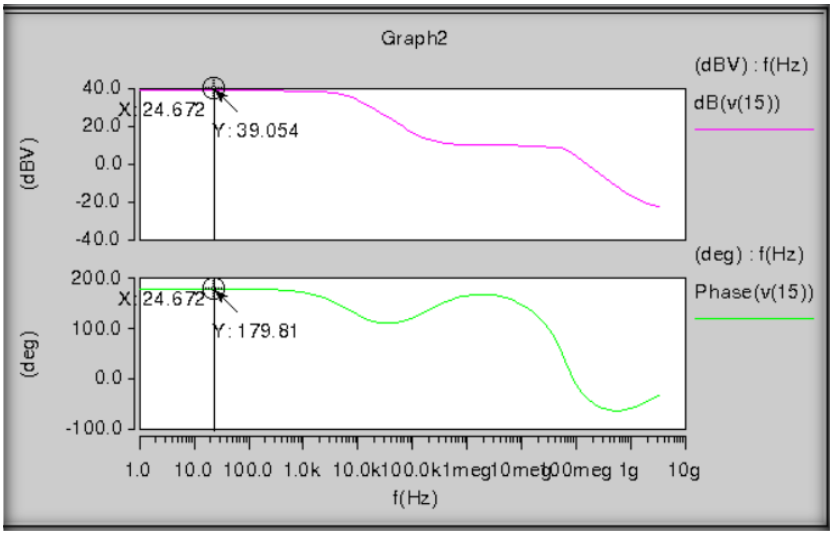
- ✓ We added resistor in this circuit that we found the value of -37dB.

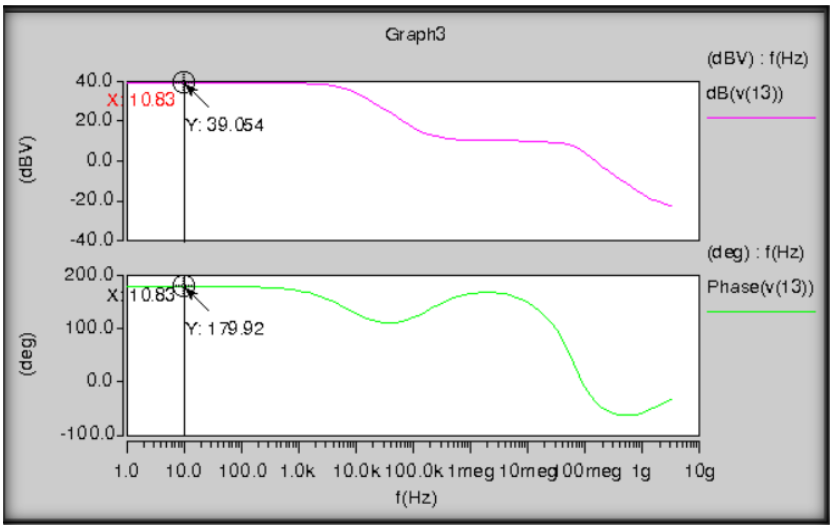
PSRR(Power Supply Rejection Ratio)

Also supply-voltage rejection ratio. In terms of operational amplifier (op-amp) it is defined as a ratio of the change in supply voltage to the equivalent (differential) output voltage it produces. It quantifies the amplifier's sensitivity to power supply changes. Ideally, the power supply rejection ratio should be infinite, which means power supply changes do not affect the output . Typical specifications for a power supply rejection ratio of an amplifier range from 60dB to 100dB.

Theorically; PSRR= 20log|ΔVDc/ΔVio|

```
VDD 1 GND 1.2 AC 1
VG 2 GND 0.5039
VIN 4 GND
VI  5 GND
```



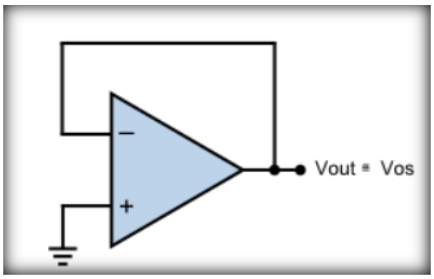



```
VDD 1 GND 1.2 AC 1 SIN(.002 .002 1mV)
VG 2 GND 0.5039
VIN 4 GND
VI GND 5
```

When we applied sin 1mV AC, the result didn't change.

INPUT OFFSET

The input offset voltage is defined as the voltage that must be applied between the two input terminals of the op amp to obtain zero volts at the output. Ideally the output of the op amp should be at zero volts when the inputs are grounded. In reality the input terminals are at slightly different dc potentials.



4	0
5	-1.31808e-005

```
VIN   4   GND
VI    15  5
```

We connected output node to negative input and positive input goes to gnd then V(+) – V(-) is equals input offset value. We calculated input offset value that is 0.013 mV.

REFERENCES

- https://www.ti.com/lit/an/sloa059/sloa059.pdf
- Hspice Quickref
- https://www.elprocus.com/common-mode-rejection-ratio-cmrr-operational-amplifier/
- CMOS Analog Circuit Design (Allen/Holberg)