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Understanding Buck Power Stages in Switchmode Power Supplies

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Understanding Buck Power Stages in Switchmode Power Supplies

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ABSTRACT

A switching power supply consists of the power stage and the control circuit. The power stage performs the basic power conversion from the input voltage to the output voltage and includes switches and the output filter. This report addresses the buck power stage only and does not cover control circuits. Detailed steady-state and small-signal analysis of the buck power stage operating in continuous and discontinuous mode are presented. Variations in the standard buck power stage and a discussion of power stage component requirements are included.

1 Introduction

The three basic switching power supply topologies in common use are the buck, boost, and buck-boost. These topologies are nonisolated, that is, the input and output voltages share a common ground. There are, however, isolated derivations of these nonisolated topologies. The power supply topology refers to how the switches, output inductor, and output capacitor are connected. Each topology has unique properties. These properties include the steady-state voltage conversion ratios, the nature of the input and output currents, and the character of the output voltage ripple. Another important property is the frequency response of the duty-cycle-to-output-voltage transfer function.

The most common and probably the simplest power stage topology is the buck power stage, sometimes called a step-down power stage. Power supply designers choose the buck power stage because the output voltage is always less than the input voltage in the same polarity and is not isolated from the input. The input current for a buck power stage is discontinuous or pulsating due to the power switch (Q1) current that pulses from zero to I_O every switching cycle. The output current for a buck power stage is continuous or nonpulsating because the output current is supplied by the output inductor/capacitor combination; the output capacitor never supplies the entire load current (for continuous inductor current mode operation, one of the two operating modes to be discussed in the next section).

This report describes the steady state operation of the buck power stage in continuous-mode and discontinuous-mode operation with ideal waveforms given. The duty-cycle-to-output-voltage transfer function is given after an introduction of the PWM switch model.

Figure 1 shows a simplified schematic of the buck power stage with a drive circuit block included. The power switch, Q1, is an n-channel MOSFET. The diode, CR1, is usually called the *catch* diode, or *freewheeling* diode. The inductor, L, and capacitor, C, make up the output filter. The capacitor ESR, R_C, (equivalent series resistance) and the inductor DC resistance, R_L, are included in the analysis. The resistor, R, represents the load seen by the power stage output.

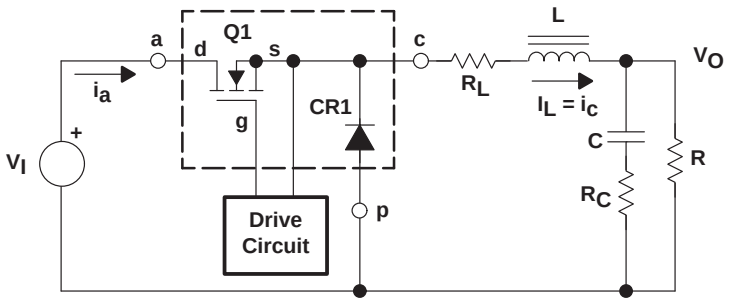

Figure 1. Buck Power Stage Schematic

During normal operation of the buck power stage, Q1 is repeatedly switched on and off with the on and off times governed by the control circuit. This switching action causes a train of pulses at the junction of Q1, CR1, and L which is filtered by the L/C output filter to produce a dc output voltage, V_O. A more detailed quantitative analysis is given in the following sections.

2 Buck Power Stage Steady-State Analysis

A power stage can operate in continuous or discontinuous inductor current mode. Continuous inductor current mode is characterized by current flowing continuously in the inductor during the entire switching cycle in steady state operation. Discontinuous inductor current mode is characterized by the inductor current being zero for a portion of the switching cycle. It starts at zero, reaches a peak value, and returns to zero during each switching cycle. The two different modes are discussed in greater detail later and design guidelines for the inductor value to maintain a chosen mode of operation as a function of rated load is given. It is very desirable for a power stage to stay in only one mode over its expected operating conditions, because the power stage frequency response changes significantly between the two modes of operation.

For this analysis, an n-channel power MOSFET is used and a positive voltage, $V_{GS(ON)}$, is applied from the Gate to the Source terminals of Q1 by the drive circuit to turn ON the FET. The advantage of using an n-channel FET is its lower $R_{DS(on)}$ but the drive circuit is more complicated because a floating drive is required. For the same die size, a p-channel FET has a higher $R_{DS(on)}$ but usually does not require a floating drive circuit.

The transistor Q1 and diode CR1 are drawn inside a dashed-line box with terminals labeled a, p, and c. The inductor current I_L is also labeled i_C and refers to current flowing out of terminal c. These items are explained fully in the Buck Power Stage Modeling section.

2.1 Buck Steady-State Continuous Conduction Mode Analysis

The following is a description of steady-state operation in continuous conduction mode. The main result of this section is a derivation of the voltage conversion relationship for the continuous conduction mode buck power stage. This result is important because it shows how the output voltage depends on duty cycle and input voltage or, conversely, how the duty cycle can be calculated based on input voltage and output voltage. Steady-state implies that the input voltage, output voltage, output load current, and duty-cycle are fixed and not varying. Capital letters are generally given to variable names to indicate a steady-state quantity.

In continuous conduction mode, the Buck power stage assumes two states per switching cycle. The ON state is when Q1 is ON and CR1 is OFF. The OFF state is when Q1 is OFF and CR1 is ON. A simple linear circuit can represent each of the two states where the switches in the circuit are replaced by their equivalent circuits during each state. The circuit diagram for each of the two states is shown in Figure 2.

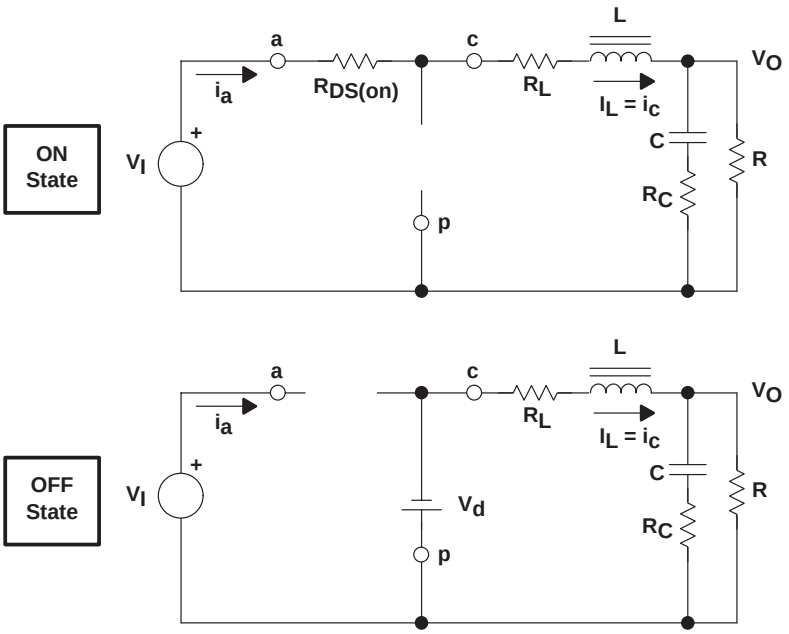

Figure 2. Buck Power Stage States

The duration of the ON state is $D \times T_S = T_{ON}$ where D is the duty cycle, set by the control circuit, expressed as a ratio of the switch ON time to the time of one complete switching cycle, T_S. The duration of the OFF state is called T_{OFF}. Since there are only two states per switching cycle for continuous mode, T_{OFF} is equal to $(1–D) \times T_S$. The quantity $(1–D)$ is sometimes called D'. These times are shown along with the waveforms in Figure 3.

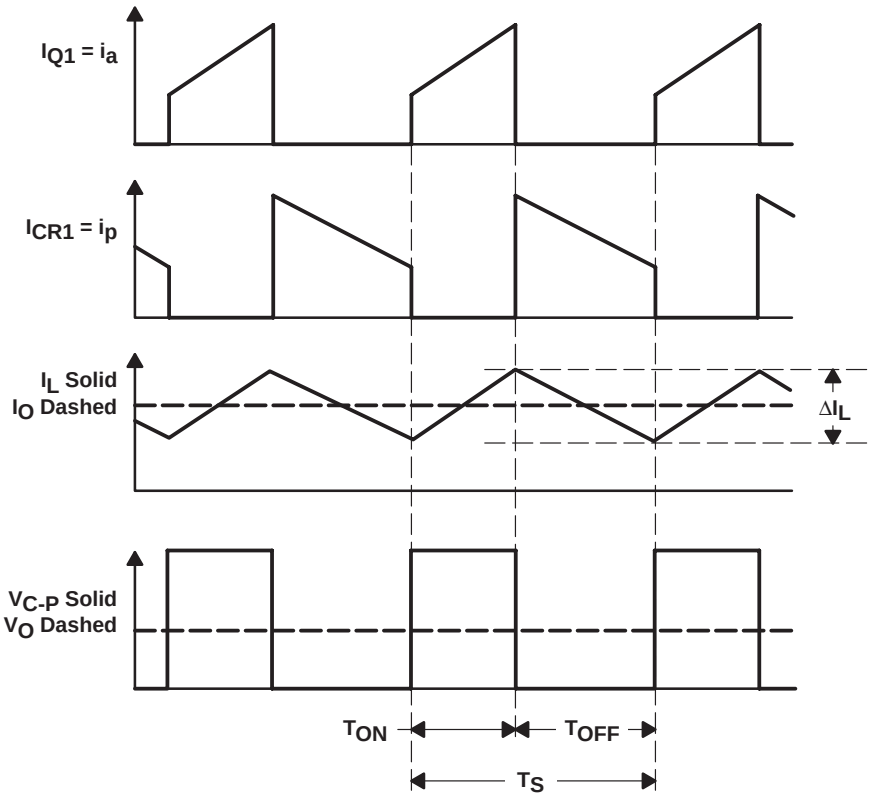

Figure 3. Continuous-Mode Buck Power Stage Waveforms

Referring to Figure 2, during the ON state, Q1 presents a low resistance, $R_{DS(on)}$, from its drain to source and has a small voltage drop of $V_{DS} = I_L \times R_{DS(on)}$. There is also a small voltage drop across the dc resistance of the inductor equal to $I_L \times R_L$. Thus, the input voltage, V_I, minus losses, ($V_{DS} + I_L \times R_L$), is applied to the left-hand side of inductor, L. CR1 is OFF during this time because it is reverse biased. The voltage applied to the right hand side of L is simply the output voltage, V_O. The inductor current, I_L, flows from the input source, V_I, through Q1 and to the output capacitor and load resistor combination. During the ON state, the voltage applied across the inductor is constant and equal to $V_I - V_{DS} - I_L \times R_L - Vo$. Adopting the polarity convention for the current I_L shown in Figure 2, the inductor current increases as a result of the applied voltage. Also, since the applied voltage is essentially constant, the inductor current increases linearly. This increase in inductor current during T_{ON} is illustrated in Figure 3.

The amount that the inductor current increases can be calculated by using a version of the familiar relationship:

$$V_L = L \times \frac{di_L}{dt} \Rightarrow \Delta I_L = \frac{V_L}{L} \times \Delta T$$

The inductor current increase during the ON state is given by:

$$\Delta I_L(+) = \frac{\left(V_I - V_{DS} - I_L \times R_L\right) - V_O}{L} \times T_{ON}$$

This quantity, $\Delta I_L(+)$, is referred to as the inductor ripple current.

Referring to Figure 2, when Q1 is OFF, it presents a high impedance from its drain to source. Therefore, since the current flowing in the inductor L cannot change instantaneously, the current shifts from Q1 to CR1. Due to the decreasing inductor current, the voltage across the inductor reverses polarity until rectifier CR1 becomes forward biased and turns ON. The voltage on the left-hand side of L becomes $-(V_d + I_L \times R_L)$ where the quantity, V_d, is the forward voltage drop of CR1. The voltage applied to the right hand side of L is still the output voltage, V_O. The inductor current, I_L, now flows from ground through CR1 and to the output capacitor and load resistor combination. During the OFF state, the magnitude of the voltage applied across the inductor is constant and equal to $(V_O + V_d + I_L \times R_L)$. Maintaining our same polarity convention, this applied voltage is negative (or opposite in polarity from the applied voltage during the ON time). Hence, the inductor current decreases during the OFF time. Also, since the applied voltage is essentially constant, the inductor current decreases linearly. This decrease in inductor current during T_{OFF} is illustrated in Figure 3.

The inductor current decrease during the OFF state is given by:

$$\Delta I_L(-) = \frac{V_O + \left(V_d + I_L \times R_L\right)}{L} \times T_{OFF}$$

This quantity, $\Delta I_L(-)$, is also referred to as the inductor ripple current.

In steady state conditions, the current increase, $\Delta I_L(+)$, during the ON time and the current decrease during the OFF time, $\Delta I_L(-)$, must be equal. Otherwise, the inductor current would have a net increase or decrease from cycle to cycle which would not be a steady state condition. Therefore, these two equations can be equated and solved for V_O to obtain the continuous conduction mode buck voltage conversion relationship.

Solving for V_O:

$$V_O = \left(V_I - V_{DS}\right) \times \frac{T_{ON}}{T_{ON} + T_{OFF}} - V_d \times \frac{T_{OFF}}{T_{ON} + T_{OFF}} - I_L \times R_L$$

And, substituting T_S for $T_{ON} + T_{OFF}$, and using $D = T_{ON}/T_S$ and $(1-D) = T_{OFF}/T_S$, the steady-state equation for V_O is:

$$V_O = \left(V_I - V_{DS}\right) \times D - V_d \times (1-D) - I_L \times R_L$$

Notice that in simplifying the above, $T_{ON} + T_{OFF}$ is assumed to be equal to T_S. This is true only for continuous conduction mode as we will see in the discontinuous conduction mode analysis.

> **NOTE:** An important observation should be made here: Setting the two values of ΔI_L equal to each other is equivalent to *balancing the volt-seconds* on the inductor. The volt-seconds applied to the inductor is the product of the voltage applied and the time that the voltage is applied. This is the best way to calculate unknown values such as V_O or D in terms of known circuit parameters and this method will be applied repeatedly in this paper. Volt-second balance on the inductor is a physical necessity and should be comprehended at least as well as Ohms Law.

In the above equations for $\Delta I_L(+)$ and $\Delta I_L(-)$, the dc output voltage was implicitly assumed to be constant with no AC ripple voltage during the ON time and the OFF time. This is a common simplification and involves two separate effects. First, the output capacitor is assumed to be large enough that its voltage change is negligible. Second, the voltage across the capacitor ESR is also assumed to be negligible. These assumptions are valid because the ac ripple voltage is designed to be much less than the dc part of the output voltage.

The above voltage conversion relationship for V_O illustrates the fact that V_O can be adjusted by adjusting the duty cycle, D, and is always less than the input because D is a number between 0 and 1. A common simplification is to assume V_{DS}, V_d, and R_L are small enough to ignore. Setting V_{DS}, V_d, and R_L to zero, the above equation simplifies considerably to:

$$V_O = V_I \times D$$

Another simplified way to visualize the circuit operation is to consider the output filter as an averaging network. This is a valid simplification because the filter cutoff frequency (usually between 500 Hz and 5 kHz) is always much less than the power supply switching frequency (usually between 100 kHz and 500 kHz). The input voltage applied to the filter is the voltage at the junction of Q1, CR1, and L, labeled as V_{c-p}. The filter passes the dc component (or average) of V_{c-p} and greatly attenuates all frequencies above the output filter cutoff frequency. Thus, the output voltage is simply the average of the V_{c-p} voltage.

To relate the inductor current to the output current, referring to Figures 2 and 3, note that the inductor delivers current to the output capacitor and load resistor combination during the whole switching cycle. The inductor current averaged over the switching cycle is equal to the output current. This is true because the average current in the output capacitor must be zero. In equation form, we have:

$$I_{L(Avg)} = I_O$$

This analysis was for the buck power stage operation in continuous inductor current mode. The next section is a description of steady-state operation in discontinuous conduction mode. The main result is a derivation of the voltage conversion relationship for the discontinuous conduction mode buck power stage.

2.2 Buck Steady-State Discontinuous Conduction Mode Analysis

We now investigate what happens when the load current is decreased. First, observe that the power stage output current is the average of the inductor current. This should be obvious since the inductor current flows into the output capacitor and load resistor combination and the average current flowing in the output capacitor is always zero.

If the output load current is reduced below the critical current level, the inductor current will be zero for a portion of the switching cycle. This should be evident from the waveforms shown in Figure 3 since the peak to peak amplitude of the ripple current does not change with output load current. In a (nonsynchronous) buck power stage, if the inductor current attempts to fall below zero, it just stops at zero (due to the unidirectional current flow in CR1) and remains there until the beginning of the next switching cycle. This operating mode is called discontinuous conduction mode. A power stage operating in discontinuous conduction mode has three unique states during each switching cycle as opposed to two states for continuous conduction mode. The load current condition where the power stage is at the boundary between continuous and discontinuous mode is shown in Figure 4. This is where the inductor current falls to zero and the next switching cycle begins immediately after the current reaches zero.

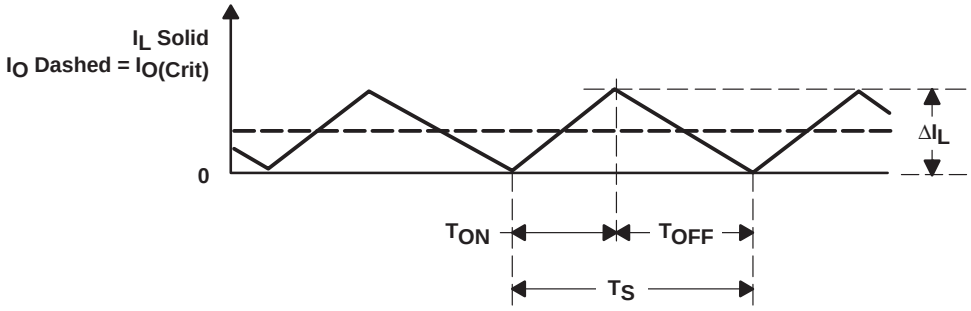

Figure 4. Boundary Between Continuous and Discontinuous Mode

Further reduction in output load current puts the power stage into discontinuous conduction mode. This condition is illustrated in Figure 5. The discontinuous mode power stage frequency response is quite different from the continuous mode frequency response and is shown in the Buck Power Stage Modeling section. Also, the input to output relationship is quite different as shown in the following derivation.

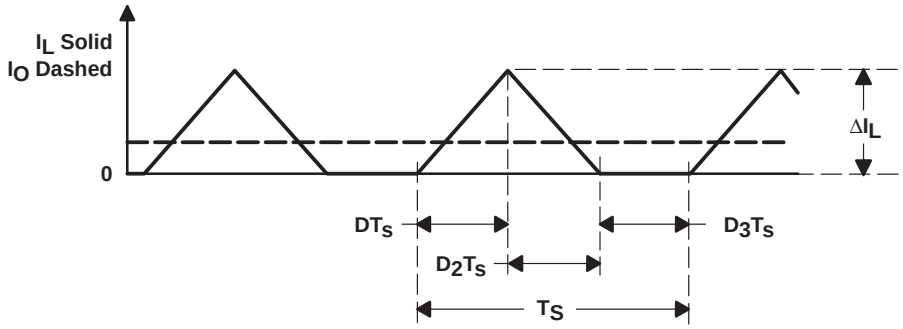

Figure 5. Discontinuous Current Mode

To begin the derivation of the discontinuous conduction mode buck power stage voltage conversion ratio, observe that there are three unique states that the power stage assumes during discontinuous current mode operation. The ON state is when Q1 is ON and CR1 is OFF. The OFF state is when Q1 is OFF and CR1 is ON. The IDLE state is when both Q1 and CR1 are OFF. The first two states are identical to those of the continuous mode case and the circuits of Figure 2 are applicable except that $T_{OFF} \neq (1–D) \times T_S$. The remainder of the switching cycle is the IDLE state. In addition, the dc resistance of the output inductor, the output diode forward voltage drop, and the power MOSFET ON-state voltage drop are all assumed to be small enough to omit.

The duration of the ON state is $T_{ON} = D \times T_S$ where D is the duty cycle, set by the control circuit, expressed as a ratio of the switch ON time to the time of one complete switching cycle, T_S. The duration of the OFF state is $T_{OFF} = D2 \times T_S$. The IDLE time is the remainder of the switching cycle and is given as $T_S - T_{ON} - T_{OFF} = D3 \times T_S$. These times are shown with the waveforms in Figure 6.

Without going through the detailed explanation as before, the equations for the inductor current increase and decrease are given below.

The inductor current increase during the ON state is given by:

$$\Delta I_L(+) = \frac{V_I - V_O}{L} \times T_{ON} = \frac{V_I - V_O}{L} \times D \times T_S = I_{PK}$$

The ripple current magnitude, $\Delta I_L(+)$, is also the peak inductor current, I_{pk}, because in discontinuous mode, the current starts at zero each cycle.

The inductor current decrease during the OFF state is given by:

$$\Delta I_L(–) = \frac{V_O}{L} \times T_{OFF}$$

As in the continuous conduction mode case, the current increase, $\Delta I_L(+)$, during the ON time and the current decrease during the OFF time, $\Delta I_L(–)$, are equal. Therefore, these two equations can be equated and solved for V_O to obtain the first of two equations to be used to solve for the voltage conversion ratio:

$$V_O = V_I \times \frac{T_{ON}}{T_{ON} + T_{OFF}} = V_I \times \frac{D}{D + D2}$$

Now we calculate the output current (the output voltage V_O divided by the output load R). It is the average of the inductor current.

$$I_O = I_{L(avg)} = \frac{V_O}{R} = \frac{I_{PK}}{2} \times \frac{D \times T_S + D2 \times T_S}{Ts}$$

Now, substitute the relationship for I_{PK} into the above equation to obtain:

$$I_O = \frac{V_O}{R} = \left(V_I - V_O\right) \times \frac{D \times T_S}{2 \times L} \times (D + D2)$$

We now have two equations, the one for the output current just derived and the one for the output voltage (above), both in terms of V_I, D, and $D2$. We now solve each equation for D2 and set the two equations equal to each other. Using the resulting equation, an expression for the output voltage, V_O, can be derived.

The discontinuous conduction mode buck voltage conversion relationship is given by:

$$V_O = V_I \times \frac{2}{1 + \sqrt{1 + \frac{4 \times K}{D^2}}}$$

Where K is defined as:

$$K = \frac{2 \times L}{R \times T_S}$$

The above relationship shows one of the major differences between the two conduction modes. For discontinuous conduction mode, the voltage conversion relationship is a function of the input voltage, duty cycle, power stage inductance, the switching frequency and the output load resistance while for continuous conduction mode, the voltage conversion relationship is only dependent on the input voltage and duty cycle.

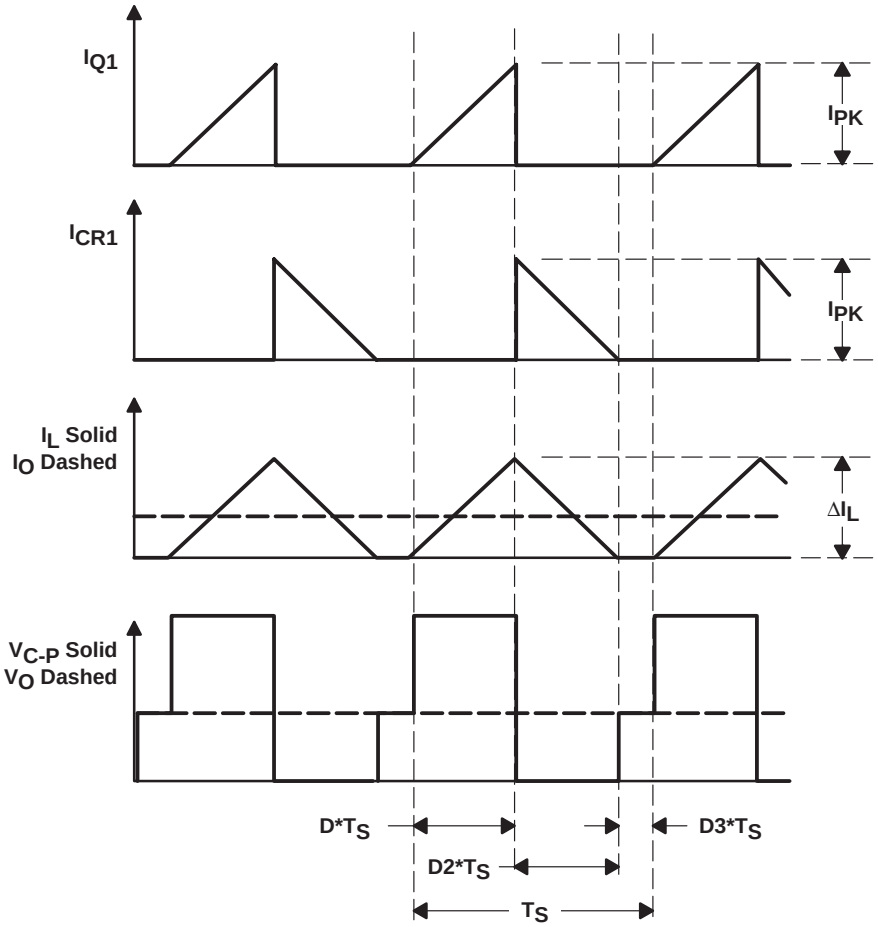

Figure 6. Discontinuous-Mode Buck Power Stage Waveforms

It should be noted that the buck power stage is rarely operated in discontinuous conduction mode in normal situations, but discontinuous conduction mode will occur anytime the load current is below the critical level.

2.3 Critical Inductance

The previous analyses for the buck power stage have been for continuous and discontinuous conduction modes of steady-state operation. The conduction mode of a power stage is a function of input voltage, output voltage, output current, and the value of the inductor. A buck power stage can be designed to operate in continuous mode for load currents above a certain level usually 5% to 10% of full load. Usually, the input voltage range, the output voltage and load current are defined by the power stage specification. This leaves the inductor value as the design parameter to maintain continuous conduction mode.

The minimum value of inductor to maintain continuous conduction mode can be determined by the following procedure.

First, define $I_{O(crit)}$ as the minimum current to maintain continuous conduction mode, normally referred to as the critical current. This value is shown in Figure 4 and is calculated as:

$$I_{O(crit)} = \frac{\Delta I_L}{2}$$

Second, calculate L such that the above relationship is satisfied. To solve the above equation, either relationship, $\Delta I_L(+)$ or $\Delta I_L(-)$ may be used for ΔI_L. Note also that either relationship for ΔI_L is independent of the output current level. Here, $\Delta I_L(-)$ is used. The worst case condition (giving the largest L_{min}) is at maximum input voltage because this gives the maximum ΔI_L.

Now, substituting and solving for L_{min}:

$$L_{min} \geq \frac{1}{2} \times \left(V_O + V_d + I_L \times R_L\right) \times \frac{T_{OFF(max)}}{I_{O(crit)}}$$

The above equation can be simplified and put in a form that is easier to apply as shown:

$$L_{min} \geq \frac{V_O \times \left[1 - \frac{V_O}{V_{I(max)}}\right] \times T_S}{2 \times I_{O(crit)}}$$

Using the inductor value just calculated will guarantee continuous conduction mode operation for output load currents above the critical current level, $I_{O(crit)}$.

3 Buck Power Stage Small Signal Modeling

We now switch gears moving from a detailed circuit oriented analysis approach to more of a system level investigation of the buck power stage. This section presents techniques to assist the power supply designer in accurately modeling the power stage as a component of the control loop of a buck power supply. The three major components of the power supply control loop (i.e., the power stage, the pulse width modulator and the error amplifier) are shown in block diagram form in Figure 7.

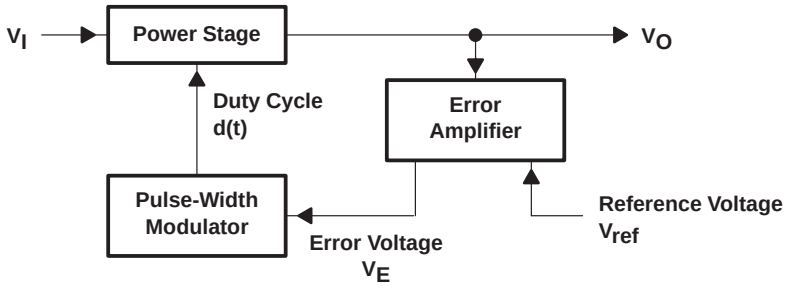

Figure 7. Power Supply Control Loop Components

Modeling the power stage presents one of the main challenges to the power supply designer. A popular technique involves modeling only the switching elements of the power stage. An equivalent circuit for these elements is derived and is called the *PWM Switch Model* where PWM is the abbreviation for pulse width modulated. This approach is presented here.

As shown in Figure 7, the power stage has two inputs: the input voltage and the duty cycle. The duty cycle is the control input, i.e., this input is a logic signal which controls the switching action of the power stage and hence the output voltage. Even though the buck power stage has an essentially linear voltage conversion ratio versus duty cycle, many other power stages have a nonlinear voltage conversion ratio versus duty cycle. To illustrate this nonlinearity, a graph of the steady-state voltage conversion ratio for a boost power stage as a function of steady-state duty cycle, D is shown in Figure 8. The nonlinear boost power stage is used here for illustration to stress the significance of deriving a linear model.

The nonlinear characteristics are a result of the switching action of the power stage switching components, Q1 and CR1. It was observed in reference [5] that the only nonlinear components in a power stage are the switching devices; the remainder of the circuit consists of linear elements. It was also shown in reference [5] that a linear model of only the nonlinear components could be derived by averaging the voltages and currents associated with these nonlinear components over one switching cycle. The model is then substituted into the original circuit for analysis of the complete power stage. Thus, a model of the switching devices is given and is called the *PWM switch* model.

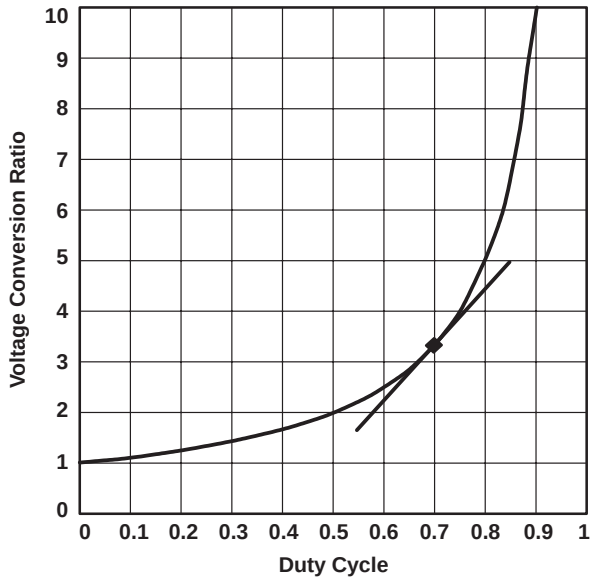

Figure 8. Boost Nonlinear Power Stage Gain vs Duty Cycle

The basic objective behind modelling power stages is to represent the ac behavior at a given operating point and to be linear around the operating point. We want linearity so that we can apply the many analysis tools available for linear systems. Referring again to Figure 8, if we choose the operating point at *D = 0.7*, a straight line can be constructed that is tangent to the original curve at the point where *D = 0.7*. This is an illustration of linearization about an operating point, a technique used in deriving the PWM switch model. Qualitatively, one can see that if the variations in duty cycle are kept small, a linear model accurately represents the nonlinear behavior of the power stage being analyzed.

Since a power stage can operate in one of two conduction modes, i.e., continuous conduction mode (CCM) or discontinuous conduction mode (DCM), there is a PWM switch model for the two conduction modes. The CCM PWM Switch model is derived here. The DCM PWM switch model is derived in the Application Report *Understanding Buck–Boost Converter Power Stages*, TI Literature Number SLVA059.

3.1 Buck Continuous Conduction Mode Small Signal Analysis

To start modeling the buck power stage, we begin with the derivation of the PWM Switch model in (CCM). We focus on the CCM Buck power stage shown in Figure 1. The strategy is to average the switching waveforms over one switching cycle and produce an equivalent circuit for substitution into the remainder of the power stage. The waveforms that are averaged are the voltage across CR1, v_{c-p}, and the current in Q1, i_a. The waveforms are shown in Figure 3.

Referring again to Figure 1, the power transistor, Q1, and the catch diode, CR1, are drawn inside a dashed-line box. These are the components that will be replaced by the PWM switch equivalent circuit. The terminals labeled a, p, and c will be used for terminal labels of the PWM switch model.

Now, an explanation of the terminal naming convention is in order. The terminal named *a* is for *active*; it is the terminal connected to the active switch. Similarly, *p* is for *passive* and is the terminal of the passive switch. Lastly, *c* is for *common* and is the terminal that is common to both the active and passive switches. Interestingly enough, all three commonly used power stage topologies contain active and passive switches and the above terminal definitions can be also applied. In addition, it is true that substituting the PWM switch model that we will derive into other power stage topologies also produces a valid model for that particular power stage. To use the PWM switch model in other power stages, just substitute the model shown below in Figure 10 into the power stage in the appropriate orientation.

Referring to the waveforms in Figure 3, regarded as instantaneous functions of time, the following relationships are true:

$$i_a(t) = \begin{cases} i_c(t) & \text{during } d \times T_S \\ 0 & \text{during } d' \times T_S \end{cases}$$

$$v_{cp}(t) = \begin{cases} v_{ap}(t) & \text{during } d \times T_S \\ 0 & \text{during } d' \times T_S \end{cases}$$

where: $i_a(t)$ and $i_c(t)$ are the instantaneous currents during a switching cycle and $v_{cp}(t)$ and $v_{ap}(t)$ are the instantaneous voltages between the indicated terminals.

If we take the average over one switching cycle of the above quantities, we get:

$$\langle i_a \rangle = d \times \langle i_c \rangle \tag{1}$$

$$\langle v_{cp} \rangle = d \times \langle v_{ap} \rangle \tag{2}$$

where the brackets indicate averaged quantities.

Now, we can implement the above averaged equations in a simple circuit using dependent sources:

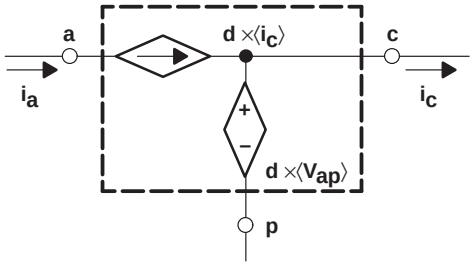

Figure 9. Averaged (Nonlinear) CCM PWM Switch Model

The above model is one form of the PWM switch model. However, in this form it is a large signal nonlinear model. We now need to perform perturbation and linearization and then the PWM switch model will be in the desired form, i.e., linearized about a given operating point.

The main idea of perturbation and linearization is assuming an operating point and introducing small variations about that operating point. For example, we assume that the duty ratio is fixed at $d = D$ (capital letters indicate steady-state, or dc quantities while lower case letters are for time-varying quantities). Then a small variation, $\hat{d}$, is added to the duty cycle so that the complete expression for the duty cycle becomes:

$$d(t) = D + \hat{d}(t)$$

Note that the ^ (hat) above the quantities represents perturbed or small ac quantities. We change notation slightly replacing the averaged quantities such as $\langle i_a \rangle$ with capitol letters (indicating dc quantities) such as I_a. Now we apply the above process to equations (1) and (2) to obtain:

$$I_a + \hat{i}_a = \left(D + \hat{d}\right) \times \left(I_c + \hat{i}_c\right) = D \times I_c + D \times \hat{i}_c + \hat{d} \times I_c + \hat{d} \times \hat{i}_c$$

$$V_{cp} + \hat{v}_{cp} = \left(D + \hat{d}\right) \times \left(V_{ap} + \hat{v}_{ap}\right) = D \times V_{ap} + D \times \hat{v}_{ap} + \hat{d} \times V_{ap} + \hat{d} \times \hat{v}_{ap}$$

Now, separate steady-state quantities from ac quantities and also drop products of ac quantities because the variations are assumed to be small and products of two small quantities are assumed to be negligible. We arrive at the steady-state and ac relationships or, in other words, the dc and small signal model:

$I_a = D \times I_c$	*Steady-state*
$\hat{i}_a = D \times \hat{i}_c + \hat{d} \times I_c$	*AC*
$V_{cp} = D \times V_{ap}$	*Steady-state*
$\hat{v}_{cp} = D \times \hat{v}_{ap} + \hat{d} \times V_{ap}$	*AC*

In order to implement the above equations into a simple circuit, first notice that the two steady-state relationships can be represented by an ideal (independent of frequency) transformer with turns ratio equal to D. Including the ac quantities is straightforward after reflecting all dependent sources to the primary side of the ideal transformer. The dc and small-signal model of the PWM switch is shown in Figure 10. It can easily be verified that the model below satisfies the above four equations.

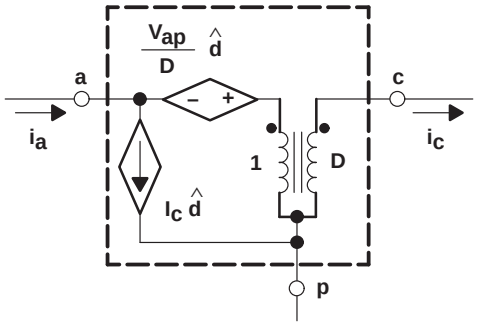

Figure 10. DC and Small Signal CCM PWM Switch Model

This model can now be substituted for Q1 and CR1 in the buck power stage to obtain a model suitable for dc or ac analysis and is shown in Figure 11.

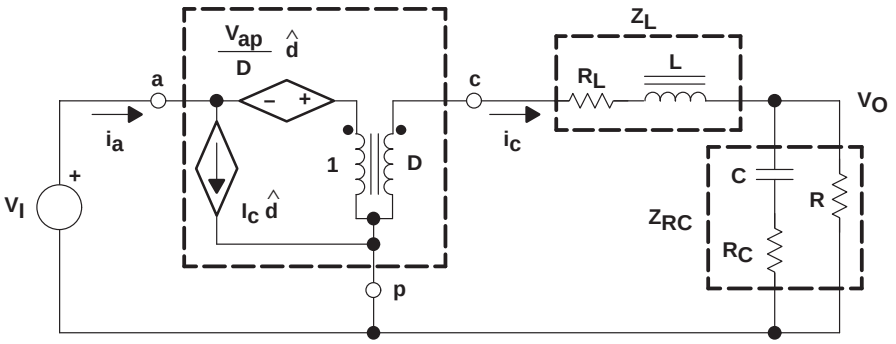

Figure 11. CCM Buck Power Stage Model

To illustrate how simple power stage analysis becomes with the PWM switch model, consider the following. For dc analysis, $\hat{d}$ is zero, L is a short, and C is an open. Then by inspection one can see $V_I \times D = V_O$. We also see that $V_{ap} = V_I$. Thus, knowing the input voltage and output voltage, D is easily calculated. For ac analysis, the following transfer functions can be calculated: open-loop line-to-output, open-loop input impedance, open-loop output impedance, and open-loop control-to-output. The control-to-output, or duty-cycle-to-output, is the transfer function most used for control loop analysis. To determine this transfer function, first, use the results from the DC analysis for operating point information. This information is used to determine the parameter values of the dependent sources; for example, $V_{ap} = V_I$. Then set the input voltage equal to zero because we only want the ac component of the transfer function. Now, writing a voltage loop equation for the *V_I – dependent voltage source – transformer primary* loop gives the transfer function from duty–cycle to v_{cp} as shown:

$$-\frac{V_{ap}}{D} \times \hat{d} + \frac{\hat{v}_{cp}}{D} = 0 \Rightarrow \hat{v}_{cp} = V_{ap} \times \hat{d} \Rightarrow \hat{v}_{cp} = V_I \times \hat{d}$$

or

$$\frac{\hat{v}_{cp}}{\hat{d}} = V_I$$

The transfer function from v_{cp} to the output voltage is:

$$\frac{\hat{v}_O}{\hat{v}_{cp}} = \frac{Z_{RC}(s)}{Z_{RC}(s) + Z_L(s)} \text{ by voltage division}$$

Where

$$Z_{RC}(s) = \frac{R \times \left(1 + s \times R_C \times C\right)}{1 + s \times C \times \left(R + R_C\right)} \text{ (parallel combination of output R and output C)}$$

$$Z_L(s) = R_L + s \times L$$

So, after simplifying, the duty-cycle-to-output transfer function is:

$$\frac{\hat{v}_O}{\hat{d}}(s) = \frac{\hat{v}_{cp}}{\hat{d}}(s) \times \frac{\hat{v}_O}{\hat{v}_{cp}}(s) = V_I \times \frac{R}{R + R_L}$$

$$\times \frac{1 + R_c \times C}{1 + s \times \left[C \times \left(R_c + \frac{R \times R_L}{R + R_L} \right) + \frac{L}{R + R_L} \right] + s^2 \times L \times C \times \frac{R + R_C}{R + R_L}}$$

The above is exactly what is obtained by other modeling procedures.

3.2 Buck Discontinuous Conduction Mode Small-Signal Analysis

To model the buck power stage operation in discontinuous conduction mode (DCM), we follow a similar path as above for CCM. A PWM switch model is inserted into the power stage circuit by replacing the switching elements. As mentioned above, the derivation for the DCM PWM switch model is given elsewhere. More details can be found in *Fundamentals of Power Electronics*. The large signal nonlinear version of the DCM PWM switch model is shown in Figure 12. This model is useful for determining the dc operating point of a power supply. The input port is simply modeled with a resistor, R_e. The value of R_e is given by:

$$R_e = \frac{2 \times L}{D^2 \times T_S}$$

The output port is modeled as a dependent power source. This power source delivers power equal to that dissipated by the input resistor, R_e. This model is analogous to the (nonlinear) CCM PWM switch model shown in Figure 9.

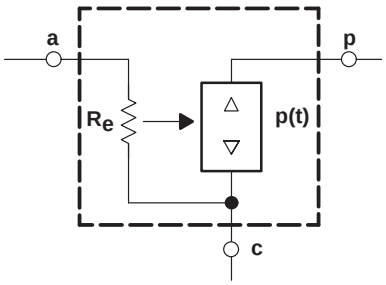

Figure 12. Averaged (Nonlinear) DCM PWM Switch Model

To illustrate discontinuous conduction mode power supply analysis using this model, we examine the buck power stage. The analysis proceeds like the CCM case. The equivalent circuit is substituted into the original circuit. The DCM buck power stage model schematic is shown in the Figure 13.

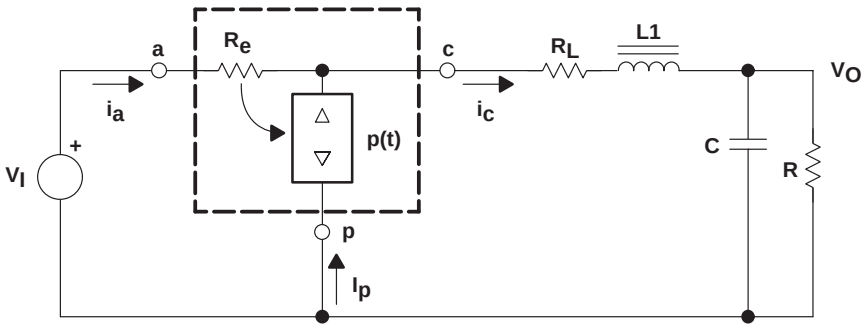

Figure 13. DCM Buck Power Stage DC Model

Notice that this model has the inductor dc resistance included. To illustrate using the model to determine the dc operating point, simply write the equations for the above circuit. This circuit can be described by the network equations shown. First, set the power dissipated in R_e equal to the power delivered by the dependent power source:

$$\frac{\left(V_I - V_{cp}\right)^2}{R_e} = V_{cp} \times I_p$$

Where the current I_p is the difference between I_C and I_A as follows:

$$I_p = I_c - I_a = \frac{V_O}{R} - \frac{V_I - V_{cp}}{R_e}$$

Now, substitute the equation for I_p into the following equation:

$$\frac{\left(V_I - V_{cp}\right)^2}{R_e} = V_{cp} \times \left(\frac{V_O}{R} - \frac{V_I - V_{cp}}{R_e}\right)$$

Now we relate V_{CP} to V_O as follows:

$$V_{cp} = V_O + \left(\frac{V_O}{R}\right) \times R_L$$

The two equations above can be solved to give V_O in terms of V_I and D by eliminating V_{cp} from the two equations and using our previous relationships for R_e and K.

The voltage conversion relationship for the DCM buck is given by:

$$V_O = V_I \times \frac{R}{R + R_L} \times \frac{2}{1 + \sqrt{1 + \frac{4 \times K}{D^2} \times \frac{R}{R + R_L}}}$$

This is similar to our previous steady-state result but with the effects of the inductor resistance included.

To derive the small signal model, the circuit of Figure 13 is perturbed and linearized following a procedure similar to the CCM derivation. To see the details of the derivation, the reader is directed to reference [4] for details. The resulting small signal model for the buck power stage operating in DCM is shown in Figure 14.

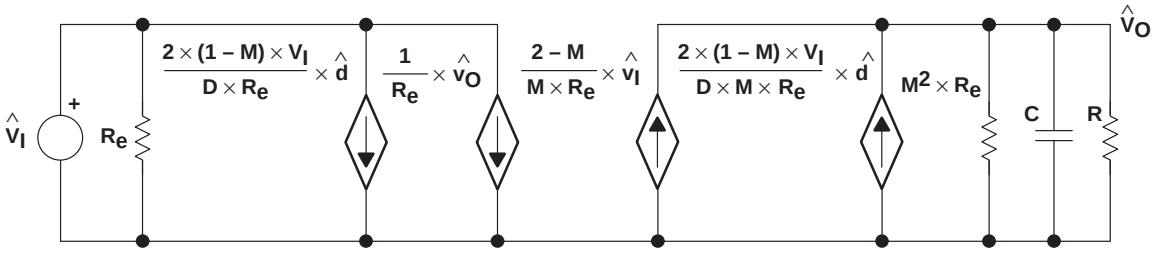

Figure 14. Small Signal DCM PWM Switch Model

The duty-cycle-to-output transfer function for the buck power stage operating in DCM is given by:

$$\frac{\hat{v}_O}{\hat{d}} = G_{do} \times \frac{1}{1 + \frac{s}{\omega_p}}$$

Where

$$G_{do} = \frac{2 \times V_O}{D} \times \frac{1 - M}{2 - M}$$

$$D = M \times \sqrt{\frac{K}{1 - M}}$$

$$M = \frac{V_O}{V_I}$$

$$K = \frac{2 \times L}{R \times T_s}$$

and

$$\omega_p = \frac{2 - M}{1 - M} \times \frac{1}{R \times C}$$

4 Variations of the Buck Power Stage

4.1 Synchronous-Buck Power Stage

A variation of the traditional buck power stage is the synchronous buck power stage. In this power stage, an active switch such as another power MOSFET, Q2 in this example, replaces the rectifier, CR1. The FET is then selected so that its ON-voltage drop is less than the forward drop of the rectifier, thus increasing efficiency. Although this complicates the drive circuit design, the gain in efficiency often makes this an attractive option. Other considerations unique to the synchronous buck power stage are preventing cross–conduction and reverse recovery of the parasitic pn diode internal to a MOSFET. Either the drive circuit or the controller used must insure that both FETs are not on simultaneously; this would place a very low resistance path from the input to ground and destructive currents could flow in the FETs. A small amount of deadtime is necessary.

To explain the reverse recovery problem, realize that in normal operation the internal diode of Q2 conducts for a short period at the beginning of the OFF state during the deadtime. MOSFET Q2 is then turned on at the end of the deadtime and its internal diode turns off. But for duty cycles approaching 1 (and very short conduction time for Q2) Q2 may not be turned on after the deadtime. In that case, the internal diode of Q2 is still conducting at the beginning of a new ON state when MOSFET Q1 is turned on. Increased power dissipation due to the diode reverse recovery current can occur if this happens.

Another characteristic of the synchronous buck power stage is that it always operates in continuous conduction mode (CCM) because current can reverse in Q2. Thus the voltage conversion relationship and the duty-cycle-to-output voltage transfer function for the synchronous buck power stage are the same as for the CCM buck power stage.

A simplified schematic of the Synchronous Buck power stage with a drive circuit block included is shown in Figure 7. Both power switches are n-channel MOSFETs. Sometimes, a p-channel FET is used for Q1, but Q2 is almost always an n-channel FET.

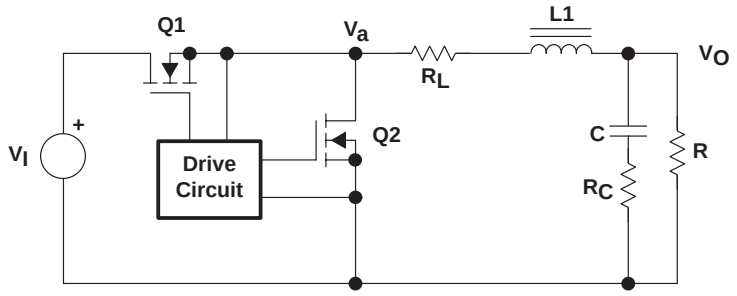

Figure 15. Synchronous Buck Power Stage Schematic

An example design using a synchronous buck power stage and the TL5001 controller is given in *SLVP089 Synchronous Buck Converter Evaluation Module User's Guide*, Texas Instruments Literature Number SLVU001A

Another example design using a synchronous buck power stage and the TPS5210 controller is given in the Application Report *Designing Fast Response Synchronous Buck Regulators Using the TPS5210*, TI Literature Number SLVA044.

A third example design using a synchronous buck power stage and the TPS5633 controller is given in *Synchronous Buck Converter Design Using TPS56xx Controllers in SLVP10x EVMs User's Guide*, Texas Instruments Literature Number SLVU007.

4.2 Forward Converter Power Stage

A transformer-coupled variation of the traditional buck power stage is the forward converter power stage. The power switch is on the primary side of an isolation transformer and a forward rectifier and a catch rectifier are on the secondary side of the isolation transformer. This power stage provides electrical isolation of the input voltage from the output voltage. Besides providing electrical isolation, the isolation transformer can perform step-down (or step-up) of the input voltage to the secondary. The transformer turns ratio can be designed so that reasonable duty cycles are obtained for almost any input voltage/output voltage combination thus avoiding extremely small or extremely high duty cycle values.

The forward converter power stage is very popular in 48-V input telecom applications and 110-VAC or 220-VAC off-line applications for output power levels up to approximately 250 Watts. The exact power rating of the forward converter power stage, of course, is dependent on the input voltage/output voltage combination, its operating environment and many other factors. The capability of obtaining multiple output voltages from a single power stage is another advantage of the forward converter power stage.

A simplified schematic of the forward converter power stage is shown in Figure 16. Not shown in the schematic but necessary for operation is a means of resetting the transformer, T1. There are many ways to accomplish this but a complete discussion is beyond the scope of this report.

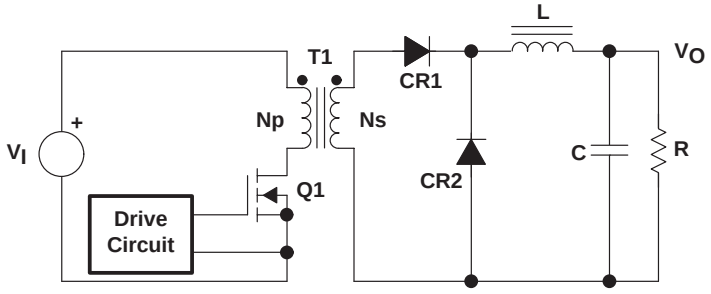

Figure 16. Forward Converter Power Stage Schematic

The simplified voltage conversion relationship for the forward converter power stage operating in CCM is given by:

$$V_O = V_I \times \frac{N_s}{N_p} \times D$$

The simplified voltage conversion relationship for the forward converter power stage operating in DCM is given by:

$$V_O = V_I \times \frac{N_s}{N_p} \times \frac{2}{1 + \sqrt{1 + \frac{4 \times K}{D^2}}}$$

Where K is defined as:

$$K = \frac{2 \times L}{R \times T_s}$$

The simplified duty-cycle-to-output transfer function for the forward converter power stage operating in CCM is given by:

$$\frac{\hat{v}_O}{\hat{d}}(s) = V_I \times \frac{N_s}{N_p} \times \frac{R}{R + R_L} \times \frac{1 + R_c \times C}{1 + s \times \left[C \times \left(R_c + \frac{R \times R_L}{R + R_L} \right) + \frac{L}{R + R_L} \right] + s^2 \times L \times C \times \frac{R + R_C}{R + R_L}}$$

Other power stages which are also variations of the buck power stage include but are not limited to the half-bridge, the full-bridge, and the push-pull power stages.

5 Component Selection

This section presents a discussion of the function of each of the main components of the buck power stage. The electrical requirements and applied stresses are given for each power stage component.

The completed power supply, made up of a power stage and a control circuit, usually must meet a set of minimum performance requirements. This set of requirements is usually referred to as the power supply specification. Many times, the power supply specification determines individual component requirements.

5.1 Output Capacitance

In switching power supply power stages, the function of output capacitance is to store energy. The energy is stored in the capacitor's electric field due to the voltage applied. Thus, qualitatively, the function of a capacitor is to attempt to maintain a constant voltage.

The value of output capacitance of a Buck power stage is generally selected to limit output voltage ripple to the level required by the specification. Since the ripple current in the output inductor is usually already determined, the series impedance of the capacitor primarily determines the output voltage ripple. The three elements of the capacitor that contribute to its impedance (and output voltage ripple) are equivalent series resistance (ESR), equivalent series inductance (ESL), and capacitance (C). The following gives guidelines for output capacitor selection.

For continuous inductor current mode operation, to determine the amount of capacitance needed as a function of inductor current ripple, ΔI_L, switching frequency, f_S, and desired output voltage ripple, ΔV_O, the following equation is used assuming all the output voltage ripple is due to the capacitor's capacitance.

$$C \geq \frac{\Delta I_L}{8 \times f_S \times \Delta V_O}$$

where ΔI_L is the inductor ripple current defined in section 2.1.

For discontinuous inductor current mode operation, to determine the amount of capacitance needed as a function of inductor current ripple, ΔI_L, output current I_O, switching frequency, f_S, and output voltage ripple, ΔV_O, the following equation is used assuming all the output voltage ripple is due to the capacitor's capacitance.

$$C \geq \frac{I_{O(Max)} \times \left(1 - \frac{I_{O(Max)}}{\Delta I_L}\right)^2}{f_S \times \Delta V_O}$$

where ΔI_L is the inductor ripple current defined in section 2.2.

In many practical designs, to get the required ESR, a capacitor with much more capacitance than is needed must be selected.

For both continuous or discontinuous inductor current mode operation and assuming there is enough capacitance such that the ripple due to the capacitance can be ignored, the ESR needed to limit the ripple to ΔV_O V peak-to-peak is:

$$ESR \leq \frac{\Delta V_O}{\Delta I_L}$$

Ripple current flowing through a capacitor's ESR causes power dissipation in the capacitor. This power dissipation causes a temperature increase internal to the capacitor. Excessive temperature can seriously shorten the expected life of a capacitor. Capacitors have ripple current ratings that are dependent on ambient temperature and should not be exceeded. Referring to Figure 3, the output capacitor ripple current is the inductor current, I_L, minus the output current, I_O. The RMS value of the ripple current flowing in the output capacitance (continuous inductor current mode operation) is given by:

$$I_{C\,RMS} = \Delta I_L \frac{\sqrt{3}}{6} = \Delta I_L(0.289).$$

ESL can be a problem by causing ringing in the low megahertz region but can be controlled by choosing low ESL capacitors, limiting lead length (PCB and capacitor), and replacing one large device with several smaller ones connected in parallel.

For some high-performance applications such as a synchronous buck hysteretic regulator controlled by the TPS5210 from Texas Instruments, the output capacitance is selected to provide satisfactory load transient response, because the peak-to-peak output voltage ripple is determined by the TPS5210 controller. For more information, see the Application Report *Designing Fast Response Synchronous Buck Regulators Using the TPS5210*, TI Literature Number SLVA044.

Three capacitor technologies—low-impedance aluminum, organic semiconductor, and solid tantalum—are suitable for low-cost commercial applications. Low-impedance aluminum electrolytics are the lowest cost and offer high capacitance in small packages, but ESR is higher than the other two. Organic semiconductor electrolytics, such as the Sanyo OS-CON series, have become very popular for the power-supply industry in recent years. These capacitors offer the best of both worlds—a low ESR that is stable over the temperature range and high capacitance in a small package. Most of the OS-CON units are supplied in lead-mounted radial packages; surface-mount devices are available but much of the size and performance advantage is sacrificed. Solid-tantalum chip capacitors are probably the best choice if a surface-mounted device is an absolute must. Products such as the AVX TPS family and the Sprague 593D family were developed for power-supply applications. These products offer a low ESR that is relatively stable over the temperature range, high ripple-current capability, low ESL, surge-current testing, and a high ratio of capacitance to volume.

5.2 Output Inductance

In switching power supply power stages, the function of inductors is to store energy. The energy is stored in their magnetic field due to the current flowing. Thus, qualitatively, the function of an inductor is usually to attempt to maintain a constant current or sometimes to limit the rate of change of current flow.

The value of output inductance of a buck power stage is generally selected to limit the peak-to-peak ripple current flowing in it. In doing so, the power stage's mode of operation, continuous or discontinuous, is determined. The inductor ripple current is directly proportional to the applied voltage and the time that the voltage is applied, and it is inversely proportional to its inductance. This was explained in detail previously.

Many designers prefer to design the inductor themselves but that topic is beyond the scope of this report. However, the following discusses the considerations necessary for selecting the appropriate inductor.

In addition to the inductance, other important factors to be considered when selecting the inductor are its maximum dc or peak current and maximum operating frequency. Using the inductor within its dc current rating is important to insure that it does not overheat or saturate. Operating the inductor at less than its maximum frequency rating insures that the maximum core loss is not exceeded, resulting in overheating or saturation.

Magnetic component manufacturers offer a wide range of off-the-shelf inductors suitable for dc/dc converters, some of which are surface mountable. There are many types of inductors available; the most popular core materials are ferrites and powdered iron. Bobbin or rod-core inductors are readily available and inexpensive, but care must be exercised in using them because they are more likely to cause noise problems than are other shapes. Custom designs are also feasible, provided the volumes are sufficiently high.

Current flowing through an inductor causes power dissipation due to the inductor's dc resistance; the power dissipation is easily calculated. Power is also dissipated in the inductor's core due to the flux swing caused by the ac voltage applied across it but this information is rarely directly given in manufacturer's data sheets. Occasionally, the inductor's maximum operating frequency and/or applied volt-seconds ratings give the designer some guidance regarding core loss. The power dissipation causes a temperature increase in the inductor. Excessive temperature can cause degradation in the insulation of the winding and also cause increased core loss. Care should be exercised to insure all the inductor's maximum ratings are not exceeded.

The loss in the inductor is given by:

$$P_{inductor} = I^2_{Lrms} \times R_{Cu} + P_{Core} \approx I^2_O \times R_{Cu} + P_{Core}$$

where, R_{Cu} is the winding resistance.

5.3 Power Switch

In switching power supply power stages, the function of the power switch is to control the flow of energy from the input power source to the output voltage. In a buck power stage, the power switch (Q1 in Figure 1) connects the input to the output filter when the switch is turned on and disconnects when the switch is off. The power switch must conduct the current in the output inductor while on and block the full input voltage when off. Also, the power switch must change from one state to the other quickly in order to avoid excessive power dissipation during the switching transition.

The type of power switch considered in this report is a power MOSFET. Other power devices are available but in most instances, the MOSFET is the best choice in terms of cost and performance (when the drive circuits are considered). The two types of MOSFET available for use are the n-channel and the p-channel. P-channel MOSFETs are popular for use in buck power stages because driving the gate is simpler than the gate drive required for an n-channel MOSFET.

The power dissipated by the power switch is given by:

$$P_{D(MOSFET)} = I_O^2 \times R_{DS(on)} \times D + \frac{1}{2} \times V_I \times I_O \times \left(t_r + t_f\right) \times f_s + Q_{Gate} \times V_{GS} \times f_s$$

Where:

t_r and t_f are the MOSFET turn-on and turn-off switching times
Q_{Gate} is the MOSFET gate-to-source capacitance

Other than selecting p-channel or n-channel, other parameters to consider while selecting the appropriate MOSFET are the maximum drain-to-source breakdown voltage, $V_{(BR)DSS}$, and the maximum drain current, $I_{D(Max)}$.

The MOSFET selected should have a $V_{(BR)DSS}$ rating greater than the maximum input voltage, and some margin should be added for transients and spikes. The MOSFET selected should also have an $I_{D(Max)}$ rating of at least two times the maximum power stage output current. However, many times this is not sufficient margin and the MOSFET junction temperature should be calculated to make sure that it is not exceeded. The junction temperature can be estimated as follows:

$$T_J = T_A + P_D \times R_{\Theta JA}$$

Where:

T_A is the ambient or heatsink temperature
$R_{\Theta JA}$ is the thermal resistance from the MOSFET chip to the ambient air or heatsink.

5.4 Catch Rectifier

The catch rectifier conducts when the power switch turns off and provides a path for the inductor current. Important criteria for selecting the rectifier include: fast switching, breakdown voltage, current rating, low–forward voltage drop to minimize power dissipation, and appropriate packaging. Unless the application justifies the expense and complexity of a synchronous rectifier, the best solution for low–voltage outputs is usually a Schottky rectifier. The breakdown voltage must be greater than the maximum input voltage, and some margin should be added for transients and spikes. The current rating should be at least two times the maximum power stage output current (normally the current rating will be much higher than the output current because power and junction temperature limitations dominate the device selection).

The voltage drop across the diode in a conducting state is primarily responsible for the losses in the diode. The power dissipated by the diode can be calculated as the product of the forward voltage and the output load current for the time that the diode is conducting. The switching losses which occur at the transitions from conducting to nonconducting states are very small compared to conduction losses and are usually ignored.

The power dissipated by the catch rectifier is given by:

$$P_{D(Diode)} = V_D \times I_O \times (1 - D)$$

where V_D is the forward voltage drop of the catch rectifier.

The junction temperature can be estimated as follows:

$$T_J = T_A + P_D \times R_{\Theta JA}$$

6 Example Designs

An example design using a buck power stage, the TPS2817 MOSFET driver, and the TL5001 controller is given in *SLVP097 Buck Converter Evaluation Module User's Guide*, Texas Instruments Literature Number SLVU002A.

Another example design using a buck power stage and the TL5001 controller is given in *SLVP087 Buck Converter Evaluation Module User's Guide*, Texas Instruments Literature Number SLVU003A.

A third example design using a buck power stage, the TPS2817 MOSFET driver, and the TL5001 controller is given in *SLVP101, SLVP102, and SLVP103 Buck Converter Design Using the TL5001 User's Guide*, Texas Instruments Literature Number SLVU005.

7 Summary

This application report described and analyzed the operation of the buck power stage. The two modes of operation, continuous conduction mode and discontinuous conduction mode, were examined. Steady-state and small-signal were the two analyses performed on the buck power stage. The synchronous buck power stage and the forward converter power stage were presented as variations of the basic buck power stage and a few of the other possible variations were listed.

The main results of the steady-state analyses are summarized below.

The voltage conversion relationship for CCM is:

$$V_O = \left(V_I - V_{DS}\right) \times D - V_d \times (1 - D) - I_L \times R_L$$

which simplifies to:

$$V_O = V_I \times D$$

The voltage conversion relationship for DCM is:

$$V_O = V_I \times \frac{R}{R + R_L} \times \frac{2}{1 + \sqrt{1 + \frac{4 \times K}{D^2} \times \frac{R}{R + R_L}}}$$

where K is defined as:

$$K = \frac{2 \times L}{R \times T_S}$$

The DCM voltage conversion relationship can be simplified to:

$$V_O = V_I \times \frac{2}{1 + \sqrt{1 + \frac{4 \times K}{D^2}}}$$

The major results of the small-signal analyses are summarized below.

The small-signal duty-cycle-to-output transfer function for the buck power stage operating in CCM is given by:

$$\frac{\hat{v}_O}{\hat{d}}(s) = V_I \times \frac{R}{R + R_L} \times \frac{1 + R_c \times C}{1 + s \times \left[C \times \left(R_c + \frac{R \times R_L}{R + R_L} \right) + \frac{L}{R + R_L} \right] + s^2 \times L \times C \times \frac{R + R_C}{R + R_L}}$$

The small-signal duty-cycle-to-output transfer function for the buck power stage operating in DCM is given by:

$$\frac{\hat{v}_O}{\hat{d}} = G_{do} \times \frac{1}{1 + \frac{s}{\omega_p}}$$

Where

$$G_{do} = \frac{2 \times V_O}{D} \times \frac{1 - M}{2 - M}$$

and

$$\omega_p = \frac{2 - M}{1 - M} \times \frac{1}{R \times C}$$

Also presented were requirements for the buck power stage components based on voltage and current stresses applied during the operation of the buck power stage.

For further study, several references are given in addition to example designs.

8 References

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