COSE222 Computer Architecture
Final Project 3rd Milestone
(25% credit towards final project)

No late turn-in accepted

Add new instructions to the provided single-cycle CPU, so that the 2 programs in the zip file can be executed on the new CPU. The programs will display `5` and `A` alternatively on HEX0 of the DE0 board with some interval of time if the CPU is implemented correctly.

http://esca.korea.ac.kr/teaching/cose222_CA/milestones/RISCV/final-project_m3.7z

Design Requirement:

- You are free to change anything in the given CPU **except** the register file
  - The provided register file has 2 read ports and 1 write port.

You should probably follow the steps below;

1. Compile the programs under Eclipse environment and generate the RV32I code
2. Open `labcode.dump` to see what kinds of RV32I instructions you should implement
   - ✓ Figure out which instructions are already there in the provided CPU and what are not there
3. Implement those new instructions to the provided single-cycle CPU
4. **Simulate with ModelSim** to debug and validate your design
5. Synthesize the single-cycle CPU with the `mif` file
6. Download the bitstream to the DE0 board.

What and How to submit:

- Create a (up to) 3-min video clip (with your smartphone or any other convenient means), showing
  - Your smiling face to camera
  - 7 segment output on DE0 board

  AND **verbally** explaining the followings:
  - **What instructions** you added to the CPU, and **how you figured out those instructions** to be added to the CPU
  - **CPU design change** (please elaborate this!)
  - **ModelSim simulation output**

- Upload **both** the video clip **and** zipped Verilog source to Blackboard

Note: This is an individual project. You are welcome to discuss, but DO NOT COPY solutions. If you are found to copy solutions from others or slightly modify the solutions from others, both of you will be given 0 credits.