

## COSE222 Computer Architecture Final Project 4<sup>th</sup> Milestone (20% credit towards final project)

**No late turn-in accepted**

Based on the Single-cycle CPU you have designed for the 3<sup>rd</sup> milestone, implement the **pipelining with data hazard detection and handling logic**. As studied in the class, the pipelining incurs hazards (structural, data and control hazards). Among them, the structural hazard does not occur in our CPU since memory provides 2 ports: one port for instruction access and the other for data access. The purpose of the 4<sup>th</sup> milestone is to implement pipelining and detect/resolve the data hazard.

Your pipelined version of CPU should be able to execute the following code. It will display 1, 2, 3, and 4 on HEX3 ~ HEX0 if the CPU is implemented correctly.

[http://esca.korea.ac.kr/teaching/cose222\\_CA/milestones/RISCV/final-project\\_m4.7z](http://esca.korea.ac.kr/teaching/cose222_CA/milestones/RISCV/final-project_m4.7z)

Note that when you change and/or modify the Verilog code, add the comment lines in the source. Following is an example.

```
// ##### Taeweon Suh: Start #####  
  
    assign branch_DE = branch_D & branch_E;  
  
// ##### Taeweon Suh: End #####
```

You should probably follow the steps below;

1. Compile the code under Eclipse and generate the RV32I binary.
2. Test-run it on your single-cycle CPU to make sure that it displays the numbers.
3. Implement the pipelining with data hazard detection and handling.
4. **Simulate with ModelSim** to debug and validate your design.
5. Synthesize the pipelined CPU with the `mif` using Quartus-II.
6. Download the bitstream to the DE0 board.

**What and How to submit:**

- Create a (up to) 3-min video clip (with your smartphone or any other convenient means), showing
  - Your smiling face to camera
  - 7 segment output on DE0 board

AND **verbally** explaining the followings:

- **What instructions** you added to the CPU, and **how you figured out those instructions** to be added to the CPU
  - **CPU design change** (please elaborate this!)
  - **ModelSim simulation output**
- Upload **both the video clip and zipped Verilog source** to Blackboard

**Note: This is an individual project. You are welcome to discuss, but DO NOT COPY solutions. If you are found to copy solutions from others or slightly modify the solutions from others, both of you will be given 0 credits.**