LS1043ARDBGSG

QorIQ LS1043A Reference Design Board Getting Started Guide

Rev. 8 — 08 May 2019 User's Guide

Contents

1 Introduction

The QorIQ® LS1043A reference design board (LS1043ARDB) is a reference platform designed to exercise most capabilities of the QorIQ LS1043A processor. This document describes different components of the LS1043ARDB and explains how to get the board up and running.

The LS1043ARDB functions with an integrated development environment (IDE), such as CodeWarrior Development Studio. For instructions on how to work with the CodeWarrior Development Studio IDE, see CodeWarrior Development Studio for QorIQ LS series - ARM V8 ISA, Targeting Manual.

2 Related documentation

The table below lists and explains the additional documents and resources that you can refer to for more information on the LS1043ARDB. Some of the documents listed below may be available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local NXP field applications engineer (FAE) or sales representative.

Table 1. Related documentation

Document	Description	Link / how to access
QorIQ LS1043A Reference Design Board Reference Manual	Provides a detailed description of the LS1043ARDB	LS1043ARDBRM.pdf
QorIQ LS1043A Product Brief	Provides a brief overview of the LS1043A processor	LS1043APB.pdf
QorIQ LS1043A Data Sheet	Provides information about electrical characteristics, hardware design considerations, and ordering information	LS1043A.pdf
QorIQ LS1043A Family Reference Manual	Provides a detailed description about the LS1043A QorIQ multicore processor and its features, such as memory map, serial interfaces, power supply, chip features, and clock information	LS1043ARM.pdf

Table continues on the next page...

Table 1. Related documentation (continued)

Document	Description	Link / how to access
QorIQ LS1043A Chip Errata	Lists the details of all known silicon errata for the LS1043A	Contact FAE / sales representative
QorIQ LS1043A Design Checklist, AN5012	This document provides recommendations for new designs based on the LS1043A. This document can also be used to debug newly designed systems by highlighting those aspects of a design that merit special attention during initial system start-up.	AN5012.pdf
Layerscape Software Development Kit Documentation	This document describes how to work with LSDK, which is a complete Linux kit for NXP QorIQ ARM-based SoCs and the reference and evaluation boards available for them.	Layerscape Software Development Kit
CodeWarrior Development Studio for QorIQ LS series - ARM V8 ISA, Targeting Manual	This manual explains how to use the CodeWarrior Development Studio for QorIQ LS series - ARM V8 ISA product.	CodeWarrior Development Studio for QorIQ LS series - ARM V8 ISA, Targeting Manual
CodeWarrior TAP Probe User Guide	Provides details of CodeWarrior® TAP, which enables target system debugging through a standard debug port (usually JTAG) while connected to a developer workstation through Ethernet or USB	CodeWarrior TAP Probe User Guide

3 Hardware kit contents

The table below lists the items included in the LS1043ARDB hardware kit.

Table 2. Hardware kit contents

Item	Description
LS1043ARDB hardware assembly with enclosure	
Universal AC input adapter	To convert the AC adapter plug to any type of standard plug
12 V, 5 A AC-DC power adapter	An external 12 V power adapter to power the board
USB Type A to mini-B cable	To make a console connection from mini-USB port on chassis front panel
RJ45-to-DB9F cable	To make a console connection from UART1 port on chassis back panel

Table continues on the next page...

Table 2. Hardware kit contents (continued)

Item	Description
Ethernet cable, straight through wiring, 6 ft min, RoHS compliant	To connect the board to network to get updated board software
Thermal pad	To be placed between the board and a Wi-Fi card for cooling purposes
A zip lock bag containing Wi-Fi card assembly accessories	To fasten Wi-Fi card on the board
LS1043ARDB insert card	A color printed card that provides quick link to the LS1043ARDB product summary page

4 Chassis and board pictures

The figure below shows the front panel of the LS1043ARDB chassis.

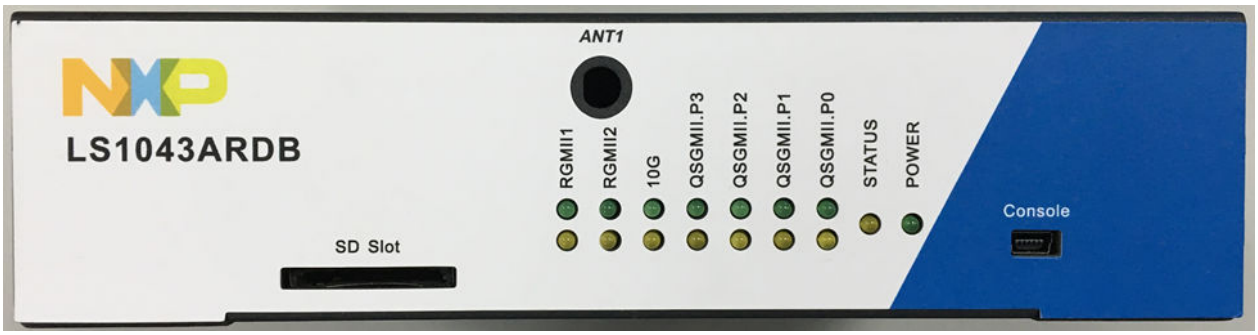

Figure 1. LS1043ARDB chassis front panel

The figure below shows the back panel of the LS1043ARDB chassis, with power and reset buttons highlighted.

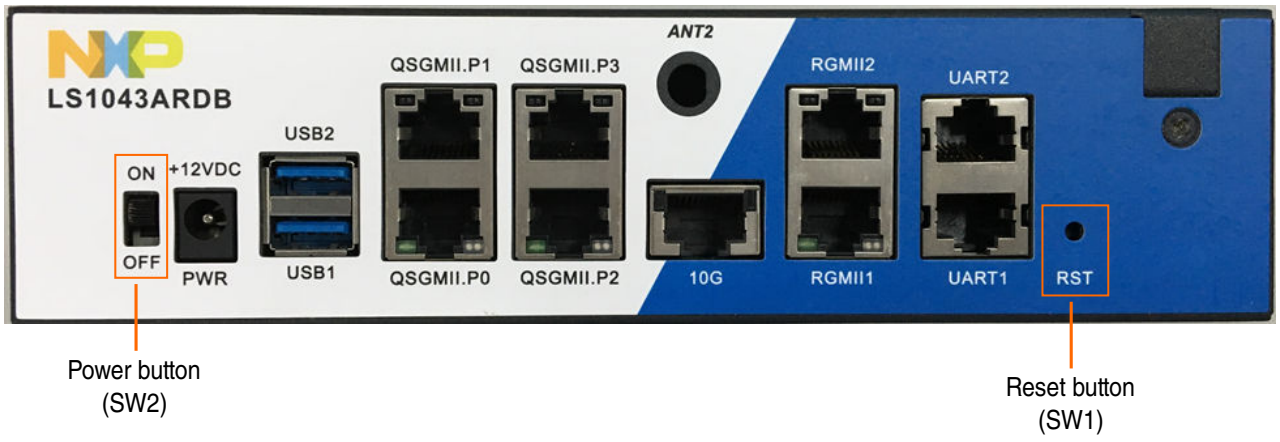

Figure 2. LS1043ARDB chassis back panel

The figure below shows the different connectors available on the LS1043ARDB.

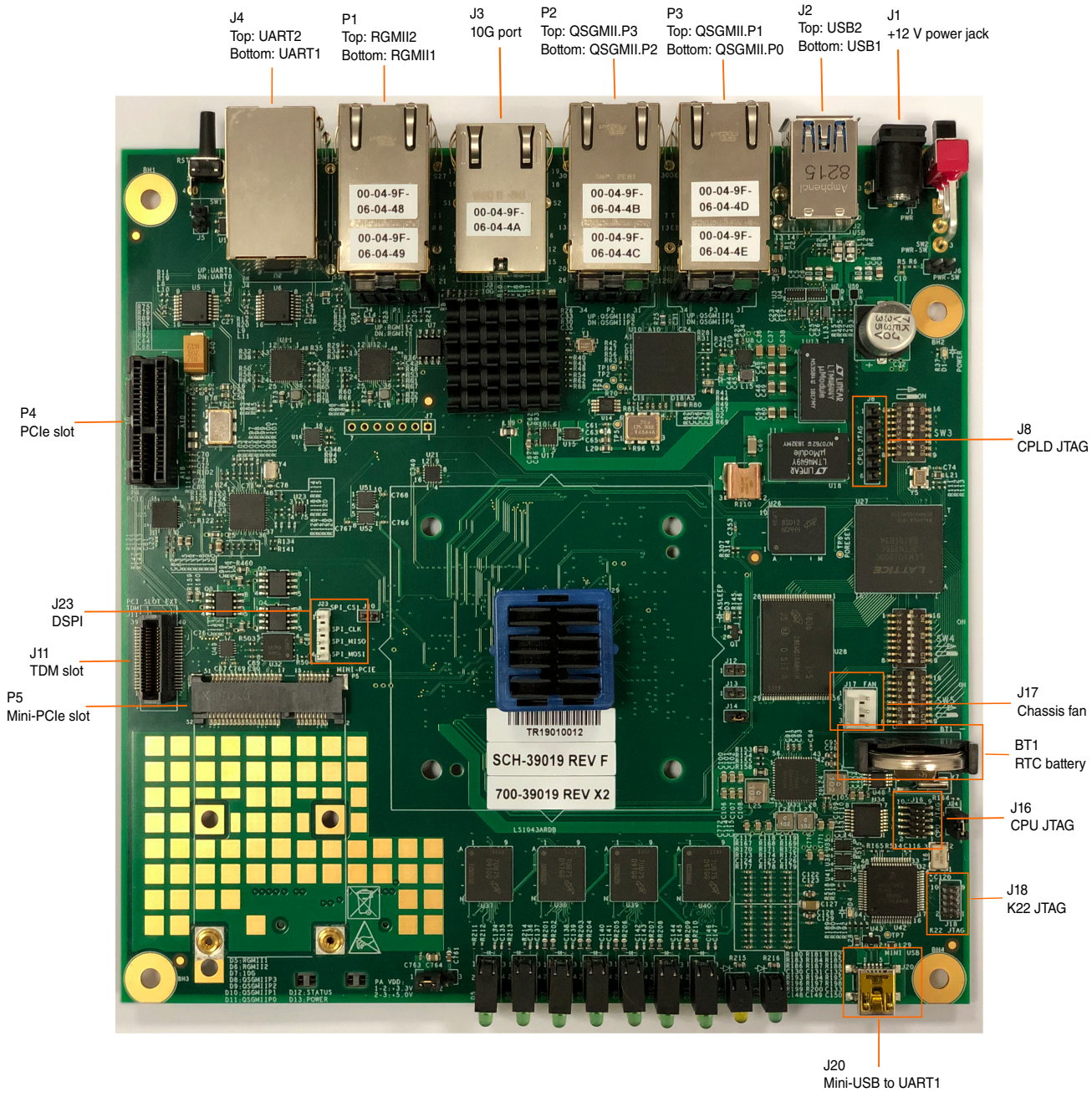

Figure 3. LS1043ARDB connectors

The figure below shows the jumpers available on the LS1043ARDB.

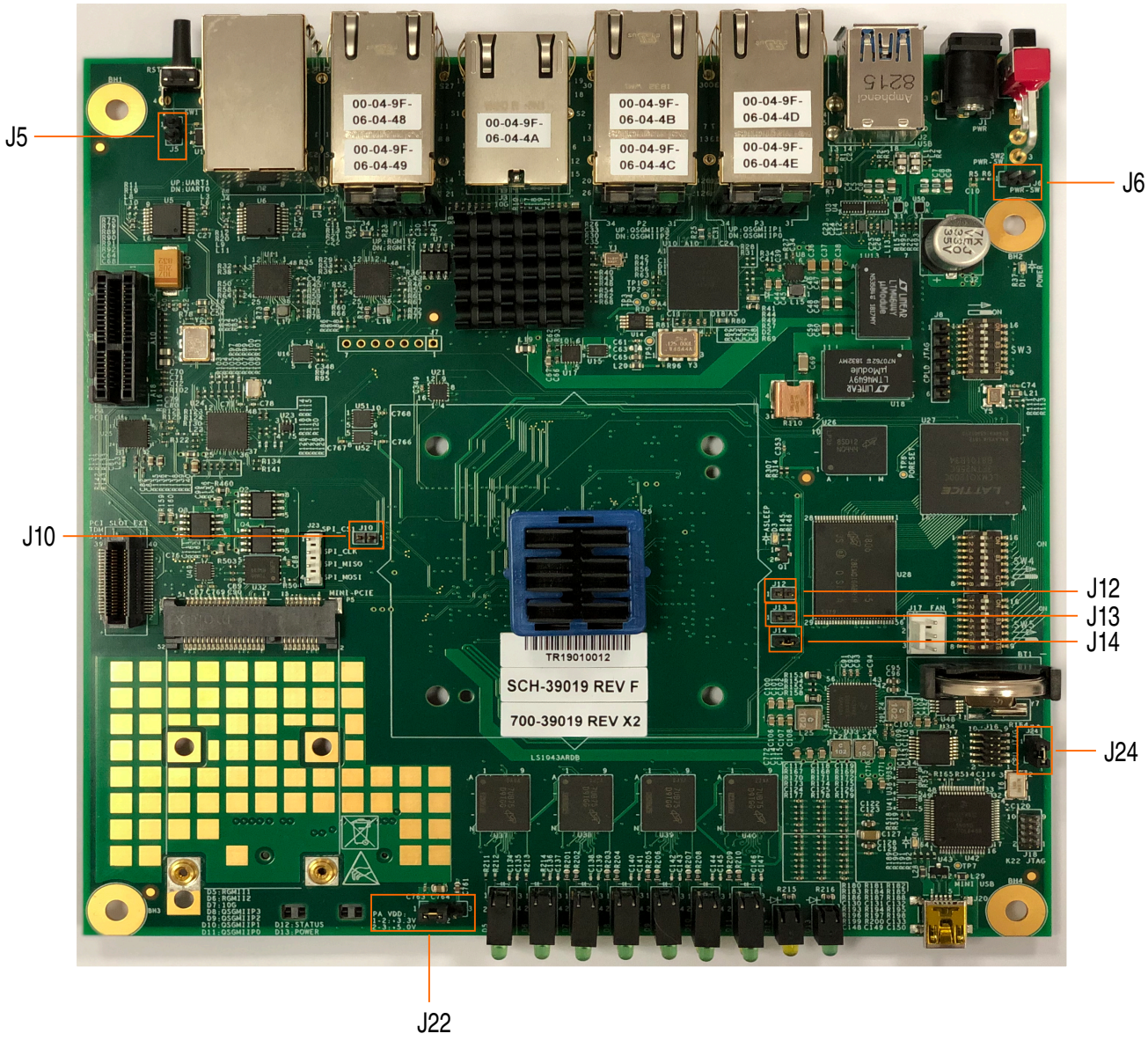

Figure 4. LS1043ARDB jumpers

The figure below shows the dual inline package (DIP) switches available on the LS1043ARDB. The DIP switches are arranged along the edge of the board.

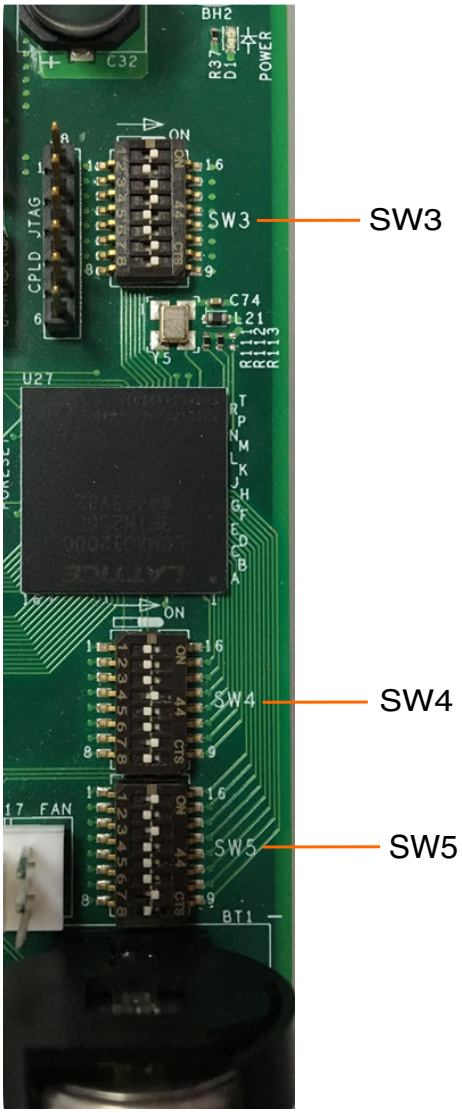

Figure 5. LS1043ARDB DIP switches

The figure below shows the light emitting diodes (LEDs) available on the LS1043ARDB.

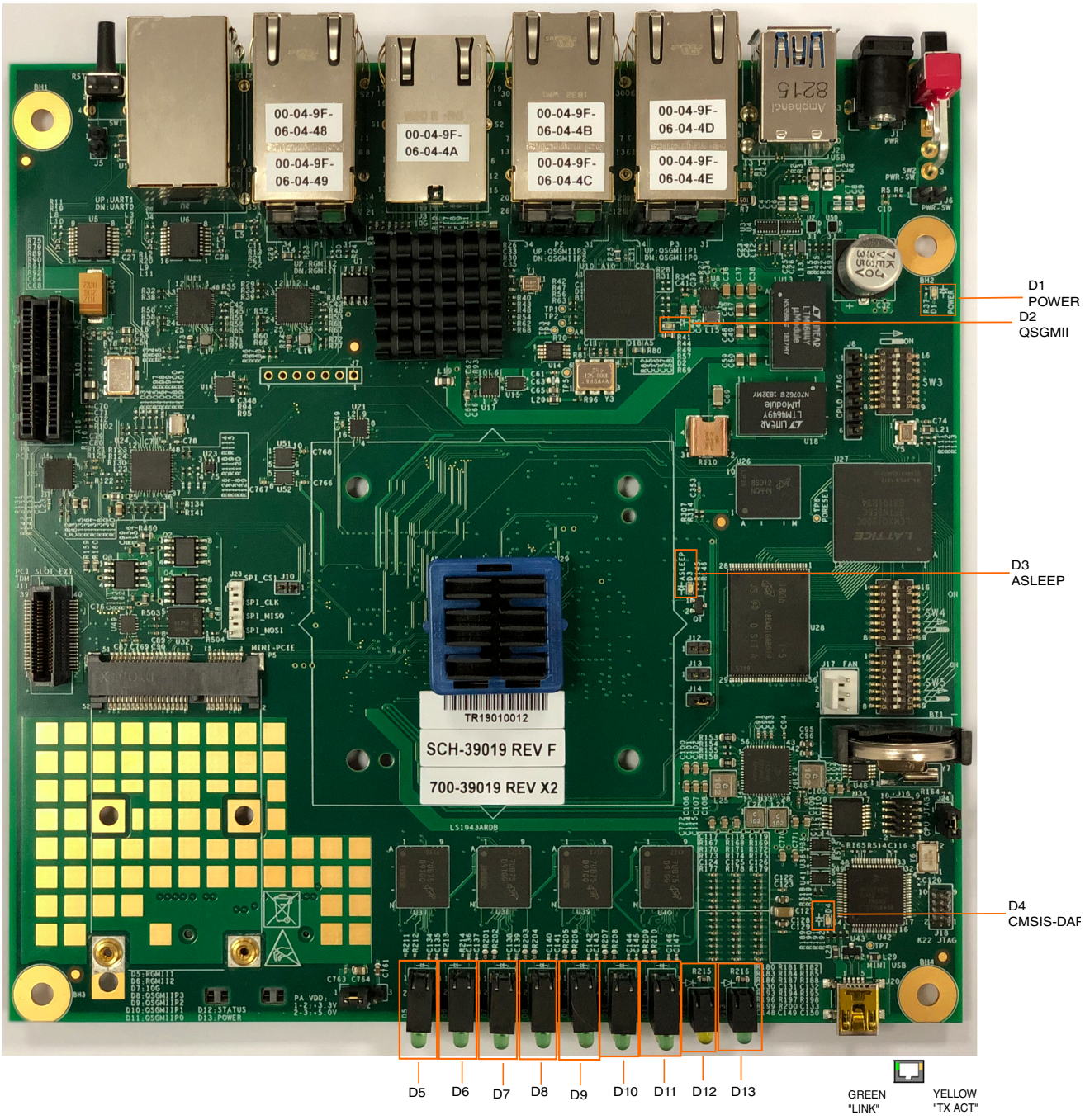

Figure 6. LS1043ARDB LEDs

5 Power and reset buttons

The power and reset buttons are present on the back panel of the LS1043ARDB chassis (see Figure 2. on page 3). The table below describes the power and reset buttons.

Table 3. Power and reset buttons

Switch	Label	Function	Description
SW1	RESET	System reset	Press SW1 to reset the system, including the device and all attached peripherals.
SW2	PWR	Power cycle	Slide SW2 to turn the power ON or OFF. **NOTE** If J6 is shorted, to force power on, then SW2 will have no effect.

6 Connectors

The LS1043ARDB has numerous onboard connectors (see Figure 3. on page 4). The table below describes the LS1043ARDB connectors.

Table 4. LS1043ARDB connectors

Part identifier	Connector type	Description	Typical connection
J1	DC power jack	12 V power jack	Connects to 12 V, 5 A power supply
J20	Mini-USB connector	Console (mini-USB to UART1) port	Connects to host computer
J21	SD card receptacle	SD card slot. It is located on the back side (bottom side) of the PCB.	Provides access to an SDHC/SDXC card
P1	RJ45 connector (2)	Dual-port (stacked) 10/100/1000M Ethernet connector: • RGMII1 (bottom) • RGMII2 (top)	Connects to external RJ45 Ethernet cables
P2	RJ45 connector (2)	Dual-port (stacked) QSGMII Ethernet connector: • Port 2 (bottom) • Port 3 (top)	Connects to external RJ45 Ethernet cables
P3	RJ45 connector (2)	Dual-port (stacked) QSGMII Ethernet connector: • Port 0 (bottom) • Port 1 (top)	Connects to external RJ45 Ethernet cables
J3	RJ45 connector	10G Ethernet port	Connects to an external RJ45 Ethernet cable
J2	USB 3.0 Type A connector (2)	Dual-port (stacked) USB Type A connector: • USB1 (bottom) • USB2 (top)	Connects to USB-compatible devices

Table continues on the next page...

Table 4. LS1043ARDB connectors (continued)

Part identifier	Connector type	Description	Typical connection
J4	RJ45 connector (2)	Dual-port (stacked) UART connector: • UART1 (bottom) • UART2 (top)	Connects to the RJ45 to DB9 serial cables
J23	1x4 connector	DSPI header	Connector for DSPI (CS1) signals
P4	PCIe connector	PCIe x1 slot	Connector for a PCIe x1 card
P5	Mini-PCIe connector	Mini-PCIe slot	Connector for a mini-PCIe card
J16	2x5 connector	Arm JTAG header (CPU JTAG)	Connects to the CodeWarrior TAP
J18	2x5 connector	Arm JTAG header (K22 MCU JTAG)	Connects to the JLINK emulation
J8	1x6 connector	JTAG header (CPLD JTAG)	Connects to the CPLD programmer
J17	1x3 connector	Chassis fan header	Provides 12 V power for cooling chassis fan
J11	2x20 connector	TDM slot	Connector for an adapter card that has slots for connecting a TDM riser card
BT1	3-pin battery holder	RTC battery	Connects to a 3 V coin battery

7 Jumpers

Jumpers (or shorting headers) are used to select some options that either do not change often or involve power conduction. The LS1043ARDB jumpers are shown in Figure 4. on page 5 and are described in the table below.

Table 5. LS1043ARDB jumpers

Part identifier	Jumper type	Description	Jumper settings
J24	1x2 connector	CMSIS-DAP reset processor header	• Open: Disable reset function. If you use Telnet serial port, then keep J24 in "Open" state; otherwise, it will cause board reset. • Shorted: Enable reset function. If use CMSIS-DAP to reset board, then keep J24 in "Shorted" state. (default setting)
J22	1x3 connector	Power amplifier (PA) voltage selection header (required for some Wi-Fi cards)	• 1-2 shorted: PA voltage = 3.3 V (default setting) • 2-3 shorted: PA voltage = 5 V
J5	1x2 connector	Remote reset header	• Open: No activity (default setting) • Shorted: Reset the board

Table continues on the next page...

Table 5. LS1043ARDB jumpers (continued)

Part identifier	Jumper type	Description	Jumper settings
J6	1x2 connector	Power switch header	• Open: Power switch is functional (default setting) • Shorted: Power switch is disabled
J13	1x2 connector	TA_PROG_SFP voltage control header	• Open: TA_PROG_SFP pin of the processor is powered off (default setting) • Shorted: TA_PROG_SFP pin is powered by OVDD (1.8 V)
J14	1x2 connector	TA_BB_VDD voltage control header	• Open: TA_BB_VDD pin of the processor is powered off • Shorted: TA_BB_VDD pin is powered by VDD (1 V) (default setting)
J10	1x2 connector	FA_VL voltage control header (for NXP use only)	• Open: FA_VL pin of the processor is powered off (default setting) • Shorted: FA_VL pin is powered by VDD (1 V)
J12	1x2 connector	PROG_MTR voltage control header (for NXP use only)	• Open: PROG_MTR pin of the processor is powered off (default setting) • Shorted: PROG_MTR pin is powered by OVDD (1.8 V)

8 DIP switches

The LS1043ARDB has three DIP switches, SW3, SW4, and SW5, which are shown in Figure 5. on page 6. For LS1043ARDB DIP switches:

- When a switch is OFF, the value is 0
- When a switch is ON, the value is 1

The LS1043ARDB DIP switches are described in the following subsections:

- SW3 switch on page 10
- SW4 switch on page 12
- SW5 switch on page 13

8.1 SW3 switch

The figure below shows the SW3 switch on the LS1043ARDB.

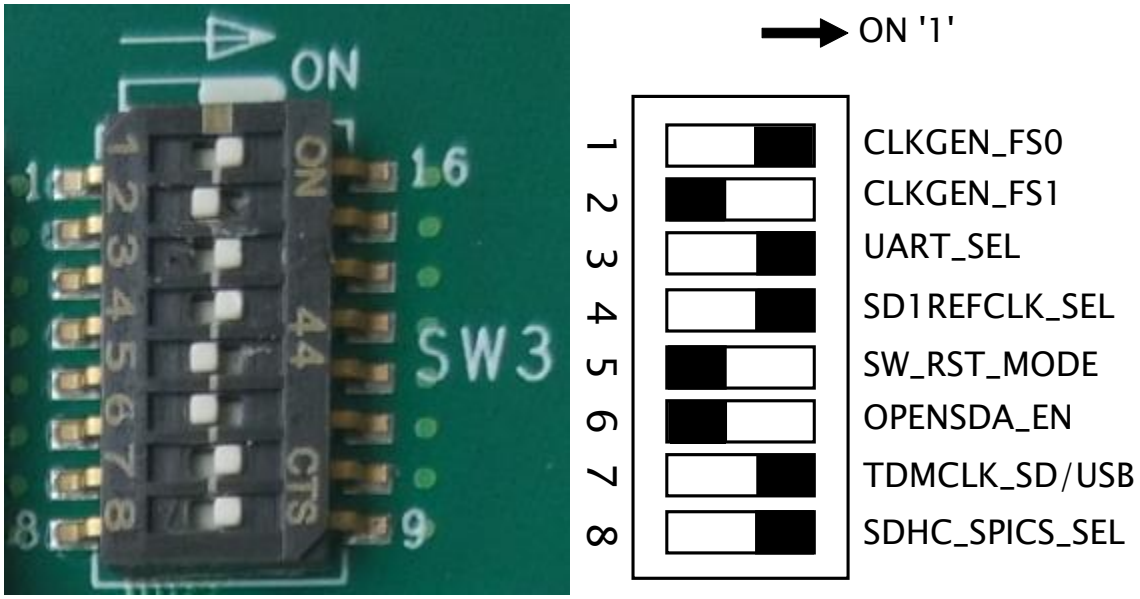

Figure 7. SW3 switch

The table below describes the SW3 settings.

Table 6. SW3 settings

Switch	Name	Description
SW3[1]	CLKGEN_FS0	SYSCLK frequency select • 00: 66.66 MHz • 01: 80 MHz • 10: 100 MHz (default setting) • 11: 83 MHz **NOTE** SW3[1:2] settings are only valid if SW5[2] = 1 (single-ended SYSCLK). SW3[1:2] settings have no impact if SW5[2] = 0 (fixed 100 MHz differential SYSCLK).
SW3[2]	CLKGEN_FS1	
SW3[3]	UART_SEL	UART1 output select • 0: RJ45, J4 lower one • 1: CMSIS-DAP, mini-USB port (default setting)
SW3[4]	SD1REFCLK_SEL	SD1 REFCLK select • 0: 100 MHz • 1: 156.25 MHz (default setting)

Table continues on the next page...

Table 6. SW3 settings (continued)

Switch	Name	Description
SW3[5]	SW_RST_MODE	Software reset mode • 0: Trigger system reset on RESET_REQ_B assertion (default setting) • 1: Ignore RESET_REQ_B assertion
SW3[6]	OPENSDA_EN	CMSIS-DAP JTAG forced disable • 0: JTAG can be used by header or CMSIS-DAP (default setting) • 1: CMSIS-DAP JTAG is forced to be disabled
SW3[7]	TDMCLK_SDHC/USB	TDM CLK or SDHC/USB select • 0: TDM CLK • 1: SDHC/USB (default setting)
SW3[8]	SDHC_SPICS	SDHC_VS or SPI_CS0 select • 0: SDHC_VS • 1: SPI_CS0 (default setting)

8.2 SW4 switch

The figure below shows the SW4 switch on the LS1043ARDB.

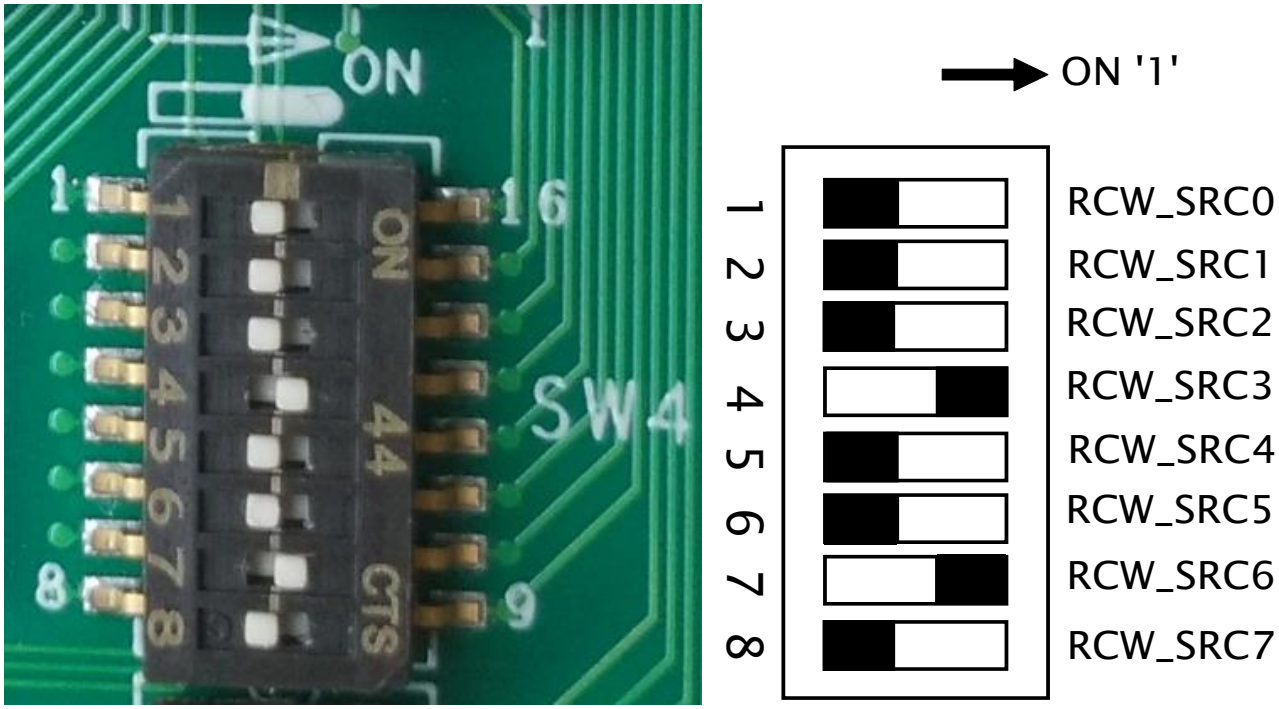

Figure 8. SW4 switch

The table below describes the SW4 settings.

Table 7. SW4 settings

Switch	Name	Description
SW4[1]	RCW_SRC0	RCW_SRC[0:8] select • 0_0010_0101: 16-bit NOR (default setting) • 0_0100_0000: SDHC/eMMC • 0_1001_1111: Hardcoded RCW • 1_0000_0110: 8-bit NAND flash, 2 KB page, 64 pages/ block **NOTE** The RCW_SRC field (9 bits) is spread over SW4 and SW5.
SW4[2]	RCW_SRC1	
SW4[3]	RCW_SRC2	
SW4[4]	RCW_SRC3	
SW4[5]	RCW_SRC4	
SW4[6]	RCW_SRC5	
SW4[7]	RCW_SRC6	
SW4[8]	RCW_SRC7	
SW5[1]	RCW_SRC8	

8.3 SW5 switch

The figure below shows the SW5 switch on the LS1043ARDB.

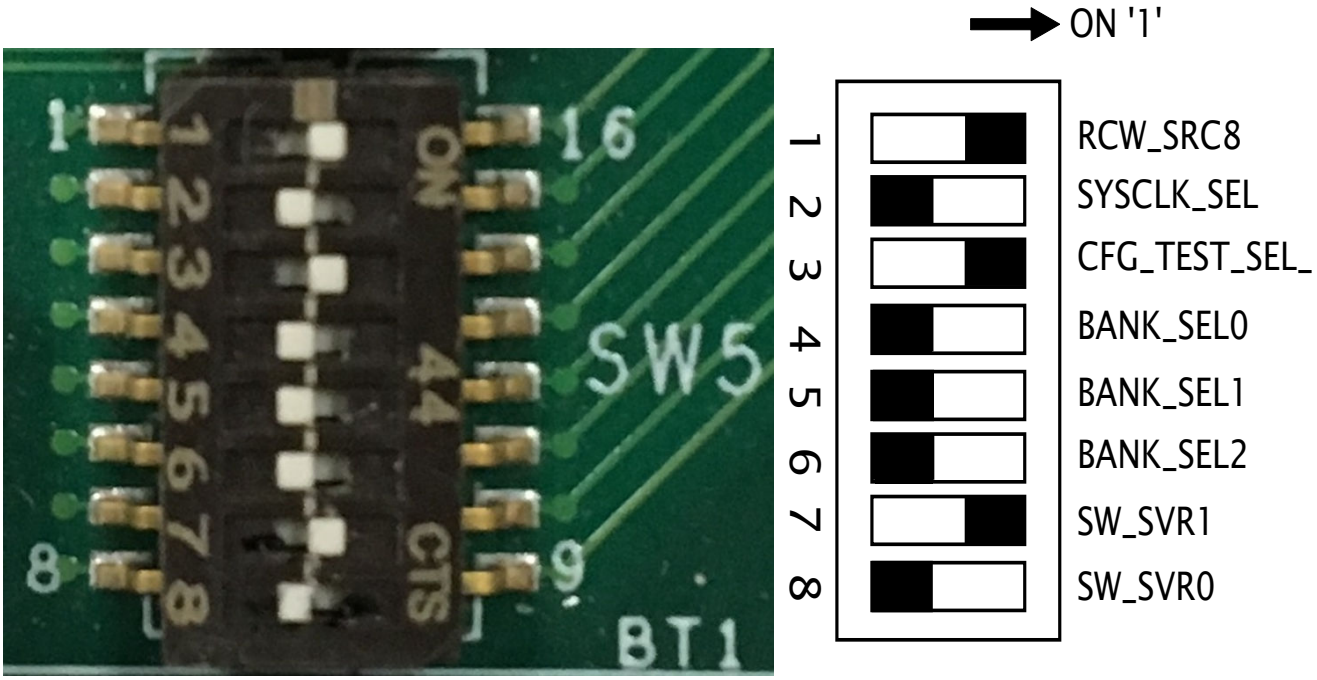

Figure 9. SW5 switch

The table below describes the SW5 settings.

Table 8. SW5 settings

Switch	Name	Description
SW5[2]	SYSCLK_SEL	Differential SYSCLK select • 0: Differential SYSCLK (default setting) • 1: Single-ended system clock
SW5[3]	CFG_TEST_SEL_B	CFG_TEST_SEL for the LS1043A processor • 0: Disables cores 3 and 4 • 1: Enables all cores (default setting)
SW5[4]	BANK_SEL0	Virtual bank select SW5[6:4] • 000: Virtual bank 0 (default setting) • 001: Virtual bank 1 • … … • 100: Virtual bank 4 • … … • 111: Virtual bank 7
SW5[5]	BANK_SEL1	
SW5[6]	BANK_SEL2	
SW5[7]	SW_SVR1	SVR[1:0] • 10: Reserved (default setting)
SW5[8]	SW_SVR0	

9 LEDs

The LS1043ARDB LEDs are shown in Figure 6. on page 7 and are described in the table below.

Table 9. LS1043ARDB LEDs

LED	Color	Positioned on	Name	Description
D1	Green	PCB	Power LED (3.3 V)	• OFF: 3.3 V power is OFF • ON: 3.3 V power is supplied
D13	Green	Chassis		
D2	RED	PCB	QSGMII F104S8A	• ON: PHY fast link fail • OFF: PHY fast link good
D3	Green	PCB	ASLEEP	• ON: If the processor is not configured properly, or if the RCW contents are not correct • OFF: RCW is fetched
D4	Green	PCB	K22	• ON: CMSIS-DAP firmware is loaded • OFF: CMSIS-DAP firmware is not loaded
D5	Yellow/green	Chassis	RGMII1	• Green: RGMII1 link • Yellow: RGMII1 activity
D6	Yellow/green	Chassis	RGMII2	• Green: RGMII2 link • Yellow: RGMII2 activity
D7	Yellow/green	Chassis	10G	• Green: AQR105 10G PHY link • Yellow: AQR105 10G PHY activity
D8	Yellow/green	Chassis	QSGMII.P3	• Green: QSGMII P3 link • Yellow: QSGMII P3 activity
D9	Yellow/green	Chassis	QSGMII.P2	• Green: QSGMII P2 link • Yellow: QSGMII P2 activity
D10	Yellow/green	Chassis	QSGMII.P1	• Green: QSGMII P1 link • Yellow: QSGMII P1 activity
D11	Yellow/green	Chassis	QSGMII.P0	• Green: QSGMII P0 link • Yellow: QSGMII P0 activity
D12	Yellow	Chassis	Status LED	Controlled through CPLD register, CPLD_STATUS_LED. See QorIQ LS1043A Reference Design Board Reference Manual for more details.

10 Getting started with LS1043ARDB

This section explains:

10.1 Prerequisites

To set up your LS1043ARDB, you need the items listed in the table below.

Table 10. Prerequisites

Item	Available in board kit?	Purpose / required action
Hardware		
Host computer system capable of running a terminal emulator	No	Host computer (for example, Windows PC, Linux system, or Mac) to control and monitor the LS1043ARDB from the serial console via a serial terminal emulator, such as Tera Term. **NOTE** You can also use a Linux machine to connect to the board console via a Linux utility, such as minicom.
12 V AC-DC power adapter	Yes	To connect the board to AC power supply
USB Type A to mini-B cable	Yes	To make a console connection from mini-USB port on chassis front panel
Ethernet cable	Yes	To connect the board to network to get updated board software
CodeWarrior TAP (optional)	No	To debug and control the board using CodeWarrior Development Studio for QorIQ LS series - ARM V8 ISA. You can order a CodeWarrior TAP from nxp.com.
Software		
mbed Windows serial port driver	No	To make the host computer allow a serial connection with the board. Download and install it on the host computer from https://developer.mbed.org/handbook/Windows-serial-configuration.
Tera Term (serial terminal emulator)	No	To configure serial connection and to see console prints. Download and install it on the host computer from Internet.
CodeWarrior Development Studio for QorIQ LS series - ARM V8 ISA (optional)	No	To debug and control the board. You can order it from nxp.com.

10.2 Booting LS1043ARDB

When power is supplied to the board, the boot loader (U-Boot) image located in NOR flash virtual bank 0 runs, if the board is configured with the default switch settings.

Follow these steps to boot the board:

1. Ensure that you have met the prerequisites described in Table 10. Prerequisites on page 16.
2. Open the chassis top cover and ensure that the board is configured with the default switch settings, as shown in the table below.

Table 11. Default switch settings

	1	2	3	4	5	6	7	8
SW3	1	0	1	1	0	0	1	1
SW4	0	0	0	1	0	0	1	0
SW5	1	0	1	0	0	0	1	0

3. Verify that the board has default jumper settings (see Jumpers on page 9).
4. Connect the power jack available on chassis back panel to the wall mount power switch through the 12 V AC-DC power adapter and turn ON the wall mount power switch.
5. Turn ON the power switch available on the chassis back panel. The power LEDs on chassis front panel (D13) and PCB (D1) turn ON. The ASLEEP LED (D3) also turns ON and turns OFF immediately, indicating that correct RCW has been loaded.
6. Connect one end (Type A) of the USB Type A to mini-B cable to the USB port of the host computer and other end (mini-B) to the "Console" (mini-USB) port on the chassis front panel (see figure below). The D4 LED on the PCB turns ON. The host computer will automatically install the USB driver and will detect the USB device.

NOTE

Ensure that SW3[3] is set to 1 (ON) before making the console connection.

If you are using a Windows 10 machine as the host computer, then stop the storage service of the Windows machine before plugging in the USB cable; otherwise, you will not get any console prints after rebooting the board. To stop the storage service:

a. Select **Start > Windows Administrative Tools > Component Services**.

b. In the **Component Services** window, select **Services**.

c. Right-click **Storage Service** and choose **Stop**.

Figure 10. Console connection from Console port

NOTE

Alternatively, you can make a console connection from UART1 port on chassis back panel using the RJ45-to-DB9F cable provided in the LS1043ARDB hardware kit. Before making the connection, set SW3[3] to 0 (OFF).

7. Set up Tera Term on the host computer:

a. Start Tera Term. The Tera Term console appears along with the **Tera Term: New connection** dialog.

b. On the **Tera Term: New connection** dialog, select the **Serial** option, and ensure that **mbed Serial Port** is selected in the **Port** menu.

c. Click **OK** to close the **Tera Term: New connection** dialog.

d. Choose **Setup > Serial port** from the Tera Term console menu bar. The **Tera Term: Serial port setup** dialog appears.

e. On the **Tera Term: Serial port setup** dialog, configure the serial port of the host computer with the following settings:

- Baud rate: 115200
- Data: 8 bit
- Parity: none
- Stop: 1 bit
- Flow control: none

f. Click **OK** to close the **Tera Term: Serial port setup** dialog and complete setting up Tera Term. This configuration sets a console connection between the board and the host computer.

8. Optionally, connect the Ethernet cable if you want to connect your board to the network, for example, for obtaining latest board software and updating board images.

9. Optionally, connect the CodeWarrior TAP to the board by performing the following steps:

NOTE

Follow the instructions included with the CodeWarrior package to set up the environment and host attachment, such as USB and Ethernet.

a. Connect the 10-pin micro adapter (CWH-CTP-CTX10-YE), provided with the CodeWarrior TAP, to the CodeWarrior TAP.

b. Connect one end of the 10-wire cable (gray ribbon cable) to the 10-pin micro adapter (both ends of the wire are keyed and can be connected on either side).

c. Connect other end of the 10-wire cable to the 10-pin Arm JTAG header (J16) on the board, as shown in the figure below.

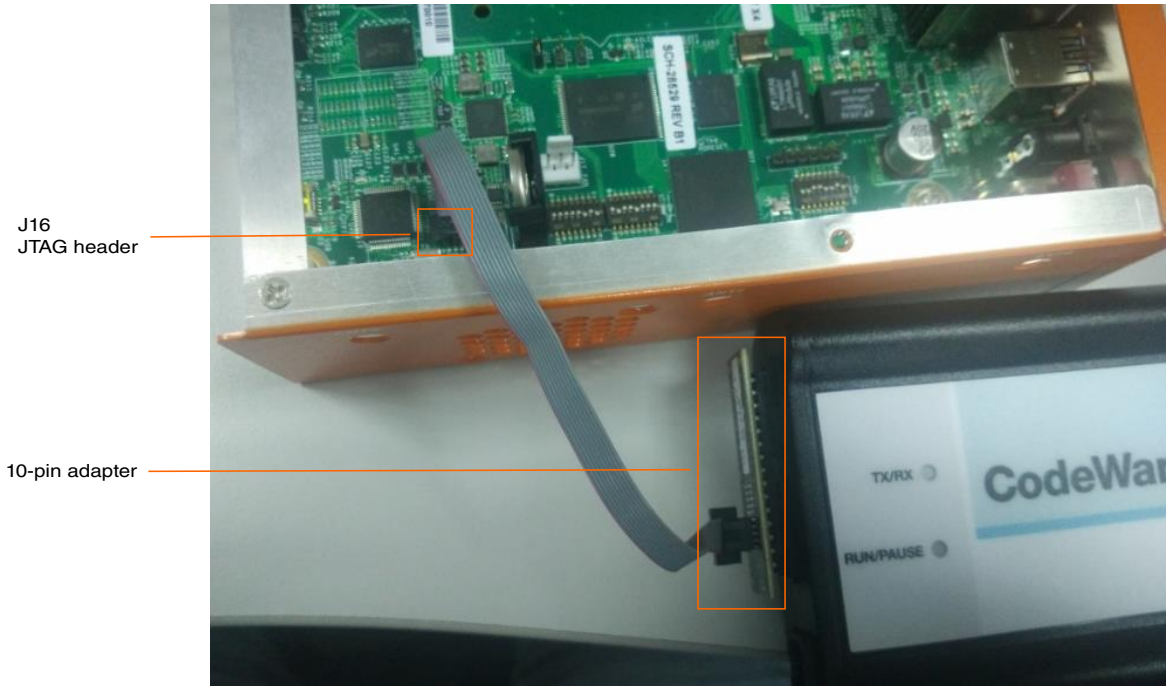

Figure 11. CodeWarrior TAP connection

NOTE

Pin 1 of the gray ribbon cable connector should align with pin 1 of the debug port header on the board.

10. Press the reset button available on chassis back panel to reboot the board. Boot log is displayed in Console window as given below:

NOTE

In case the storage service was not stopped before plugging in the USB cable, the ASLEEP LED (D3) remains ON and the serial console does not show any prints. In this case, you need to stop the storage service and unplug and replug the USB cable for the serial connection to work.

```
U-Boot 2017.07-g503eff0 (Sep 26 2017 - 15:00:50 +0800)

SoC:  LS1043AE Rev1.1 (0x87920011)
Clock Configuration:
       CPU0(A53):1600 MHz  CPU1(A53):1600 MHz  CPU2(A53):1600 MHz
       CPU3(A53):1600 MHz
       Bus:      400  MHz  DDR:      1600 MT/s  FMAN:     500  MHz
Reset Configuration Word (RCW):
       00000000: 08100010 0a000000 00000000 00000000
       00000010: 14550002 80004012 e0025000 c1002000
       00000020: 00000000 00000000 00000000 00038800
       00000030: 00000000 00001101 00000096 00000001
Model: LS1043A RDB Board
Board: LS1043ARDB, boot from vBank 0
CPLD:  V2.0
PCBA:  V6.0
SERDES Reference Clocks:
SD1_CLK1 = 156.25MHZ, SD1_CLK2 = 100.00MHZ
I2C:   ready
```

```
DRAM:  Initializing DDR....
Detected UDIMM Fixed DDR on board
1.9 GiB (DDR4, 32-bit, CL=11, ECC off)
Using SERDES1 Protocol: 5205 (0x1455)
SEC0: RNG instantiated
PPA Firmware: Version LSDK-17.09
Firmware 'Microcode version 0.0.1 for LS1021a r1.0' for 1021 V1.0
QE: uploading microcode 'Microcode for LS1021a r1.0' version 0.0.1
Flash: 128 MiB
NAND:  512 MiB
MMC:   FSL_SDHC: 0
EEPROM: NXID v1
In:    serial
Out:   serial
Err:   serial
Net:   Fman1: Uploading microcode version 108.4.9
PCIe0: pcie@3400000 disabled
PCIe1: pcie@3500000 Root Complex: no link
PCIe2: pcie@3600000 Root Complex: no link
FM1@DTSEC1, FM1@DTSEC2, FM1@DTSEC3 [PRIME], FM1@DTSEC4, FM1@DTSEC5, FM1@DTSEC6, FM1@TGEC1
Hit any key to stop autoboot: 0
```

NOTE

The above U-Boot log is an example log; the actual U-Boot log may vary slightly depending on the software version available on the board.

NOTE

By default, the LS1043ARDB comes preloaded with LSDK composite firmware image. You can deploy Ubuntu userland on the board, but due to limited NOR flash memory (128 MB), you need to use an external memory device, such as an SDHC card, a USB mass storage device, or a SATA device for storing the LSDK images.

For steps to download and assemble LSDK images and then to deploy LSDK Ubuntu distribution on the LS1043ARDB, see "LSDK Quick Start Guide for LS1043ARDB" section in Layerscape Software Development Kit <version> Documentation.

11 Using a mini-PCIe Wi-Fi card with LS1043ARDB

You can use a mini-PCIe Wi-Fi card with the LS1043ARDB. NXP has tested a mini-PCIe Wi-Fi card with the following features on the mini-PCIe slot of the LS1043ARDB:

- Wireless standard: 802.11ac Wave 2
- Wireless chipset: Qualcomm Atheros QCA9984
- Interface: PCIe
- Physical connector: Mini-PCIe

NOTE

By default, a Wi-Fi card based on the QCA9984 chipset is not supported by the LS1043ARDB software. To add support for the card, refer to OpenWRT upstreamed support of the LS1043ARDB, available at https://github.com/lede-project/source/tree/master/target/linux/layerscape.

The open source Wi-Fi driver, Ath10k, is supported as part of the OpenWRT framework. Ath10k supports various Qualcomm Atheros Wi-Fi chipsets, including QCA9984.

NOTE

The LS1043ARDB hardware kit does not include a mini-PCIe Wi-Fi card.

Perform these steps to connect a mini-PCIe Wi-Fi card to the LS1043ARDB:

1. Place the thermal pad available with the board kit near the mini-PCIe slot on the board, as shown in the figure below.

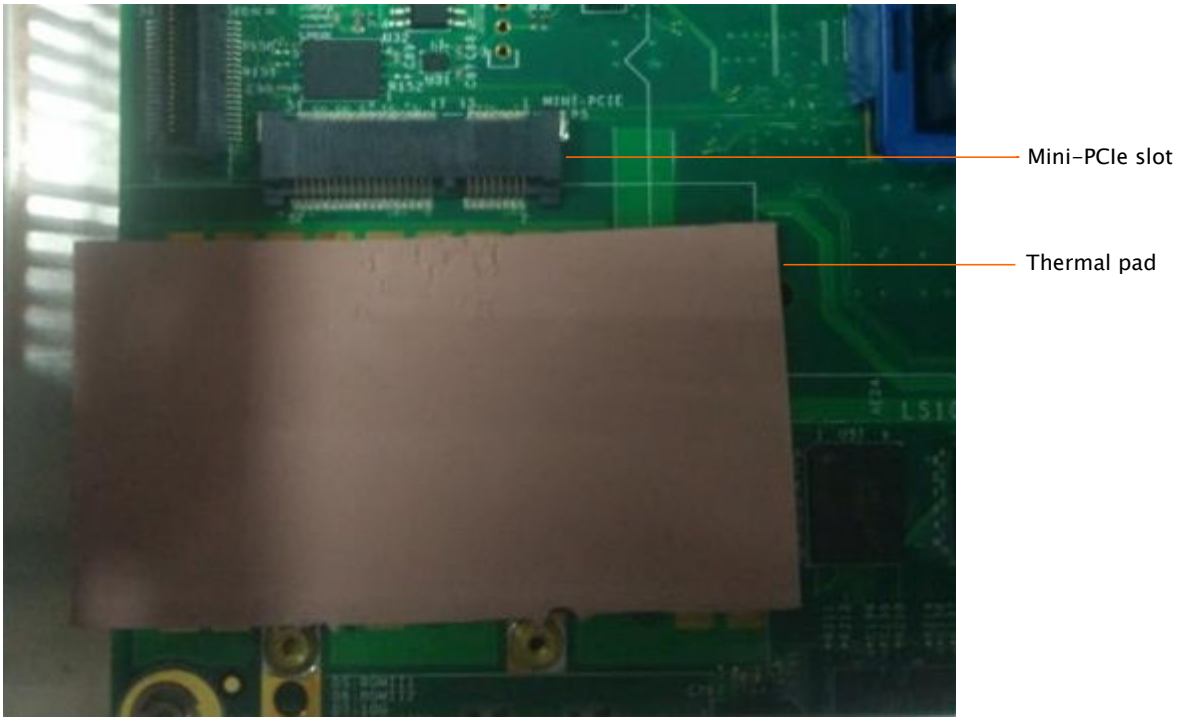

Figure 12. Add thermal pad

2. Connect the mini-PCIe Wi-Fi card to the mini-PCIe slot on the board, as shown in the figure below.

Figure 13. Connect mini-PCIe Wi-Fi card

12 Troubleshooting

This section explains the basic troubleshooting tips for the LS1043ARDB.

Console not showing any print

Perform the following steps in case console is not showing any print:

1. Ensure that the board is configured for the default switch settings, as described in Table 11. Default switch settings on page 17.
2. Ensure that the power adapter is connected to the wall mount power switch and the power switch is turned ON.
3. Ensure that the power adapter is connected to the board power jack and the power button is turned ON.
4. Ensure that the cable making console connection is properly connected as mentioned in Booting LS1043ARDB on page 16.
5. Ensure that Tera Term has communication settings as mentioned in section Booting LS1043ARDB on page 16.
6. Press the reset button to reboot the board. The Tera Term console should display U-Boot log.
7. If U-Boot log is still not showing on console, then the LSDK image available in the current NOR flash virtual bank (bank 0) may be corrupt. Try to boot the board from alternative virtual bank (bank 4) by powering OFF the board, changing SW5[6:4] settings from 000 to 100, and then powering ON the board.
8. If U-Boot log is still not showing on console, then the LSDK images on both bank 0 and bank 4 may be corrupt. Use CodeWarrior TAP to flash new images and recover the board. For details, see CodeWarrior TAP Probe User Guide.

13 Revision history

The table below summarizes revisions to this document.

Table 12. Revision history

Revision	Date	Topic cross-reference	Change description
Rev. 8	05/2019	Using a mini-PCIe Wi-Fi card with LS1043ARDB on page 20	Updated first note
Rev. 7	04/2019		Restructured and cleaned up document
		Connectors on page 8	Added J23 connector to Table 4. LS1043ARDB connectors on page 8
		Jumpers on page 9	Added J24 jumper to Table 5. LS1043ARDB jumpers on page 9
Rev. 6	11/2017	SW3 switch on page 10	Updated SW3[8] description in Table 6. SW3 settings on page 11
		Booting LS1043ARDB on page 16	• Added a note about a Windows 10 machine issue • Updated CPLD and PCBA versions in boot log
		LSDK memory layout	Added as a new section
		Deploying/Updating LSDK images on board	Added as a new section

Table continues on the next page...

Table 12. Revision history (continued)

Revision	Date	Topic cross-reference	Change description
Rev. 5	08/2017		Removed obsolete SDK information and added reference to LSDK Knowledge Center
		Jumpers on page 9	Removed the J9 and J15 jumpers from Table 5. LS1043ARDB jumpers on page 9
Rev. 4	02/2017	Jumpers on page 9	Changed the default setting for the jumper J10 in Table 5. LS1043ARDB jumpers on page 9
		SW4 switch on page 12	Changed switch settings for hardcoded RCW from 0_1001_1011 to 0_1001_1111
Rev. 3	12/2016	Hardware kit contents on page 2	Updated the section
		Booting LS1043ARDB on page 16	Updated the section
		Booting board using NOR alternate bank	Updated the section
		LS1043ARDB operating configurations	Added a note
Rev. 2	08/2016		Updated chassis images throughout the document
		LEDs on page 15	Updated the section
		SW3 switch on page 10	Updated details of SW3[5]
		SW5 switch on page 13	Updated details of SW5[6:4]
		Booting LS1043ARDB on page 16	Updated the section
		Ethernet port mapping	Updated section
		NOR flash memory map	Updated the "NOR flash memory map" table
		Supported boot options	Added as a new section
		Board recovery	Added as a new section
Rev. 1	11/2015	Booting LS1043ARDB on page 16	Updated console output
		Connecting a TDM riser card	Added as a new section
		LS1043ARDB operating configurations	Updated section
Rev. 0	08/2015		Initial public release

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