ASSIGNMENT 10

[Design a **4-BIT REGISTER** with (i) parallel-in/parallel-out (ii) serial-in/serial-out features using 2 input NAND GATES]

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Objective :- To implement a 4-bit Register with
(a) Parallel - In / Parallel - Out
(b) Serial - In / Serial - Out features.

Theory :- Shift Registers load the data present on its inputs and then shift it to its output once every clock cycle. Data bits may be fed in or out of a shift register serially, or all together at the same time in a parallel configuration.

In a Parallel-In / Parallel-Out register, the parallel data is loaded simultaneously into the register and transferred together to their respective outputs by the same clock pulse.

In a Serial In / Serial Out Register, the register is loaded with serial data, one bit at a time, and the data is shifted serially out of the register, one bit at a time.

Onward

Teacher's Signature.....

CIRCUIT DIAGRAM: