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Roll No. - 002010501024
Department - CSE
Year - 2nd
Semester - 1st
Assignment No. - 10

OBJECTIVE : Implementing a 4-bit Register with

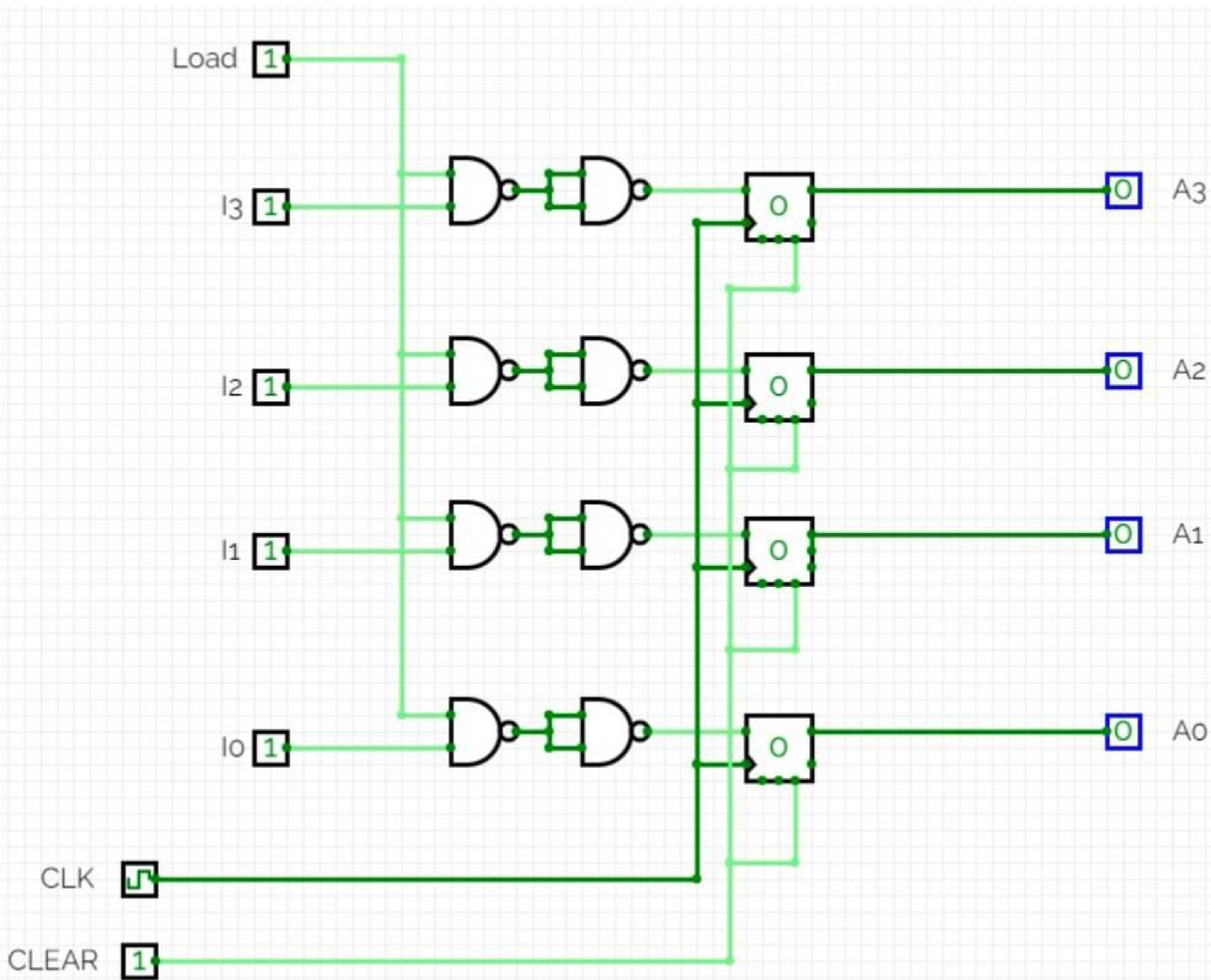
- (a) Parallel-In / Parallel-Out
- (b) Serial-In / Serial-Out

features.

THEORY : Shift Registers load the data present on its inputs and then shifts it to its output once every clock cycle. Data bits may be ~~shifted~~ fed in or out of a shift register serially, or all together at the same time in a parallel configuration.

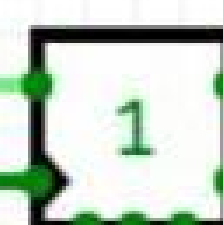
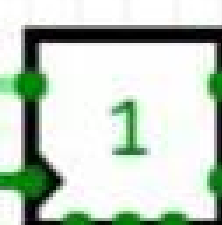
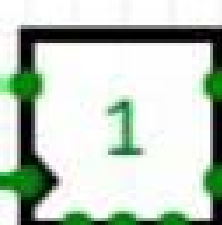
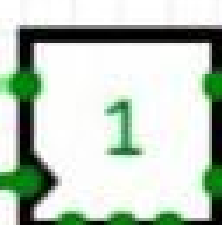
In a Parallel-In / Parallel-Out Register, the parallel data is loaded simultaneously into the register and transferred together to their respective outputs by the same clock pulse.

In a Serial-In / Serial-Out Register, the register is loaded with serial data, one bit at a time, and the data is shifted serially out of the register, one bit at a time.



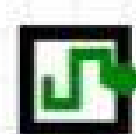
Serial Data In

1



1

Serial Data Out



CLK