

[Design of a combinational logic circuit for **ODD/EVEN PARITY GENERATOR AND CHECKER** using 2 input NAND GATES]

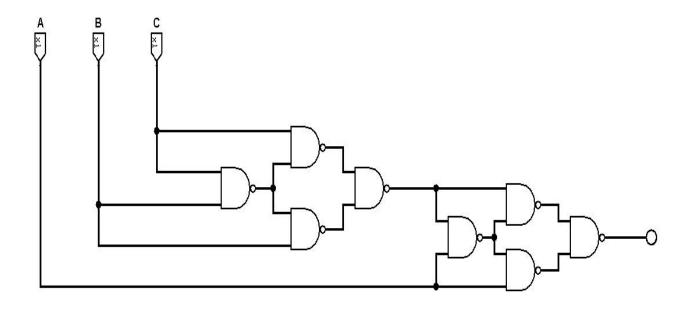
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Expt. No.	6			Page					
		To installer	ent an odd !	even parity checker.					
	and generat	or using	only 2-inp	it NAND Gales.					
		0	h .:+ 10	1. The parity bit is 0					
	mery: J	In even por	by of 18 in	the data stream and is					
			Handhan M d	) 100	-				
					71				
	ander Mum	ber of 18,	in the data	0					
0	odd numbe	ur of 18 in	the data str	lam.					
	A parity generator is a combinational logic circuit that								
	A . L	, T.h = 0	compination	nal logic circuit that					
	. Fit this	e natiate hit							
	. Fit this	e natiate hit							
	A parity of	e partity bit	detect ever	s in data transmission.	× .				
	A parity of by checkin	e partity bit nicker can a the pari	detect ever						
	A parity of by sheckin	e partity bit hecker can g the pari lynvator:	detect everor		,				
0	A parity of by wheckin From Parity Truth Tabl	e partity bit hicker can gethe pari	detect ever	s in data transmission.					
0	A parity of by wheckin From Parity Truth Tabl	e partity bit hecker can g the pari lynvator:	detect ever						
0	A parity of by wheckin From Parity Truth Tabl	e partity bit hicker can gethe pari	detect ever	s in data transmission.					
0	A parity of by checkin  Even Parity  Truth Table	e partity bit hicker can a the pari luntrator:	detect error	s in data transmission.					
0	A parity of by wheckin  From Parity  Truth Table	e partity bit hicker can a the parties of the parti	detect error	s in data transmission.					
0	penerates the A parity of by wheakin  From Parity Truth Table  A  O  O	e partity bit hicker can a the parties of the parti	detect evror try.	s in data transmission.					
0	penerates the A parity of by checkin  From Parity  Truth Table  A  O  O	e partity bit hecker can gethe parties of the parti	detect error	Parity Bit P 0					
Onward	penerates the A parity of by checkin  From Parity  Truth Table  A  O  O	e partity bit hicker can a the parties of the parti	detect evror try.	Parity Bit P  0  1					
Önward	penerates the A parity of by checkin  From Parity  Truth Table  A  O  O	e partity bit hecker can gethe parties of the parti	detect evror try.	Parity Bit P 0					
Önward	penerates the A parity of by checkin  From Parity  Truth Table  A  O  O	e partity bit hecker can gethe parties of the parti	detect evror	Parity Bit P  0  1					

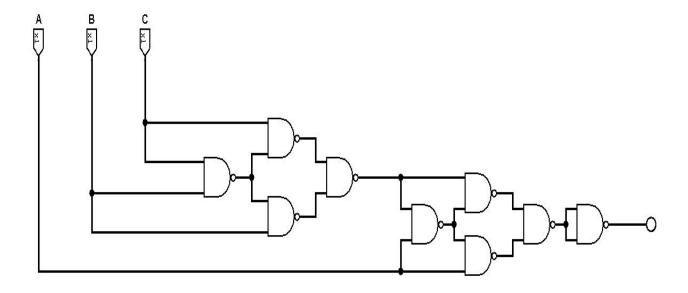
	Date Page
Expt. No.	0 0 1 0 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1
	P = A'B'C + A'BC' + AB'C' + ABC $= A'(BBC) + A(BBC)$ $[P = ABBCC]$
0	DD Parity Generator:  Truth Table:  3 input merrage Parity Bit  A B C P
0	
	P = A'B'C' + AB'C + ABC'
Onward -	[P = A ⊕ B ⊕ C ]  Teacher's Signature

## CIRCUIT DIAGRAM:

### **EVEN PARITY GENERATOR:**



### **ODD PARITY GENERATOR:**

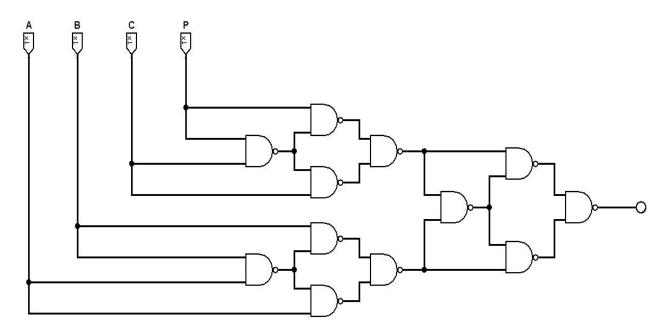


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E	ven Parit	y checker	7			
	Truth Pa	ble:		0	Parity Checker	
			t m	essage P		
	<u>A</u>	<u>B</u>	0	0	0	
	0	0	O			
	0	0	1	0		
	0	0	1		0	-
0 -	0	1	0	0		
	0	1	0	01	0	
	0	1	1	0	0	
	0		1	81		
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	1	t	0	p	0	
0	1	1	0	@1	1	
	1	1	1	Ö	1	
	1	1	1	1	0	
		AB C	00	01 11	10	
		00	0	1 0	1	
		01	ı	0 1	0	
		(1)	0	1 0	1	
Önward		01	1	0 1	0	
Orusina -						
		PC=	( A	( B) ( C	(⊕P)	
					Teacher's Signature	

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C	DD Parity	Checker:					
	Truth T	able:					
			nessa	ge		Parity Checker	
	^	В	C	P		PC	
	0	0	0	O		A .	
	0	0	0	1		0	
	0	0	1	0		0	
	0	0	1	1			- 1
	0	1	0	0		Ü	
	0	1	0	1		!	
	0	1	1	0			
	0-	1	1	1		0	
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	1	0	1	0		1	
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0	1	1	0	1		0	
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	1	1	1	1		(	
		ABCP	00 01	11	10.		
		00	10	1	0		
			0 1	0	1.		
		01	1 0		0		
TM		11	0 1	0			
rward —		10					
		0.0	<u> </u>	2 / 0	- 70		
		PC=	(AG	) ( )	COP)		

# CIRCUIT DIAGRAM:

## **EVEN PARITY CHECKER:**



## **ODD PARITY CHECKER:**

