



ASSIGNMENT 5

[Design of a combinational logic circuit for 3-BIT COMPARATOR using 2 input NAND GATES]

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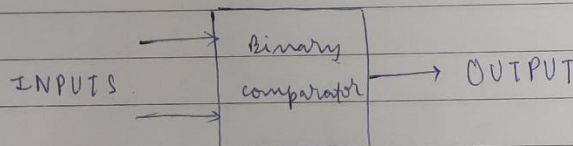
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Objective:- To implement a comparator circuit for two 3-bit numbers using only 2-input NAND gates.

Theory:- comparator is a combinational logic circuit that compares the magnitude of two binary quantities to determine which one has the greater magnitude. In other words, a comparator determines the relationship of two binary quantities.



Working:- Let the two 3-bit nos. be A and B.

$A \rightarrow A_2 A_1 A_0$ and $B \rightarrow B_2 B_1 B_0$.

where A_2 and B_2 are MSB whereas A_0 and B_0 are LSB of A and B respectively.

Notations:-

$E \rightarrow A = B$

$G \rightarrow A > B$

$L \rightarrow A < B$

Conditions:-

For $A > B$:

$A_2 > B_2$, or.

$A_2 = B_2$ and $A_1 > B_1$, or

$A_2 = B_2$ and $A_1 = B_1$ and $A_0 > B_0$

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For $A=B$, $A_2=B_2$ and $A_1=B_1$ and $A_0=B_0$

For $A < B$, $A_2 < B_2$ or
 $A_2=B_2$ and $A_1 < B_1$ or
 $A_2=B_2$ and $A_1=B_1$ and $A_0 < B_0$.

Truth Table:-

A_2	A_1	A_0	B_2	B_1	B_0	$A < B$	$A = B$	$A > B$
0	0	0	0	0	0	0	1	0
0	0	0	0	0	1	1	0	0
0	0	0	0	1	0	1	0	0
0	0	0	0	1	1	1	0	0
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1	1	1	1	0	0	0	0	1
1	1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0	1
1	1	1	1	1	1	0	1	0

Expression:-

$$L = \{A < B\} = A_2' B_2 + (A_2 B_2 + A_2' B_2') (A_1' B_1) + (A_2 B_2 + A_2' B_2') (A_1 B_1 + A_1' B_1') A_0' B_0$$

$$E = \{A = B\} = (A_0 B_0 + A_0' B_0') (A_1 B_1 + A_1' B_1') (A_2 B_2 + A_2' B_2')$$

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$$G = (A > B) = A_2 B_2' + (A_2 B_2 + A_2' B_2') A_1 B_1' + (A_2 B_2 + A_2' B_2') (A_1 B_1 + A_1' B_1') A_0 B_0'$$

Comments:-

(i) The total no. of gates (NAND) required are = 41

(ii) Lower no. of gates results in.

- Reduced cost
- Reduction in complexity and interconnections (wiring)
- Lesser chances of troubleshooting.
- Smaller area covered by circuit onboard.

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CIRCUIT DIAGRAM:

