ASSIGNMENT 7

[Design of a combinational logic circuit for **3-BIT ADDER AND SUBTRACTOR** using 2 input NAND GATES]

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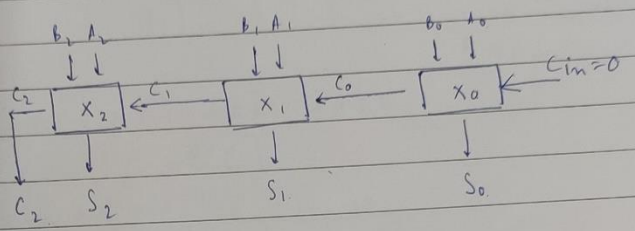
Expt. No. 7A

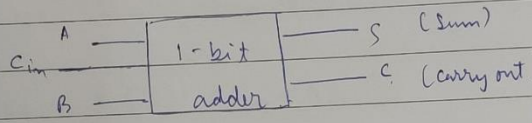
Date
Page

Objective:- Implementing a 3 bit adder using only 2 input NAND GATES.

Circuit:-



where, X_0, X_1, X_2 are 1 bit adder



Truth Table:- (1 bit adder).

A	B	C_{in}	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Onward

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Date
Page

Expt. No.

K-Map for 1 bit adder

S →

A \ BCin	00	01	11	10
0		1		1
1	1		1	

→ Check board configuration. (No pairing)

$S = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$

⇒ $[S = A \oplus B \oplus C]$

Co →

A \ BCin	00	01	11	10
0			1	
1		1	1	1

$Co = BCin + ACin + AB = AB + Cin(A \oplus B)$

For 3 bit adder we use combination of these 1 bit adders.

ward

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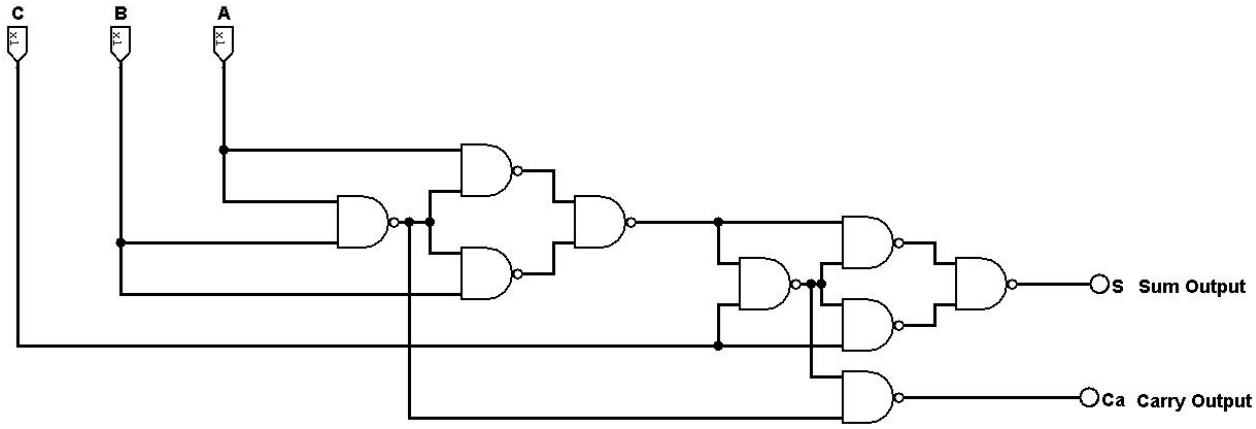
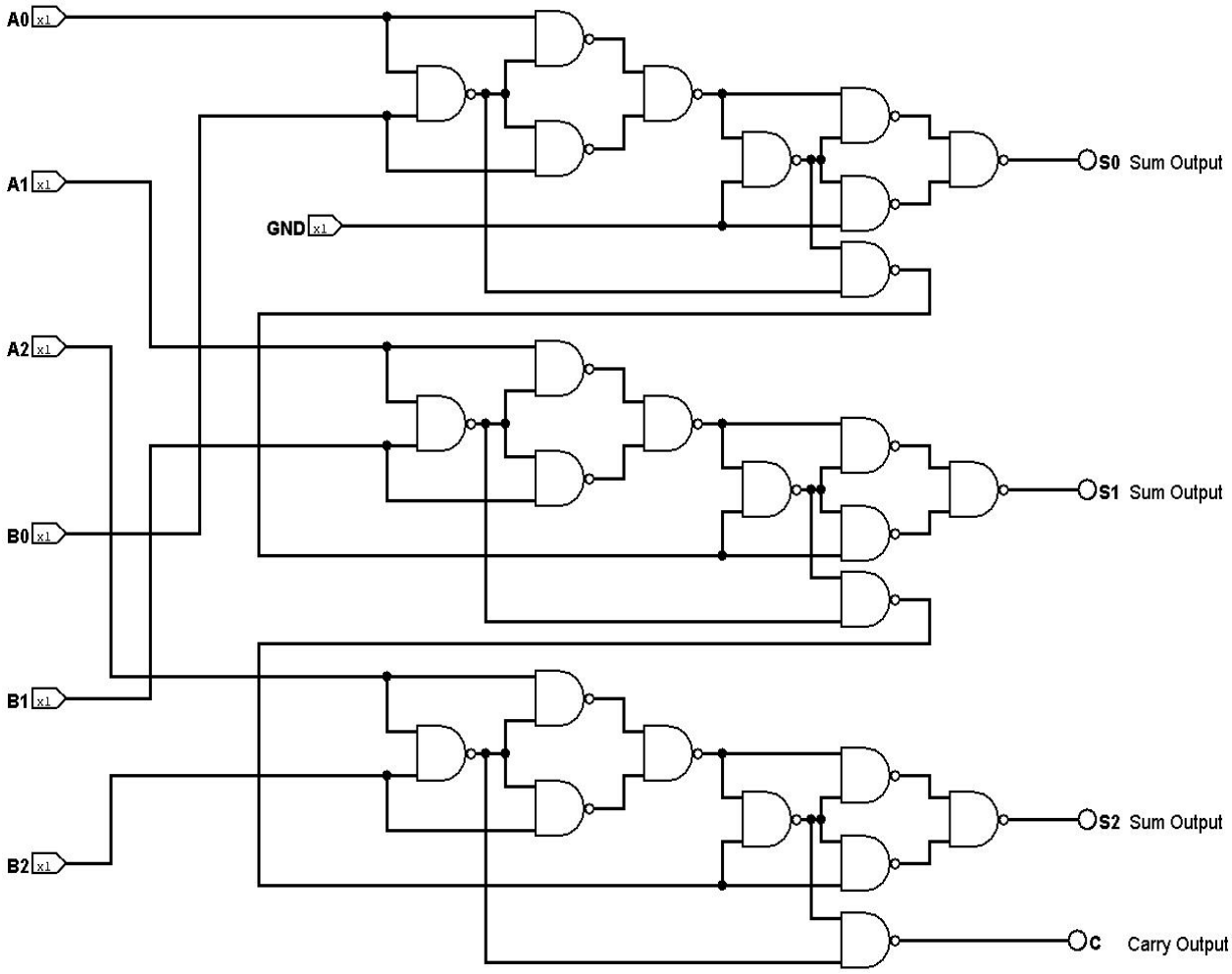
CIRCUIT DIAGRAM:

1 BIT FULL ADDER:



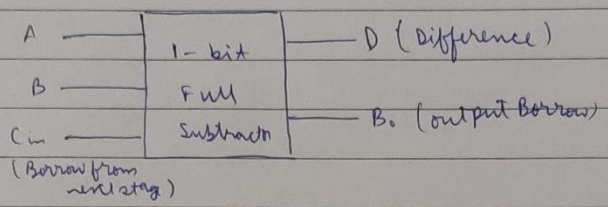
3 BIT FULL ADDER:



Expt. No.

Date
Page

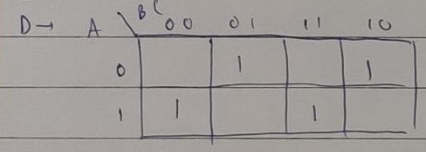
3-bit subtractor :-



Truth Table :- (1 bit subtractor)

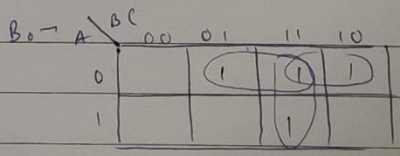
A	B	Cin	D	Bo
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

K-Map :-



checkboard config.

$[D = A \oplus B \oplus C_{in}]$



$B_o = BC + \bar{A}C + \bar{A}B$

$= BC + \bar{A}(B \oplus C)$

Onward

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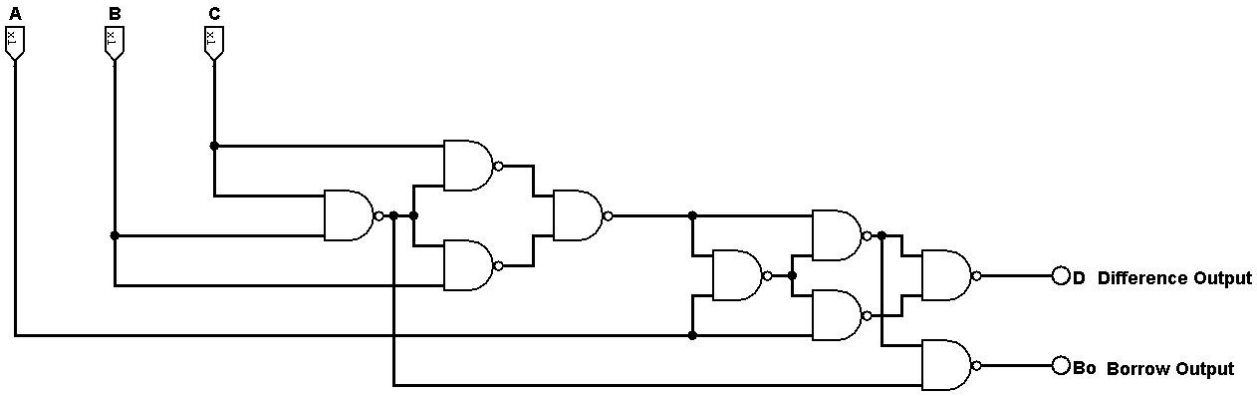
CIRCUIT DIAGRAM:

1 BIT FULL SUBTRACTOR:



3 BIT FULL SUBTRACTOR: