ASSIGNMENT 4

[Design of a combinational logic circuit using 2 input NAND gates for

(i)   4X1 MULTIPLEXER
(ii)   1X4 DEMULTIPLEXER]
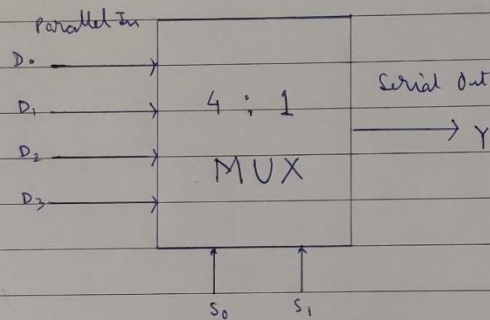
NAME: ROHIT SADHU

ROLL NO.: 002010501074

Expt. No. 4 A

Objective :- Implement a 4 to 1 multiplexer, and a

Theory :- A multiplexer is a device that selects one of several analog or digital input signals and forwards the selected input into a signal line.
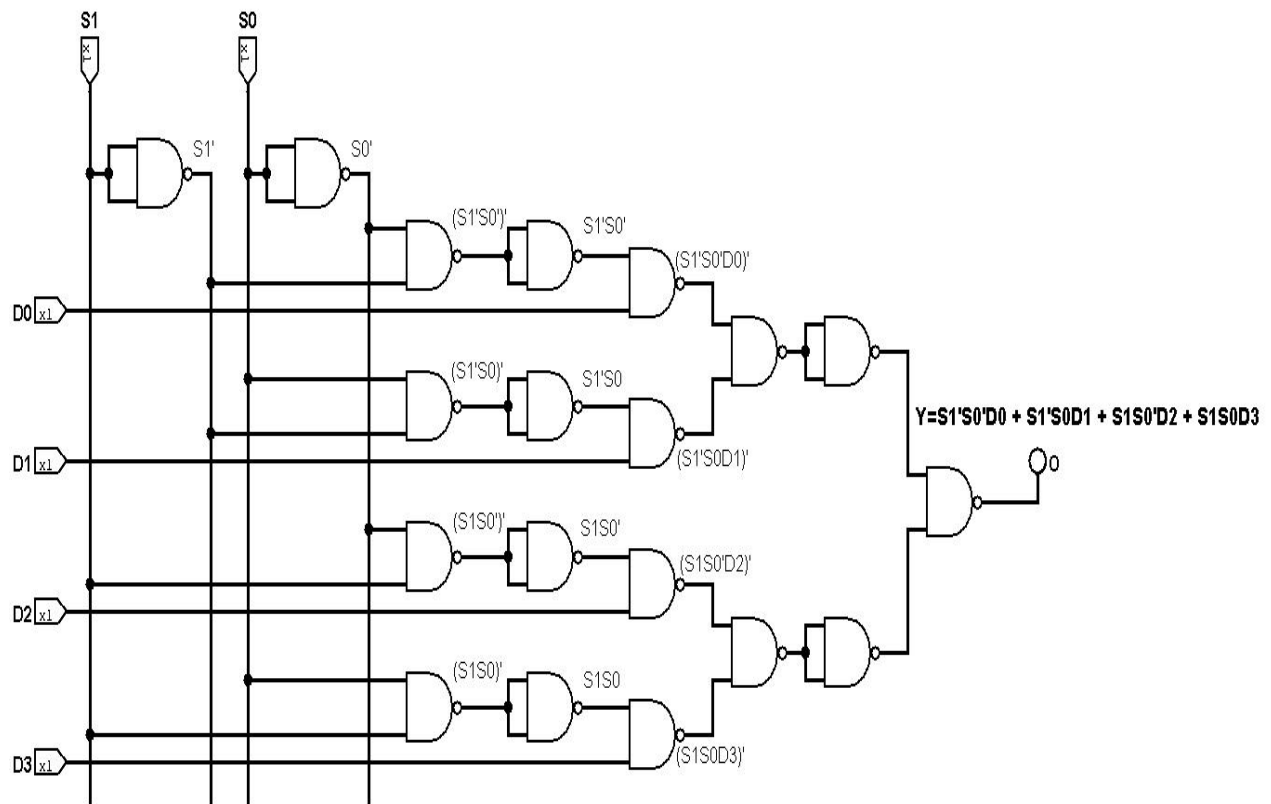
Block Diagram :-

Parallel In

D_0

D_1

4 : 1

MUX

D_2

D_3

Serial Out

$\rightarrow$ Y

S_0 S_1

Truth Table :-

Select Lines		Data	Lines			Output
S_0	S_1	D_0	D_1	D_2	D_3	Y
0	0	D_0	x	x	x	D_0
0	1	x	D_1	x	x	D_1
1	0	x	x	D_2	x	D_2
1	1	x	x	x	D_3	D_3

Expression :- $Y = \overline{S_0}\,\overline{S_1}\,D_0 + \overline{S_0}\,S_1 D_1 + S_0\,\overline{S_1}\,D_2 + S_0\,S_1 D_3$

Teacher's Signature...........................

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CIRCUIT DIAGRAM: –

$Y = S1'S0'D0 + S1'S0D1 + S1S0'D2 + S1S0D3$

Comments :-

a) No. of gates required for implementing the circuit. = 19

b) Lower no. of gates result in :-

(i) Reduced cost.

(ii) Reduction in complexity and interconnection.

(iii) Lesser chances of trouble shooting.

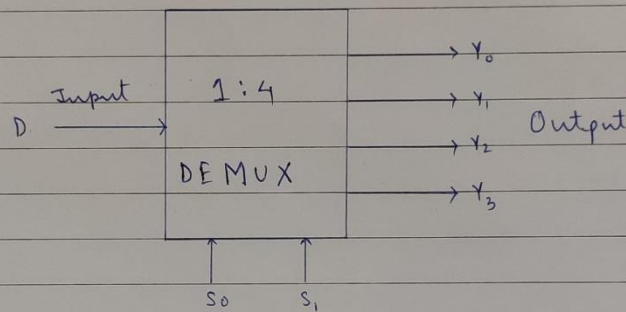(iv) Smaller area covered by circuit on circuit board.

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Date

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Objective:- Implementing a 1 to 4 Demultiplexer.

Theory:- A demultiplexer is a device that takes a single input line and routes it to one of the several output lines.

Block Diagram :-

Truth Table :-

Data	Select Lines		Output			
	S_0	S_1	Y_0	Y_1	Y_2	Y_3
D	0	0	D	X	X	X
D	0	1	X	D	X	X
D	1	0	X	X	D	X
D	1	1	X	X	X	D

Expressions:- $\quad Y_0 = D\,\overline{S_0}\,\overline{S_1} \qquad Y_1 = D\,\overline{S_0}\,S_1$

$\qquad\qquad\qquad Y_2 = D\,S_0\,\overline{S_1} \qquad Y_3 = D\,S_0\,S_1$

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CIRCUIT DIAGRAM: -
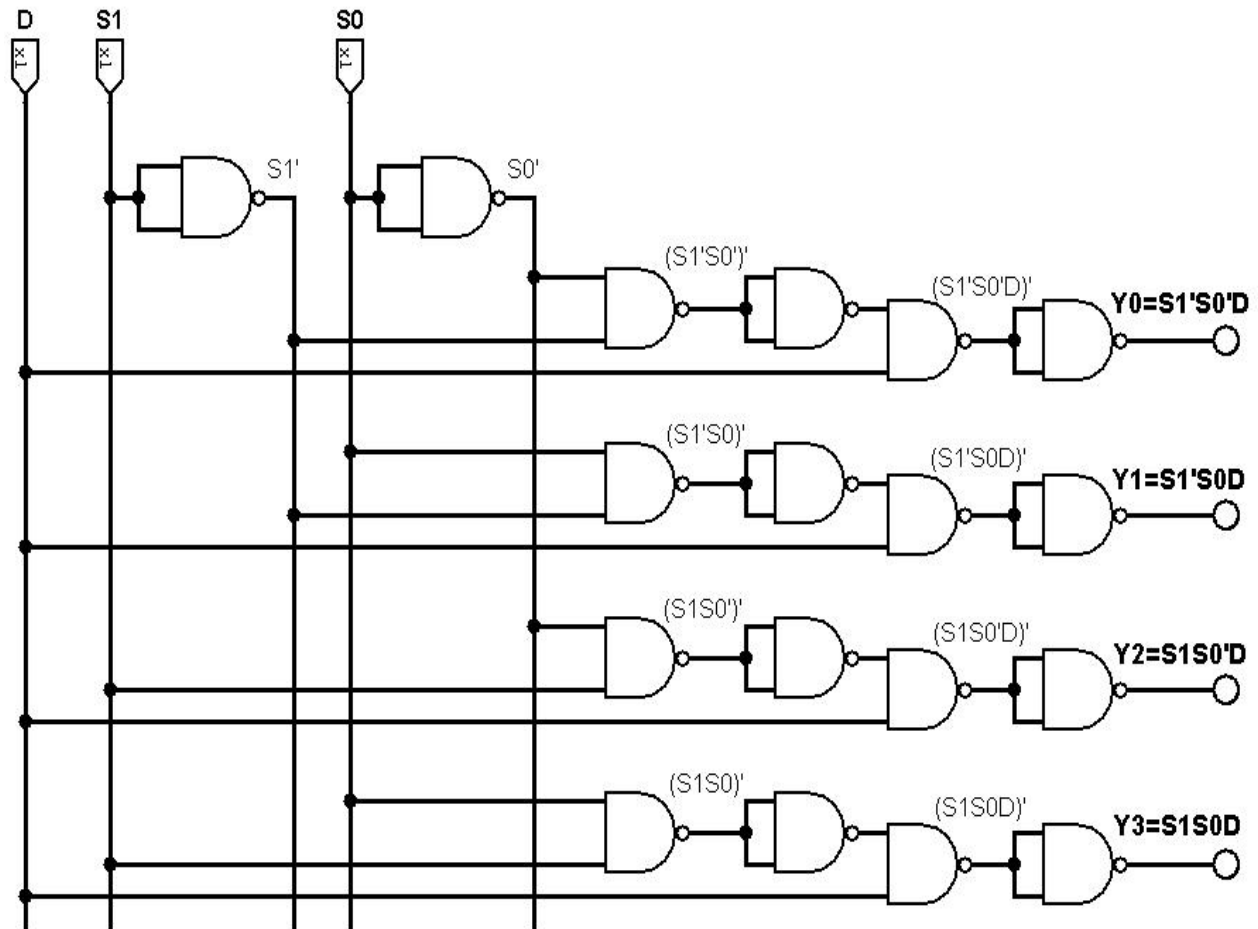
Comments :-

a) No. of gates required for implementing the circuit = 18

b) Lower no of gates result in:-

(i) Reduced cost.

(ii) Reduction in complexity and interconnections.

(iii) Lesser chances of troubleshooting.

(iv) Smaller area covered by the circuit on the circuit board.