Exam Related for BAIT2123 IoT

UART (Universal Asynchronous Receiver Transmitter)

- One data frame consists of 1 start bit, 8 data bits and 1 stop bit
- Start bit is high-to-low
- Stop bit it low-to-high

Advantages

- No clock needed
- Simple to operate, well documented as it is a widely used method with a lot of resources online
- It includes a parity bit to check the errors

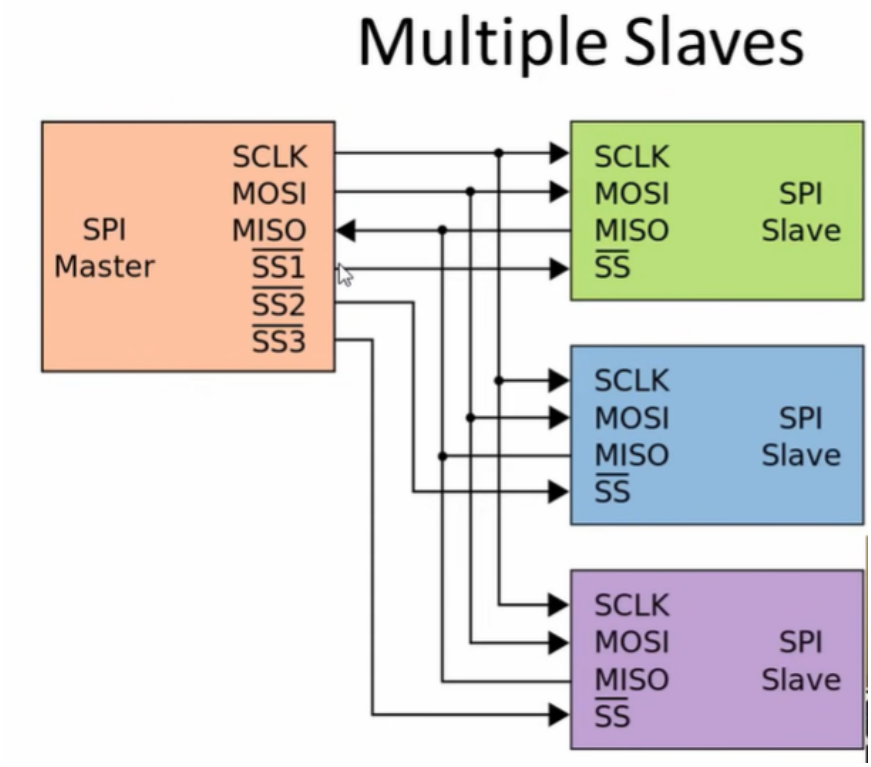
Disadvantages

- Cannot use multiple master and slaves
- Only suitable for communication between 2 devices (one to one communication)
- Transmitter and receiver must agree on the transmission speed
- Low data transmission speed compared to I2C and SPI

SPI (Serial Peripheral Interfaces)

- MISO is unidirectional bus and data is sent from slave to the master
- MOSI is unidirectional bus and data is sent from master to the slave
- SCK is unidirectional bus and is used by the master for data synchronization
- CS is unidirectional bus and is used by the master to select a slave device

Diagram for SPI



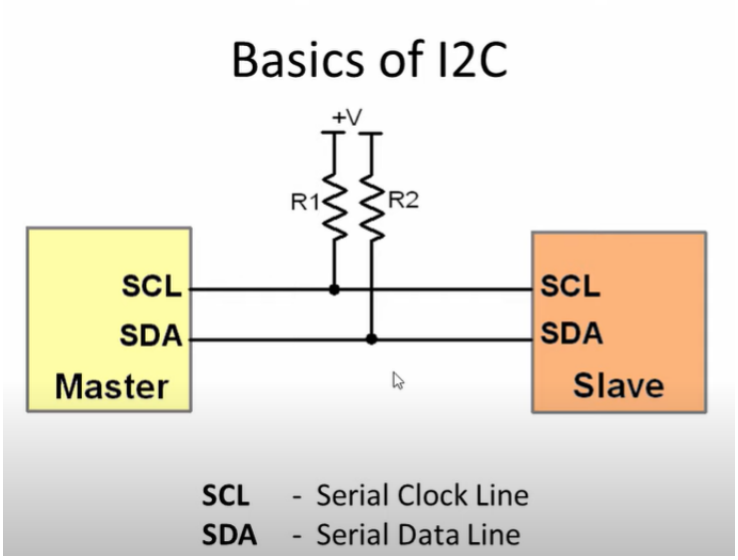
Advantages

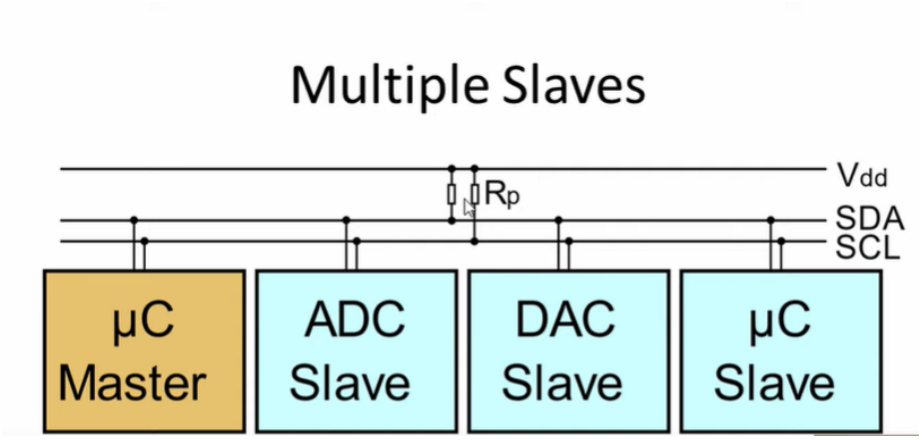
- Full Duplex (send and receive at both direction at the same time)
- Higher speed than UART and I2C
- Ubiquitous (It's used in everywhere, popular)

Disadvantages

- More pins than UART and I2C (minimum 4 pins)
- Short distance vs RS232 / RS485
- Lots of variants

I2C (Inter Integrated Circuit)





- SCL is the clock line. It is used to synchronize all data transfers over the I2C bus.
- SDA is the data line to send data in both directions (bi-directional communication).

Advantages

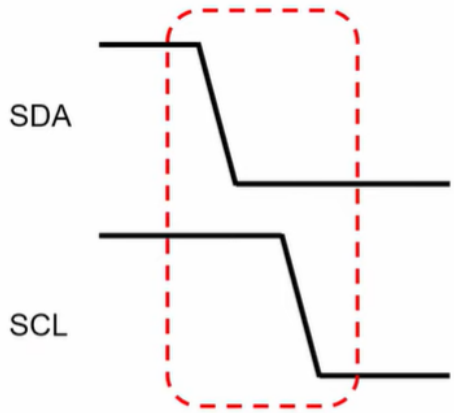
- Low pin count (just 2!)
- Addressing built-in
- Ubiquitous

Disadvantages

- Half-Duplex (might cause collision), 400 kbps max (sorta)
- Careful consideration of hardware - Need to know where pull-up resistors are (SDA, SCL), addressing that would not make collision
- More complicated than SPI or UART

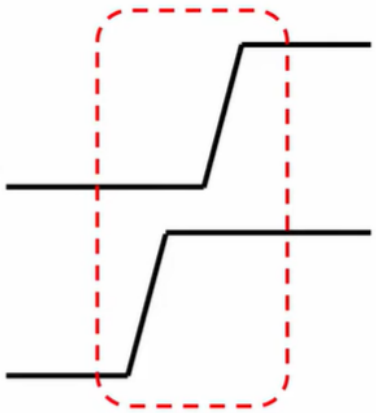
I2C Mode	Speed
Standard Mode	100 kbps
Fast Mode	400 kbps
Fast Mode Plus	1 Mbps
High Speed Mode	3.4 Mbps
Ultra-Fast Mode	5 Mbps

I2C Protocol – START and STOP



I2C START

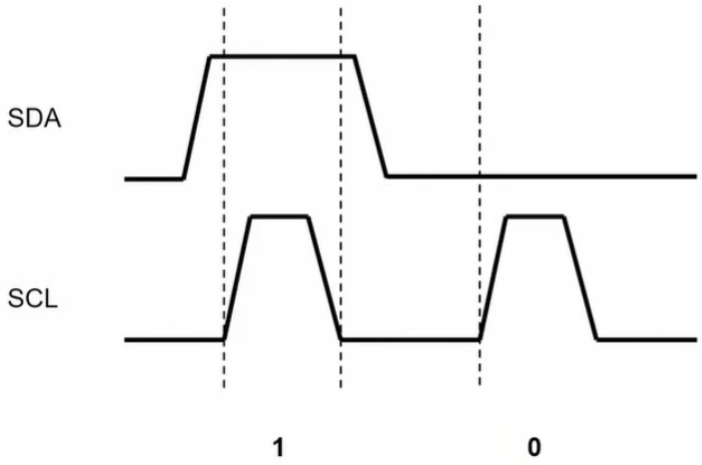
A controller device claims the I2C bus for communication with a target device



I2C STOP

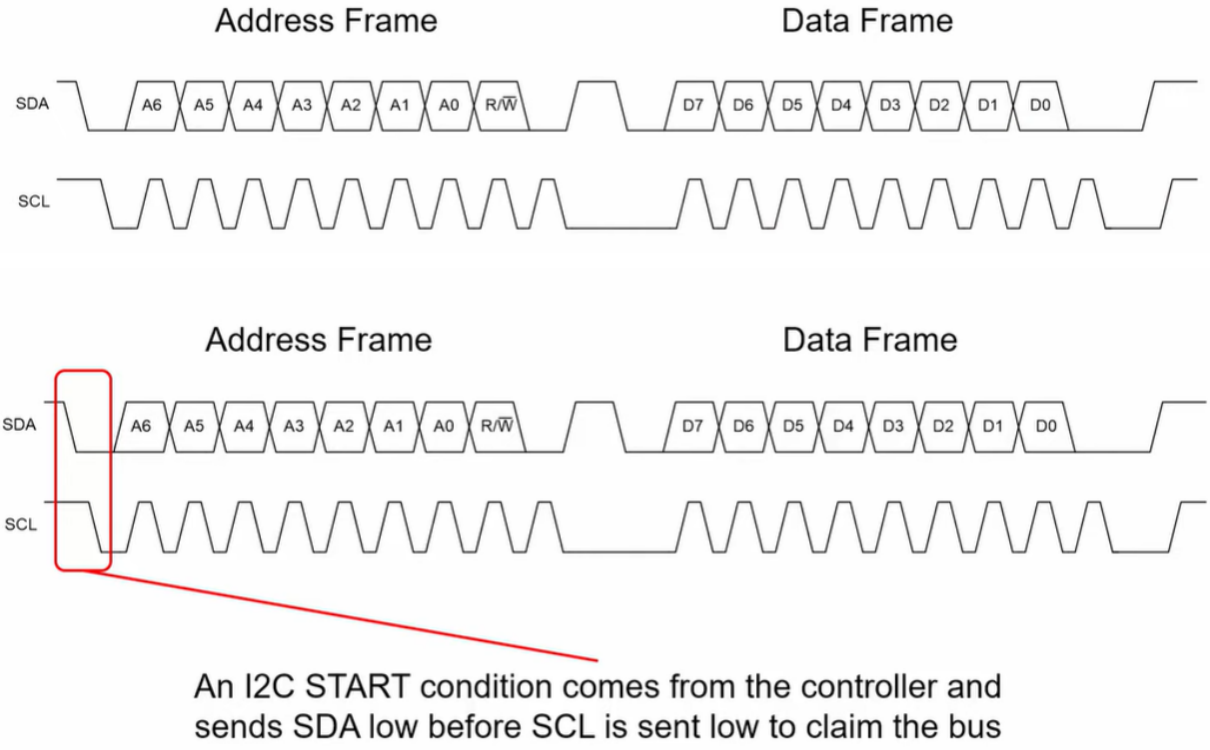
A controller device completes communication with a target device and releases the I2C bus

I2C Protocol – Logical Ones and Zeros

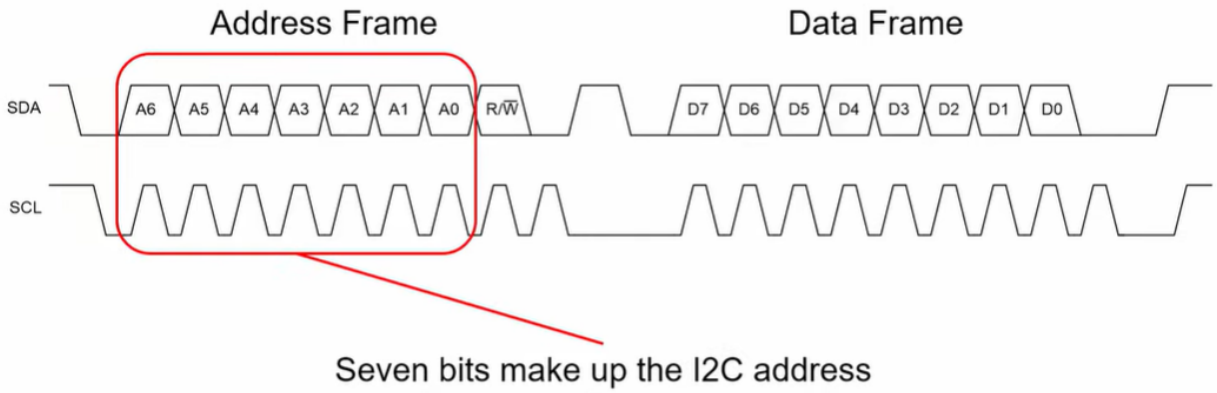


I2C Logical Bits
SDA is the data line, SCL is serial clock
SDA only transitions when SCL is low (except during START and STOP)
SDA is high when SCL pulses is a logical one
SDA is low when SCLK pulses is a logical zero

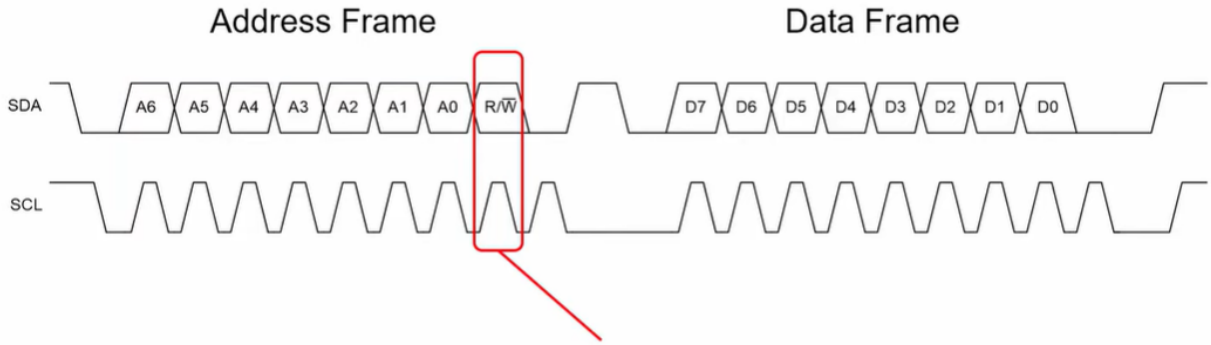
I2C Protocol – Timing Diagram



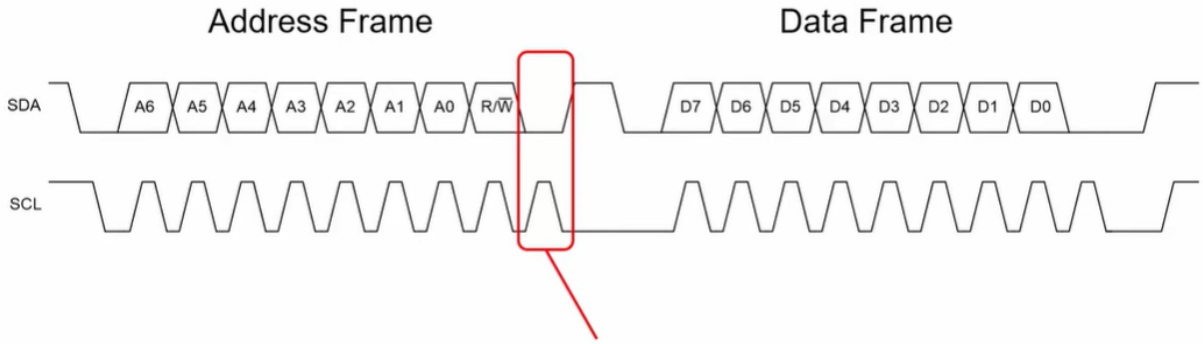
An I2C START condition comes from the controller and sends SDA low before SCL is sent low to claim the bus



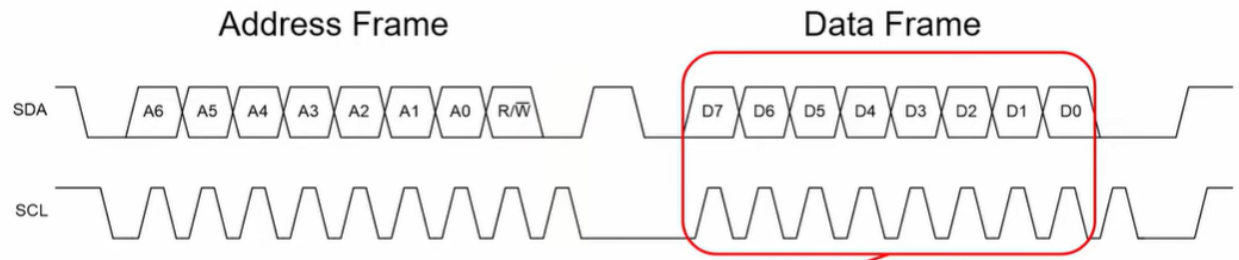
Seven bits make up the I2C address



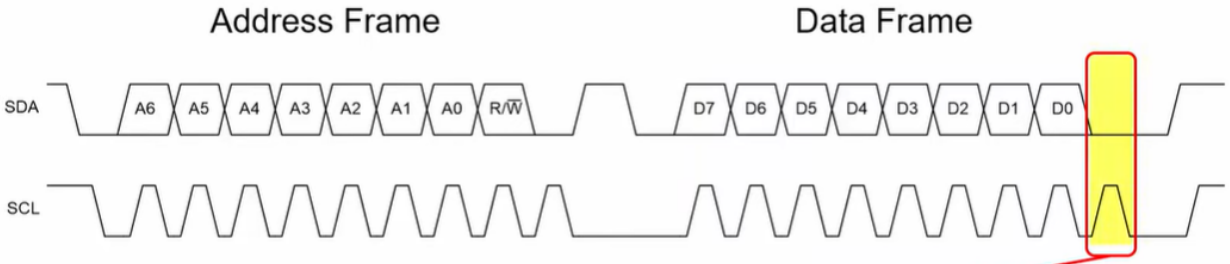
R/W bit indicates the direction of communication
1: Controller wants to read from the target device
0: Controller wants to write to the target device



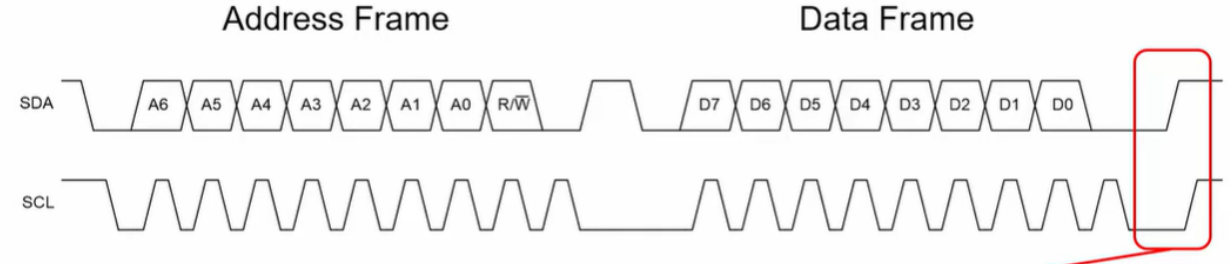
SDA is pulled down as an ACKT (acknowledge, target)
After the address byte, the target device ACKs the communication



Single byte communication for data frames

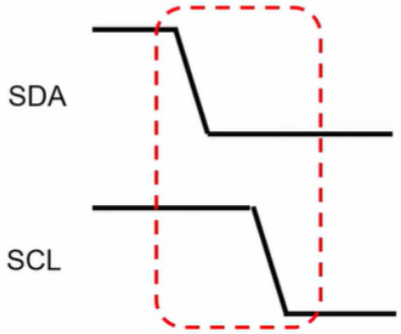


ACK follows each data frame
Write to the target – ACKT comes from the target device
Read from the target – ACKC comes from the controller device

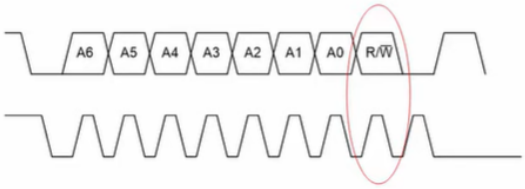


I2C STOP condition comes from the controller and sends
SDA high before SCL is sent high to release the bus

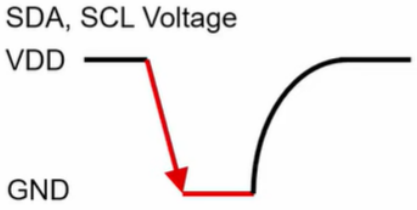
1. Before the address frame of I2C communication, what actions make up the START condition?
   a. The controller device sets the SDA low, and then sets the SCL low
   b. The controller device sets the SCL low, and then sets the SDA low
   c. The controller device sets the SCL low, and the target device pulls the SDA low as an ACK



2. In the address frame, after the controller device sends the 7 bit address, what is the next part of the I2C protocol sent?
   a. The target device sends the ACK to acknowledge the communication coming from the controller device
   b. The controller device sends the R/W bit to indicate if it wants to read from or write to the target device
   c. The controller device send a STOP condition before sending the next data



3. Because of the NMOS open-drain connection to SDA and SCL, which part of the communication waveform is faster?
   a. The rise time of SDA and SCL
   b. The fall time of SDA and SCL
   c. The rise time and fall time of SDA and SCL are the same



Open-drain connections are actively pulled down instead and are faster than a resistive pull up

4. What is the benefit of having an open-drain connection over push-pull outputs for I2C?
   a. High speed drive for the bus outputs
   b. Reduction of bus capacitance
   c. Prevents destructive current draw during bus contention when outputs are tied together

Push-Pull outputs may pull a large current when the outputs are tied together and there is bus contention

UART	I2C	SPI
1 to 1	Simplex	Duplex
Asynchronous	Synchronous	Synchronous
2 wires	2 wires	4+ wires
20Kbps	1Mbps	25Mbps
Acknowledge pins	NO acknowledge	NO acknowledge
Medium power	Medium power	Lower power
15m distance	1m distance	20cm distance