Final Project: Two-Stage Single-Ended CMOS Operational Amplifier

ECE 422

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Problem Statement

The task at hand is to design a two-stage single-ended CMOS op amp with Miller compensation and a minimum channel length of $0.18\ \mu m$. The constraints for this project are expressed in Table 1.

Load Capacitances	$5\ pF$
Power Supply	$V_{dd} = 0.9V$, $V_{ss} = -0.9$
Open Loop Gain	$\geq 65\ dB$
Phase Margin	$\geq 60^o$
Unity Frequency Gain	$\geq 12\ MHz$

Table 1: Design parameters for the two-stage amplifier.

After having designed and simulated the two-stage amplifier, one was also tasked with determining the input common-mode range $V_{ic,min}$ and $V_{ic,max}$, and the output voltage swing $V_{o,min}$ and $V_{o,max}$.

Assumptions

Assumptions include the following:

- AD = AS = $0.6\ \mu m \times W$, where W is the width in μm.
- PD = PS = $1.2\ \mu m + 2W$, where W is the width in μm.
- $\lambda = 0.25$
- $V_{BS} = 0$, thus making $V_{th,N} = V_{th0,N}$ and $V_{th,P} = V_{th0,P}$
- Saturation is the desired region of operation for each MOSFET.

Design Procedure

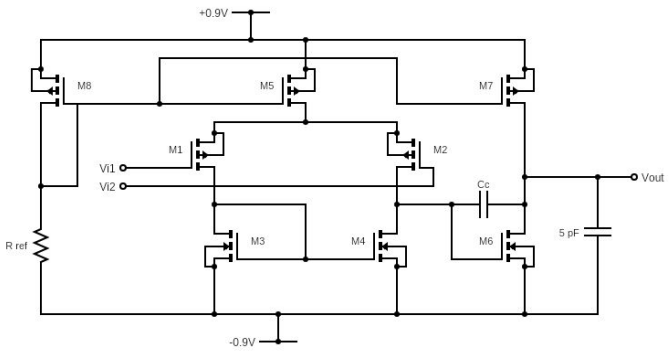


Figure 1. Amplifier Layout

DC Biasing

The first step is to set a reference current that allows the ideal operation of the circuit. Setting this current will set the bias voltage for the upper MOSFETs for the first and second stage. The bias voltage is dictated by the current through M8 and R_ref resistor. To determine the resistance, we start by finding V_{GS} of M8 using equation 2. By finding V_{GS}, the voltage drop across the leftmost diode-tied MOSFET, one will be able to use KVL to solve for the unknown resistance. Our desired current through M8 is 20uA and with our calculated R_ref resistance is ~63.89k ohms; this gives us a voltage of about 0.38V at the gates of M5 and M7. In the simulation, these values are appropriate to set M8, M5, and M7 in saturation. Here, we approached the design with an experimental (W/L) to begin our calculations. From this calculation, the rest of the currents are derived from the current through M8. One key thing to keep in mind while setting the (W/L) for the rest of the MOSFETs is the following equation: $\frac{I_{M7}}{I_{M5}} = \frac{(\frac{W}{L})_{M7}}{(\frac{W}{L})_{M5}} = \frac{(\frac{W}{L})_{M6}}{2*(\frac{W}{L})_{M3}}$. This last equation will assure that the drains of M3 and M4 will be the same otherwise, there will be an offset in currents. All of the values were run through a spreadsheet that would expedite the calculation process and output the values faster.

Open Loop Gain

To be able to find open-loop gain, we must first determine gm1, gm6, rds4, rds2, rds7, and rds6. These values are dependant on their respective large-signal currents. We calculated these values using equations 4 and 5. The overall gain is calculated by this equation:
$A_v = -gm_1 gm_6 (rds_2 || rds_4)(rds_6 || rds_7)$.

Unity Gain Frequency

The unity gain frequency is determined using the dominant pole, P1, and gain of the system. P1 is calculated using the following equation: $P_1 = \frac{1}{C_1R_1+C_2R_2+C_c(R_1R_2+gm_2R_1R_2)}$ where $C_2 = C_{gd,7} + C_{db,7} + C_{db,6} + C_{load}$, $C_1 = C_{gs,6} + C_{gd,4} + C_{db,4} + C_{db,2} + C_{gd,2}$, and C_C is defined by us for compensation.

Phase Margin

As one may recall, the phase margin plays a role in the stability of a system. In this implementation, the phase margin is determined by simulation after having obtained the open-loop bode plots. If a different approach is taken, one must already know the unity gain frequency to proceed. As defined by Razavi in page 416 of his textbook *Design of Analog CMOS Integrated Circuits,* "[unity gain] must drop to unity before [it] crosses -180^o" (2014). To perform this operation, one will take the angle of each pole by performing the following arithmetic:

Want $< T(j\omega)$ to be greater than -180,

$< T(j\omega) = - \ tan^{-1}(\frac{Wu}{p1}) \ - \ tan^{-1}(\frac{Wu}{p2})$

*Note: we know that p1 ~ $7.144 \times 10^5 \ Hz$, p2 ~ $3.1911 \times 10^6 \ Hz$, and $w_u = 1.568 \times 10^9 \ Hz$

$PM \ = \ 180 + < T(j\omega) = 180 - (89.97+89.8834) = 0.1426$ degrees

This value differs from the simulation result, which is depicted in Figure 3 of the Appendix. Although the calculation is off, the simulation meets the parameter of the P.M. being greater than 60 degrees.

Simulation Results & Discussion

The simulation results can be viewed in Figure 3. The following table compares our op-amp's performance with the requirements.

	Requirement	**Actual**
Open Loop Gain	$\geq 65 \ dB$	71.025 dB
Phase Margin	$\geq 60^o$	173.14
Unity Frequency Gain	$\geq 12 \ MHz$	41.305MHz

It is clear that the op-amp's performance is adequate for the requirements as established by the assignment. For the gain, we are above the minimum by 6.025, for the phase margin we are above the minimum by 113.14 degrees, and for the unity frequency gain we were above the minimum by about 29MHz. Although the actual characteristics of the op-amp are good, they do not match the calculations that we ran on our spreadsheet. We don't understand why this is the case as we ran our calculations very carefully and many times to assure that our values would be correct. Also, our Cc compensation was not very necessary, as the output was very good even without the capacitor. This again is directly related to the fact the results do not match our calculations.

Conclusions

The two-stage single-ended CMOS op-amp with Miller compensation designed required a handful of assumptions and fundamental grasp of the course. The knowledge required to assemble it ranged from a fundamental understanding of small-signal analysis and large-signal analysis to frequency response behavior. The largest issue encountered was getting the op-amp to perform closer to the parameters that were set. Although it didn't meet this team's design goals, it did meet instructor parameters. Open-loop gain, unity gain frequency, and phase margin restraints were successfully met. To improve this design, one would need to address calculations and assumptions that may be inaccurate. Given more time, we would be able to address these discrepancies and be able to design a better op-amp.

Appendix

Equations used for the design:

(1) $I_{DS} = \frac{K_n W}{2L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$

(2) $V_{GS} = \sqrt{\frac{2I_D}{K_n(\frac{W}{L})}} + V_{TH}$

(3) $V_{ov} = \sqrt{\frac{2I_D}{K_n(\frac{W}{L})}}$

(4) $g_{m,sat} = \sqrt{\frac{2K_n W I_{Ds}}{L}}$

(5) $r_{ds} = \frac{1}{\lambda \times I_{DS}}$

Table 2 of Capacitances for a FET:

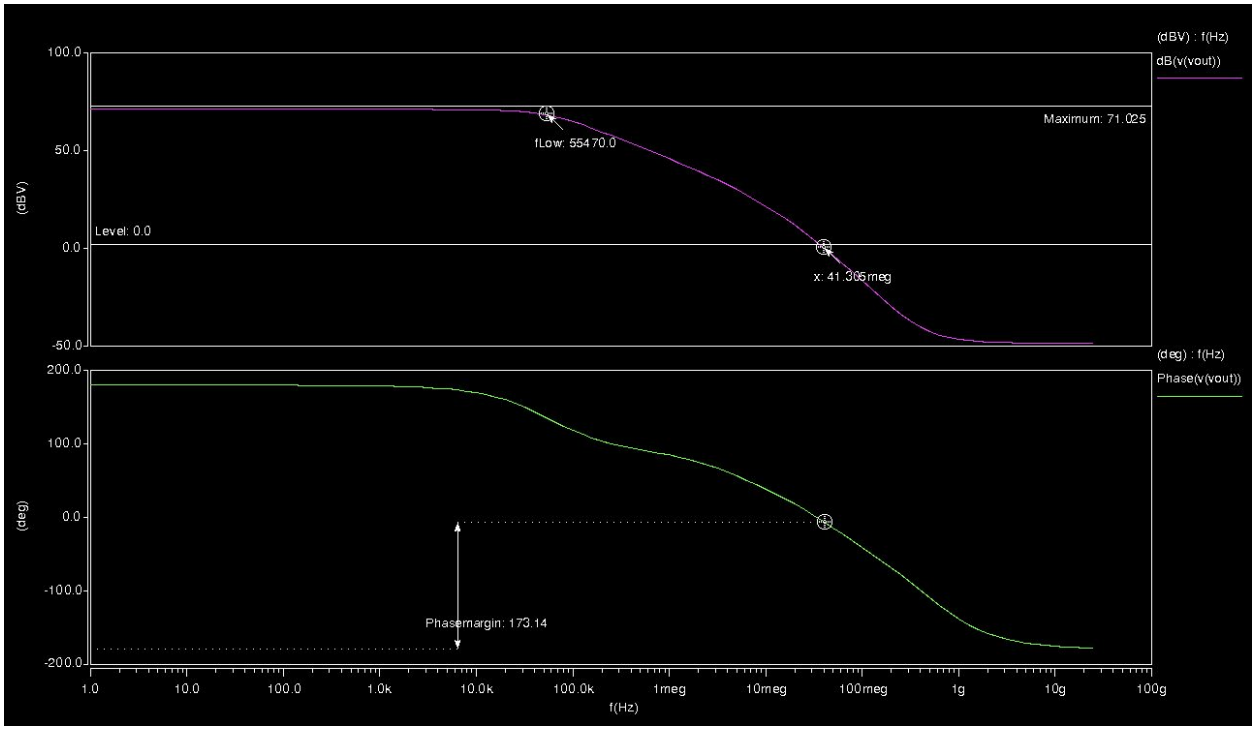
	Saturation
$C_{GD} =$	$C_{OV} * W$
$C_{GS} =$	$\frac{W*L*C_{OX}*2}{3} + C_{OV} * W$

$C_{GB} =$	0
$C_{SB} =$	$C_{SB} = EWC_j + 2(W+E)C_{jsw}$ Note:Bias dependant
$C_{DB} =$	$C_{SB} = EWC_j + 2(W+E)C_{jsw}$ Note:Bias dependant

Table 3 of Calculated Values for MOSFETS:

Transistor	Width (m)	Length (m)	W/L	AD (m^2)	AS (m^2)	PD (m)	PS(m)	Current (A)	Vgs	Vov	gm	rds		
M1	**5.0E-05**	**1.00E-06**	50.00	30.0E-12	30.0E-12	1.01200E-04	1.01200E-04	4.00E-05	0.5588299959		6.40937E-04			
M2	**5.0E-05**	**1.00E-06**	50.00	30.0E-12	30.0E-12	1.01200E-04	1.01200E-04	4.00E-05	0.5588299959		6.40937E-04	1.00E+05		
M3	**1.00E-04**	**1.00E-06**	100.00	60.0E-12	60.0E-12	2.01200E-04	2.01200E-04	4.00E-05	0.4344287162					
M4	**1.00E-04**	**1.00E-06**	100.00	60.0E-12	60.0E-12	2.01200E-04	2.01200E-04	4.00E-05	0.4344287162			1.00E+05		
M5	**2.00E-04**	**1.00E-06**	200.00	01.2E-10	01.2E-10	4.01200E-04	4.01200E-04	8.00E-05	0.5222718563					
M6	**4.00E-04**	**1.00E-06**	400.00	02.4E-10	02.4E-10	8.01200E-04	8.01200E-04	1.60E-04	0.4344287162		5.48E-03	2.50E+04		
M7	**4.00E-04**	**1.00E-06**	400.00	02.4E-10	02.4E-10	8.01200E-04	8.01200E-04	**1.60E-04**	0.5222718563			2.50E+04		
M8	**5.00E-05**	**1.00E-06**	50.00	30.0E-12	30.0E-12	1.01200E-04	1.01200E-04	**2.00E-05**	0.5222718563	0.08825915633				
Kn:	**2.3460E-04**	A/V^2			**Ratios:**			**Rout1:**	5.00E+04			**Av1:**	32.05	
Kp	**1.0270E-04**	A/V^2			I7/I5:	2.00E+00		**Rout2:**	1.25E+04			**Av2:**	-68.50	
Vth N:	**0.376033**	0.376033	V		(w/l)7/(w/l)5:	2.00E+00						**Av system:**	-2195.150109	
Vth P:	**-4.340127E-01**	0.4340127	V		(w/l)6/(2*(w/l)3):	2.00E+00								
Vin common:	**0.1**													
-0.8995839838	**<=**	Vin common (v)	**<=**	0.2529108478										
Lambda:	**0.25**													
V1	**V2**	**V3**	**V4**											
0.3777	0.6588299959	-0.4655712838	-0.4655712838											
Resistor	**Resistance (ohm)**	**Current (A)**	**Voltage drop(V)**											
R_ref	6.389E+04	2.00E-05	1.28E+00											
NMOS Capacitor Parameters:						**PMOS Capacitor Parameters:**						Cox:	8.85E-03	F/m^2
CGDO:	7.68E-10	F/m	NOTE: CGDO & CGSO are Cov			CGDO:	5.75E-10	F/m	NOTE: CGDO & CGSO are Cov					
CGSO:	7.68E-10	F/m				CGSO:	5.75E-10	F/m						
Cj:	9.623602E-04	F/m^2				Cj:	1.163939E-03	F/m^2						
Cjsw:	2.37186E-10	F/m				Cjsw:	1.656135E-10	F/m						
Cout:				**Cin:**				**Cc:**	1.00E-15	F		**P1:**	4.4886204E+06	rad/sec
CL:	5.00E-12	F		Cgs6:	2.6680E-12	F							7.1438612E+05	Hz
Cdb7:	4.12034896E-13	F		Cgd4:	7.680E-14	F						**P2:**	2.0050590E+07	rad/sec
Cgd7:	2.3000E-13	F		Cdb4:	10.5463435E-14	F							3.1911505E+06	Hz
Cdb6:	42.09998712E-14	F		Cdb2:	05.1678256E-14	F								
C2:	6.06303476 7E-12	F		Cgd2:	2.8750E-14	F						**Wu:**	1.5681848E+09	Hz
				C1:	2.9306917E-12	F								

Figure 3. Simulation Output of the Designed Op-Amp


(dBV) : f(Hz)
dB(v(vout))
Maximum: 71.025
fLow: 55470.0
Level: 0.0
x: 41.385meg
(dBV)
100.0
50.0
0.0
-50.0
(deg) : f(Hz)
Phase(v(vout))
200.0
100.0
0.0
-100.0
-200.0
(deg)
Phasemargin: 173.14
1.0
10.0
100.0
1.0k
10.0k
100.0k
1meg
10meg
100meg
1g
10g
100g
f(Hz)