(a) Upload the project report and netlist into Canvas. Report should be ECE422_YourName/Names_Project.pdf

(b) Further testbench instructions will be provided in class.

(c) Project can be done alone or in a group of two.

You are required to design a two-stage single ended CMOS opamp with Miller (pole-splitting) compensation in the 0.18μm process (the minimum channel length is 0.18μm). The parameters for this process are provided on Canvas. Your simulation results with the BSIM3 model must meet the specifications given below.

The final report should be no longer than 3 pages of text. Include a table comparing simulated results with the specifications. Attach all relevant analysis and simulations as appendices. If you are using hspice, you need to include AD/AS and PD/PS in your SPICE simulations. Assume AD = AS = 0.6μm $\cdot$ W, PD = PS = 1.2μm + 2$\cdot$W where W is the transistor width in μm. The layout is not part of the project.

What is the simulated input common mode range (i.e., V_{icmin} and $V_{ic,max}$) and output swing (i.e., $V_{o,max}$ and $V_{o,min}$) for the designed opamp? Please make sure that the project report is concise and well documented.

Load capacitance	5pF
Power supply	Vdd = 0.9V, Vss = -0.9V
Open loop gain	$\geq 65dB$
Phase margin	$\geq 60^{\circ}$
Unity gain frequency	$\geq 12MHz$