ECE 3410 Lecture Plan

A tentative lecture schedule is provided below. Homework problems are assigned weekly, on Wednesdays, and are due two weeks later on Wednesday. Each homework assignment is worth 100 points. There are 7 bi-weekly assignments, making 700 possible points. The number of problems in each assignment will vary according to their difficulty. Your final homework score will be adjusted based on the highest homework score in the class (i.e. if the highest achievement is 600 points, then 600 points = 100%).

Monday	Tuesday	Wednesday	Friday
Jan 9th **1** Introduction: History of Electronics. Ch. 1	10th	11th **2** History continued; review of signals, systems and amplifiers, frequency response, Bode plots. Ch. 1	13th **3** Ideal amplifier models; input and output resistance. Ch. 1
16th **MLK/Human Rights Day**	17th	18th **4** Small-signal models, linearization, capacitive coupling. Ch. 1	20th **5** Cascades of amplifiers, negative feedback. Ch. 1
23rd **6** Operational Amplifiers: Ideal Behavior; inverting and non-inverting configurations; transconductance configuration. Ch. 2.1–2.4	24th	25th **7** Operational Amplifiers: Differential and common-mode analysis of instrumentation amplifiers. Ch. 2.3–2.6	27th **8** Common-mode analysis of instrumentation amplifier; finite gain effects; offset voltage.
30th **9** Non-ideal effects continued; bias current.	31st	Feb 1st **10** Operational Amplifiers: Integrators and Differentiators Ch. 2.5	3rd **11** Frequency Response, Gain-Bandwidth Tradeoff, Slewing Ch. 2.7–2.8
6th **12** Diodes: Device models, basic analysis. Ch. 4.1–4.3	7th	8th **13** Diode logic, crossbar logic. Ch. 4.1–4.3	10th **14** Basic rectifier circuits, iterative analysis, linearized analysis. Ch. 4.3
13th **15** Voltage regulators. Ch. 4.3	14th	15th **16** Rectifier Circuits, peak rectifier, superdiodes Ch. 4.5	17th **17** DC Restoration, envelope detector applications.
20th **Presidents' Day**	21st **18** Reverse bias operation, Zener diodes, photodiodes, LEDs. Ch. 4.4, 4.7	22nd **19** Limiting and clamping circuits, ESD protection. Ch. 4.5–4.6	24th **20** Power conversion, boost converters. Handout.
27th **Midterm Review**	28th	Mar 1st **Midterm Exam**	3rd Advanced diode applications
6th **Spring Break**	7th	8th **Spring Break**	10th **Spring Break**

Monday	Tuesday	Wednesday	Friday
13th **21** Semiconductor physics. 3.1–3.3	14th	15th **22** PN junction theory. 3.4–3.5	17th **23** Reverse-biased junctions; capacitive effects. 3.5–3.6
20th **24** MOSFETs: switch model; complementary PMOS and NMOS devices; Threshold voltage; square-law characteristics. 5.1–5.2	21st	22nd **25** MOSFET modes: saturation, triode and cutoff. 5.2	24th **26** DC analysis of MOSET circuits. 5.3
27th **27** Small-signal analysis of MOSFET circuits. 5.4–5.5	28th	29th **28** MOSFET amplifiers: Common Source configurations. 5.6.1–5.6.4	31st **29** MOSFET amplifiers: Common Gate configurations. 5.6.5
Apr 3rd **30** MOSFET amplifiers: Source Follower configurations. 5.6.6	4th	5th **31** Biasing and signal coupling in discrete MOSFET amplifiers 5.7–5.8	7th **32** BJT physical structure; differences from MOSFETs Ch. 6.1
10th **33** BJT operation: Active and Saturation. Ch. 6.1–6.2	11th	12th **34** DC analysis of BJT circuits. Ch. 6.3	14th **35** BJT amplifiers and small-signal models. Ch. 6.4–6.5
17th **36** BJT amplifiers: Common Emitter configuration. Ch. 6.6.1–6.6.3	18th	19th **37** BJT amplifiers: Common Base configuration. Ch. 6.6.4	21st **38** BJT amplifiers: Emitter Follower configuration. Ch. 6.6.5
24th **39** Biasing BJT amplifier circuits. Ch. 6.7	25th	26th **40** Signal coupling and frequency response of BJT amplifiers. Ch. 6.8	28th **41** **Final Review**
May 1st **Final Exam** **9:30am–11:20am**	2nd	3rd	5th

Lab Schedule

Lab sessions are held in the ECE Circuits Lab, EL 104. Some sessions, particularly SPICE exercises, will be held across the hall in the Design Automation Lab (DAL), EL 105. You may continue working on hardware labs during weeks when SPICE tutorials are assigned. The SPICE exercises may be done at any time, but you will have access to TA or instructor assistance during the official lab sessions.

You must complete each lab assignment before the scheduled start date of the next lab assignment. The final lab assignment must be completed *before* finals week. A lab assignment is considered complete when (1) the TA has checked off your lab book and recorded your score, and (2) you have turned in a written report on your findings.

Week 1. (Jan. 12) NO LAB

Week 2. (Jan. 19) Lab Introduction; Policies and Procedures,
Linux tutorial, SPICE 1 (EL 105, DAL).

Week 3. (Jan. 26) Lab 1 – Equipment and Methods (EL 104).

Week 4. (Feb. 2) SPICE 2 (EL 105, DAL).

Week 5. (Feb. 9) Lab 2 – Operational Amplifiers, Part I (EL 104).

Week 6. (Feb. 16) SPICE 3 (EL 105, DAL).

Week 7. (Feb. 23) Lab 3 – Operational Amplifiers, Part II (EL 104).

Week 8. (Mar. 2) Lab 3 continued (EL 104).

Week 9. SPRING BREAK

Week 10. (Mar. 16) SPICE 4 (EL 105, DAL).

Week 11. (Mar. 23) Lab 4 – Diodes (EL 104).

Week 12. (Mar. 30) SPICE 5 (EL 105, DAL).

Week 13. (Apr. 6) Lab 5 – MOSFETs (EL 104).

Week 14. (Apr. 13) SPICE 6 (EL 105, DAL).

Week 15. (Apr. 20) Lab 6 – BJTs (EL 104).

Week 16. (Apr. 27) Extra time.