HVcounter:

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
entity HVcounter is
Port ( clk : in std_logic ;
H : out std_logic_vector (9 downto 0);
V : out std_logic_vector(9 downto 0));
end HVcounter ;
architecture arch of HVcounter is
        signal hh: unsigned(9 downto 0) := "0000000000";
        signal vv: unsigned(9 downto 0) := "0000000000";
begin
process(clk) is
begin
        if rising_edge(clk) then
        if hh=799 then
        if vv=524 then
                H<=std_logic_vector(hh);
                V<=std_logic_vector(vv);
        else
                hh<="00000000";
                vv<=vv + 1;
        end if;
        else
                hh<=hh+ 1;
end if;
end if;
end process;
end arch;
```

V_sync_gen:

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
entity V_sync_gen is
Port (
V : in std_logic_vector (9 downto 0);
V_sync : out std_logic);
end V_sync_gen;
architecture arch of V_sync_gen is
signal vv: unsigned (9 downto 0);
begin
process(vv)is
begin
if vv>2 then
V_sync<='1';
end if;
end process;
vv <= unsigned(V);
end arch;
```

H_sync_gen:

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
entity H_sync_gen is
Port (
H : in std_logic_vector (9 downto 0);
H_sync : out std_logic);
end H_sync_gen;
architecture arch of H_sync_gen is
signal hh: unsigned (9 downto 0);
begin
process(hh)is
begin
if hh < 97 then
H_sync<='0';
elsif hh>96 then
H_sync<='1';
end if;
end process;
hh <= unsigned(H);
end arch;
```

RGBgenerator:

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
entity RGBgenerator is
Port (
H : in std_logic_vector (9 downto 0);
V : in std_logic_vector (9 downto 0);
R : out std_logic;
G : out std_logic;
B : out std_logic);
end RGBgenerator;
architecture arch of RGBgenerator is
signal vv: unsigned(9 downto 0);
signal hh: unsigned(9 downto 0);
begin
process(hh,vv) is
begin
if vv<3 then
R<='0';
G<='0';
B<='0';
elsif vv > 1 then
if vv < 11 and vv > 1 then
if hh>95 then
R<='0';
G<='0';
B<='0';
end if;
elsif vv> 11 then
if hh>95 and hh<112 then
```

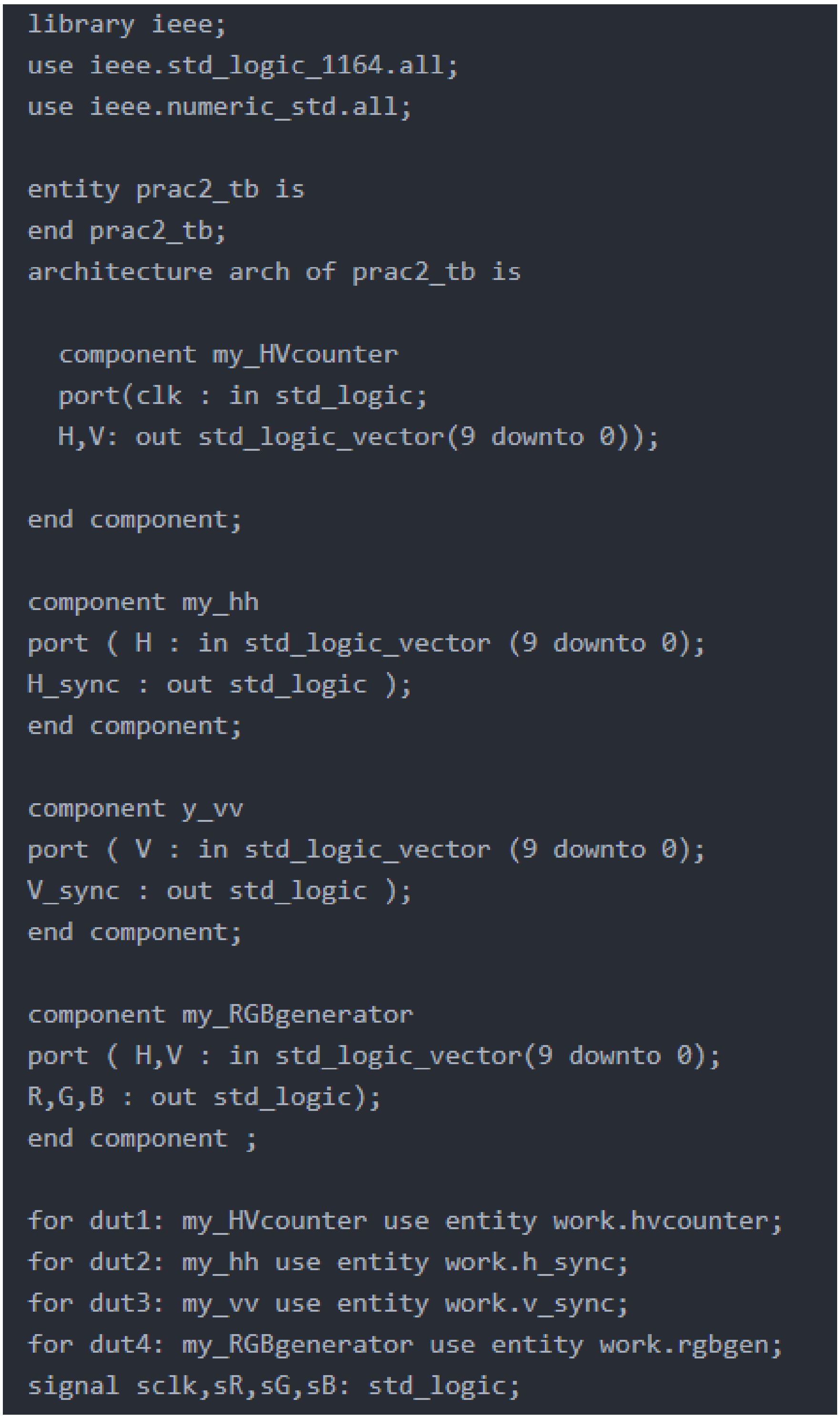
```
R<='0';

G<='0';

B<='0';

elsif hh>111 and hh<752 then

R<='1';

G<='0';

B<='0';

elsif hh>751 then

R<='0';

G<='0';

B<='0';

end if;

end if;

end if;

end process;

hh<=unsigned(H);

vv<=unsigned(V);

end arch;
```

Previ 9:

```
-- Declarem les llibraries
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
-- Inici
entity rgbBRgen is
Port (
H : in STD_LOGIC_VECTOR (9 downto 0);
V : in STD_LOGIC_VECTOR (9 downto 0);
R : out STD_LOGIC;
G : out STD_LOGIC;
B : out STD_LOGIC);
end rgbBRgen;
architecture arch of rgbBRgen is
signal vv: unsigned( 9 downto 0);
signal hh: unsigned (9 downto 0);
begin
process(hh,vv) is
begin
if vv < 2 then
R <= '1';
G <= '1';
B <= '1';
elsif vv > 1 then
if vv < 12 and vv > 1 then
if hh > 95 then
R <= '0';
G <= '0';
B <= '0';
end if;
```

```
elsif vv > 11 then
if hh > 95 and hh < 112 then
R <= '0';
G <= '0';
B <= '0';
elsif hh > 111 and hh < 432 then
R <= '0';
G <= '0';
B <= '1';
elsif hh < 752 and hh > 431 then
R <= '1';
G <= '0';
B <= '0';
elsif hh > 751 then
R <= '0';
G <= '0';
B <= '0';
end if;
end if;
end if;
end process;
vv <= unsigned(V);
hh <= unsigned(H);
end arch;
```

TEST BENCH's:



```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity prac2_tb is
end prac2_tb;
architecture arch of prac2_tb is

  component my_HVcounter
  port(clk : in std_logic;
  H,V: out std_logic_vector(9 downto 0));

end component;

component my_hh
port ( H : in std_logic_vector (9 downto 0);
H_sync : out std_logic );
end component;

component y_vv
port ( V : in std_logic_vector (9 downto 0);
V_sync : out std_logic );
end component;

component my_RGBgenerator
port ( H,V : in std_logic_vector(9 downto 0);
R,G,B : out std_logic);
end component ;

for dut1: my_HVcounter use entity work.hvcounter;
for dut2: my_hh use entity work.h_sync;
for dut3: my_vv use entity work.v_sync;
for dut4: my_RGBgenerator use entity work.rgbgen;
signal sclk,sR,sG,sB: std_logic;
```

No he pogut fer cap simulació amb GTKWave perquè m'és impossible instal·lar-lo.