***HVcounter:***

library ieee;

use ieee.std\_logic\_1164.all;

use ieee.numeric\_std.all;

entity HVcounter is

Port ( clk : in std\_logic ;

H : out std\_logic\_vector (9 downto 0);

V : out std\_logic\_vector(9 downto 0));

end HVcounter ;

architecture arch of HVcounter is

signal hh: unsigned(9 downto 0) := "0000000000";

signal vv: unsigned(9 downto 0) := "0000000000";

begin

process(clk) is

begin

if rising\_edge(clk) then

if hh=799 then

if vv=524 then

H<=std\_logic\_vector(hh);

V<=std\_logic\_vector(vv);

else

hh<="00000000";

vv<=vv + 1;

end if;

else

hh<=hh+ 1;

end if;

end if;

end process;

end arch;

***V\_sync\_gen:***

library ieee;

use ieee.std\_logic\_1164.all;

use ieee.numeric\_std.all;

entity V\_sync\_gen is

Port (

V : in std\_logic\_vector (9 downto 0);

V\_sync : out std\_logic);

end V\_sync\_gen;

architecture arch of V\_sync\_gen is

signal vv: unsigned (9 downto 0);

begin

process(vv)is

begin

if vv>2 then

V\_sync<='1';

end if;

end process;

vv <= unsigned(V);

end arch;

***H\_sync\_gen***:

library ieee;

use ieee.std\_logic\_1164.all;

use ieee.numeric\_std.all;

entity H\_sync\_gen is

Port (

H : in std\_logic\_vector (9 downto 0);

H\_sync : out std\_logic);

end H\_sync\_gen;

architecture arch of H\_sync\_gen is

signal hh: unsigned (9 downto 0);

begin

process(hh)is

begin

if hh < 97 then

H\_sync<='0';

elsif hh>96 then

H\_sync<='1';

end if;

end process;

hh <= unsigned(H);

end arch;

***RGBgenerator:***

library ieee;

use ieee.std\_logic\_1164.all;

use ieee.numeric\_std.all;

entity RGBgenerator is

Port (

H : in std\_logic\_vector (9 downto 0);

V : in std\_logic\_vector (9 downto 0);

R : out std\_logic;

G : out std\_logic;

B : out std\_logic);

end RGBgenerator;

architecture arch of RGBgenerator is

signal vv: unsigned(9 downto 0);

signal hh: unsigned(9 downto 0);

begin

process(hh,vv) is

begin

if vv<3 then

R<='0';

G<='0';

B<='0';

elsif vv > 1 then

if vv < 11 and vv > 1 then

if hh>95 then

R<='0';

G<='0';

B<='0';

end if;

elsif vv> 11 then

if hh>95 and hh<112 then

R<='0';

G<='0';

B<='0';

elsif hh>111 and hh<752 then

R<='1';

G<='0';

B<='0';

elsif hh>751 then

R<='0';

G<='0';

B<='0';

end if;

end if;

end if;

end process;

hh<=unsigned(H);

vv<=unsigned(V);

end arch;

***Previ 9:***

-- Declarem les llibraries

library ieee;

use ieee.std\_logic\_1164.all;

use ieee.numeric\_std.all;

-- Inici

entity rgbBRgen is

Port (

H : in STD\_LOGIC\_VECTOR (9 downto 0);

V : in STD\_LOGIC\_VECTOR (9 downto 0);

R : out STD\_LOGIC;

G : out STD\_LOGIC;

B : out STD\_LOGIC);

end rgbBRgen;

architecture arch of rgbBRgen is

signal vv: unsigned( 9 downto 0);

signal hh: unsigned (9 downto 0);

begin

process(hh,vv) is

begin

if vv < 2 then

R <= '1';

G <= '1';

B <= '1';

elsif vv > 1 then

if vv < 12 and vv > 1 then

if hh > 95 then

R <= '0';

G <= '0';

B <= '0';

end if;

elsif vv > 11 then

if hh > 95 and hh < 112 then

R <= '0';

G <= '0';

B <= '0';

elsif hh > 111 and hh < 432 then

R <= '0';

G <= '0';

B <= '1';

elsif hh < 752 and hh > 431 then

R <= '1';

G <= '0';

B <= '0';

elsif hh > 751 then

R <= '0';

G <= '0';

B <= '0';

end if;

end if;

end if;

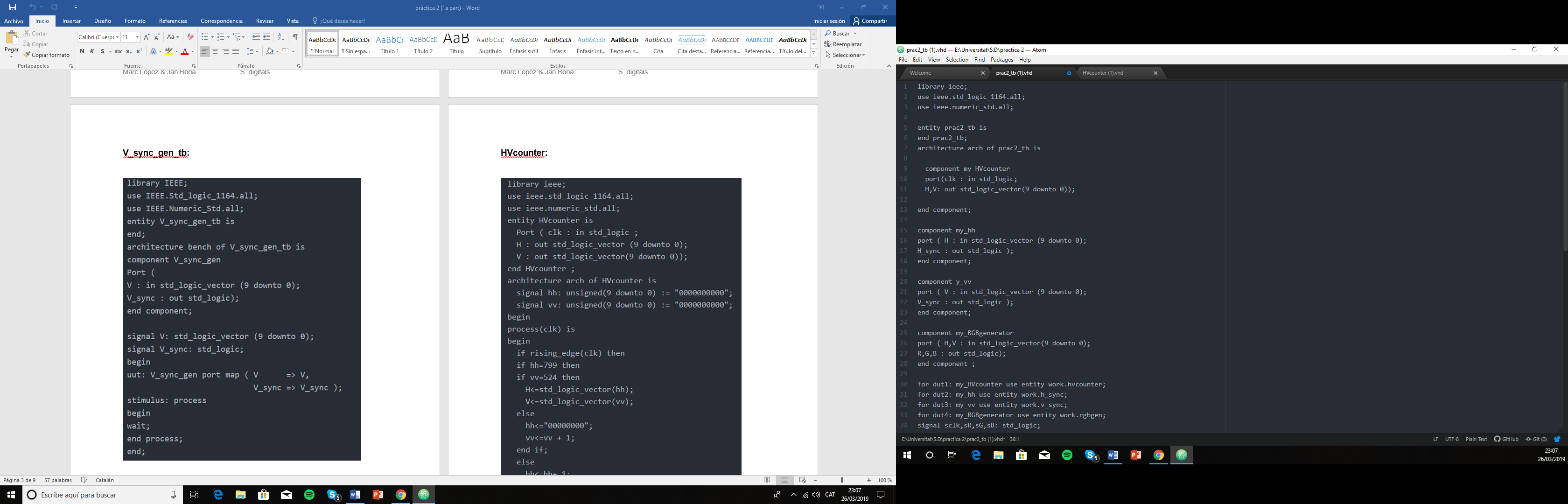
end process;

vv <= unsigned(V);

hh <= unsigned(H);

end arch;

TEST BENCH’s:



No he pogut fer cap simulació amb GTKWave perquè m’és impossible instal·lar-lo.