Section 36. Configurable Logic Cell

HIGHLIGHTS

This section of the manual contains the following major topics:

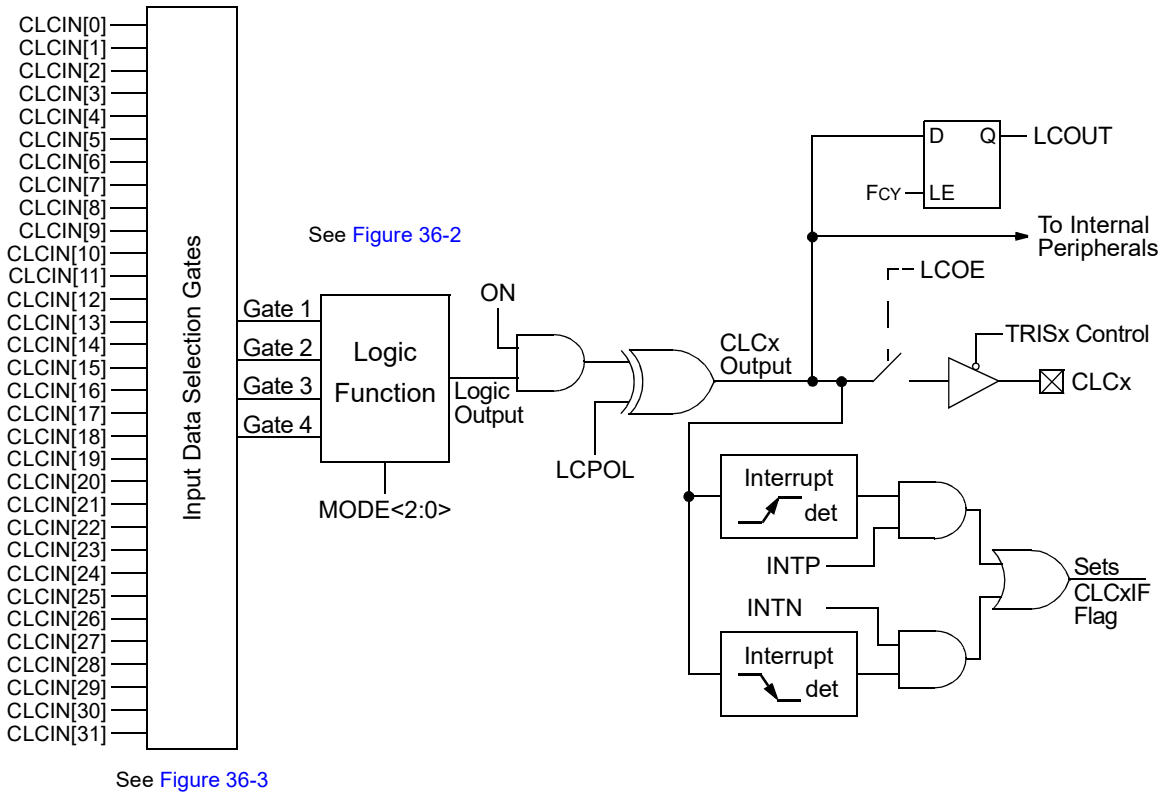
Note:	This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all PIC32 devices. Please consult the note at the beginning of the **"Configurable Logic Cell (CLC)"** chapter in the current device data sheet to check whether this document supports the device you are using. Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Web site at: http://www.microchip.com

36.1 INTRODUCTION

The Configurable Logic Cell (CLC) module enables the user to specify combinations of signals as inputs to a logic function, and to use the logic output to control other peripherals or I/O pins. This provides greater flexibility and potential in embedded designs, because the CLC module can operate outside the limitations of software execution, and supports a vast amount of output designs.

Each of the four independent input provider gates can execute a simple function of application defined inputs to produce a logic function input. A typical input selector configuration, as shown in Figure 36-1, has four inputs selected from a pool of 32 signals.

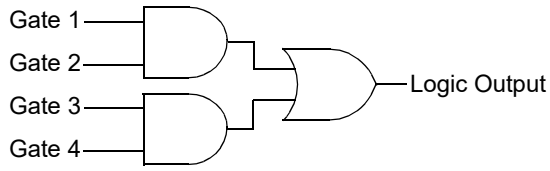
Figure 36-1: Configurable Logic Cell



Note: All register bits shown in this figure can be found in the CLCxCON register.

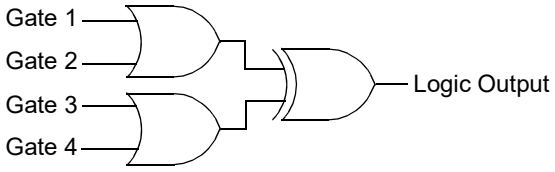
Figure 36-2: Logic Function Combinatorial Options

AND – OR



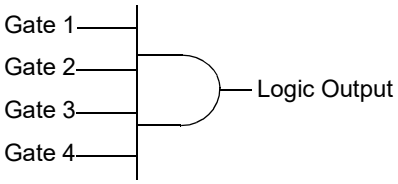
MODE<2:0> = 000

OR – XOR



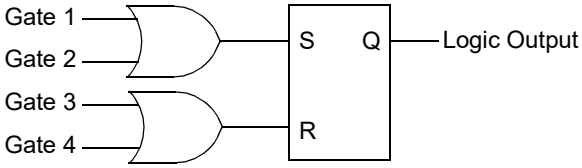
MODE<2:0> = 001

4-Input AND



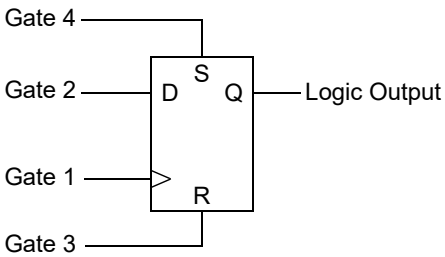
MODE<2:0> = 010

S-R Latch



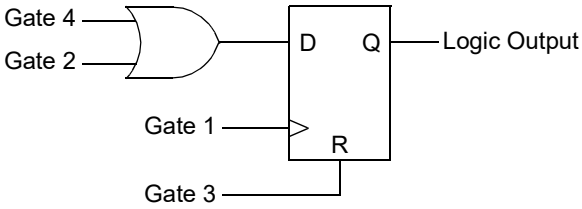
MODE<2:0> = 011

1-Input D Flip-Flop with S and R



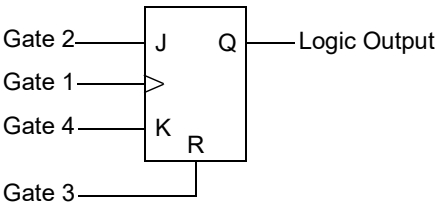
MODE<2:0> = 100

2-Input D Flip-Flop with R



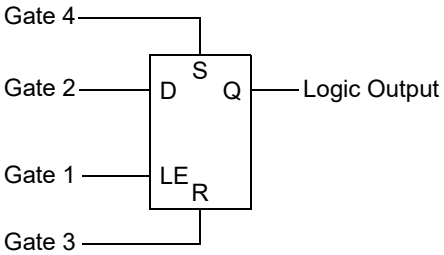
MODE<2:0> = 101

J-K Flip-Flop with R



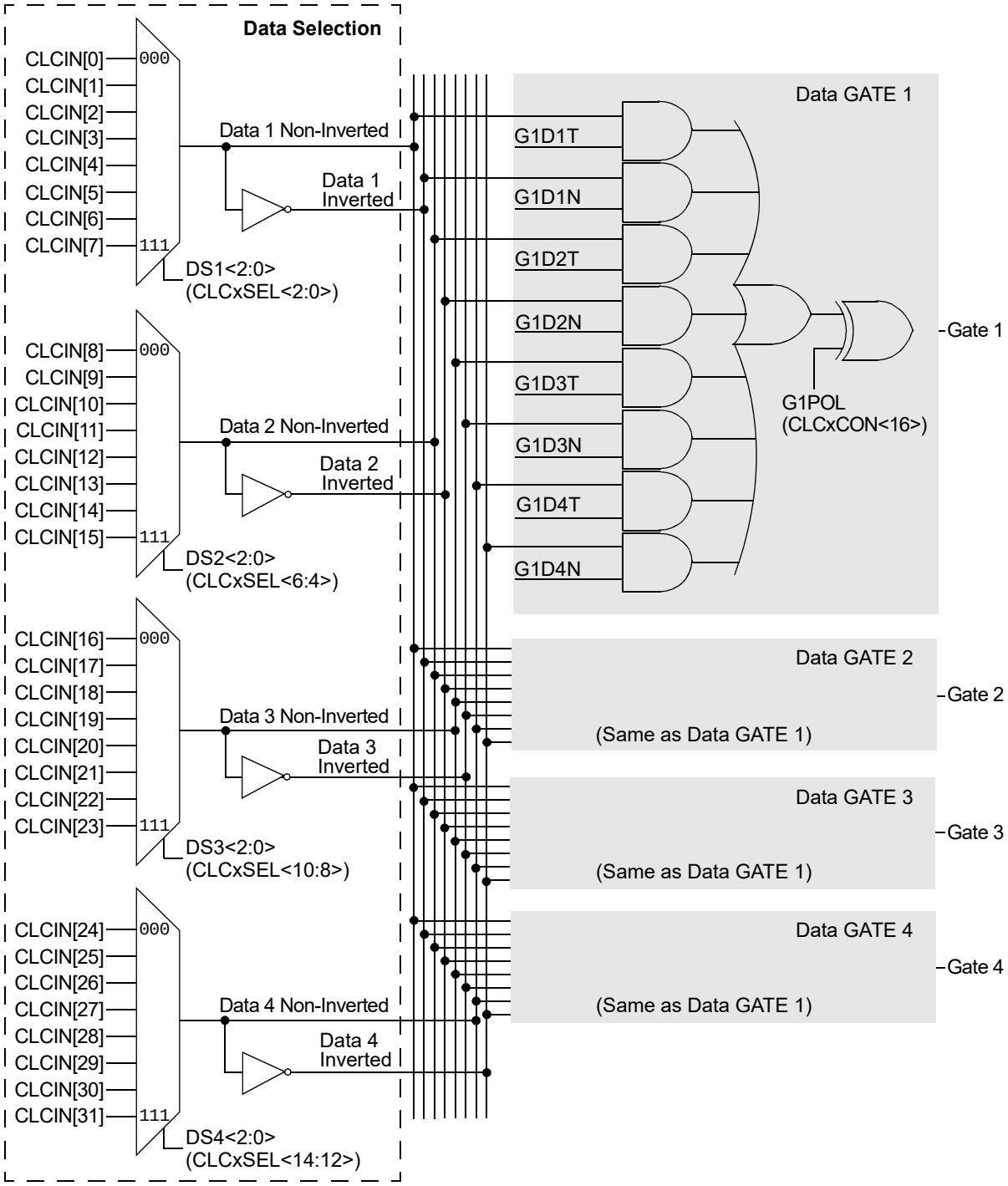
MODE<2:0> = 110

1-Input Transparent Latch with S and R



MODE<2:0> = 111

Figure 36-3: CLC Input Source Selection Diagram



Note: All controls are undefined at power-up.

36.2 REGISTERS

The CLC module is controlled by the following registers:

- CLCxCON
- CLCxSEL
- CLCxGLS

The CLCx Control register (CLCxCON) is used to enable the module and interrupts, control the output enable bit, select output polarity and select the logic function. The CLCx Control register also allows the user to control the logic polarity of not only the cell output, but also some intermediate variables.

The CLCx Input MUX Select register (CLCxSEL) allows the user to select one out of eight input signals for each of the four data selection multiplexers, pictured inside the dashed line in Figure 36-3. The output of each of the four data selection multiplexers is connected to the inputs of the logic function selected by the MODE<2:0> bits (CLCxCON<2:0>), see Figure 36-2.

The CLCx Source Enable register (CLCxGLS) allows the user to create any four variable boolean expressions from the four input data sources configured by CLCxSEL. Both the True and complimentary values for each of the four signals, chosen by the CLCx Input MUX Select register (CLCxSEL), are available to the sum-of-products circuit pictured in the data gate in Figure 36-3.

Table 36-1 provides a brief summary of all CLC module-related registers. Corresponding registers appear after the summary, followed by a detailed description of each register.

Table 36-1: Configurable Logic Cell SFRs Summary

Name	Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
CLCxCON	31:24	—	—	—	—	—	—	—	—
	23:16	—	—	—	—	G4POL	G3POL	G2POL	G1POL
	15:8	ON	—	—	—	INTP	INTN	—	—
	7:0	LCOE	LCOUT	LCPOL	—	—	MODE<2:0>		
CLCxSEL	31:24	—	—	—	—	—	—	—	—
	23:16	—	—	—	—	—	—	—	—
	15:8	—	DS4<2:0>			—	DS3<2:0>		
	7:0	—	DS2<2:0>			—	DS1<2:0>		
CLCxGLS	31:24	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N
	23:16	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
	15:8	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
	7:0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N

Register 36-1: CLCxCON: Configurable Logic Cell x Control Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	G4POL	G3POL	G2POL	G1POL
15:8	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0
	ON	—	—	—	INTP	INTN	—	—
7:0	R-0	R-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	LCOE	LCOUT	LCPOL	—	—	MODE<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-20 **Unimplemented:** Read as '0'

bit 19 **G4POL:** Gate 4 Polarity Control bit
1 = The output of Gate 4 logic is inverted when applied to the logic cell
0 = The output of Gate 4 logic is not inverted

bit 18 **G3POL:** Gate 3 Polarity Control bit
1 = The output of Gate 3 logic is inverted when applied to the logic cell
0 = The output of Gate 3 logic is not inverted

bit 17 **G2POL:** Gate 2 Polarity Control bit
1 = The output of Gate 2 logic is inverted when applied to the logic cell
0 = The output of Gate 2 logic is not inverted

bit 16 **G1POL:** Gate 1 Polarity Control bit
1 = The output of Gate 1 logic is inverted when applied to the logic cell
0 = The output of Gate 1 logic is not inverted

bit 15 **ON:** Configurable Logic Cell Enable bit
1 = Configurable Logic Cell is enabled and mixing input signals
0 = Configurable Logic Cell is disabled and has logic zero outputs

bit 14-12 **Unimplemented:** Read as '0'

bit 11 **INTP:** Configurable Logic Cell Positive Edge Interrupt Enable bit
1 = Interrupt will be generated when a rising edge occurs on LCOUT
0 = Interrupt will not be generated

bit 10 **INTN:** Configurable Logic Cell Negative Edge Interrupt Enable bit
1 = Interrupt will be generated when a falling edge occurs on LCOUT
0 = Interrupt will not be generated

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **LCOE:** Configurable Logic Cell Port Enable bit
1 = Configurable Logic Cell port pin output is enabled
0 = Configurable Logic Cell port pin output is disabled

bit 6 **LCOUT:** Configurable Logic Cell Data Output Status bit
1 = Configurable Logic Cell output high
0 = Configurable Logic Cell output low

bit 5 **LCPOL:** Configurable Logic Cell Output Polarity Control bit
1 = The output of the module is inverted
0 = The output of the module is not inverted

Register 36-1: CLCxCON: Configurable Logic Cell x Control Register (Continued)

bit 4-3 **Unimplemented:** Read as '0'

bit 2-0 **MODE<2:0>:** Configurable Logic Cell Mode bits

111 = Cell is 1-input transparent latch with S and R
110 = Cell is J-K flip-flop with R
101 = Cell is 2-input D flip-flop with R
100 = Cell is 1-input D flip-flop with S and R
011 = Cell is SR latch
010 = Cell is 4-input AND
001 = Cell is OR-XOR
000 = Cell is AND-OR

Register 36-2: CLCxSEL: Configurable Logic Cell x Input MUX Select Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
	—	DS4<2:0>			—	DS3<2:0>		
7:0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
	—	DS2<2:0>			—	DS1<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-15 **Unimplemented:** Read as '0'

bit 14-12 **DS4<2:0>:** Data Selection MUX 4 Signal Selection bits
xxx = Device-specific; refer to the device data sheet for gate select mapping for MUX 4

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **DS3<2:0>:** Data Selection MUX 3 Signal Selection bits
xxx = Device-specific; refer to the device data sheet for gate select mapping for MUX 3

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **DS2<2:0>:** Data Selection MUX 2 Signal Selection bits
xxx = Device-specific; refer to the device data sheet for gate select mapping for MUX 2

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **DS1<2:0>:** Data Selection MUX 1 Signal Selection bits
xxx = Device-specific; refer to the device data sheet for gate select mapping for MUX 1

Register 36-3: CLCxGLS: Configurable Logic Cell x Source Enable Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **G4D4T:** Gate 4 Data 4 True Enable bit
1 = The Data 4 (non-inverted) signal is enabled for Gate 4
0 = The Data 4 (non-inverted) signal is disabled for Gate 4

bit 30 **G4D4N:** Gate 4 Data 4 Negated Enable bit
1 = The Data 4 (inverted) signal is enabled for Gate 4
0 = The Data 4 (inverted) signal is disabled for Gate 4

bit 29 **G4D3T:** Gate 4 Data 3 True Enable bit
1 = The Data 3 (non-inverted) signal is enabled for Gate 4
0 = The Data 3 (non-inverted) signal is disabled for Gate 4

bit 28 **G4D3N:** Gate 4 Data 3 Negated Enable bit
1 = The Data 3 (inverted) signal is enabled for Gate 4
0 = The Data 3 (inverted) signal is disabled for Gate 4

bit 27 **G4D2T:** Gate 4 Data 2 True Enable bit
1 = The Data 2 (non-inverted) signal is enabled for Gate 4
0 = The Data 2 (non-inverted) signal is disabled for Gate 4

bit 26 **G4D2N:** Gate 4 Data 2 Negated Enable bit
1 = The Data 2 (inverted) signal is enabled for Gate 4
0 = The Data 2 (inverted) signal is disabled for Gate 4

bit 25 **G4D1T:** Gate 4 Data 1 True Enable bit
1 = The Data 1 (non-inverted) signal is enabled for Gate 4
0 = The Data 1 (non-inverted) signal is disabled for Gate 4

bit 24 **G4D1N:** Gate 4 Data 1 Negated Enable bit
1 = The Data 1 (inverted) signal is enabled for Gate 4
0 = The Data 1 (inverted) signal is disabled for Gate 4

bit 23 **G3D4T:** Gate 3 Data 4 True Enable bit
1 = The Data 4 (non-inverted) signal is enabled for Gate 3
0 = The Data 4 (non-inverted) signal is disabled for Gate 3

bit 22 **G3D4N:** Gate 3 Data 4 Negated Enable bit
1 = The Data 4 (inverted) signal is enabled for Gate 3
0 = The Data 4 (inverted) signal is disabled for Gate 3

bit 21 **G3D3T:** Gate 3 Data 3 True Enable bit
1 = The Data 3 (non-inverted) signal is enabled for Gate 3
0 = The Data 3 (non-inverted) signal is disabled for Gate 3

Register 36-3: CLCxGLS: Configurable Logic Cell x Source Enable Register (Continued)

bit 20 **G3D3N:** Gate 3 Data 3 Negated Enable bit
1 = The Data 3 (inverted) signal is enabled for Gate 3
0 = The Data 3 (inverted) signal is disabled for Gate 3

bit 19 **G3D2T:** Gate 3 Data 2 True Enable bit
1 = The Data 2 (non-inverted) signal is enabled for Gate 3
0 = The Data 2 (non-inverted) signal is disabled for Gate 3

bit 18 **G3D2N:** Gate 3 Data 2 Negated Enable bit
1 = The Data 2 (inverted) signal is enabled for Gate 3
0 = The Data 2 (inverted) signal is disabled for Gate 3

bit 17 **G3D1T:** Gate 3 Data 1 True Enable bit
1 = The Data 1 (non-inverted) signal is enabled for Gate 3
0 = The Data 1 (non-inverted) signal is disabled for Gate 3

bit 16 **G3D1N:** Gate 3 Data 1 Negated Enable bit
1 = The Data 1 (inverted) signal is enabled for Gate 3
0 = The Data 1 (inverted) signal is disabled for Gate 3

bit 15 **G2D4T:** Gate 2 Data 4 True Enable bit
1 = The Data 4 (non-inverted) signal is enabled for Gate 2
0 = The Data 4 (non-inverted) signal is disabled for Gate 2

bit 14 **G2D4N:** Gate 2 Data 4 Negated Enable bit
1 = The Data 4 (inverted) signal is enabled for Gate 2
0 = The Data 4 (inverted) signal is disabled for Gate 2

bit 13 **G2D3T:** Gate 2 Data 3 True Enable bit
1 = The Data 3 (non-inverted) signal is enabled for Gate 2
0 = The Data 3 (non-inverted) signal is disabled for Gate 2

bit 12 **G2D3N:** Gate 2 Data 3 Negated Enable bit
1 = The Data 3 (inverted) signal is enabled for Gate 2
0 = The Data 3 (inverted) signal is disabled for Gate 2

bit 11 **G2D2T:** Gate 2 Data 2 True Enable bit
1 = The Data 2 (non-inverted) signal is enabled for Gate 2
0 = The Data 2 (non-inverted) signal is disabled for Gate 2

bit 10 **G2D2N:** Gate 2 Data 2 Negated Enable bit
1 = The Data 2 (inverted) signal is enabled for Gate 2
0 = The Data 2 (inverted) signal is disabled for Gate 2

bit 9 **G2D1T:** Gate 2 Data 1 True Enable bit
1 = The Data 1 (non-inverted) signal is enabled for Gate 2
0 = The Data 1 (non-inverted) signal is disabled for Gate 2

bit 8 **G2D1N:** Gate 2 Data 1 Negated Enable bit
1 = The Data 1 (inverted) signal is enabled for Gate 2
0 = The Data 1 (inverted) signal is disabled for Gate 2

bit 7 **G1D4T:** Gate 1 Data 4 True Enable bit
1 = The Data 4 (non-inverted) signal is enabled for Gate 1
0 = The Data 4 (non-inverted) signal is disabled for Gate 1

bit 6 **G1D4N:** Gate 1 Data 4 Negated Enable bit
1 = The Data 4 (inverted) signal is enabled for Gate 1
0 = The Data 4 (inverted) signal is disabled for Gate 1

bit 5 **G1D3T:** Gate 1 Data 3 True Enable bit
1 = The Data 3 (non-inverted) signal is enabled for Gate 1
0 = The Data 3 (non-inverted) signal is disabled for Gate 1

bit 4 **G1D3N:** Gate 1 Data 3 Negated Enable bit
1 = The Data 3 (inverted) signal is enabled for Gate 1
0 = The Data 3 (inverted) signal is disabled for Gate 1

Register 36-3: CLCxGLS: Configurable Logic Cell x Source Enable Register (Continued)

bit 3 **G1D2T:** Gate 1 Data 2 True Enable bit
1 = The Data 2 (non-inverted) signal is enabled for Gate 1
0 = The Data 2 (non-inverted) signal is disabled for Gate 1

bit 2 **G1D2N:** Gate 1 Data 2 Negated Enable bit
1 = The Data 2 (inverted) signal is enabled for Gate 1
0 = The Data 2 (inverted) signal is disabled for Gate 1

bit 1 **G1D1T:** Gate 1 Data 1 True Enable bit
1 = The Data 1 (non-inverted) signal is enabled for Gate 1
0 = The Data 1 (non-inverted) signal is disabled for Gate 1

bit 0 **G1D1N:** Gate 1 Data 1 Negated Enable bit
1 = The Data 1 (inverted) signal is enabled for Gate 1
0 = The Data 1 (inverted) signal is disabled for Gate 1

36.3 CLC SETUP

CLCxCON configures the overall operation of the CLC. The ON bit must be set for the CLC to operate. All registers can be programmed while ON is clear. The GxPOL bits configure the polarity of the data selection multiplexer's output. The LCOUT bit is read-only and reflects the status of the logic cell output. The CLC interrupt can be triggered on the positive or negative edge of LCOUT by setting INTP or INTN. Both the ON and LCOE bits must be set for the module to control the CLCxOUT pin (the I/O pin must be configured as a digital output for CLCxOUT to be present and the presence of the signal is subject to peripherals of higher priority). The logic cell output is driven to an I/O pin when LCOE = 1. When set, the CLC requests control of an I/O pin. When cleared, the logic cell output is kept internal to the microcontroller.

The MODE<2:0> bits set the functional behavior of the logic cell. There are eight logic cells available, as shown in Figure 36-2. When the MODE<2:0> bits are changed, the value of the latch and flip-flop logic cells remains the same, provided LE, R or S do not force a change.

Three of the state options define "Gate 1" as a rising edge clock with the traditional meanings of D and J-K flip-flops. The 4th state option (MODE<2:0> = 111) is a transparent latch; Q follows D when LE is true; Q holds state when LE is false. For options with both S (Set) and R (Reset) inputs, the output changes asynchronously to the clock when S or R is a logic '1'; R is dominant. The R and S inputs to the combinatorial RS latch (MODE<2:0> = 011) do not affect the value of the state register ('1xx'). Options drawn with an unconnected S input have S tied to an inactive state.

The final polarity of the CLC module output is controlled by LCPOL. The output is inverted when LCPOL = 1 and uninverted when LCPOL = 0. The GxPOL bits control the polarity of the logic function inputs.

The CLCxSEL (Register 36-2) register controls which input signals are routed to the input bus of Figure 36-3. Both the True (T) and Negated (N) values are made available in the data bus. The CLCxGLS register selects which signals from the data bus are applied to the input OR gates. True and Negated inputs are separately enabled; enabling both is not recommended. Refer to Example 36-1 for sample CLC configuration code.

Example 36-1: Sample CLC Configuration Code

```
ANSELBbits.ANSB15 = 0;    // configure pins used for CLC input as digital pins
ANSELBbits.ANSB14 = 0;
ANSELBbits.ANSB13 = 0;
ANSELBbits.ANSB12 = 0;

CLC1CONbits.G4POL= 0;     // CLC gate outputs non-inverting
CLC1CONbits.G3POL= 0;
CLC1CONbits.G2POL= 0;
CLC1CONbits.G1POL= 0;

CLC1SELbits.DS4 = 3;      // Data4 input is SDI1 pin
CLC1SELbits.DS3 = 4;      // Data3 input is U1RX pin
CLC1SELbits.DS2 = 0;      // Data2 input is CLC1B
CLC1SELbits.DS1 = 0;      // Data1 input CLC1A

CLC1GLS = 0x80200802;     // G4D4, G3D3, G2D2, G1D1 selected

CLC1CONbits.MODE = 2;     // AND operation

CLC1CONbits.LCPOL = 0;    // non-inverting output

CLC1CONbits.LCOE = 1;     // CLC output enabled
CLC1CONbits.ON = 1;       // enable CLC

RPINR12bits.CLCINBR = 13; // map CLCA input to RP11
RPINR12bits.CLCINAR = 12; // map CLCB input to RP12

RPOR4bits.RP18R = 8;      // map CLC output to RP17
```

Note: This example is for a PIC32MMXXXXGPL028 device. CLC inputs selection, analog select and PPS configurations may vary for different device families and packages.

36.4 INPUT PROVIDERS

Each logic cell in the CLC takes four inputs, one from each of the four data gates. Each data gate is connected to eight input sources. The data gate allows the selection between the inverted or non-inverted polarity of each input source. Input sources available for use with the CLC vary by device. Refer to the specific device data sheet for available options.

36.4.1 Source Multiplexers

The module has four input source multiplexers. Multiplexer inputs are selected by setting control bits in the CLCxSEL register to define the data source selected through each of four data selection multiplexers. Each of the four data selection multiplexers feeds one of the four logic function input gates, shown in Figure 36-2. The module has an internal data bus created from the output of each input source multiplexer, see Figure 36-3. The data bus has both True (T) and Negated (N) versions of each selected input source. Therefore, up to eight signals are available on the internal data bus to connect to the input gates of the logic function.

36.4.2 Logic Input Gates

Four logic input gates are used to route input sources from the data selection multiplexers into the four logic function inputs. The True and Negated forms of each input source signal are available for use by each logic gate. The input signal sources are enabled for use by each logic function input using the CLCxGLS register. There are up to eight signals that can be enabled for use by each logic function input. Any number of the eight signal sources may be enabled for each of the four logic function inputs. Each logic gate provides a logical OR of the input signals. The selected (True or Negated) signals are OR'd to form the gate output data. The logical NAND is obtained by changing the output polarity with the GxPOL bits. If the logical AND is required instead, select Negated inputs and invert the output polarity according to DeMorgan's theorem. If all inputs are Negated and applied to a NOR, the result is identical to an AND operation. Written algebraically:

C = A AND B, which is the same as C = NOT (NOT(A) OR NOT(B))

Table 36-2 summarizes the basic functions that can be obtained by using the gate control bits. The table shows the use of all four input multiplexer sources, but the input gates can be configured to use less. If no inputs are selected (CLCxGLS = 0), the output will be zero or one, depending on the GxPOL bits.

Table 36-2: Desired Logic Operation(1)

Operation	CLCxGLS	G1POL	G2POL	G3POL	G4POL	LCPOL	Mode	G1	G2	G3	G4
AND (D1, D2, D3, D4)	0x80200802	0	0	0	0	0	0x2	D1 &	D2 &	D3 &	D4
NAND (D1, D2, D3, D4)	0x80200802	0	0	0	0	1	0x2	!(D1 &	D2 &	D3 &	D4)
OR (D1, D2, D3, D4)	0xAA000000	1	1	1	0	0	0x2	1 &	1 &	1 &	(D4 | D3 | D2 | D1)
NOR (D1, D2, D3, D4)	0xAA000000	1	1	1	0	1	0x2	!(1 &	1 &	1 &	(D4 | D3 | D2 | D1))
XOR (D1, D4)	0x80000002	0	1	1	0	0	0x1	(D1 &	1) ^	(1 &	D4)
1	0x00000000	1	1	1	1	0	0x2	1 &	1 &	1 &	1
0	0x00000000	0	0	0	0	0	0x2	0 &	0 &	0 &	0

Note 1: Refer to Figure 36-3 for more information on gate outputs.

It is possible, but not recommended, to select both the True and Negated values of an input. When this is done, the gate output is one, regardless of the other inputs (1 = D OR NOT(D)), but may emit logic glitches (transient-induced pulses). If the output of a gate must be zero or one, the recommended method is to set all of the bits related to that gate in CLCxGLS to zero and use the Gate Polarity bit, GxPOL, to set the desired level.

36.4.3 Logic Function

The following eight logic functions are available as shown in Figure 36-2.

- AND-OR
- OR-XOR
- AND
- S-R Latch
- D Flip-Flop with Set and Reset
- D Flip-Flop with Reset
- J-K Flip-Flop with Reset
- Transparent Latch with Set and Reset

Each logic function has four inputs and one output. The four inputs are the four data gate outputs of the previous stage. The output is fed to the inversion stage, and from there to other peripherals an output pin, and then back to the CLC.

36.4.4 Software Inputs

The gate data input to the logic function can be directly controlled by software by setting all of the CLCxGLS bits associated with the logic gate to '0' and writing to the appropriate GxPOL bit, for additional information see Table 36-2. The gate output will be equal to the value of the GxPOL bit.

36.5 OUTPUT

LCOUT is the logic cell output and is routed to the I/O port pin or to other modules within the device. In all cases, the signal value is taken after the LCPOL inverter. To observe this output on an I/O pin, the user will need to set LCOE.

36.6 APPLICATION LOGIC

The CLC provides both combinatorial (see Figure 36-2) and state (see Figure 36-3) logic function options. The outputs of the input gates are applied to the logic function. If CLCxGLS = 0x00, the function receives a logic '0' when the GxPOL bits are clear or a logic '1' when the GxPOL bits are set.

36.6.1 Combinatorial Logic

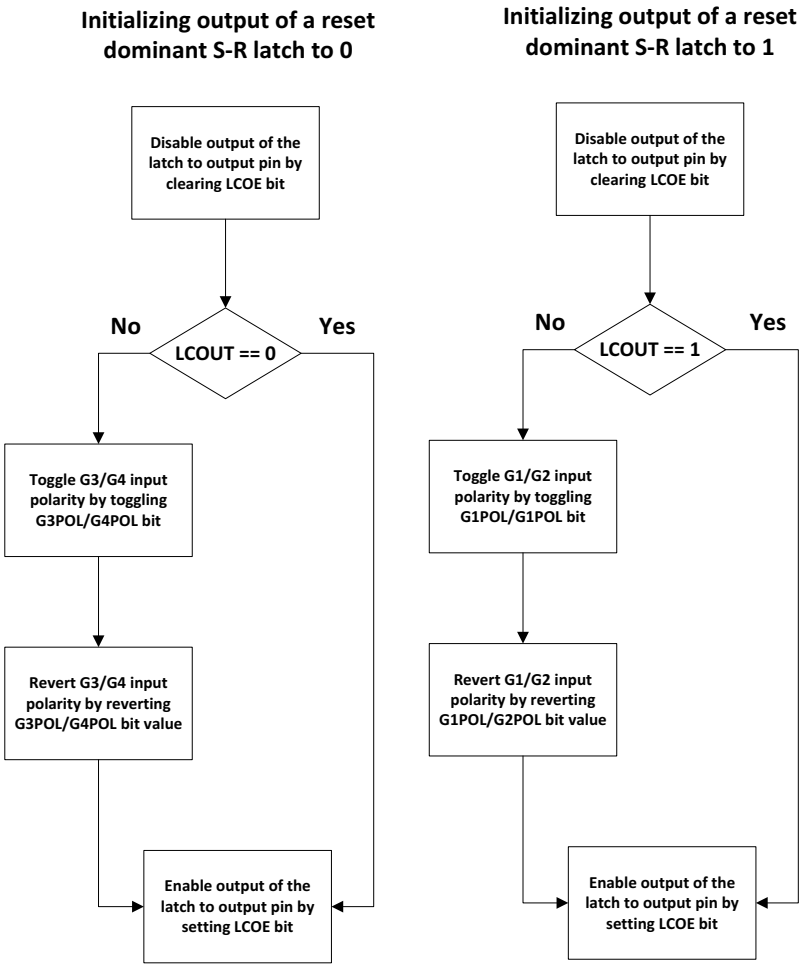
The combinatorial functions, shown in Figure 36-2, build on the AND/OR logic of the input gate. The 4-input AND can provide an OR function by inverting the inputs and outputs using DeMorgan's theorem. Inverting the output of the XOR is the same as inverting one input (but not both).

The SR function (MODE<2:0> = 011) is not affected when ON is cleared, as is the case with the state logic register. The latch is Reset-dominant, meaning that the Reset signal takes precedent over any Set (S) signal that may be present.

Because the S-R latch has its inputs coming from combinational logic, the default output of the S-R latch upon reset cannot be deterministic. The system reset does not affect this default state due to the nature of the design. If required, the S-R latch output can be initialized to a desired state, without changing the state of the inputs, by momentarily inverting the polarity of input OR gates to S/R input depending upon the desired output state. Refer to the following flowchart for the steps involved in initializing the output of reset dominant S-R latch logic cell.

Note: The following initialization procedure is effective only if the both S and R inputs are driven to 0 by the external signals connected to the input pins. In all other cases, the output of the latch is governed by the truth table of the reset dominant S-R latch.

Figure 36-4: Initialization Procedure



36.6.2 State Logic

The state functions of Figure 36-3 include both D and J-K flip-flops with asynchronous Set (S) and Reset (R). Input Gate 1 provides a rising edge clock. If a falling edge clock is required, Gate 1 can be inverted in the gate logic (G1POL). Input Gate 2, and sometimes also Gate 4, provide data to the register or latch input(s). When operating in Transparent Latch mode (MODE<2:0> = 111), the output, Q, follows D, while LE is high and holds state while LE is low.

The various modes may or may not share state memory and Switching modes may or may not change the state of the state variable. For all modes, the register is Reset-dominant.

36.7 CLC INTERRUPTS

The CLC module has two types of interrupts that can be enabled: rising edge interrupt events and falling edge interrupt events. These events are enabled by the INTP and INTN control bits, respectively.

A valid occurrence of either interrupt will set the CLC Interrupt Flag, CLCIF. This will occur when the module is enabled (ON = 1) and either a rising edge output occurs when INTP = 1, or a falling edge event occurs when INTN = 1.

If the initial output state of the CLC logic is '1' and INTP = 1, an interrupt will be generated when ON is set to '1'. Likewise, an interrupt will be generated if the initial output state of the CLC is '0' and INTN = 1. These conditions must be detected and cleared in software. Similarly, a false interrupt could be generated if INTP or INTN is set while the CLC module is enabled.

The user should be sure to clear any spurious interrupt events that may occur in the initialization process of the CLC module.

If the CLC Interrupt Enable bit, CLCIE, is cleared, an interrupt will not be generated. However, the CLCIF bit will still be set if an interrupt condition occurs. The user can clear the interrupt in the Interrupt Service Routine (ISR) by clearing the CLCIF bit. For additional information, refer to the PIC32 Family Reference Manual "***Section 8. Interrupts"*** (DS60001108).

36.8 OPERATION IN SLEEP MODE

The CLC module is not affected by Sleep mode, since it does not rely on system clock sources for operation. However, some input sources might be disabled during Sleep, so the function could be disrupted. If the source continues to operate, so will the module. Refer to the specific device data sheet for more information.

36.9 OPERATION IN IDLE MODE

The CLC module is not affected by Idle mode, because it does not rely on system clock sources for operation. However, some input sources might be disabled during Idle and the function could be disrupted. If the sources continue to operate, so will the module. Refer to the specific device data sheet for more information.

36.10 RESET

When the ON bit is written to '0', the output of all state logic functions will be reset to '0'. A system Reset returns the CLCxCON, CLCxSEL and CLCxGLS registers to the default state and disables the module.

Asserting a device Reset returns all bits in the module registers to the default state. The output of all logic functions is '0' after a Reset; this includes both latch and flip-flop functions. When a device Reset is asserted (ON = 0), the state logic is reset and the output of the logic function is forced low.

36.11 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC32 device families, but the concepts are pertinent and could be used with modification and possible limitations.

The current application notes related to the Configurable Logic Cell module are:

Title	Application Note #
No related application notes at this time.	

36.12 REVISION HISTORY

Revision A (August 2015)

This is the initial revision of this document.

Revision B (August 2019)

Added the Initialization Sequence for the S-R Latch in 36.6.1 Combinatorial Logic.

Note the following details of the code protection feature on Microchip devices:

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