ESP32 Series

Datasheet

2.4 GHz Wi-Fi + Bluetooth® + Bluetooth LE SoC

Including:

- ESP32-D0WD-V3
- ESP32-D0WDR2-V3
- ESP32-U4WDH
- ESP32-S0WD – Not Recommended for New Designs (NRND)
- ESP32-D0WD – Not Recommended for New Designs (NRND)
- ESP32-D0WDQ6 – Not Recommended for New Designs (NRND)
- ESP32-D0WDQ6-V3 – Not Recommended for New Designs (NRND)

Version 4.5
Espressif Systems

Product Overview

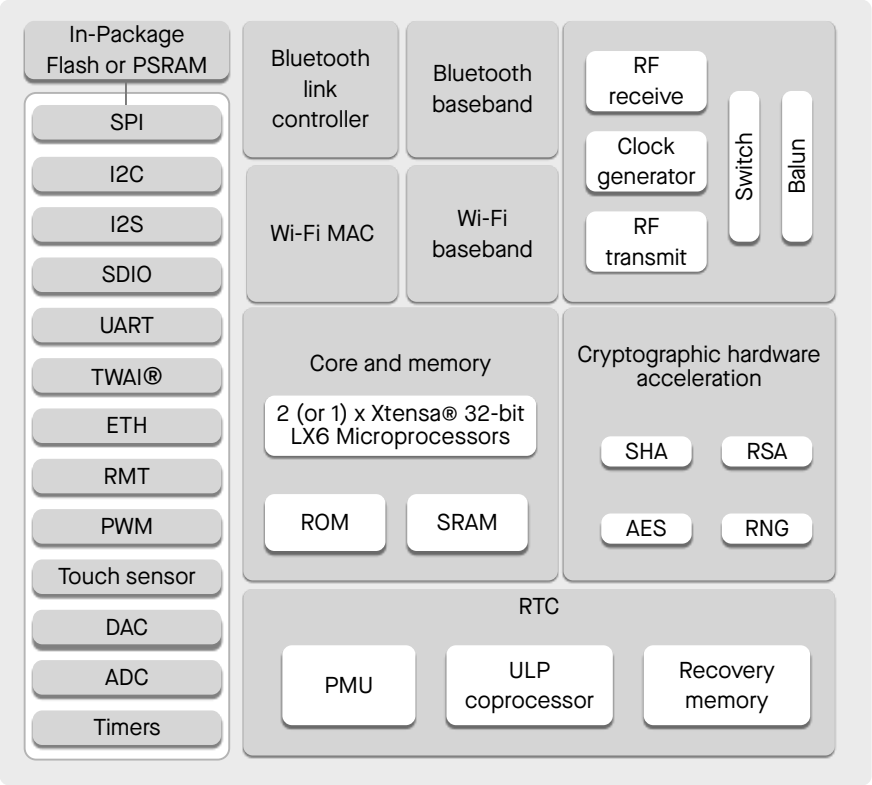
ESP32 is a single 2.4 GHz Wi-Fi-and-Bluetooth combo chip designed with the TSMC low-power 40 nm technology. It is designed to achieve the best power and RF performance, showing robustness, versatility and reliability in a wide variety of applications and power scenarios.

The ESP32 series of chips includes ESP32-D0WD-V3, ESP32-D0WDR2-V3, ESP32-U4WDH, ESP32-S0WD (NRND), ESP32-D0WDQ6-V3 (NRND), ESP32-D0WD (NRND), and ESP32-D0WDQ6 (NRND), among which,

- ESP32-S0WD (NRND), ESP32-D0WD (NRND), and ESP32-D0WDQ6 (NRND) are based on chip revision v1 or chip revision v1.1.
- ESP32-D0WD-V3, ESP32-D0WDR2-V3, ESP32-U4WDH, and ESP32-D0WDQ6-V3 (NRND) are based on chip revision v3.0 or chip revision v3.1.

For details on part numbers and ordering information, please refer to Section 1 ESP32 Series Comparison. For details on chip revisions, please refer to *ESP32 Chip Revision v3.0 User Guide* and *ESP32 Series SoC Errata*.

The functional block diagram of the SoC is shown below.



ESP32 Functional Block Diagram

Features

Wi-Fi

- 802.11b/g/n
- 802.11n (2.4 GHz), up to 150 Mbps
- WMM
- TX/RX A-MPDU, RX A-MSDU
- Immediate Block ACK
- Defragmentation
- Automatic Beacon monitoring (hardware TSF)
- 4 × virtual Wi-Fi interfaces
- Simultaneous support for Infrastructure Station, SoftAP, and Promiscuous modes
  Note that when ESP32 is in Station mode, performing a scan, the SoftAP channel will be changed.
- Antenna diversity

Bluetooth®

- Compliant with Bluetooth v4.2 BR/EDR and Bluetooth LE specifications
- Class-1, class-2 and class-3 transmitter without external power amplifier
- Enhanced Power Control
- +9 dBm transmitting power
- NZIF receiver with –94 dBm Bluetooth LE sensitivity
- Adaptive Frequency Hopping (AFH)
- Standard HCI based on SDIO/SPI/UART
- High-speed UART HCI, up to 4 Mbps
- Bluetooth 4.2 BR/EDR and Bluetooth LE dual mode controller
- Synchronous Connection-Oriented/Extended (SCO/eSCO)
- CVSD and SBC for audio codec
- Bluetooth Piconet and Scatternet
- Multi-connections in Classic Bluetooth and Bluetooth LE
- Simultaneous advertising and scanning

CPU and Memory

- Xtensa® single-/dual-core 32-bit LX6 microprocessor(s)
- CoreMark® score:
  - 1 core at 240 MHz: 504.85 CoreMark; 2.10 CoreMark/MHz

  - 2 cores at 240 MHz: 994.26 CoreMark; 4.14 CoreMark/MHz
- 448 KB ROM
- 520 KB SRAM
- 16 KB SRAM in RTC
- QSPI supports multiple flash/SRAM chips

Clocks and Timers

- Internal 8 MHz oscillator with calibration
- Internal RC oscillator with calibration
- External 2 MHz ~ 60 MHz crystal oscillator (40 MHz only for Wi-Fi/Bluetooth functionality)
- External 32 kHz crystal oscillator for RTC with calibration
- Two timer groups, including 2 × 64-bit timers and 1 × main watchdog in each group
- One RTC timer
- RTC watchdog

Advanced Peripheral Interfaces

- 34 × programmable GPIOs
  - 5 strapping GPIOs
  - 6 input-only GPIOs
  - 6 GPIOs needed for in-package flash/PSRAM (ESP32-D0WDR2-V3, ESP32-U4WDH)
- 12-bit SAR ADC up to 18 channels
- 2 × 8-bit DAC
- 10 × touch sensors
- 4 × SPI
- 2 × I2S
- 2 × I2C
- 3 × UART
- 1 host (SD/eMMC/SDIO)
- 1 slave (SDIO/SPI)
- Ethernet MAC interface with dedicated DMA and IEEE 1588 support
- TWAI®, compatible with ISO 11898-1 (CAN Specification 2.0)
- RMT (TX/RX)
- Motor PWM
- LED PWM up to 16 channels

Power Management

- Fine-resolution power control through a selection of clock frequency, duty cycle, Wi-Fi operating modes, and individual power control of internal components
- Five power modes designed for typical scenarios: Active, Modem-sleep, Light-sleep, Deep-sleep, Hibernation
- Power consumption in Deep-sleep mode is 10 μA
- Ultra-Low-Power (ULP) coprocessors
- RTC memory remains powered on in Deep-sleep mode

Security

- Secure boot
- Flash encryption
- 1024-bit OTP, up to 768-bit for customers
- Cryptographic hardware acceleration:
  - AES
  - Hash (SHA-2)
  - RSA
  - ECC
  - Random Number Generator (RNG)

Applications

With low power consumption, ESP32 is an ideal choice for IoT devices in the following areas:

- Smart Home
- Industrial Automation
- Health Care
- Consumer Electronics
- Smart Agriculture
- POS machines
- Service robot
- Audio Devices
- Generic Low-power IoT Sensor Hubs
- Generic Low-power IoT Data Loggers
- Cameras for Video Streaming
- Speech Recognition
- Image Recognition
- SDIO Wi-Fi + Bluetooth Networking Card
- Touch and Proximity Sensing

1 ESP32 Series Comparison

1.1 Nomenclature

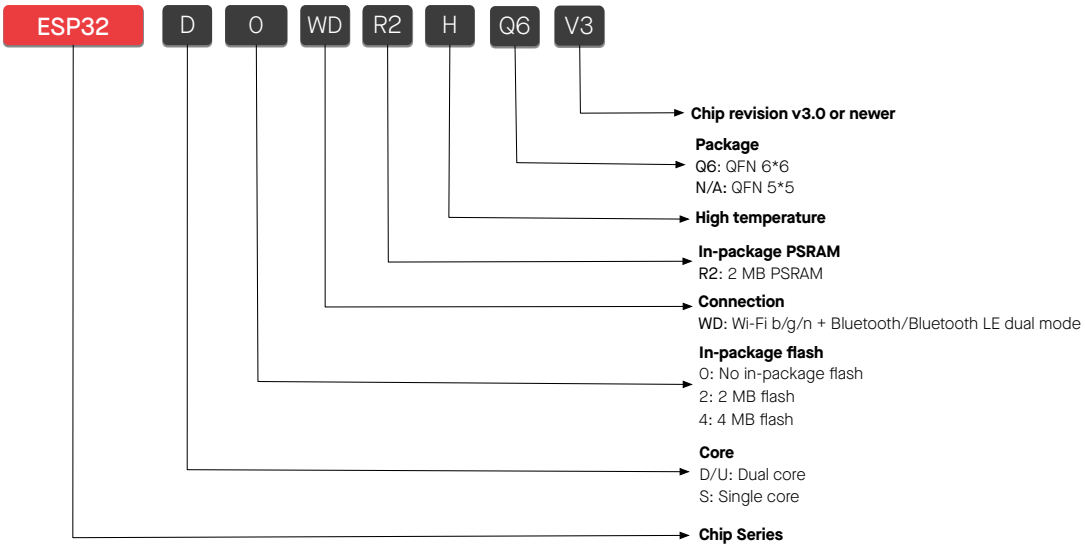


Figure 1-1. ESP32 Series Nomenclature

1.2 Comparison

Table 1-1. ESP32 Series Comparison

Ordering code[1]	Core	Chip Revision[2]	In-Package Flash/PSRAM	Package	VDD_SDIO Voltage
ESP32-D0WD-V3	Dual core	v3.0/v3.1[4]	—	QFN 5*5	1.8 V/3.3 V
ESP32-D0WDR2-V3	Dual core	v3.0/v3.1[4]	2 MB PSRAM	QFN 5*5	3.3 V
ESP32-U4WDH	Dual core[3]	v3.0/v3.1[4]	4 MB flash[6]	QFN 5*5	3.3 V
ESP32-D0WDQ6-V3 (NRND)	Dual core	v3.0/v3.1[4]	—	QFN 6*6	1.8 V/3.3 V
ESP32-D0WD (NRND)	Dual core	v1.0/v1.1[5]	—	QFN 5*5	1.8 V/3.3 V
ESP32-D0WDQ6 (NRND)	Dual core	v1.0/v1.1[5]	—	QFN 6*6	1.8 V/3.3 V
ESP32-S0WD (NRND)	Single core	v1.0/v1.1[5]	—	QFN 5*5	1.8 V/3.3 V

[1] All above chips support Wi-Fi b/g/n + Bluetooth/Bluetooth LE Dual Mode connection. For details on chip marking and packing, see Section 5 Packaging.

[2] Differences between ESP32 chip revisions and how to distinguish them are described in *ESP32 Series SoC Errata*.

[3] ESP32-U4WDH will be produced as dual-core instead of single core. See PCN-2021-021 for more details.

[4] The chips will be produced with chip revision v3.1 inside. See PCN20220901 for more details.

[5] The chips will be produced with chip revision v1.1 inside. See PCN20220901 for more details.

[6] The in-package flash supports:
- More than 100,000 program/erase cycles
- More than 20 years data retention time

2 Pins

2.1 Pin Layout

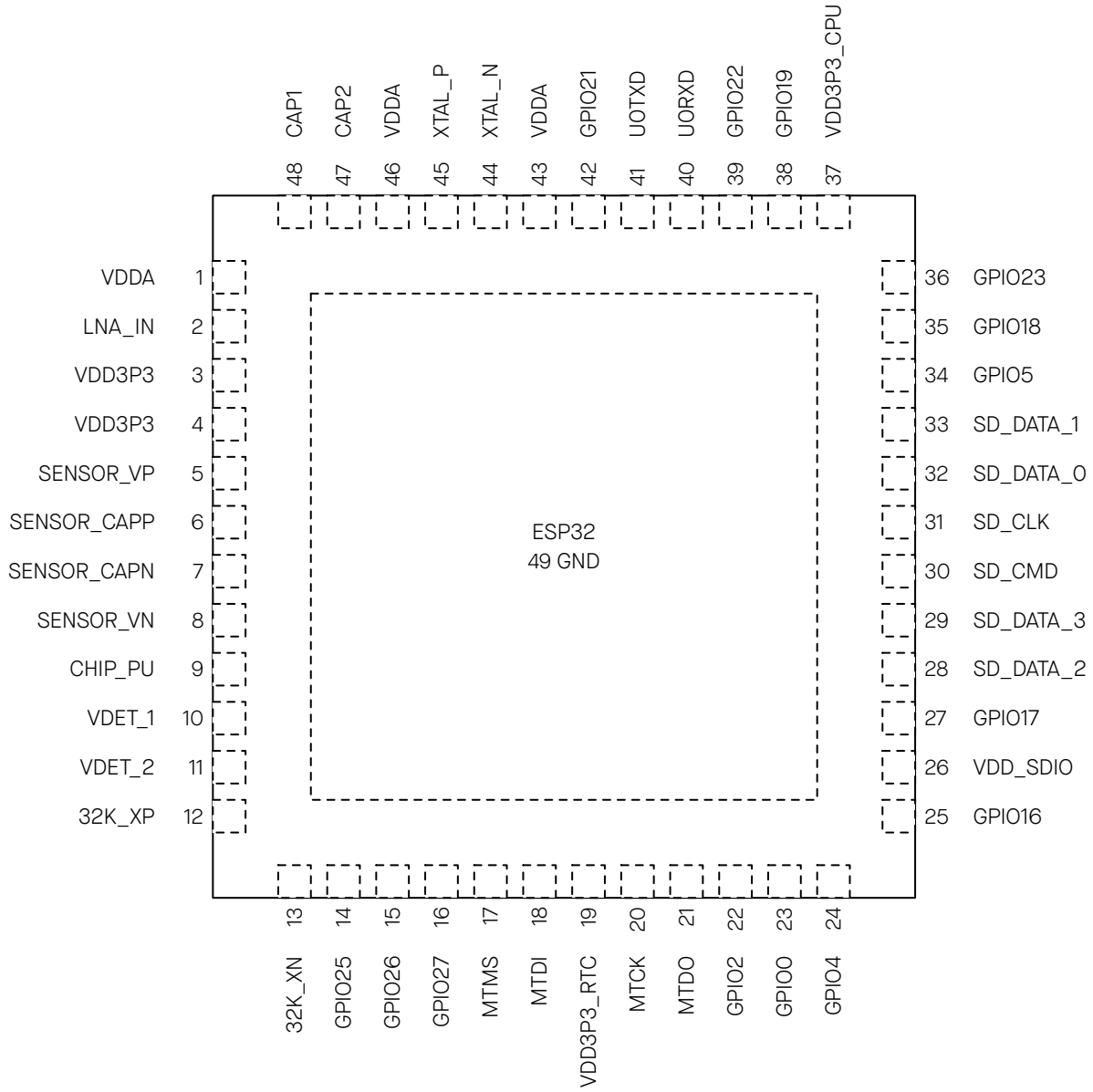


Figure 2-1. ESP32 Pin Layout (QFN 6*6, Top View)

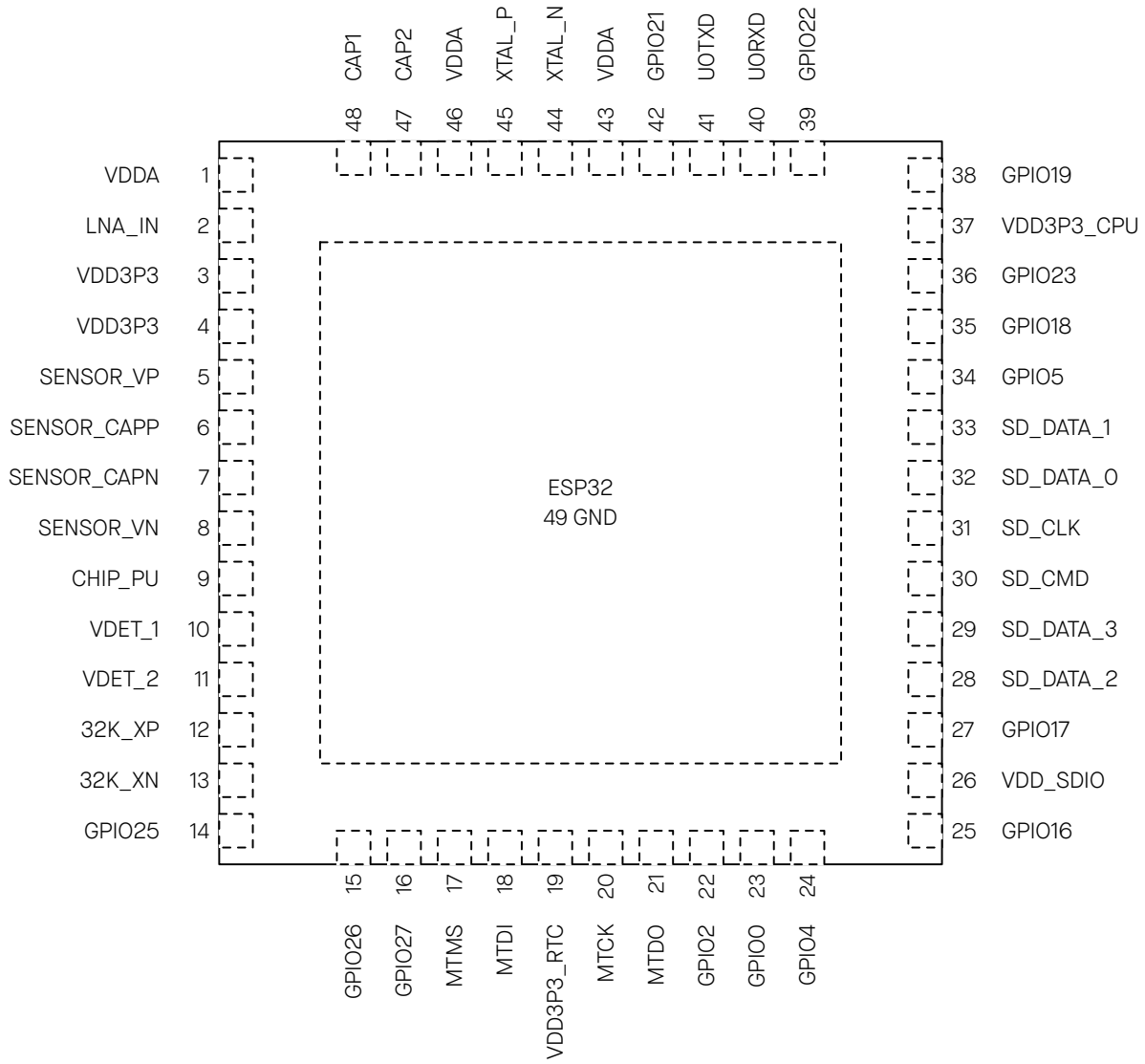


Figure 2-2. ESP32 Pin Layout (QFN 5*5, Top View)

2.2 Pin Overview

Table 2-1. Pin Overview

Name	No.	Type	Function
Analog			
VDDA	1	P	Analog power supply (2.3 V ~ 3.6 V)
LNA_IN	2	I/O	RF input and output
VDD3P3	3	P	Analog power supply (2.3 V ~ 3.6 V)
VDD3P3	4	P	Analog power supply (2.3 V ~ 3.6 V)
VDD3P3_RTC			
SENSOR_VP	5	I	GPIO36, ADC1_CH0, RTC_GPIO0
SENSOR_CAPP	6	I	GPIO37, ADC1_CH1, RTC_GPIO1
SENSOR_CAPN	7	I	GPIO38, ADC1_CH2, RTC_GPIO2
SENSOR_VN	8	I	GPIO39, ADC1_CH3, RTC_GPIO3
CHIP_PU	9	I	High: On; enables the chip Low: Off; the chip shuts down Note: Do not leave the CHIP_PU pin floating.
VDET_1	10	I	GPIO34, ADC1_CH6, RTC_GPIO4
VDET_2	11	I	GPIO35, ADC1_CH7, RTC_GPIO5
32K_XP	12	I/O	GPIO32, ADC1_CH4, RTC_GPIO9, TOUCH9, 32K_XP (32.768 kHz crystal oscillator input)
32K_XN	13	I/O	GPIO33, ADC1_CH5, RTC_GPIO8, TOUCH8, 32K_XN (32.768 kHz crystal oscillator output)
GPIO25	14	I/O	GPIO25, ADC2_CH8, RTC_GPIO6, DAC_1, EMAC_RXD0
GPIO26	15	I/O	GPIO26, ADC2_CH9, RTC_GPIO7, DAC_2, EMAC_RXD1
GPIO27	16	I/O	GPIO27, ADC2_CH7, RTC_GPIO17, TOUCH7, EMAC_RX_DV
MTMS	17	I/O	GPIO14, ADC2_CH6, RTC_GPIO16, TOUCH6, EMAC_TXD2, HSPICLK, HS2_CLK, SD_CLK, MTMS
MTDI	18	I/O	GPIO12, ADC2_CH5, RTC_GPIO15, TOUCH5, EMAC_TXD3, HSPIQ, HS2_DATA2, SD_DATA2, MTDI
VDD3P3_RTC	19	P	Input power supply for RTC IO (2.3 V ~ 3.6 V)
MTCK	20	I/O	GPIO13, ADC2_CH4, RTC_GPIO14, TOUCH4, EMAC_RX_ER, HSPID, HS2_DATA3, SD_DATA3, MTCK
MTDO	21	I/O	GPIO15, ADC2_CH3, RTC_GPIO13, TOUCH3, EMAC_RXD3, HSPICS0, HS2_CMD, SD_CMD, MTDO

Name	No.	Type	Function							
GPIO2	22	I/O	GPIO2,	ADC2_CH2,	RTC_GPIO12,	TOUCH2,		HSPIWP,	HS2_DATA0,	SD_DATA0
GPIO0	23	I/O	GPIO0,	ADC2_CH1,	RTC_GPIO11,	TOUCH1,	EMAC_TX_CLK,	CLK_OUT1,		
GPIO4	24	I/O	GPIO4,	ADC2_CH0,	RTC_GPIO10,	TOUCH0,	EMAC_TX_ER,	HSPIHD,	HS2_DATA1,	SD_DATA1
VDD_SDIO										
GPIO16	25	I/O	GPIO16,	HS1_DATA4,	U2RXD,	EMAC_CLK_OUT				
VDD_SDIO	26	P	Output power supply: 1.8 V or the same voltage as VDD3P3_RTC							
GPIO17	27	I/O	GPIO17,	HS1_DATA5,	U2TXD,	EMAC_CLK_OUT_180				
SD_DATA_2	28	I/O	GPIO9,	HS1_DATA2,	U1RXD,	SD_DATA2,	SPIHD			
SD_DATA_3	29	I/O	GPIO10,	HS1_DATA3,	U1TXD,	SD_DATA3,	SPIWP			
SD_CMD	30	I/O	GPIO11,	HS1_CMD,	U1RTS,	SD_CMD,	SPICS0			
SD_CLK	31	I/O	GPIO6,	HS1_CLK,	U1CTS,	SD_CLK,	SPICLK			
SD_DATA_0	32	I/O	GPIO7,	HS1_DATA0,	U2RTS,	SD_DATA0,	SPIQ			
SD_DATA_1	33	I/O	GPIO8,	HS1_DATA1,	U2CTS,	SD_DATA1,	SPID			
VDD3P3_CPU										
GPIO5	34	I/O	GPIO5,	HS1_DATA6,	VSPICS0,	EMAC_RX_CLK				
GPIO18	35	I/O	GPIO18,	HS1_DATA7,	VSPICLK					
GPIO23	36	I/O	GPIO23,	HS1_STROBE,	VSPID					
VDD3P3_CPU	37	P	Input power supply for CPU IO (1.8 V ~ 3.6 V)							
GPIO19	38	I/O	GPIO19,	U0CTS,	VSPIQ,	EMAC_TXD0				
GPIO22	39	I/O	GPIO22,	U0RTS,	VSPIWP,	EMAC_TXD1				
U0RXD	40	I/O	GPIO3,	U0RXD,	CLK_OUT2					
U0TXD	41	I/O	GPIO1,	U0TXD,	CLK_OUT3,	EMAC_RXD2				
GPIO21	42	I/O	GPIO21,		VSPIHD,	EMAC_TX_EN				
Analog										
VDDA	43	P	Analog power supply (2.3 V ~ 3.6 V)							
XTAL_N	44	O	External crystal output							
XTAL_P	45	I	External crystal input							
VDDA	46	P	Analog power supply (2.3 V ~ 3.6 V)							
CAP2	47	I	Connects to a 3.3 nF (10%) capacitor and 20 kΩ resistor in parallel to CAP1							

Name	No.	Type	Function
CAP1	48	I	Connects to a 10 nF series capacitor to ground
GND	49	P	Ground

Regarding highlighted cells, see Section 2.2.1 Restrictions for GPIOs and RTC_GPIOs.

For a quick reference guide to using the IO_MUX, Ethernet MAC, and GPIO Matrix pins of ESP32, please refer to Appendix ESP32 Pin Lists.

2.5 Pin Mapping Between Chip and Flash/PSRAM

Table 2-5 lists the pin-to-pin mapping between the chip and the in-package flash/PSRAM. The chip pins listed here are not recommended for other usage.

For the data port connection between ESP32 and off-package flash/PSRAM please refer to Table 2-6.

Table 2-5. Pin-to-Pin Mapping Between Chip and In-Package Flash/PSRAM

ESP32-U4WDH	In-Package Flash (4 MB)
SD_DATA_1	IO0/DI
GPIO17	IO1/DO
SD_DATA_0	IO2/WP#
SD_CMD	IO3/HOLD#
SD_CLK	CLK
GPIO16	CS#
GND	VSS
VDD_SDIO[1]	VDD
ESP32-D0WDR2-V3	**In-Package PSRAM (2 MB)**
SD_DATA_1	SIO0/SI
SD_DATA_0	SIO1/SO
SD_DATA_3	SIO2
SD_DATA_2	SIO3
SD_CLK	SCLK
GPIO16[2]	CE#
GND	VSS
VDD_SDIO[1]	VDD

Table 2-6. Pin-to-Pin Mapping Between Chip and Off-Package Flash/PSRAM

Chip Pin	Off-Package Flash
SD_DATA_1/SPID	IO0/DI
SD_DATA_0/SPIQ	IO1/DO
SD_DATA_3/SPIWP	IO2/WP#
SD_DATA_2/SPIHD	IO3/HOLD#
SD_CLK	CLK
SD_CMD	CS#
GND	VSS
VDD_SDIO	VDD
Chip Pin	**Off-Package PSRAM**
SD_DATA_1	SIO0/SI
SD_DATA_0	SIO1/SO
SD_DATA_3	SIO2
SD_DATA_2	SIO3
SD_CLK/GPIO17[3]	SCLK

Cont'd on next page

Table 2-6 – cont'd from previous page

Chip Pin	Off-Package PSRAM
GPIO16[2]	CE#
GND	VSS
VDD_SDIO	VDD

Note:

1. As the in-package flash/PSRAM in ESP32-U4WDH/ESP32-D0WDR2-V3 operates at 3.3 V, VDD_SDIO must be powered by VDD3P3_RTC via a 6 Ω resistor. See Figure 2-3 ESP32 Power Scheme.
2. If GPIO16 is used to connect to PSRAM's CE# signal, please add a pull-up resistor at the GPIO16 pin. See *ESP32-WROVER-E Datasheet* > Figure *Schematics of ESP32-WROVER-E*.
3. SD_CLK and GPIO17 pins are available to connect to the SCLK signal of external PSRAM.
   - If SD_CLK pin is selected, one GPIO (i.e., GPIO17) will be saved. The saved GPIO can be used for other purposes. This connection has passed internal tests, but relevant certification has not been completed.
   - Or GPIO17 pin is used to connect to the SCLK signal. This connection has passed relevant certification, see certificates for ESP32-WROVER-E.

   Please select the proper pin for your specific applications.

3.3 RTC and Low-power Management

3.3.1 Power Management Unit (PMU)

With the use of advanced power-management technologies, ESP32 can switch between different power modes.

- Power modes
  - **Active mode**: The chip radio is powered up. The chip can receive, transmit, or listen.
  - **Modem-sleep mode**: The CPU is operational and the clock is configurable. The Wi-Fi/Bluetooth baseband and radio are disabled.
  - **Light-sleep mode**: The CPU is paused. The RTC memory and RTC peripherals, as well as the ULP coprocessor are running. Any wake-up events (MAC, SDIO host, RTC timer, or external interrupts) will wake up the chip.
  - **Deep-sleep mode**: Only the RTC memory and RTC peripherals are powered up. Wi-Fi and Bluetooth connection data are stored in the RTC memory. The ULP coprocessor is functional.
  - **Hibernation mode**: The internal 8 MHz oscillator and ULP coprocessor are disabled. The RTC recovery memory is powered down. Only one RTC timer on the slow clock and certain RTC GPIOs are active. The RTC timer or the RTC GPIOs can wake up the chip from the Hibernation mode.

Table 3-2. Power Consumption by Power Modes

Power mode	Description			Power Consumption
Active (RF working)	Wi-Fi Tx packet			Please refer to Table 4-4 for details.
	Wi-Fi/BT Tx packet			
	Wi-Fi/BT Rx and listening			
Modem-sleep	The CPU is powered up.	240 MHz *	Dual-core chip(s)	30 mA ~ 68 mA
			Single-core chip(s)	N/A
		160 MHz *	Dual-core chip(s)	27 mA ~ 44 mA
			Single-core chip(s)	27 mA ~ 34 mA
		Normal speed: 80 MHz	Dual-core chip(s)	20 mA ~ 31 mA
			Single-core chip(s)	20 mA ~ 25 mA
Light-sleep	-			0.8 mA
Deep-sleep	The ULP coprocessor is powered up.			150 μA
	ULP sensor-monitored pattern			100 μA @1% duty
	RTC timer + RTC memory			10 μA
Hibernation	RTC timer only			5 μA
Power off	CHIP_PU is set to low level, the chip is powered down.			1 μA

- * Among the ESP32 series of SoCs, ESP32-D0WD-V3, ESP32-D0WDR2-V3, ESP32-U4WDH, ESP32-D0WD (NRND), ESP32-D0WDQ6 (NRND), and ESP32-D0WDQ6-V3 (NRND) have a maximum CPU frequency of 240 MHz, ESP32-S0WD (NRND) has a maximum CPU frequency of 160 MHz.
- When Wi-Fi is enabled, the chip switches between Active and Modem-sleep modes. Therefore, power consumption changes accordingly.
- In Modem-sleep mode, the CPU frequency changes automatically. The frequency depends on the CPU load and the peripherals used.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Stresses above those listed in Table 4-1 *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and normal operation of the device at these or any other conditions beyond those indicated in Section 4.2 Recommended Power Supply Characteristics is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 4-1. Absolute Maximum Ratings

Parameter	Description	Min	Max	Unit
VDDA, VDD3P3, VDD3P3_RTC, VDD3P3_CPU, VDD_SDIO	Allowed input voltage	–0.3	3.6	V
I_{output} [1]	Cumulative IO output current	—	1200	mA
T_{STORE}	Storage temperature	–40	150	°C

[1] The product proved to be fully functional after all its IO pins were pulled high while being connected to ground for 24 consecutive hours at ambient temperature of 25 °C.

4.2 Recommended Power Supply Characteristics

Table 4-2. Recommended Power Supply Characteristics

Parameter	Description	Min	Typ	Max	Unit
VDDA, VDD3P3_RTC *note 1* , VDD3P3, VDD_SDIO (3.3 V mode) *note 2*	Voltage applied to power supply pins per power domain	2.3/3.0 *note 3*	3.3	3.6	V
VDD3P3_CPU	Voltage applied to power supply pin	1.8	3.3	3.6	V
I_{VDD}	Current delivered by external power supply	0.5	—	—	A
T *note 4*	Operating temperature	–40	—	125	°C

1. When writing eFuse, VDD3P3_RTC should be at least 3.3 V.
2. - VDD_SDIO works as the power supply for the related IO, and also for an external device. Please refer to the Appendix IO_MUX of this datasheet for more details.
   - VDD_SDIO can be sourced internally by the ESP32 from the VDD3P3_RTC power domain:
     - When VDD_SDIO operates at 3.3 V, it is driven directly by VDD3P3_RTC through a 6 Ω resistor, therefore, there will be some voltage drop from VDD3P3_RTC.
     - When VDD_SDIO operates at 1.8 V, it can be generated from ESP32' s internal LDO. The maximum current this LDO can offer is 40 mA, and the output voltage range is 1.65 V ~ 2.0 V.
   - VDD_SDIO can also be driven by an external power supply.
   - Please refer to Section 2.3.1 Power Scheme, for more information.
3. - Chips with a 3.3 V flash or PSRAM in-package: this minimum voltage is 3.0 V;
   - Chips with no flash or PSRAM in-package: this minimum voltage is 2.3 V;
   - For more information, see Section 1 ESP32 Series Comparison.
4. - The operating temperature of ESP32-U4WDH ranges from –40 °C to 105 °C, due to the in-package flash.
   - The operating temperature of ESP32-D0WDR2-V3 ranges from –40 °C to 85 °C, due to the in-package PSRAM.
   - For other chips that have no in-package flash or PSRAM, their operating temperature is –40 °C ~ 125 °C.

4.3 DC Characteristics (3.3 V, 25 °C)

Table 4-3. DC Characteristics (3.3 V, 25 °C)

Parameter	Description		Min	Typ	Max	Unit
C_{IN}	Pin capacitance		—	2	—	pF
V_{IH}	High-level input voltage		0.75×VDD[1]	—	VDD[1]+0.3	V
V_{IL}	Low-level input voltage		–0.3	—	0.25×VDD[1]	V
I_{IH}	High-level input current		—	—	50	nA
I_{IL}	Low-level input current		—	—	50	nA
V_{OH}	High-level output voltage		0.8×VDD[1]	—	—	V
V_{OL}	Low-level output voltage		—	—	0.1×VDD[1]	V
I_{OH}	High-level source current (VDD[1] = 3.3 V, V_{OH} >= 2.64 V, output drive strength set to the maximum)	VDD3P3_CPU power domain [1, 2]	—	40	—	mA
		VDD3P3_RTC power domain [1, 2]	—	40	—	mA
		VDD_SDIO power domain [1, 3]	—	20	—	mA
I_{OL}	Low-level sink current (VDD[1] = 3.3 V, V_{OL} = 0.495 V, output drive strength set to the maximum)		—	28	—	mA
R_{PU}	Resistance of internal pull-up resistor		—	45	—	kΩ
R_{PD}	Resistance of internal pull-down resistor		—	45	—	kΩ
V_{IL_nRST}	Low-level input voltage of CHIP_PU to shut down the chip		—	—	0.6	V

1. Please see Table IO_MUX for IO's power domain. VDD is the I/O voltage for a particular power domain of pins.
2. For VDD3P3_CPU and VDD3P3_RTC power domain, per-pin current sourced in the same domain is gradually reduced from around 40 mA to around 29 mA, V_{OH}>=2.64 V, as the number of current-source pins increases.
3. For VDD_SDIO power domain, per-pin current sourced in the same domain is gradually reduced from around 30 mA to around 10 mA, V_{OH}>=2.64 V, as the number of current-source pins increases.

4.4 RF Current Consumption in Active Mode

The current consumption measurements are taken with a 3.3 V supply at 25 °C of ambient temperature at the RF port. All transmitters' measurements are based on a 50% duty cycle.

Table 4-4. Current Consumption Depending on RF Modes

Work Mode	Min	Typ	Max	Unit
Transmit 802.11b, DSSS 1 Mbps, POUT = +19.5 dBm	—	240	—	mA
Transmit 802.11g, OFDM 54 Mbps, POUT = +16 dBm	—	190	—	mA
Transmit 802.11n, OFDM MCS7, POUT = +14 dBm	—	180	—	mA
Receive 802.11b/g/n	—	95 ~ 100	—	mA
Transmit BT/BLE, POUT = 0 dBm	—	130	—	mA
Receive BT/BLE	—	95 ~ 100	—	mA

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