

COMPUTER ARCHITECTURE WITH RISC-V: THE IMAGINATION UNIVERSITY PROGRAMME

Robert Owen - Director: Worldwide University Programme

Building a global community

Telecom ParisTech
Connected MCU
Workshop
Feb. 2017



BUPT: Beijing
University of Posts &
Telecommunications
MIPSfpga Workshop,
Beijing, April 2016



Xuetang X MOOC
Beijing, 2017

First Course Online: Nov. 2020 !



UK: Elektra Award 2015



London 2021: January 6th
Introduction to Mobile Graphics
Workshop

University Programme: Mission & Objectives

Mission:

"TO CREATE AN INSTINCTIVE PREFERENCE AMONGST THE NEXT GENERATION OF CHIP DESIGNERS AND PROGRAMMERS TO DESIGN-IN AND USE OUR TECHNOLOGIES"

Objectives:

1. **Loyalty** – create awareness of, and instinctive preference for, our technologies
2. **Research** – augment, inspire, and enrich our R&D
3. **Talent** – attract excellent people worldwide

The importance of “doing”

Xunzi, an apprentice of Confucius

- 《儒孝篇》中的名句“不闻不若闻之，闻之不若见之，见之不若知之，知之不若行之” - 《荀子·修身》
- *I hear, but I forget*
I see, and I remember
I do, and I understand

Teaching Projects:

- **Enable Educators to use our technologies in teaching and student projects**

1. An Introduction to Mobile Graphics v2.0

- PowerVR based
- 2020 Edition (v2.0) released 30th March (En), May (Cn)

2. Artificial Intelligence at the Edge

- GPU based
- Platform agreed
- Partners chosen, platform confirmed, development started
- Announce Q1'21, launch Q2'21

3. Understanding Computer Architecture

- RISC-V based
- Supporters engaged
- Development well underway
- Announced Sept.'20, launch Nov'20

Special Projects:

- How to design an SoC around RISC-V
- Launch March '21
- Hobbyist Self-Study: *"Fun with the BeagleBoneBlack GPU"*
- Launch Dec. '20
- Developers Guide to RISC-V
- Joint Digi-Key+Imagination project
- Launch Nov.'20
- Online Learning: Xuetang X MOOC "Intro Mobile Graphics"
- Launch Nov.'20
- Chinese Textbook: Graphics with PowerVR
- Architecture, Tools & Applications
- Looking for an Author...
- Global Workshop Series, Conferences/Events....TBC

A Winning Lab Package

The four key elements of a successful teaching lab:

Hardware	Software
<ul style="list-style-type: none"> • Low cost: ~\$200 max. • Fully Featured: interfaces, memory, display(s) • Proven, credible silicon • Robust • Debuggable 	<ul style="list-style-type: none"> • Effective: 'SDK' package, with full de-bug • Free for academic use • No code size limits, no time limits! • Student versions for at home/"pocket lab" use • Online User Licence & distribution
Support	Teaching Materials
<ul style="list-style-type: none"> • Responsive, active, useful... • Forums / Communities • E-mail: IUP@imgtec.com 	<ul style="list-style-type: none"> • Written by academics for academics <ul style="list-style-type: none"> - not in-house training or marketing materials! • Up to 1 semester duration (~12 modules) • Slides and lecture notes <ul style="list-style-type: none"> - Student manual and exercises - Tests and solutions - Online video tutorials • "Train the Teacher" Workshops • Languages: English, Chinese (Simplified & Traditional), Japanese, Korean

An Introduction to Mobile Graphics 2020 Edition

- Objectives: understanding graphics, constraints of mobile, and effective use of PVR SDK tools

Introduction to Mobile Graphics 2020 Edition (v2.0)

Author	Darren McKie, University of Hull, UK
Guidance Panel	Darren McKie, Dr. Iain Hunter, Prof. Paul Chapman, Gerry Raptis, Jackie Qin, RCWO
Languages	English & Chinese (Simplified. Trad. to follow)
Timing	Launched 31 st March 2020 (En), May'20 (Cn) Access now: www.imgtec.com/university
Software	PowerVR SDK (full-features & free download)
Platforms	Software Simulator (PC/MAC), Acer Chromebook (\$450), BeagleBone Black (\$60)
Support	PowerVR Developer Forum here
Online version	Hosted by Xuetang X. Presented by Dr. Yang, PKU. Launch Nov.'20
Workshop(s)	London 6 th Jan. 2021 (+videos online)

Lecture Topic	Week	Details
Introduction to mobile graphics technologies	1	Introduction to the different graphics APIs available and how they compare.
Basics of the PowerVR Framework, and simple Object Orientated Design	1-2	How the simple triangle graphics program has been written using the PowerVR SDK. How to separate the triangle code out of the main drawing function and into its own class.
Introduction to mobile graphics architectures	2-3	Comparison of mobile's dominant graphics hardware, an introduction to the concerns relating to power consumption and performance, and to understand the cross-platform/cross-compilation benefits of OpenGL ES. The PowerVR Graphics architecture case study will be outlined.
Introduction to mobile graphics SDKs and forums	3-4	Learn about the main technologies used in mobile graphics SDKs up to OpenGL ES 3.2 and to learn how to use some of the SDK utilities and how to use forums for help.
Texturing	4-5	How texturing works, including the coordinate system and performance concerns.
Transformations	5	How transformations can be applied to vertices, including how to use the Model matrix for translations and rotations, and to understand the use of the View and Projection matrices.
OpenGL ES basics	6-7	Learn the basics of the OpenGL ES commands and Shader Language.
OpenGL ES lighting	7-8	Learn how to use different lighting models to illuminate objects in a scene.
Reflection and Refraction	9	Learn how cubemaps can be created and how they are used for calculating reflections and refractions.
Introduction to Vulkan	9-10	Introduction to Vulkan and a comparison with OpenGL ES.

Artificial Intelligence at the Edge: Principles & Practices

- Objectives: understanding edge-AI, the top 10 algorithms, learning to map Tensor Flow to a PVR GPU with NC-SDK-AC

Artificial Intelligence at the Edge

Authors	Peking University and UCM Madrid
Guidance Panel	Prof. Xiaohui Duan (PKU) & Student Team, Prof. Luis Piñuel Moreno (UCM), Prof. Francisco Igual Pena (UCM), Tia Miao, Florin Buica, Remus Radita, Paul Buxton, Alex Pim, Guanyang He, RCWO
Languages	En, Cn (Simplified & Trad), Jpn
Timing	Launch Q2'21. Workshops Q3'21
Status	Platform completed. Dev't just starting.
Platform	SEED Studio "Pumpkin" i300 Board (\$229)
Software	Neural Compute SDK: "NC-SDK-AC" Academic Edition (Free download)

Objectives of the course:

AI Edge Computing:

- Not just vision
- Also voice, health monitoring, hand-writing recognition, translation engines, anomaly detection, predictive maintenance...

Target Audience:

- Undergraduate students (3rd/4th year) with a preliminary knowledge of: Programming (C++, Python), Computer Organisation, Artificial Intelligence

Contents:

- General AI intro/recap
- Relevant applications in AI Edge Computing: different targets, algorithms, neural networks, tools, platforms...
- Cover the 10 most popular algorithms...

For each algorithm: define the problem, describe the algorithm, and implement using IMG software stack. Evaluate/optimise (performance, power...)

RVfpga: Understanding Computer Architecture

- Objectives: Influence thousands of future programmers & SoC designers and establish Imagination's reputation in RISC-V

Understanding Computer Architecture

Authors	Prof. Sarah Harris (UNLV, USA), Prof. Daniel Chaver-Martinez (UCM, Spain), Zubair Kakakhel & their teams
Guidance Panel	The Authors, Ivan Kravets, Ted Marena, Ali Abuassal, Guanyang He, RCWO
Languages	En, Cn + to follow: Es & Jpn
Timing	Started Jan'20, launch Nov'20 (v1) & Q3'21 (v2). Workshops Q1'21
Status	Announced. Development well underway, beta-testing started
Platforms	HW Dev't Board - Nexys A7 by Digilent SW: PlatformIO, Vivado Core: Western Digital SweRV
Textbook	<i>Digital Design & Computer Architecture RISC-V Edition</i> by David Harris and Sarah Harris. Published mid-2021

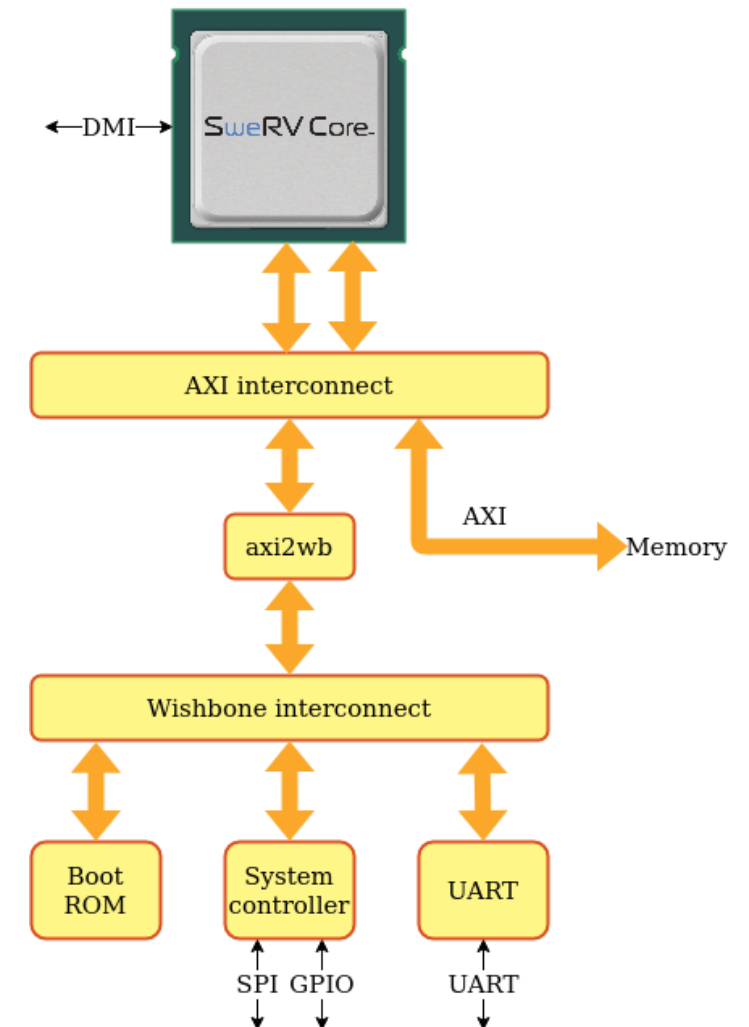


Figure from <https://github.com/chipsalliance/Cores-SweRVolf>

RVfpga: Understanding Computer Architecture

- **Objective:** Influence thousands of future programmers & SoC designers

Target Audience:

- Undergraduate students in EE, CS, CE

Track Record:

- We built & ran the “MIPSfpga” project, based on real-world MIPS microAptiv core:
 - Launched April 2015
 - Engaged 800 Universities WW, achieved leadership in Cn&Ru
 - Winner: Elektra Best Education Support, Europe 2015
 - Supported by China’s MoE
- Imagination is now using RISC-V inside its GPU and Connectivity IP products

Textbook:

- The Harris & Harris book is the most popular on this subject.
- RISC-V edition due mid 2021

Teaching Materials Package:

RISC-V FPGA “Rvfpga” provides a set of instructions, tools, and labs that show how to:

- Target a commercial RISC-V system to an FPGA
- Add more functionality to the RISC-V system
- Analyze and modify the RISC-V core and memory hierarchy

The Core:

- The RVfpga system is built around Chips Alliance’s SweRVolf SoC, which is based on Western Digital’s RISC-V SweRV EH1 core.

Future:

- Extend from 10 to 20 Labs
- Create Masters-level Introduction to SoC Design course
- Global “Teach the Teacher” Workshop series
- Online learning: Videos & MOOCs

RVfpga: Understanding Computer Architecture

Curriculum – enough for 3 Semesters !

The RVfpga Package includes material for a 1 or 2 semester course. Your course can be built around all or a subset of materials in RVfpga Labs.

RVfpga Labs Nov'20

Parts 1 & 2: Programming & I/O:

For undergraduates who have taken a digital design and basic computer architecture course, such as textbook “Digital Design and Computer Architecture” by Harris & Harris

- Students expand their **fundamental** understanding of a commercial RISC-V core and SoC (RVfpga) and modify RVfpga to include additional I/O

RVfpga Labs Q3'21

Parts 3 & 4: RISC-V Core and Memories:

- More **advanced**, for 3rd/4th year undergraduates or master's students.
- Students explore and modify the RISC-V core and memory system

RVfpga Introduction to SoC Design March'21

- Masters level
- High level Starter Tutorial
- RTL focused: build the SoC by adding GPIO, UART, DDR
- Software focused: introduce Zephyr & how to interact with the RVfpga SoC

HandsOn Labs:

- Lab 1 (RTL): Introduction to RISC-Vfpga SoC.
Setting up RTL for SweRV, BootROM, GPIO, LED
- Lab 2 (SW): running bare metal code on RVfpga SoC, IDE/Software environment/toolchain setup
- Lab 3 (RTL): Adding UART and DDR memory controllers
- Lab 4-5 (SW): Running Zephyr on RVfpga SoC
- Lab 6 (RTL): Adding SPI to RISC-Vfpga SoC
- Lab 7 (SW): Using SPI on Zephyr, Accessing Accelerometer
- Lab 8-9 (SW): Demonstrate Tensorflow Lite on RVfpga SoC

Languages:

- English, Chinese (Simplified)
- To follow: Japanese, Spanish, Chinese (Traditional)

RVfpga: Understanding Computer Architecture

- Key Components & Costs:

Software

(free downloads
from their websites)

Xilinx **Vivado** 2019.2 WebPACK

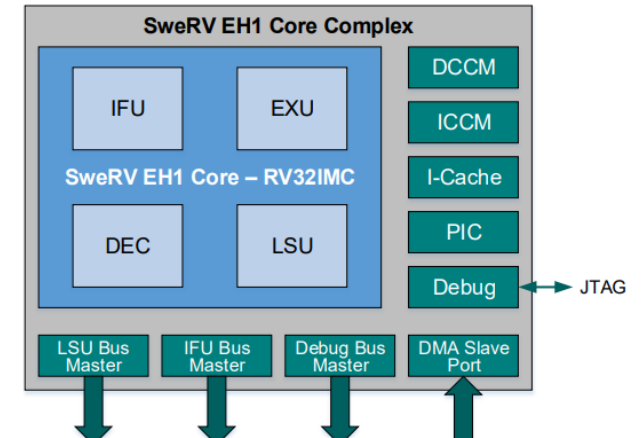
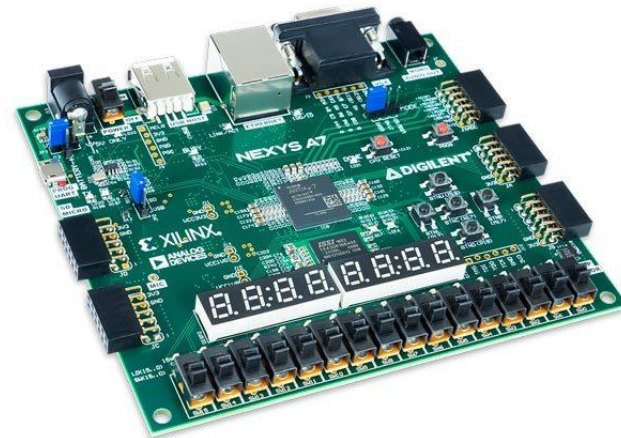
Microsoft's **Visual Studio Code**

PlatformIO with Chips Alliance platform,
which includes: RISC-V Toolchain,
OpenOCD, Verilator HDL Simulator, WD
Whisper ISS.

Hardware

(Global Distributors, incl. Digi-Key)

Digilent's **Nexys A7** (Academic Price \$199)
- or Nexys 4 DDR FPGA Board



RISC-V Core & SoC

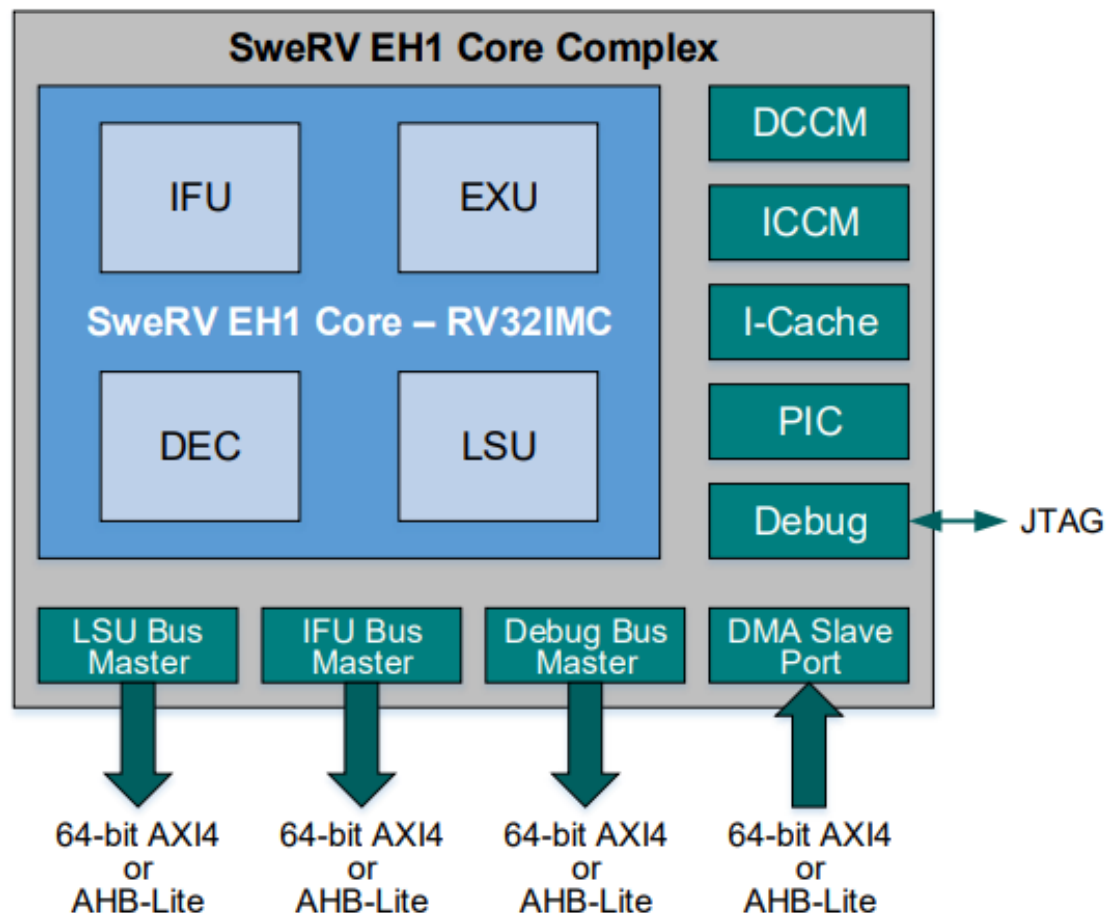
(free downloads from GitHub)

Core: Western Digital's **SweRV EH1**

SoC: Chips Alliance's **SweRVolf**

RVfpga: Understanding Computer Architecture

- SweRV EH1 Core



Not a “black box” obfuscated or “Education core”...

- RTL of a “real world” core - fully verified, in-production, industrial-grade
- 32-bit (RV32I) superscalar core, with dual-issue 9-stage pipeline
- Instruction sets: RV32**ICM**
- Separate instruction and data memories (ICCM and DCCM) tightly coupled to the core
- 4-way set-associative I\$ with parity or ECC protection
- Programmable Interrupt Controller
- Core Debug Unit compliant with the RISC-V Debug specification
- System Bus: AXI4 or AHB-Lite

RVfpga: Understanding Computer Architecture

- Sponsors, Contributors & Supporters



RVfpga: Global Team



Academic Adviser: <div> Prof. David Patterson University of California, Berkeley </div>	Authors: <div> Prof. Sarah Harris University of Nevada, Las Vegas </div>	<div> Assoc. Prof. Daniel Chaver Martinez Complutense University of Madrid </div>	<div> Zubair Kakakhel AZKY Tech Ltd, Birmingham, UK </div>
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Supporters: <div>  </div>	<div>  </div>	<div>  </div>	<div>  </div>
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RVfpga: Understanding Computer Architecture

- **SUMMARY: Comprehensive & Complete!**

RVfpga Getting Started Guide

How to install tools, download RVfpga onto the FPGA, load and run programs, and simulate programs running on RVfpga

RVfpga Quick Start Guide

Abbreviated version of Getting Started Guide

RVfpga Labs

Part 1: Vivado Project & Programming

Part 2: I/O Systems

Part 3: RISC-V Core

Part 4: RISC-V Memory Systems

The RVfpga Package provides:

a **comprehensive** introductory RISC-V course

a **hands-on** and **easily accessible** way to learn about RISC-V processors and the RISC-V ecosystem

a **freely distributed** complete RISC-V course

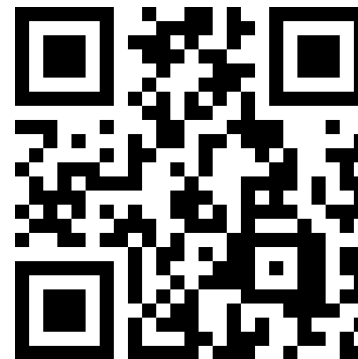
a RISC-V system targeted to **low-cost FPGAs**, which are readily available at many universities and companies.

→ After completing the RVfpga Course, users will walk away with a working RISC-V processor, SoC and ecosystem, that they understand and know how to use and modify!

The IUP website - our support hub – www.imgtec.com/University



- **Registration**
Active teachers, researchers and students worldwide
- **Downloads**
Licensing and delivery mechanism for all our teaching materials, books and software
- **Support Forums**
 - PowerVR Developer Forums
 - RVfpga Forum, AI Forum
 - IUP Forum for curriculum/teaching discussions
- **Hosting Online:**
 - ✓ Brochures
 - ✓ Events diary
 - ✓ Teaching materials
 - ✓ Video Tutorials: IUP & Graphics
 - ✓ Supported Languages: Cn, En...+
- **Social Media:**
 - ✓ Robert Owen @UniPgm
 - ✓ Imagination Technologies @ImaginationTech
 - ✓ WeChat & Weibo: ImaginationTech

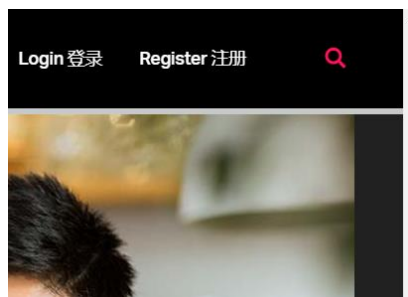


Take the Next Steps...

1. Join our Community...

<https://www.imgtec.com/university>

→ Click: “Register”



2. Please tell your colleagues!



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