# EXERCISES

**Exercise 1**

Complete solutions for this exercise are provided in folder:

*[RVfpgaPath]/RVfpga/Labs/RVfpgaLabsSolutions/Programs\_Solutions/Lab18/Minu*

**Exercise 2**

Complete solutions for this exercise are provided in folder:

*[RVfpgaPath]/RVfpga/Labs/RVfpgaLabsSolutions/Programs\_Solutions/Lab18/MinMaxMinuMaxu*

**Exercises 3 and 4**

Complete solutions for these two exercises are provided in folder:

*[RVfpgaPath]/RVfpga/Labs/RVfpgaLabsSolutions/Programs\_Solutions/Lab18/FloatingPoint*

**Exercises 5 and 6**

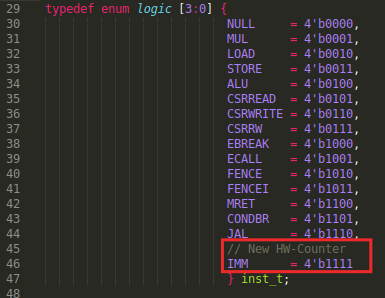
Solutions not provided.

**Exercise 7**

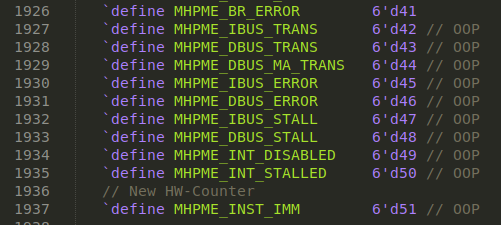
Complete solutions for this exercise are provided in folder:

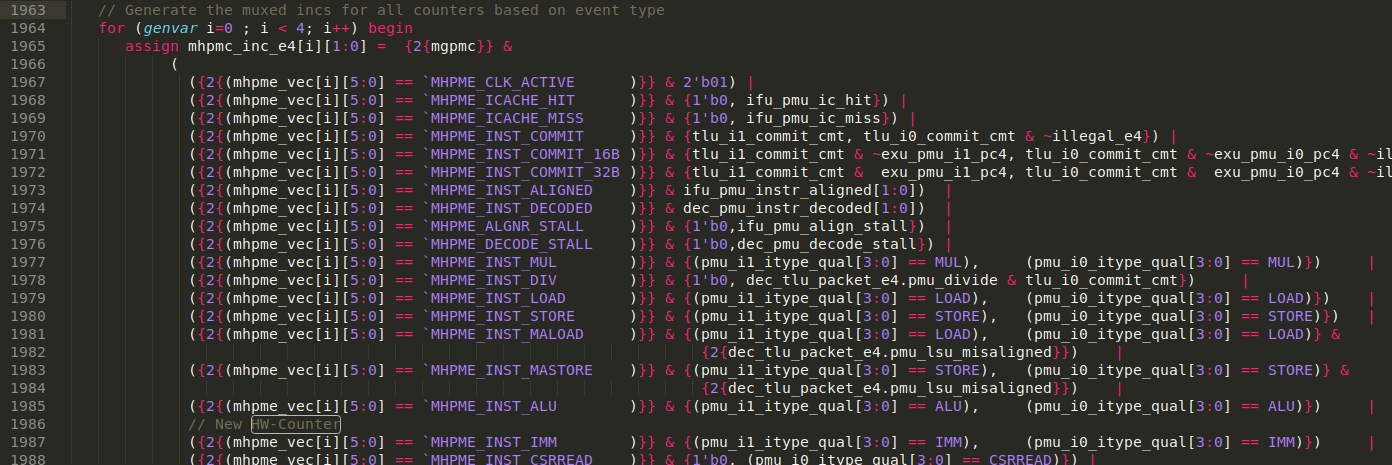
*[RVfpgaPath]/RVfpga/Labs/RVfpgaLabsSolutions/Programs\_Solutions/Lab18/NewHwCounter*

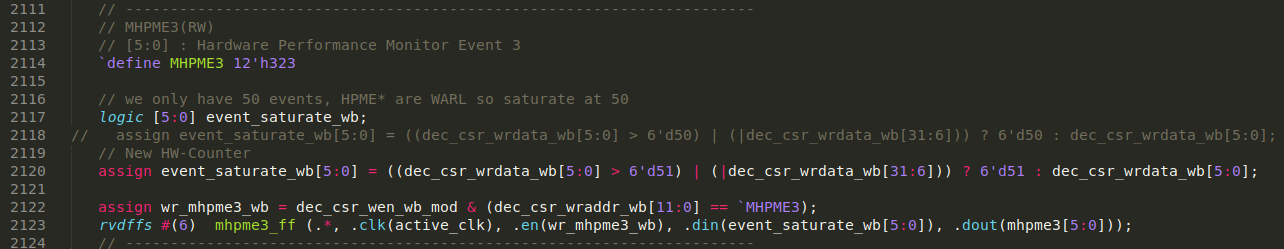
* 1. **Changes in the Verilog Code**:
     1. File **swerv\_types.sv**:



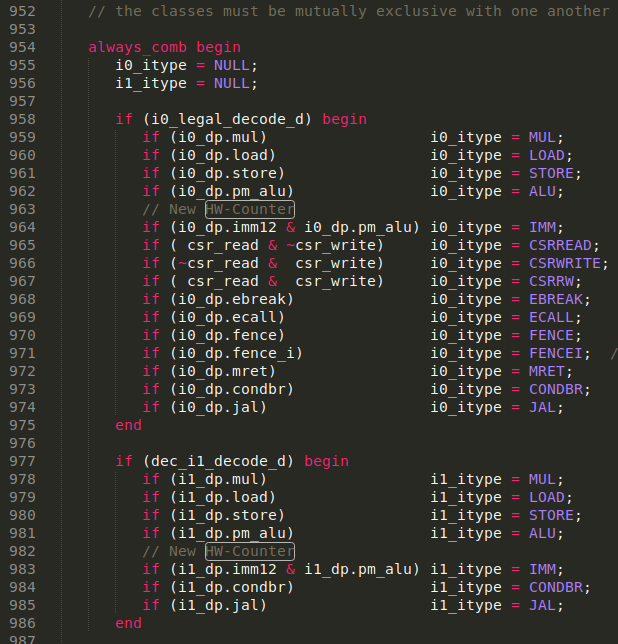
* + 1. File **dec\_tlu.ctl.sv**:



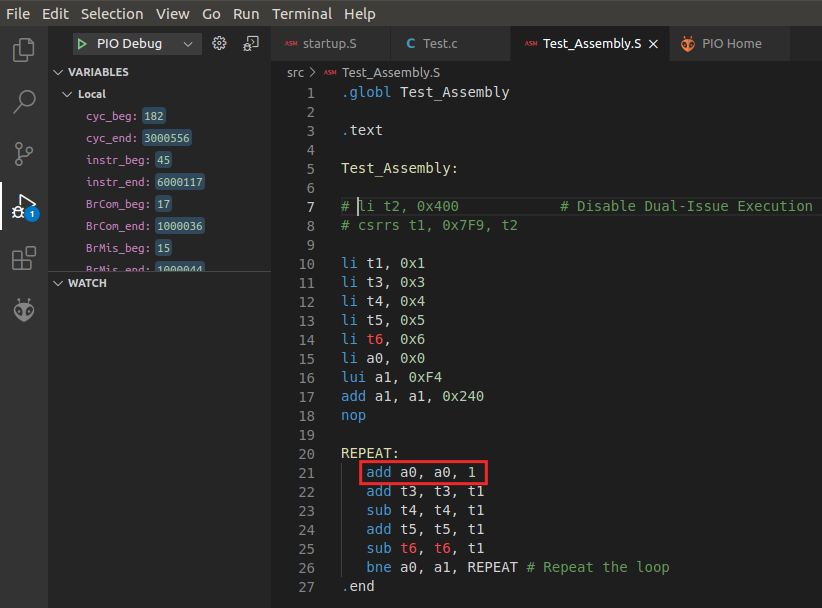


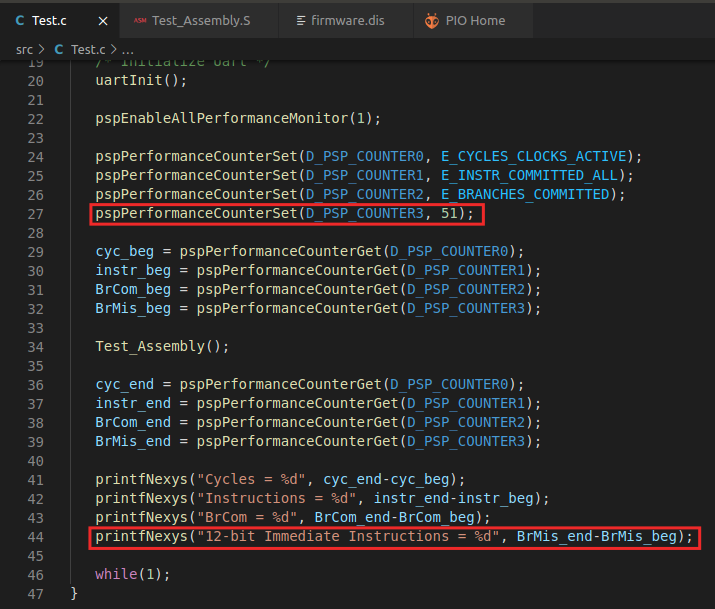


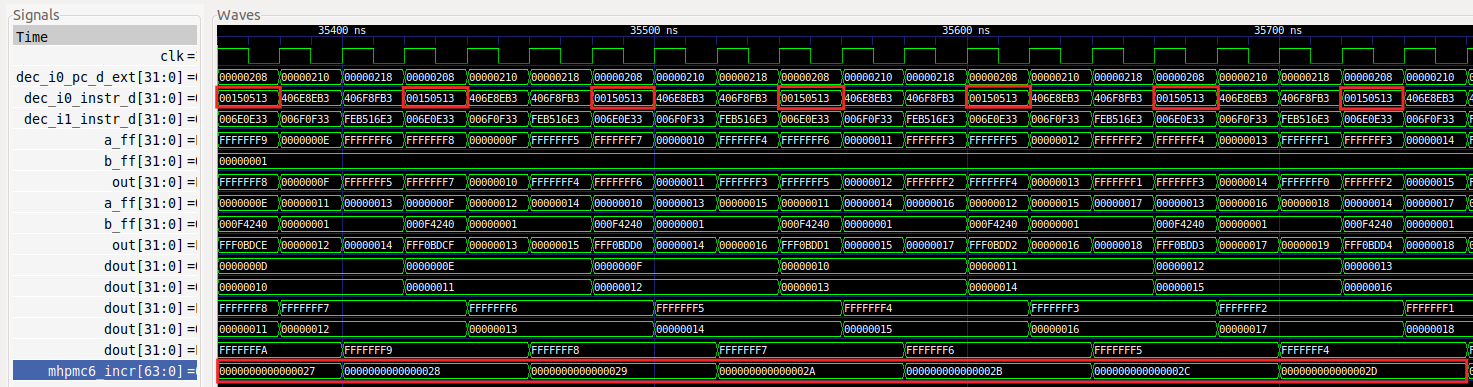
* + 1. File **dec\_decode\_ctl.sv**:



* 1. **Verilator Simulation**:







* 1. **On-board execution**:

