Wireless Modular Diagnostic Tooling

Nick Hamann Matthew Morgan

May 4, 2009

Introduction

This report documents three approaches to designing and simulating a biquad low-pass filter. Structural Verilog is the design medium for the filter and Modelsim was used to produce raw output data while Matlab is used to plot and interpret the results. The output waveforms should indicate the attenuation of high frequencies and noise filtration.

First Design

The first design considered is a basic IIR filter with a critical delay path of one multipler and one adder. This design includes a simple data truncation at the output Y[N] such that the lower order bits are discarded completely. Refer to Figure 1(a) for the general block diagram. operands are eight bits, outputs of the multipliers are sixteen bits, and all adders are sixteen bit. The input and output waveforms, see Figure 1(b), indicate that this design is not optimal, however, we will see that further optimization also had little impact on this initial result.

Truncation Code

The code used in the first design to truncate the lower order bits simply only sends the higher order eight bits to the output.

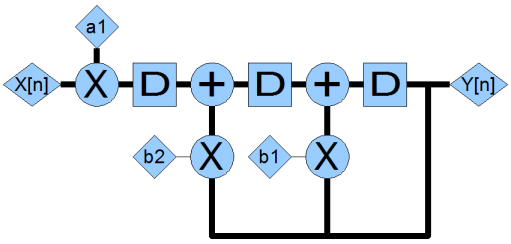
```
always @ (posedge clk)
begin
y = d3[15:8];
end
```

First Design Timing Analysis

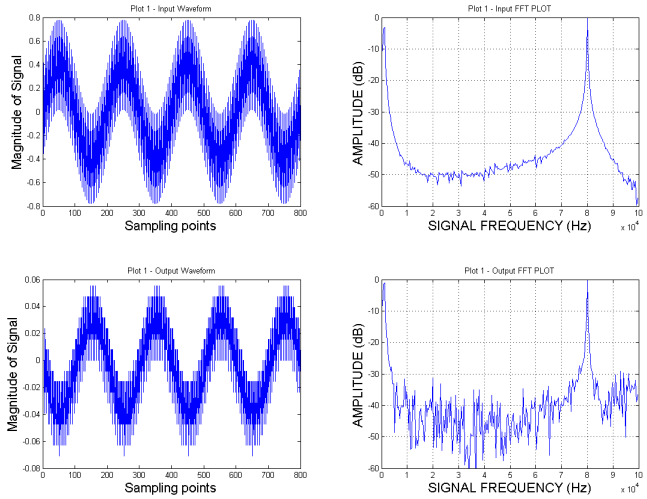
Table 1: Xilinx Timing Report

	Timing in (ns)
Minimum Period	18.684
Slack	81.391
Requrement	100
Data Path Delay	18.538

According to Table 1, the maximum clock frequency for this design has been calculated to be approximately: 81 MHz



(a) Functional block diagram



(b) Input/Output comparison

Figure 1: First Design Results

Second Design

The second design considered is a simple improvement over the first design which includes rounding before truncation a the output in an effort to improve resolution. This implementation will require another adder, though only eight bit instead of sixteen, that will increase the critical delay path from one multiplier and one adder to two adders and one multiplier. It should also be noted that this critical path will exist twice, refer to Figure 2(a). This increase in overall delay and probability of use is reflected in the timing analysis. Unfortunately, the output waveform shows little improvement in terms of attenuation; see Figure 2(b).

Rounding Truncation

The code used in the second design is uses an XOR gate to compare the ninth bit with the most significant or s̈ignb̈it. In the case that the number is a negative two's complement number, if the ninth bit is zero, the output is rounded up by one (add one), otherwise, the least significant eight bits are simply truncated as with the first design. This process is inverter in the case of positive numbers.

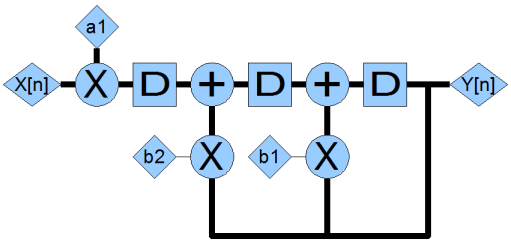
```
xor xor1(s3, d3[15], d3[7]);
add8 add3(d3[15:8], 7'b0, s3, 1'b0, ad3, cout3);
always @ (posedge clk) begin
y = ad3;
end
```

Second Design Timing Analysis

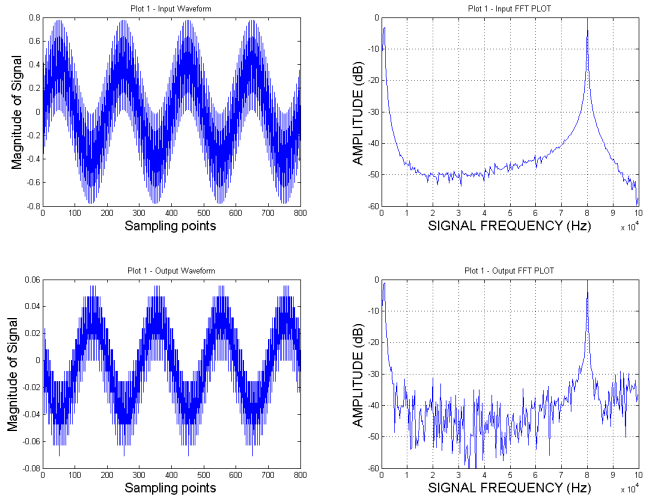
Table 2: Xilinx Timing Report

	Timing in (ns)
Minimum Period	
Slack	
Requrement	
Data Path Delay	

According to Table 2, the maximum clock frequency for the second design has been calculated to be approximately: MHz



(a) Functional block diagram



(b) Input/Output comparison

Figure 2: Second Design Results

Third Design

–Talk about basic design difference/advantages here–

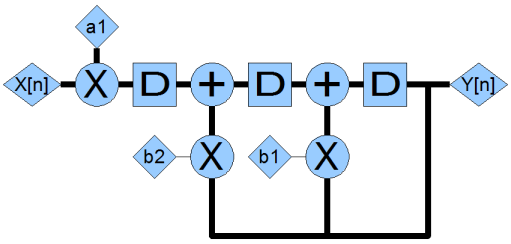
–Show differing code here–

Third Design Timing Analysis

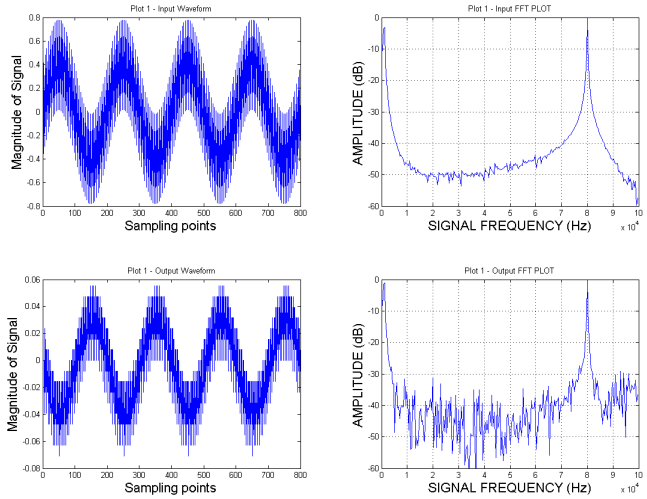
Table 3: Xilinx Timing Report

	Timing in (ns)
Minimum Period	
Slack	
Requrement	
Data Path Delay	

According to Table 3, the maximum clock frequency for the this design has been calculated to be approximately: MHz



(a) Functional block diagram



(b) Input/Output comparison

Figure 3: Second Design Results

Fourth Design

–Talk about basic design difference/advantages here–

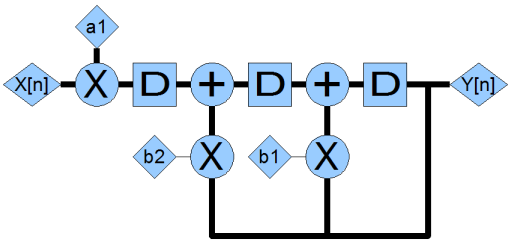
–Show differing code here–

Fourth Design Timing Analysis

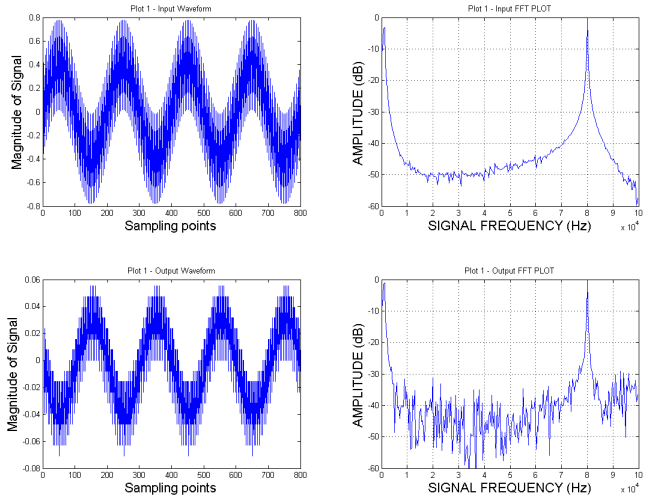
Table 4: Xilinx Timing Report

	Timing in (ns)
Minimum Period	
Slack	
Requrement	
Data Path Delay	

According to Table 4, the maximum clock frequency for the this design has been calculated to be approximately: MHz



(a) Functional block diagram



(b) Input/Output comparison

Figure 4: Second Design Results