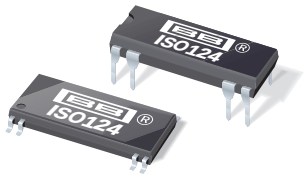
ISO124



SBOS074B – SEPTEMBER 1997 – REVISED APRIL 2003

Precision Lowest-Cost ISOLATION AMPLIFIER

FEATURES

- **100% TESTED FOR HIGH-VOLTAGE BREAKDOWN**
- **RATED 1500Vrms**
- **HIGH IMR: 140dB at 60Hz**
- **0.010% max NONLINEARITY**
- **BIPOLAR OPERATION: V_O = ±10V**
- **DIP-16 AND SO-28**
- **EASE OF USE: Fixed Unity Gain Configuration**
- **±4.5V to ±18V SUPPLY RANGE**

APPLICATIONS

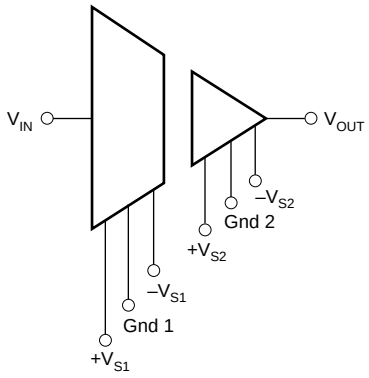
- **INDUSTRIAL PROCESS CONTROL: Transducer Isolator, Isolator for Thermocouples, RTDs, Pressure Bridges, and Flow Meters, 4-20mA Loop Isolation**
- **GROUND LOOP ELIMINATION**
- **MOTOR AND SCR CONTROL**
- **POWER MONITORING**
- **PC-BASED DATA ACQUISITION**
- **TEST EQUIPMENT**

DESCRIPTION

The ISO124 is a precision isolation amplifier incorporating a novel duty cycle modulation-demodulation technique. The signal is transmitted digitally across a 2pF differential capacitive barrier. With digital modulation, the barrier characteristics do not affect signal integrity, resulting in excellent reliability and good high-frequency transient immunity across the barrier. Both barrier capacitors are imbedded in the plastic body of the package.

The ISO124 is easy to use. No external components are required for operation. The key specifications are 0.010% max nonlinearity, 50kHz signal bandwidth, and 200µV/°C V_{OS} drift. A power supply range of ±4.5V to ±18V and quiescent currents of ±5.0mA on V_{S1} and ±5.5mA on V_{S2} make these amplifiers ideal for a wide range of applications.

The ISO124 is available in DIP-16 and SO-28 plastic surface mount packages.



ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	±18V
V_{IN}	±100V
Continuous Isolation Voltage	1500Vrms
Junction Temperature	+150°C
Storage Temperature	+125°C
Lead Temperature (soldering, 10s)	+300°C
Output Short to Common	Continuous

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

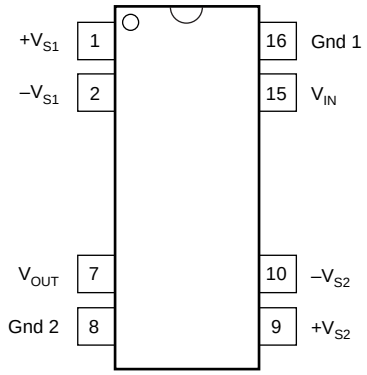
PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ISO124P	Plastic DIP-16	NVF	–25°C to +85°C	ISO124P	ISO124P	Rails, 50
ISO124U	Plastic SO-28	DVA	–25°C to +85°C	ISO124U	ISO124U	Rails, 28
"	"	"	"	ISO124U	ISO124U/1K	Tape and Reel, 1000

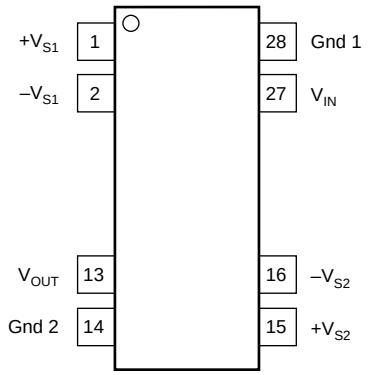
NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

PIN CONFIGURATIONS

Top View **DIP**



Top View **SO**



ELECTRICAL CHARACTERISTICS

At T_A = +25°C , V_{S1} = V_{S2} = ±15V, and R_L = 2kΩ, unless otherwise noted.

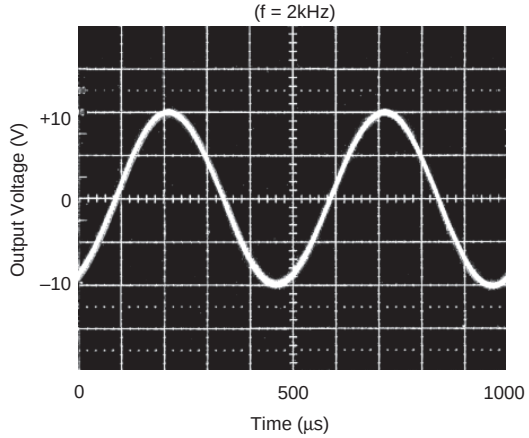
PARAMETER	CONDITIONS	ISO124P, U			UNITS
		MIN	TYP	MAX	
ISOLATION					
Rated Voltage, continuous ac 60Hz		1500			Vac
100% Test (1)	1s, 5pc PD	2400			Vac
Isolation Mode Rejection	60Hz		140		dB
Barrier Impedance			10^{14} || 2		Ω || pF
Leakage Current at 60Hz	V_{ISO} = 240Vrms		0.18	0.5	µArms
GAIN	V_O = ±10V				
Nominal Gain			1		V/V
Gain Error			±0.05	±0.50	%FSR
Gain vs Temperature			±10		ppm/°C
Nonlinearity(2)			±0.005	±0.010	%FSR
INPUT OFFSET VOLTAGE					
Initial Offset			±20	±50	mV
vs Temperature			±200		µV/°C
vs Supply			±2		mV/V
Noise			4		µV/√Hz
INPUT					
Voltage Range		±10	±12.5		V
Resistance			200		kΩ
OUTPUT					
Voltage Range		±10	±12.5		V
Current Drive		±5	±15		mA
Capacitive Load Drive			0.1		µF
Ripple Voltage(3)			20		mVp-p
FREQUENCY RESPONSE					
Small-Signal Bandwidth			50		kHz
Slew Rate			2		V/µs
Settling Time	V_O = ±10V				
0.1%			50		µs
0.01%			350		µs
Overload Recovery Time			150		µs
POWER SUPPLIES					
Rated Voltage			±15		V
Voltage Range		±4.5		±18	V
Quiescent Current: V_{S1}			±5.0	±7.0	mA
V_{S2}			±5.5	±7.0	mA
TEMPERATURE RANGE					
Specification		–25		+85	°C
Operating		–25		+85	°C
Storage		–40		+125	°C
Thermal Resistance, θ_{JA}			100		°C/W
θ_{JC}			65		°C/W

NOTES: (1) Tested at 1.6 X rated, fail on 5pC partial discharge. (2) Nonlinearity is the peak deviation of the output voltage from the best-fit straight line. It is expressed as the ratio of deviation to FSR. (3) Ripple frequency is at carrier frequency (500kHz).

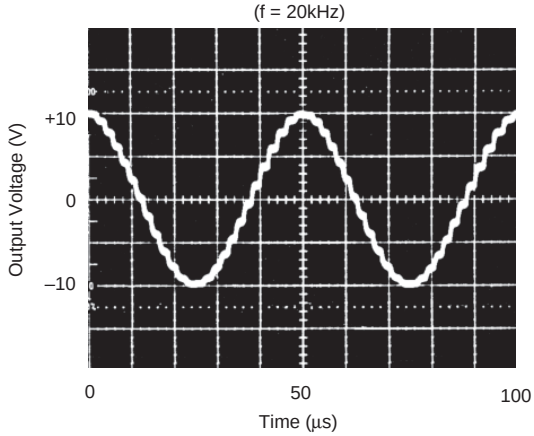
TYPICAL CHARACTERISTICS

At T_A = +25°C, and V_S = ±15V, unless otherwise noted.

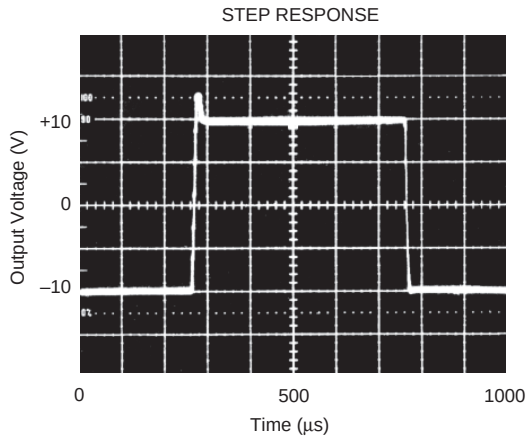
SINE RESPONSE
(f = 2kHz)



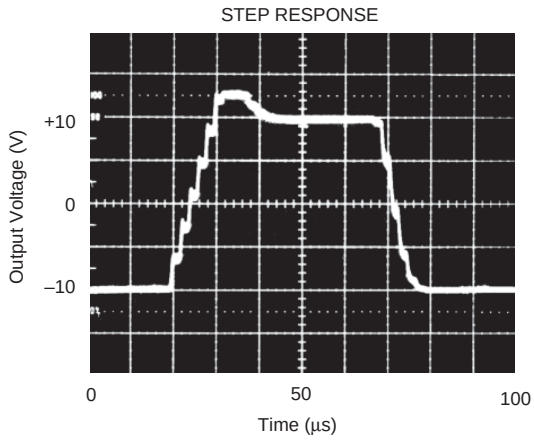
SINE RESPONSE
(f = 20kHz)



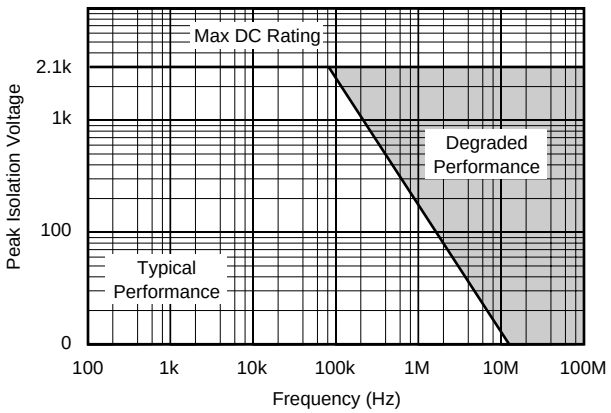
STEP RESPONSE



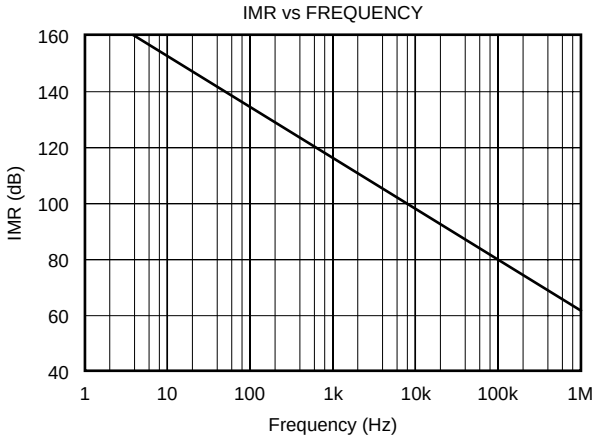
STEP RESPONSE



ISOLATION VOLTAGE
vs FREQUENCY



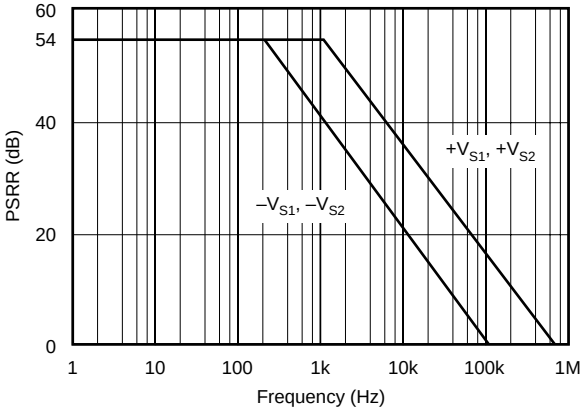
IMR vs FREQUENCY



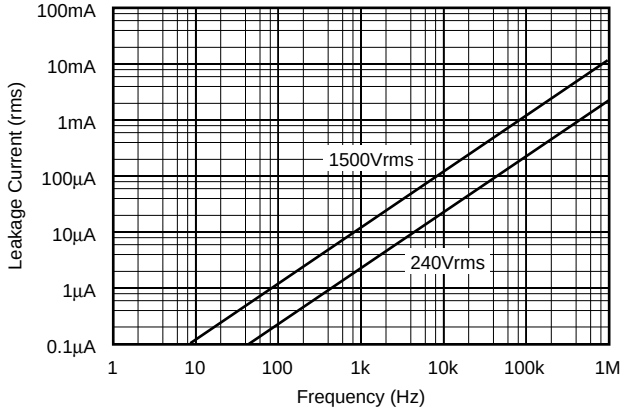
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, and V_S = ±15V, unless otherwise noted.

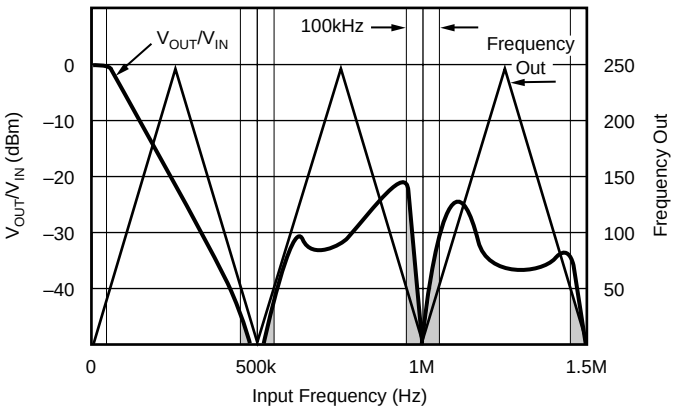
PSRR vs FREQUENCY



ISOLATION LEAKAGE CURRENT vs FREQUENCY



SIGNAL RESPONSE TO
INPUTS GREATER THAN 250kHz



(NOTE: Shaded area shows aliasing frequencies that cannot be removed by a low-pass filter at the output.)

THEORY OF OPERATION

The ISO124 isolation amplifier uses an input and an output section galvanically isolated by matched 1pF isolating capacitors built into the plastic package. The input is duty-cycle modulated and transmitted digitally across the barrier. The output section receives the modulated signal, converts it back to an analog voltage and removes the ripple component inherent in the demodulation. Input and output sections are fabricated, then laser trimmed for exceptional circuitry matching common to both input and output sections. The sections are then mounted on opposite ends of the package with the isolating capacitors mounted between the two sections. The transistor count of the ISO124 is 250 transistors.

MODULATOR

An input amplifier (A1, as shown in Figure 1) integrates the difference between the input current (V_{IN}/200kΩ) and a switched ±100µA current source. This current source is implemented by a switchable 200µA source and a fixed 100µA current sink. To understand the basic operation of the modulator, assume that V_{IN} = 0.0V. The integrator will ramp in one direction until the comparator threshold is exceeded. The comparator and sense amp will force the current source to switch; the resultant signal is a triangular waveform with a 50% duty cycle. The internal oscillator forces the current source to switch at 500kHz. The resultant capacitor drive is a complementary duty-cycle modulation square wave.

DEMODULATOR

The sense amplifier detects the signal transitions across the capacitive barrier and drives a switched current source into integrator A2. The output stage balances the duty-cycle modulated current against the feedback current through the 200kΩ feedback resistor, resulting in an average value at the V_{OUT} pin equal to V_{IN}. The sample-and-hold amplifiers in the output feedback loop serve to remove undesired ripple voltages inherent in the demodulation process.

BASIC OPERATION

SIGNAL AND SUPPLY CONNECTIONS

Each power-supply pin should be bypassed with 1µF tantalum capacitors located as close to the amplifier as possible. The internal frequency of the modulator/demodulator is set at 500kHz by an internal oscillator. Therefore, if it is desired to minimize any feedthrough noise (beat frequencies) from a DC/DC converter, use a π filter on the supplies (see Figure 4). The ISO124 output has a 500kHz ripple of 20mV, which can be removed with a simple 2-pole low-pass filter with a 100kHz cutoff using a low-cost op amp (see Figure 4).

The input to the modulator is a current (set by the 200kΩ integrator input resistor) that makes it possible to have an input voltage greater than the input supplies, as long as the output supply is at least ±15V. It is therefore possible, when using an unregulated DC/DC converter, to minimize PSR related output errors with ±5V voltage regulators on the isolated side and still get the full ±10V input and output swing. See Figure 9 for an example of this application.

CARRIER FREQUENCY CONSIDERATIONS

The ISO124 amplifier transmits the signal across the isolation barrier by a 500kHz duty-cycle modulation technique. For input signals having frequencies below 250kHz, this system works like any linear amplifier. But for frequencies

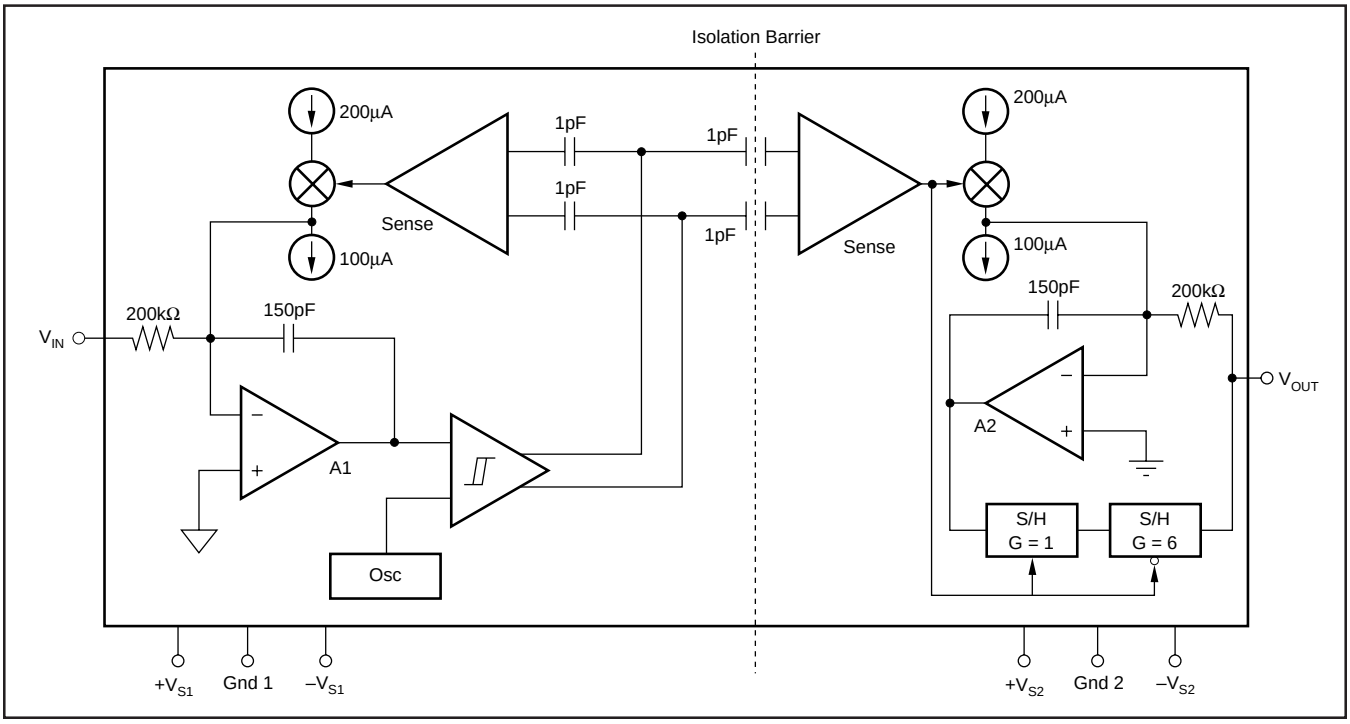


FIGURE 1. Block Diagram.

above 250kHz, the behavior is similar to that of a sampling amplifier. The typical characteristic "Signal Response to Inputs Greater Than 250kHz" shows this behavior graphically; at input frequencies above 250kHz, the device generates an output signal component of reduced magnitude at a frequency below 250kHz. This is the aliasing effect of sampling at frequencies less than 2 times the signal frequency (the Nyquist frequency). Note that at the carrier frequency and its harmonics, both the frequency and amplitude of the aliasing go to zero.

ISOLATION MODE VOLTAGE INDUCED ERRORS

IMV can induce errors at the output as indicated by the plots of IMV vs Frequency. It should be noted that if the IMV frequency exceeds 250kHz, the output also will display spurious outputs (aliasing) in a manner similar to that for V_{IN} > 250kHz and the amplifier response will be identical to that shown in the "Signal Response to Inputs Greater Than 250kHz" typical characteristic. This occurs because IMV-induced errors behave like input-referred error signals. To predict the total error, divide the isolation voltage by the IMR shown in the "IMR versus Frequency" typical performance curve and compute the amplifier response to this input-referred error signal from the data given in the "Signal Response to Inputs Greater Than 250kHz" typical characteristic. For example, if a 800kHz 1000Vrms IMR is present, then a total of [(–60dB) + (–30dB)] x (1000V) = 32mV error signal at 200kHz plus a 1V, 800kHz error signal will be present at the output.

HIGH IMV dV/dt ERRORS

As the IMV frequency increases and the dV/dt exceeds 1000V/µs, the sense amp may start to false trigger, and the output will display spurious errors. The common-mode current being sent across the barrier by the high slew rate is the cause of the false triggering of the sense amplifier. Lowering the power-supply voltages below ±15V may decrease the dV/dt to 500V/µs for typical performance.

HIGH VOLTAGE TESTING

Texas Instruments has adopted a partial discharge test criterion that conforms to the German VDE0884 Optocoupler Standards. This method requires the measurement of minute current pulses (< 5pC) while applying 2400Vrms, 60Hz high-voltage stress across every ISO124 isolation barrier. No partial discharge may be initiated to pass this test. This criterion confirms transient overvoltage (1.6 x 1500Vrms) protection without damage to the ISO124. Lifetest results verify the absence of failure under continuous rated voltage and maximum temperature.

This new test method represents the "state-of-the art" for non-destructive high-voltage reliability testing. It is based on the effects of non-uniform fields that exist in heterogeneous dielectric material during barrier degradation. In the case of void non-uniformities, electric field stress begins to ionize the void region before bridging the entire high-voltage barrier. The transient conduction of charge during and after the ionization can be detected externally as a burst of 0.01-0.1µs current pulses that repeat on each ac voltage cycle. The minimum ac barrier voltage that initiates partial discharge is defined as the "inception voltage." Decreasing the barrier voltage to a lower level is required before partial discharge ceases and is defined as the "extinction voltage." We have characterized and developed the package insulation processes to yield an inception voltage in excess of 2400Vrms so that transient overvoltages below this level will not damage the ISO124. The extinction voltage is above 1500Vrms so that even overvoltage induced partial discharge will cease once the barrier voltage is reduced to the 1500Vrms (rated) level. Older high-voltage test methods relied on applying a large enough overvoltage (above rating) to break down marginal parts, but not so high as to damage good ones. Our new partial discharge testing gives us more confidence in barrier reliability than breakdown/no breakdown criteria.

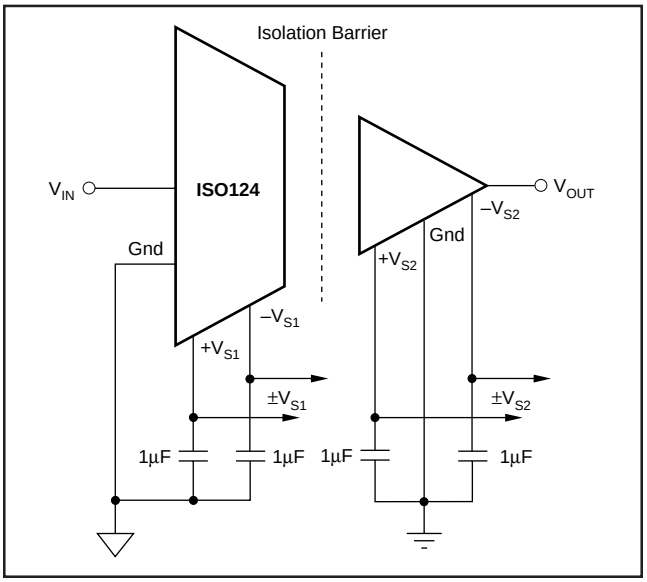


FIGURE 2. Basic Signal and Power Connections.

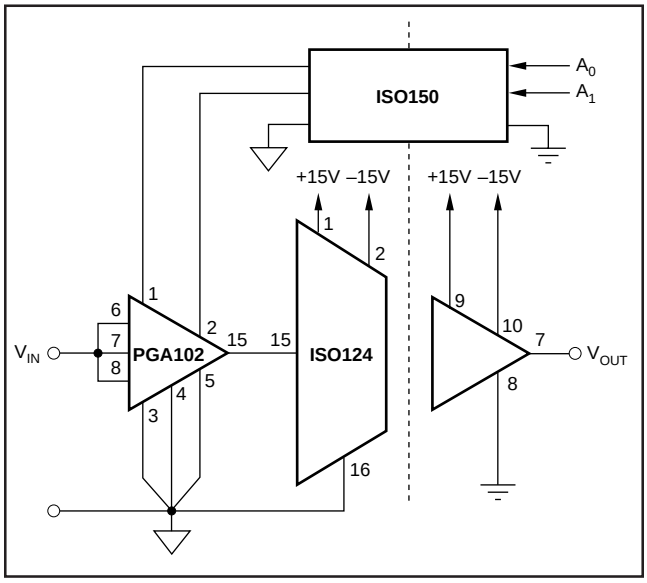


FIGURE 3. Programmable-Gain Isolation Channel with Gains of 1, 10, and 100.

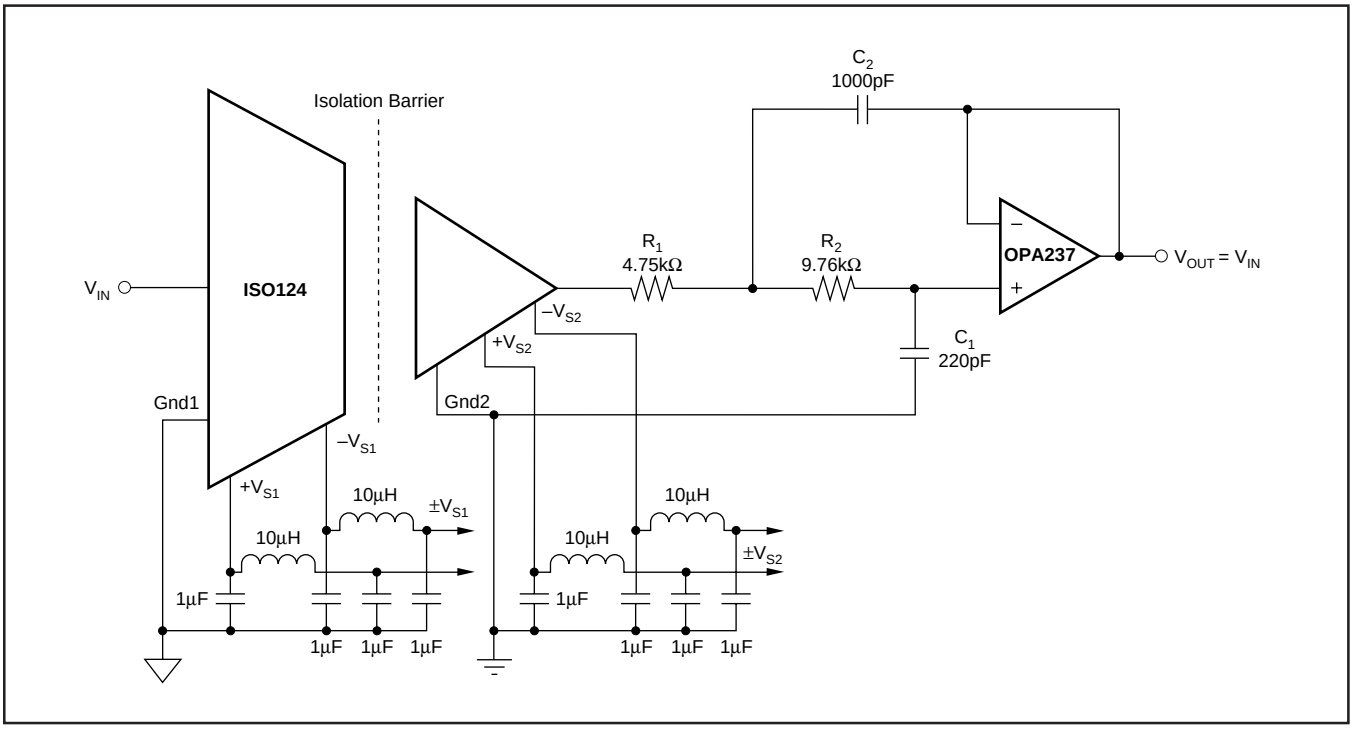


FIGURE 4. Optional π Filter to Minimize Power-Supply Feedthrough Noise; Output Filter to Remove 500kHz Carrier Ripple. For more information concerning output filters refer to Application Notes SBOA012 and SBFA001.

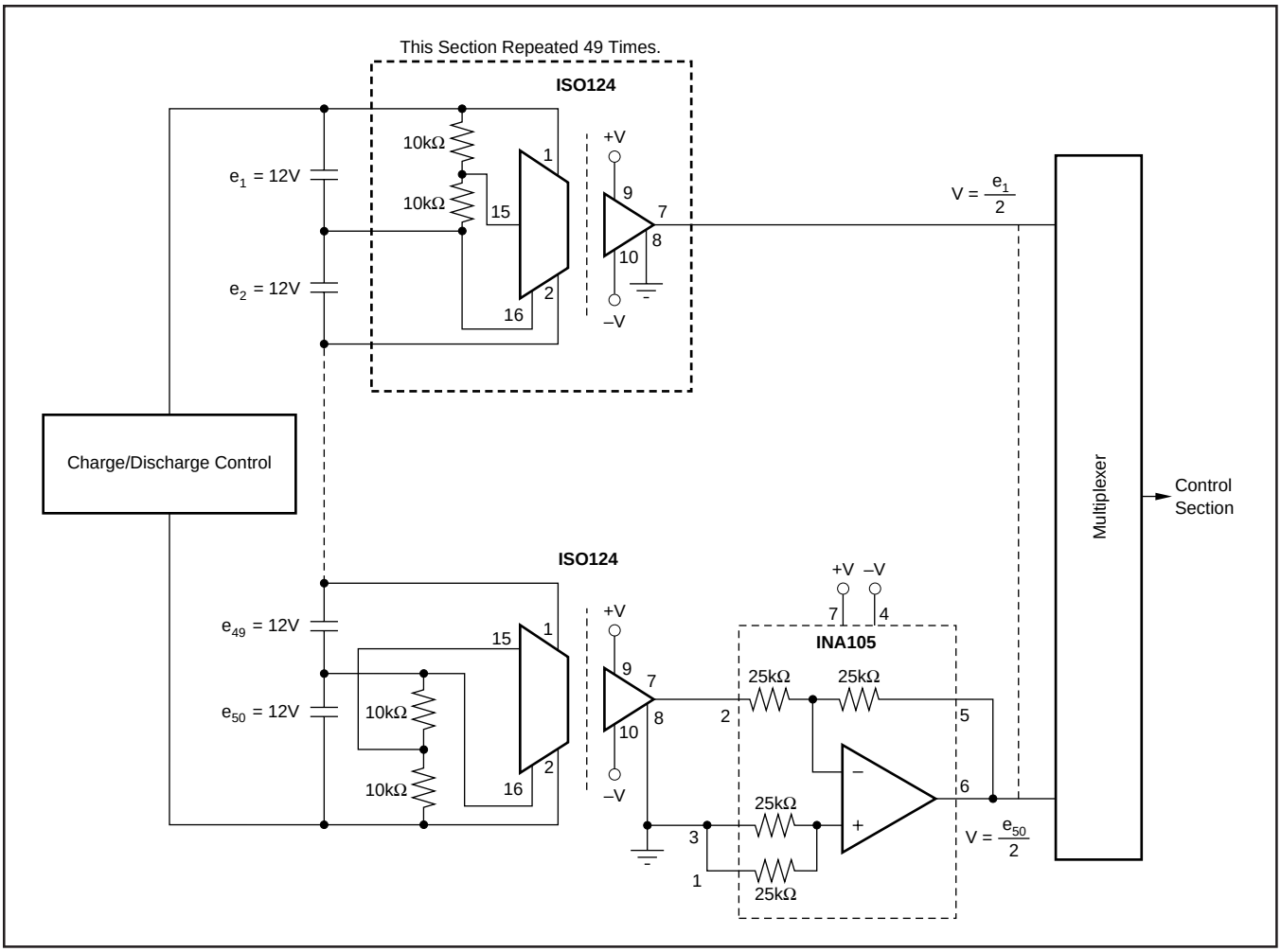
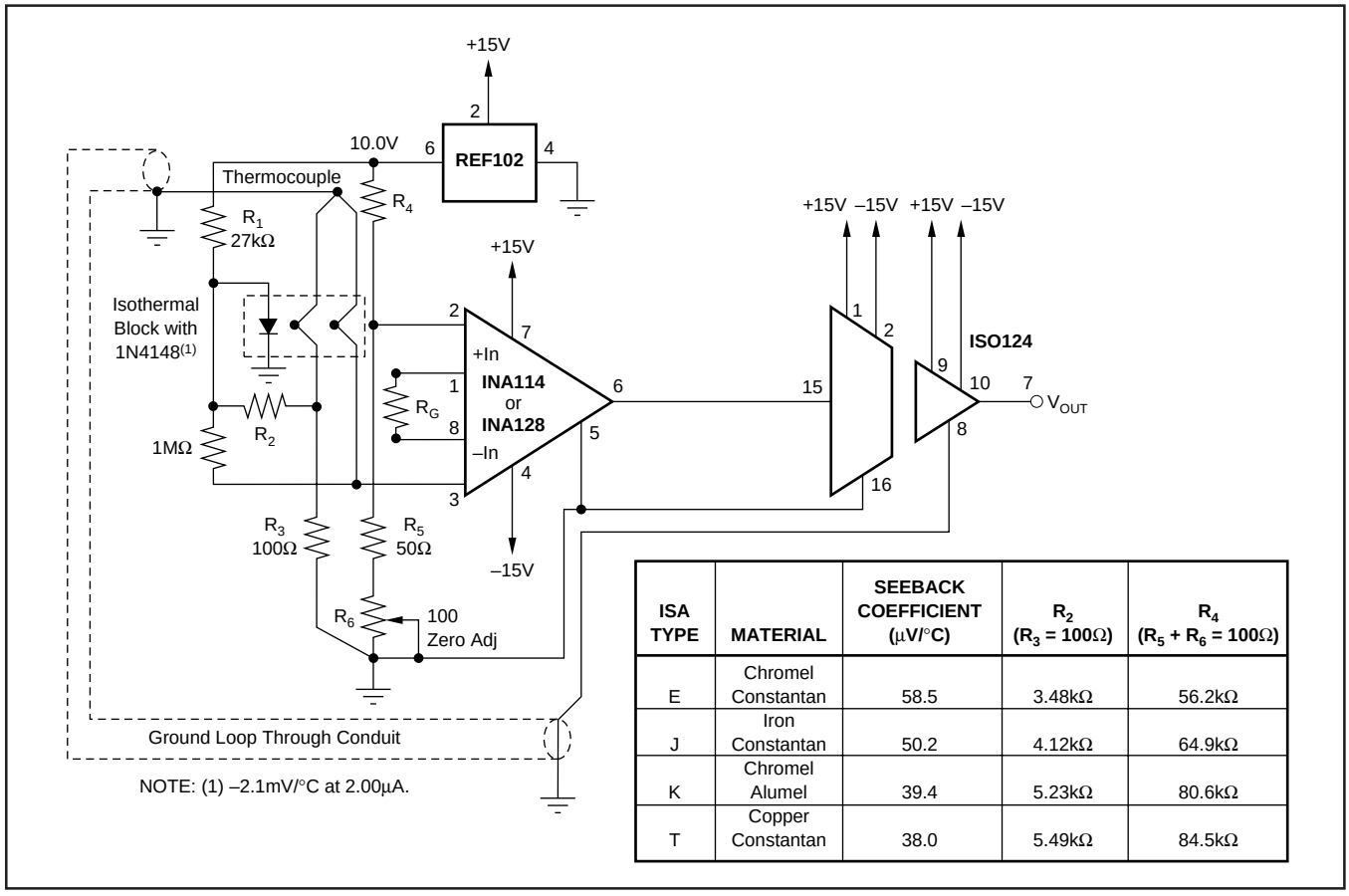


FIGURE 5. Battery Monitor for a 600V Battery Power System. (Derives input power from the battery.)



ISA TYPE	MATERIAL	SEEBACK COEFFICIENT (µV/°C)	R_2 (R_3 = 100Ω)	R_4 (R_5 + R_6 = 100Ω)
E	Chromel Constantan	58.5	3.48kΩ	56.2kΩ
J	Iron Constantan	50.2	4.12kΩ	64.9kΩ
K	Chromel Alumel	39.4	5.23kΩ	80.6kΩ
T	Copper Constantan	38.0	5.49kΩ	84.5kΩ

FIGURE 6. Thermocouple Amplifier with Ground Loop Elimination, Cold Junction Compensation, and Up-scale Burn-out.

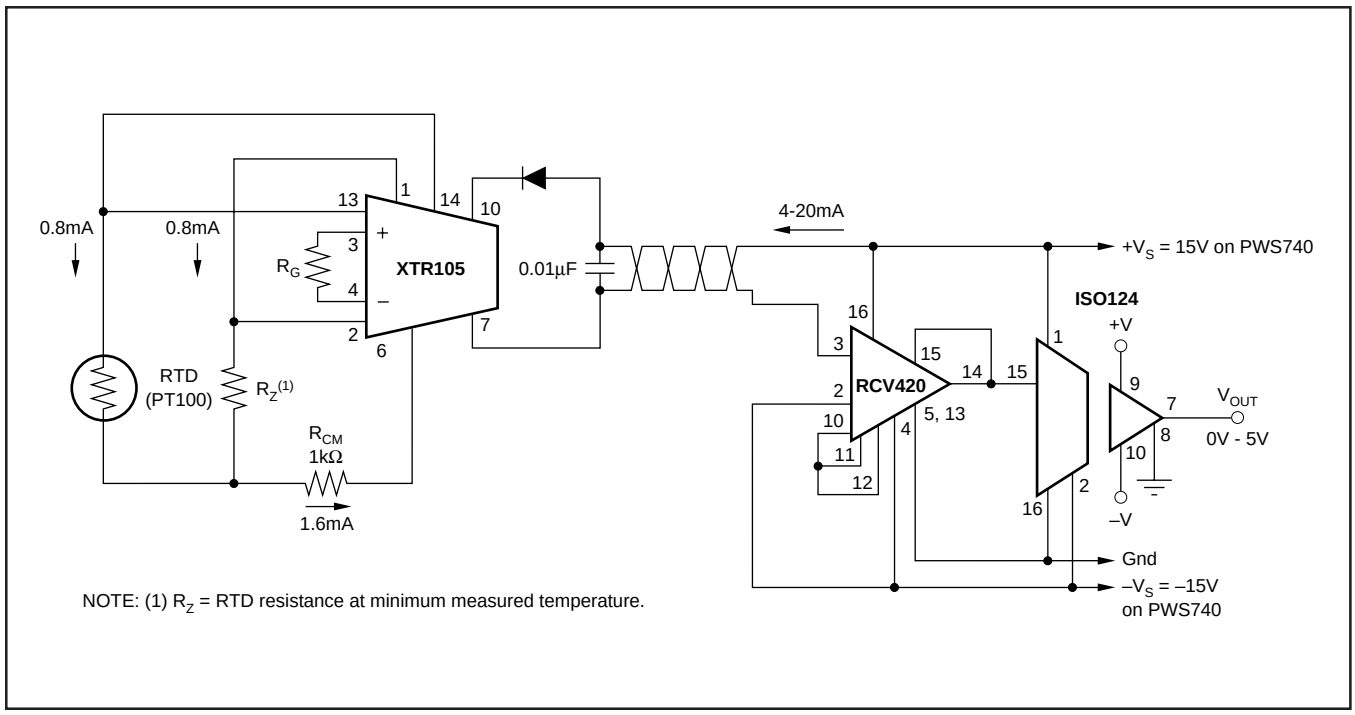


FIGURE 7. Isolated 4-20mA Instrument Loop. (RTD shown.)

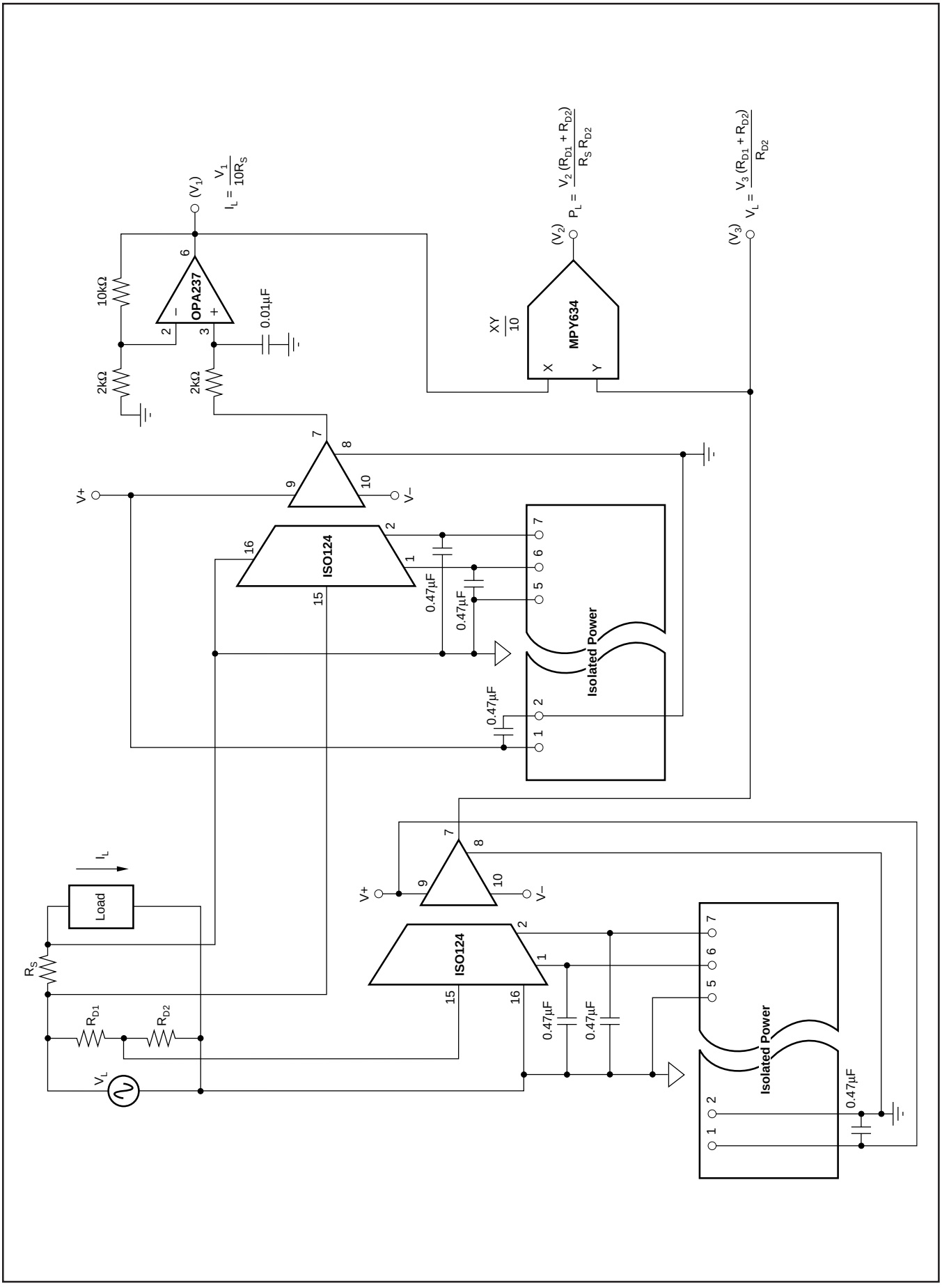
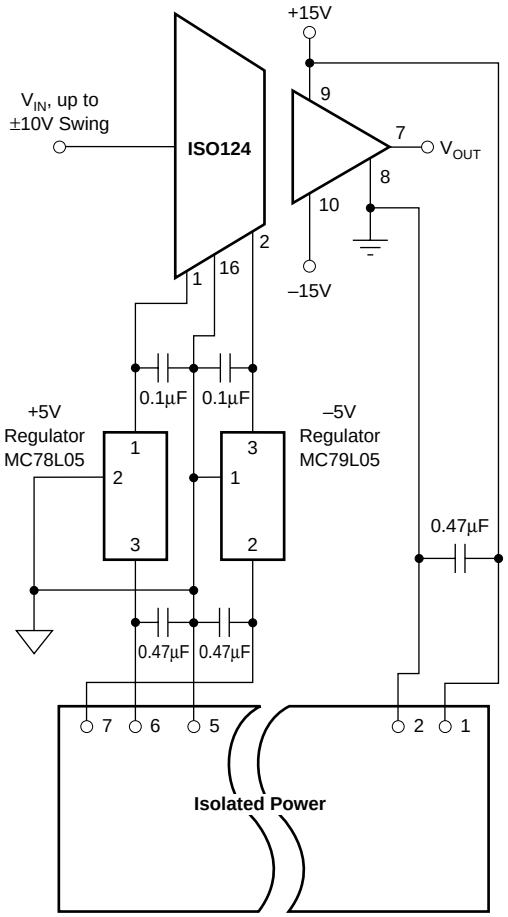


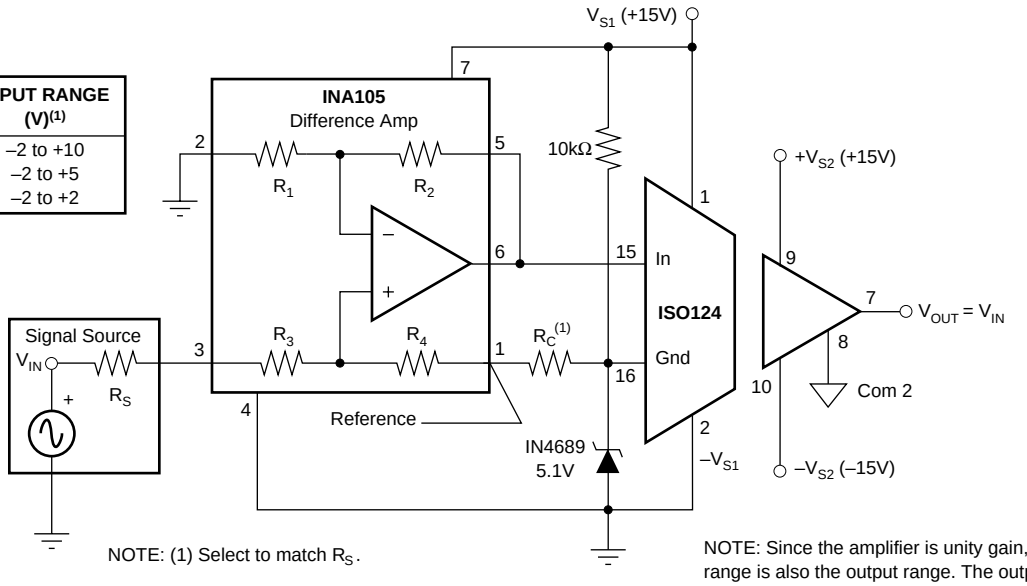
FIGURE 8. Isolated Power Line Monitor.



NOTE: The input supplies can be subregulated to ±5V to reduce PSR related errors without reducing the ±10V input range.

FIGURE 9. Improved PSR Using External Regulator.

V_S (V)	INPUT RANGE (V)(1)
20+	–2 to +10
15	–2 to +5
12	–2 to +2



NOTE: (1) Select to match R_S.

NOTE: Since the amplifier is unity gain, the input range is also the output range. The output can go to –2V since the output section of the ISO amp operates from dual supplies.

FIGURE 10. Single-Supply Operation of the ISO124 Isolation Amplifier. For additional information refer to Application Note SBOA004.

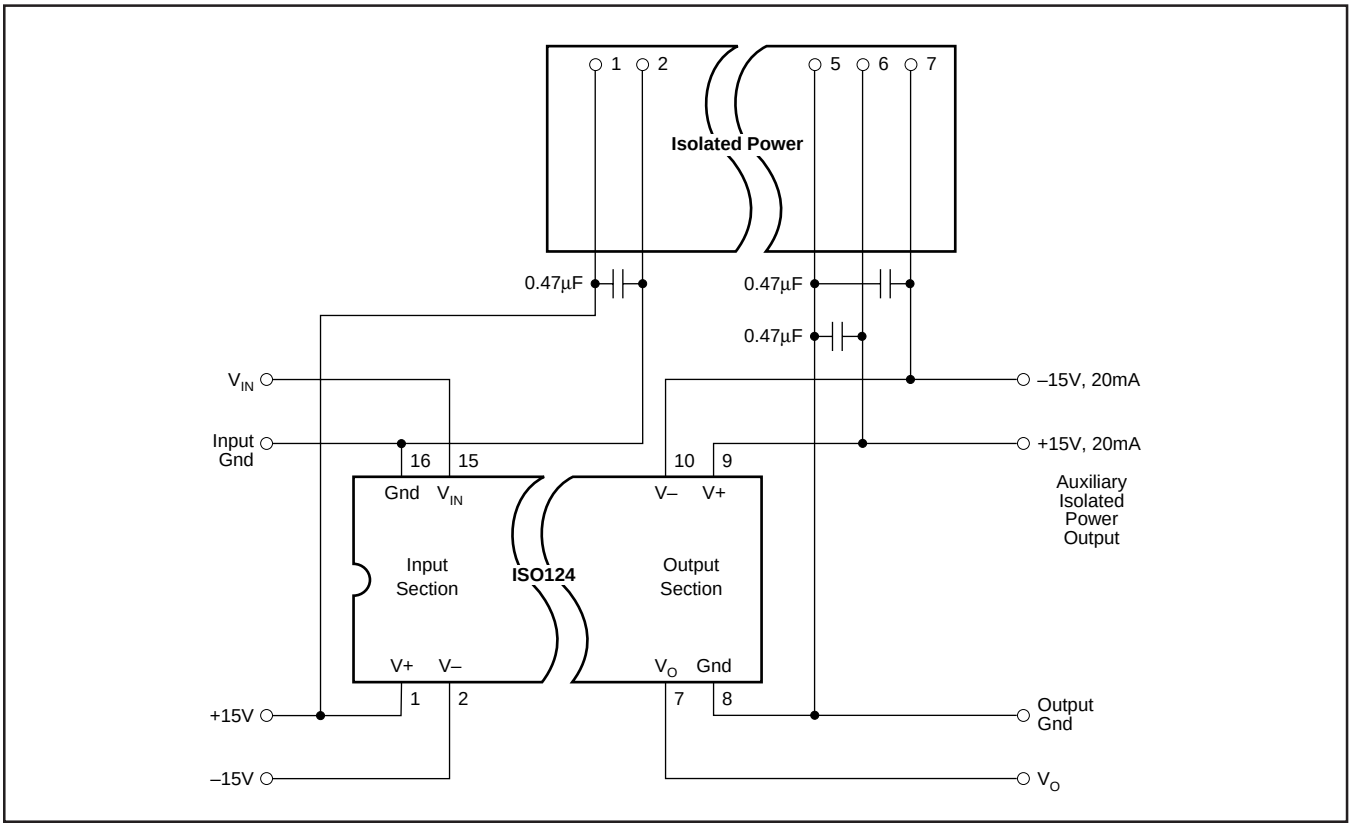


FIGURE 11. Input-Side Powered ISO Amp.

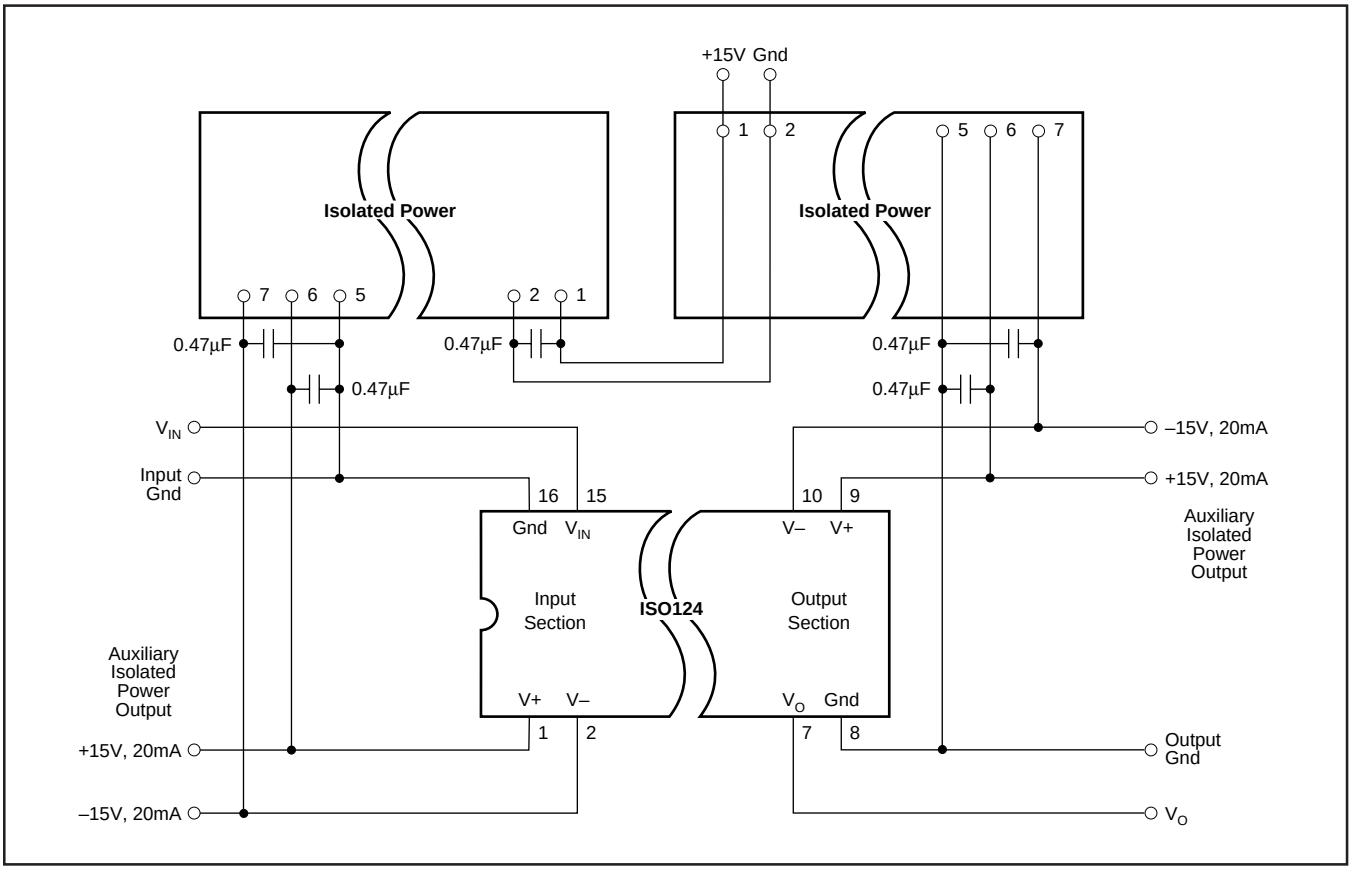
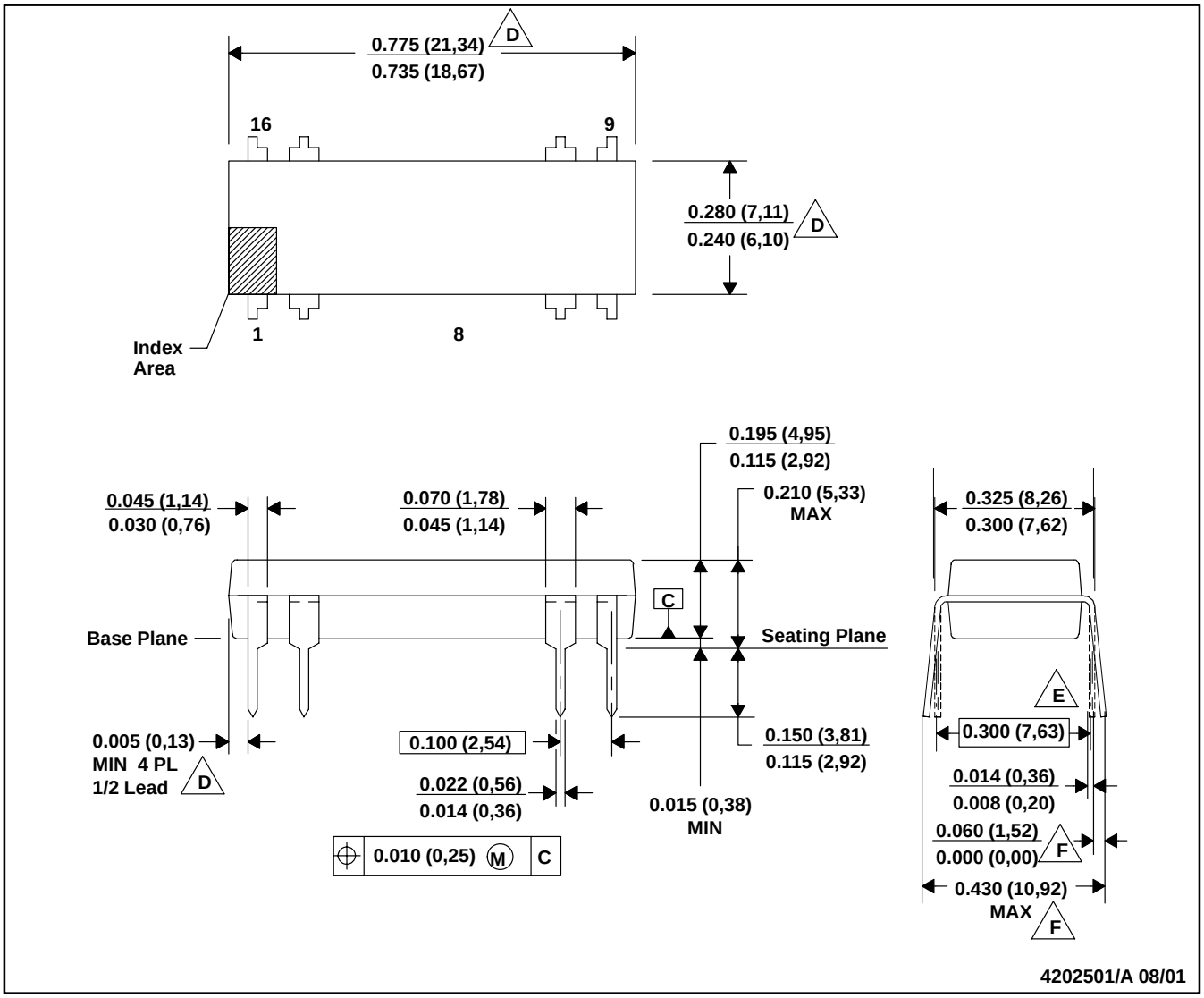


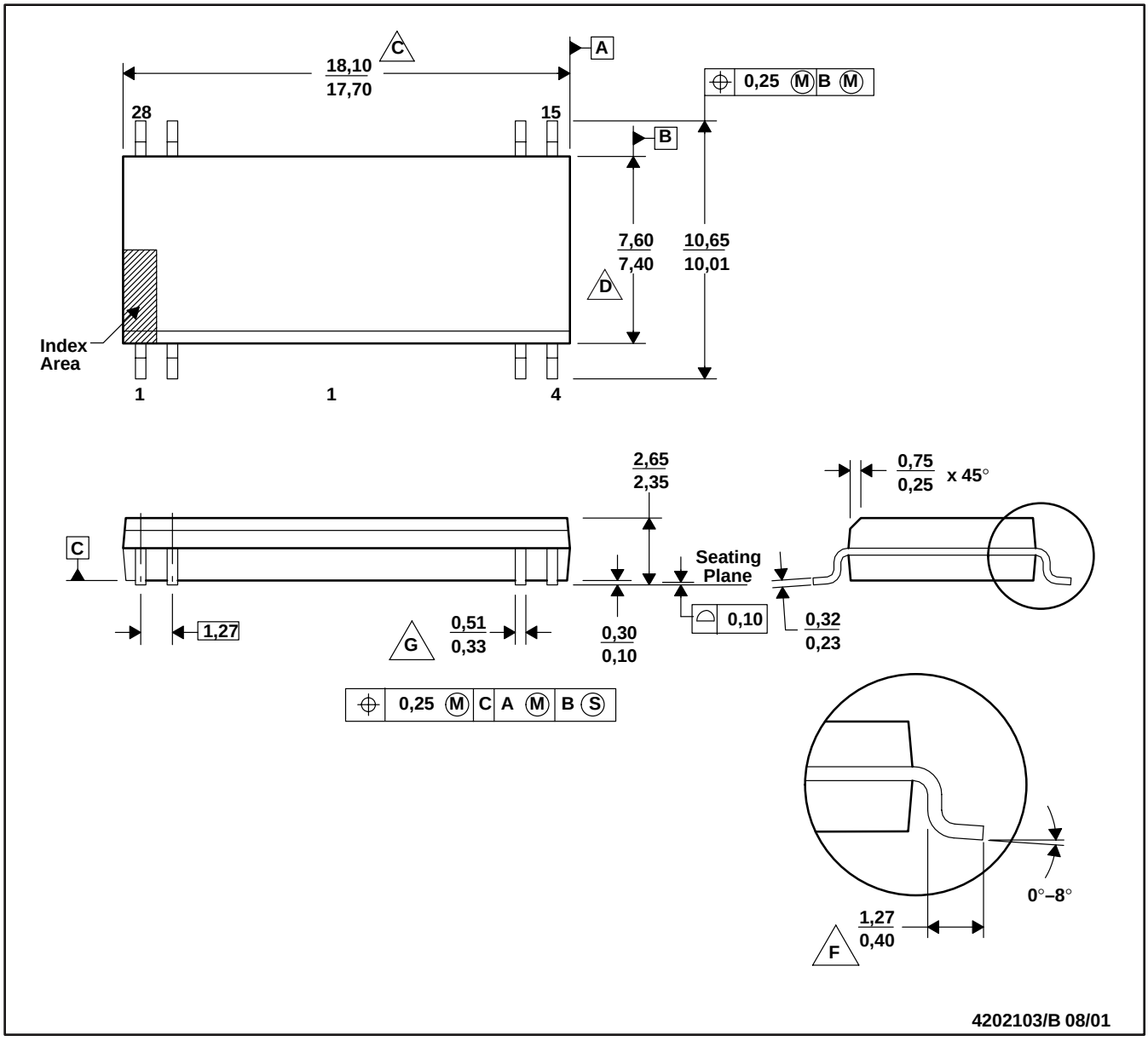
FIGURE 12. Powered ISO Amp with Three-Port Isolation.

NVF (R-PDIP-T8/16) **PLASTIC DUAL-IN-LINE**



A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001-BB with the exception of lead count.
D. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 (0,25).
E. Dimensions measured with the leads constrained to be perpendicular to Datum C.
F. Dimensions are measured at the lead tips with the leads unconstrained.
G. A visual index feature must be located within the cross-hatched area.

DVA (R-PDSO-G8/28) **PLASTIC SMALL-OUTLINE**



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0,15 mm per side.
D. Body width dimension does not include inter-lead flash or portrusions. Inter-lead flash and protrusions shall not exceed 0,25 mm per side.
E. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.
F. Lead dimension is the length of terminal for soldering to a substrate.
G. Lead width, as measured 0,36 mm or greater above the seating plane, shall not exceed a maximum value of 0,61 mm.
H. Lead-to-lead coplanarity shall be less than 0,10 mm from seating plane.
I. Falls within JEDEC MS-013-AE with the exception of the number of leads.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
ISO124P	ACTIVE	PDIP	NVF	8	50	None	Call TI	Level-NA-NA-NA
ISO124U	ACTIVE	SO	DVA	8	28	None	CU SNPB	Level-3-260C-168 HR
ISO124U/1K	ACTIVE	SO	DVA	8	1000	None	CU SNPB	Level-3-260C-168 HR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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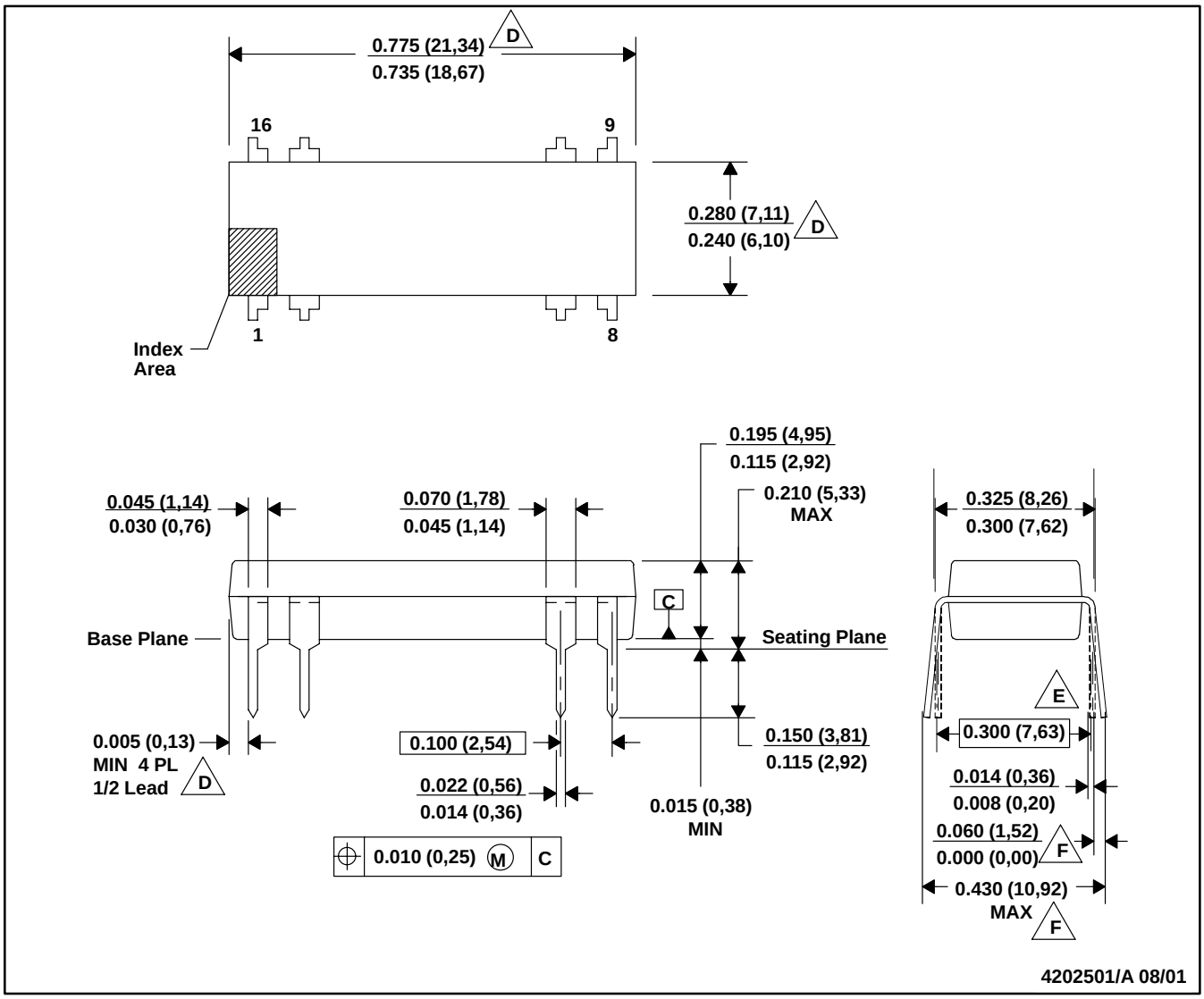
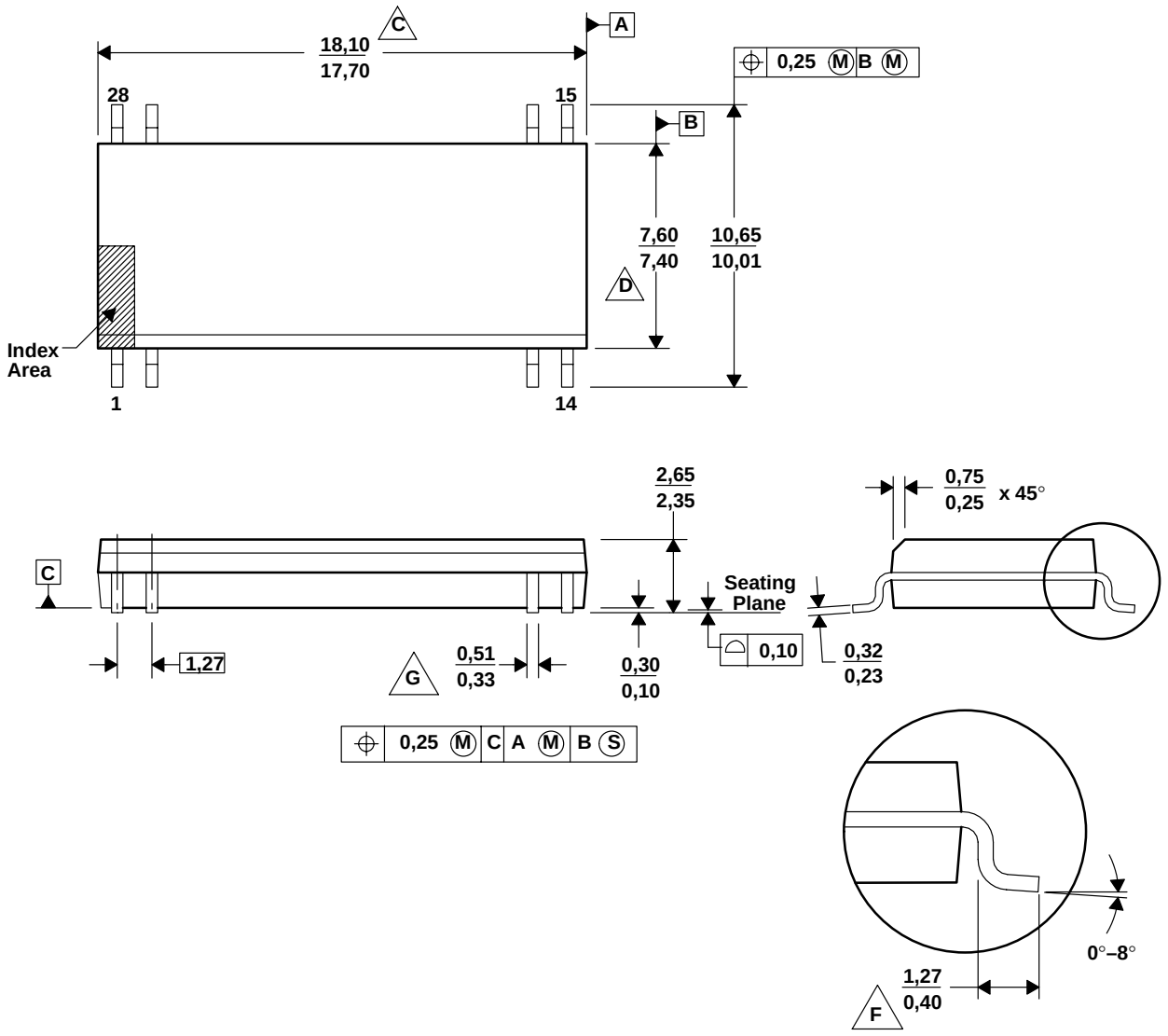
NVF (R-PDIP-T8/16) **PLASTIC DUAL-IN-LINE**



A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001-BB with the exception of lead count.
D. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 (0,25).
E. Dimensions measured with the leads constrained to be perpendicular to Datum C.
F. Dimensions are measured at the lead tips with the leads unconstrained.
G. A visual index feature must be located within the cross-hatched area.

DVA (R-PDSO-G8/28) **PLASTIC SMALL-OUTLINE**



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0,15 mm per side.
D. Body width dimension does not include inter-lead flash or portrusions. Inter-lead flash and protrusions shall not exceed 0,25 mm per side.
E. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.
F. Lead dimension is the length of terminal for soldering to a substrate.
G. Lead width, as measured 0,36 mm or greater above the seating plane, shall not exceed a maximum value of 0,61 mm.
H. Lead-to-lead coplanarity shall be less than 0,10 mm from seating plane.
I. Falls within JEDEC MS-013-AE with the exception of the number of leads.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265