#### Architetture dei Sistemi di Elaborazione

Delivery date:

November 5<sup>th</sup> 2021

Laboratory

Expected delivery of lab\_04.zip must include:

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- this document compiled possibly in pdf format.

### 1) Introducing gem5

gem5 is freely available at: http://gem5.org/

the laboratory version uses the ALPHA CPU model previously compiled and placed at:

```
/opt/gem5/
```

# the ALPHA compilation chain is available at:

```
/opt/alphaev67-unknown-linux-gnu/bin/
```

a. Write a hello world C program (hello.c). Then compile the program, using the ALPHA compiler, by running this command:

```
\label{linux-gnu} $$ \sim \proonup gem5Dir$ /opt/alphaev67-unknown-linux-gnu-gcc -static -o hello hello.c
```

## b. Simulate the program

```
~/my_gem5Dir$ /opt/gem5/build/ALPHA/gem5.opt /opt/gem5/configs/example/se.py -c hello
```

In this simulation, gem5 uses *AtomicSimpleCPU* by default.

#### c. Check the results

your simulation output should be similar than the one provided in the following:

```
~/my gem5Dir$ /opt/gem5/build/ALPHA/gem5.opt /opt/gem5/configs/example/se.py -c hello
gem5 Simulator System. http://gem5.org
gem5 is copyrighted software; use the --copyright option for details.
gem5 compiled Sep 20 2017 12:34:54
gem5 started Jan 19 2018 10:57:58
gem5 executing on this pc, pid 5477
command line: /opt/gem5/build/ALPHA/gem5.opt /opt/gem5/configs/example/se.py -c hello
Global frequency set at 100000000000 ticks per second
warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned
(512 Mbytes)
0: system.remote gdb.listener: listening for remote gdb #0 on port 7000
warn: ClockedObject: More than one power state change request encountered within the
same simulation tick
**** REAL SIMULATION ****
info: Entering event queue @ 0. Starting simulation...
info: Increasing stack size by one page.
Exiting @ tick 2623000 because target called exit()
```

## •Check the output folder

in your working directory, gem5 creates an output folder (m5out), and saves there 3 files: config.ini, config.json, and stats.txt. In the following, some extracts of the produced files are reported.

#### •Statistics (stats.txt)

```
------ Begin Simulation Statistics -------
sim_seconds 0.000003 # Number of seconds simulated
sim_ticks 2623000 # Number of ticks simulated
final_tick 2623000 # Number of ticks from beginning of simulation
```

```
100000000000 # Frequency of simulated ticks
sim freq
host_inst_rate 1128003  # Simulator instruction rate (inst/s)
host_op_rate 1124782  # Simulator op (including micro ops) rate(op/s)
host_tick_rate 564081291  # Simulator tick_rate (ticks/s)
host_mem_usage 640392  # Number of bytes of host memory used
host_inst_tot
host_op_rate
host_tick_rate
                                                   # Real time elapsed on the host
                                       0.00
host seconds
sim insts
                                       5217
                                                   # Number of instructions simulated
                                       5217
                                                    # Number of ops (including micro ops) simulated
sim_ops
. . . . . . . . . . . . . . .
system.cpu_clk_domain.clock 500
                                                      # Clock period in ticks
```

### •Configuration file (config.ini)

```
[system.cpu]
type=AtomicSimpleCPU
children=dtb interrupts isa itb tracer workload
branchPred=Null
checker=Null
clk domain=system.cpu clk domain
cpu_id=0
default_p_state=UNDEFINED
do checkpoint insts=true
do quiesce=true
do statistics insts=true
dtb=system.cpu.dtb
eventq index=0
fastmem=false
function trace=false
```

## 2) Simulate the same program using different CPU models.

## Help command:

```
~/my gem5Dir$ /opt/gem5/build/ALPHA/gem5.opt /opt/gem5/configs/example/se.py -h
```

#### List the CPU available models:

```
~/my_gem5Dir$ /opt/gem5/build/ALPHA/gem5.opt /opt/gem5/configs/example/se.py --list-cpu-types
```

#### a. TimingSimpleCPU simple CPU that includes an initial memory model interaction

```
\label{lem:configs} $$ \sim \proon_{gem5} \pr
```

## b. *MinorCPU* the CPU is based on an in order pipeline including caches

```
~/my_gem5Dir$ /opt/gem5/build/ALPHA/gem5.opt /opt/gem5/configs/example/se.py --cpu-type=MinorCPU --caches -c hello
```

#### c. *DerivO3CPU* is a superscalar processor

```
~/my_gem5Dir$ /opt/gem5/build/ALPHA/gem5.opt /opt/gem5/configs/example/se.py --cpu-type=DerivO3CPU --caches -c hello
```

#### Create a table gathering for every simulated CPU the following information:

- Ticks
- Number of instructions simulated
- Number of CPU Clock Cycles
  - Number of CPU clock cycles = Number of ticks / CPU Clock period in ticks (usually 500)
- Clock Cycles per Instruction (CPI)

- CPI = CPU Clock Cycles / instructions simulated
- Number of instructions committed
- Host time in seconds
- Number of instructions Fetch Unit has encountered (this should be gathered for the out-of-order processor only).

TABLE1: Hello program behavior on different CPU models

СРИ				
Parameters	AtomicSimpleCPU	TimingSimpleCPU	MinorCPU	DeriveO3CPU
Ticks	2654500	342272000	30117500	17146000
CPU clock domain	500	500	500	500
Clock Cycles	5310	684544	60235	34293
Instructions simulated	5280	5280	5292	5080
CPI	1.0057	129.64	11.38	6.75
Committed instructions	5280	5280	5292	5080
Host seconds	0.00	0.02	0.03	0.05
Instructions encountered				
by Fetch Unit				10950

- 3) Download the test programs related to the **automotive** sector available in MiBench: basicmath, bitcount, qsort, and susan. These programs are freely available at <a href="http://vhosts.eecs.umich.edu/mibench/">http://vhosts.eecs.umich.edu/mibench/</a>
  - a) compile the program basicmath using the provided *Makefile* using the ALPHA compiler *hint*:

b) Simulate the program basicmath using the *large* set of inputs and the default processor (*AtomicSimpleCPU*), saving the output results. In the case the simulation time is higher than a couple of minutes, modify the program in order to reduce the simulation time; for example, in the case of basicmath, it is necessary to reduce the number of iterations the program executes in order to reduce the computational time.

<u>TODO</u>: To reduce the simulation time of *basicmath\_large.c*, modify the number of iterations of the <u>for loops</u> as follows:

- c) Simulate the resulting program using the gem5 different CPU models and collect the following information:
  - a) Number of instructions simulated
  - b) Number of CPU Clock Cycles
  - c) Clock Cycles per Instruction (CPI)
  - d) Number of instructions committed

- e) Host time in seconds
- f) Prediction ratio for Conditional Branches (Number of Incorrect Predicted Conditional Branches / Number of Predicted Conditional Branches)
- g) BTB hits
- h) Number of instructions Fetch Unit has encountered.

Parameters f, g and h should be gathered exclusively for the out-of-order processor.

TABLE2: basicmath large program behavior on different CPU models

CPUs				
Parameters	AtomicSimpleCPU	TimingSimpleCPU	MinorCPU	DerivO3CPU
Ticks	222416570500	27849853285000	358284775500	142889111500
CPU clock domain	500	500	500	500
Clock Cycles	444833142	5569970650	716569551	285778225
Instructions simulated	444833079	444833079	444833105	436251129
СРІ	1.0000	12.5200	1.6108	0.655077
Committed instructions	444833079	444833079	444833105	436251129
Host seconds	225.15	121699	1142.47	1292.11
Prediction ratio				0.0267
BTB hits				46229517
Instructions encountered				
by Fetch Unit				485513496