Politecnico di Torino

III Facoltà di Ingegneria

Laboratory 3
Design of a RISC-V-lite processor

Master degree in Electronic Engineering

Authors: Group 21

Dilillo Nicola S284963
Moncalvo Stefano S290315
Carrano Lorenzo S281565

Github Repository

Contents

CHAPTER 1

Introduction

1.1 Introduction

CHAPTER 2

Datapath

2.1 Fetch Stage

2.2 Decode Stage

2.3 Execute Stage

2.4 Memory Stage

2.5 Write Back Stage

CHAPTER 3

Control Unit

3.1 Introduction

CHAPTER 4

Hazards

CHAPTER 5

Testbench

CHAPTER 6

Synthesis and Place & Route