



Politecnico di Torino
III Facoltà di Ingegneria

Laboratory 3

Design of a RISC-V-lite processor

Master degree in Electronic Engineering

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GitHub Repository

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Introduction

1.1 Introduction

CHAPTER 2

Datapath

2.1 Fetch Stage

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CHAPTER 3

Control Unit

3.1 Introduction

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Hazards

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Testbench

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Synthesis and Place & Route