



Politecnico di Torino
III Facoltà di Ingegneria

Laboratory 3

Design of a RISC-V-lite processor

Master degree in Electronic Engineering

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[Github Repository](#)

Contents

1	Introduction	1
1.1	Introduction	1
2	Datapath	2
2.1	Fetch Stage	2
2.2	Decode Stage	2
2.3	Execute Stage	2
2.4	Memory Stage	2
2.5	Write Back Stage	2
3	Control Unit	3
3.1	Introduction	3
4	Hazards	4
5	Testbench	5
6	Synthesis and Place & Route	6

CHAPTER 1

Introduction

1.1 Introduction

CHAPTER 2

Datapath

- 2.1 Fetch Stage
- 2.2 Decode Stage
- 2.3 Execute Stage
- 2.4 Memory Stage
- 2.5 Write Back Stage

CHAPTER 3

Control Unit

3.1 Introduction

CHAPTER 4

Hazards

CHAPTER 5

Testbench

CHAPTER 6

Synthesis and Place & Route