Politecnico di Torino

III Facoltà di Ingegneria

Laboratory 3
RISCV Processor

Master degree in Electrical Engineering

Authors: Group 21

Dilillo Nicola S284963
Moncalvo Stefano S290315
Carrano Lorenzo S281565

February 13, 2022

Contents

CHAPTER 1

Introduction

1.1 Introduction

Datapath

2.1 Fetch Stage

2.2 Decode Stage

2.3 Execute Stage

2.3.1   ALU

2.3.2   Forwarding Unit

2.4 Memory Stage

2.5 Write Back Stage

CHAPTER 3

Control Unit

3.1   Introduction