Politecnico di Torino

III Facoltà di Ingegneria

Laboratory 3
Design of a RISC-V-lite processor

Master degree in Electronic Engineering

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GitHub Repository

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6.1 Shynthesis

The two different designs have been synthesized using Synopsys Design Compiler, in order to obtain the maximum working frequency and an area estimation of the circuits. The following table summarizes the obtained results.

	RISCV	**Modified RISCV**
Min. Period	3.55 ns	3.6 ns
Max. Frequency	281.7 MHz	277.8 MHz
Area	14006.23 μm^2	14802.1 μm^2

Table 6.1: **Design Compiler Reports**

As expected, the modified design with the added component occupies more area. Moreover, since the added hardware is placed along the critical path, the maximum frequency is also slightly lower; however this is compensated by the reduced time needed for the computation of the instruction.

The report of the *elaborate* command lists the inferred memory devices inserted in the netlist. Every element was checked to avoid the insertion of latch instead of flip-flops. Finally, both synthesized netlists were simulated with Modelsim to confirm they still behaved correctly.

6.2 Place & Route

After the synthesis of the circuits, place & route was performed using Cadence Innovus. This requires to perform the following steps:

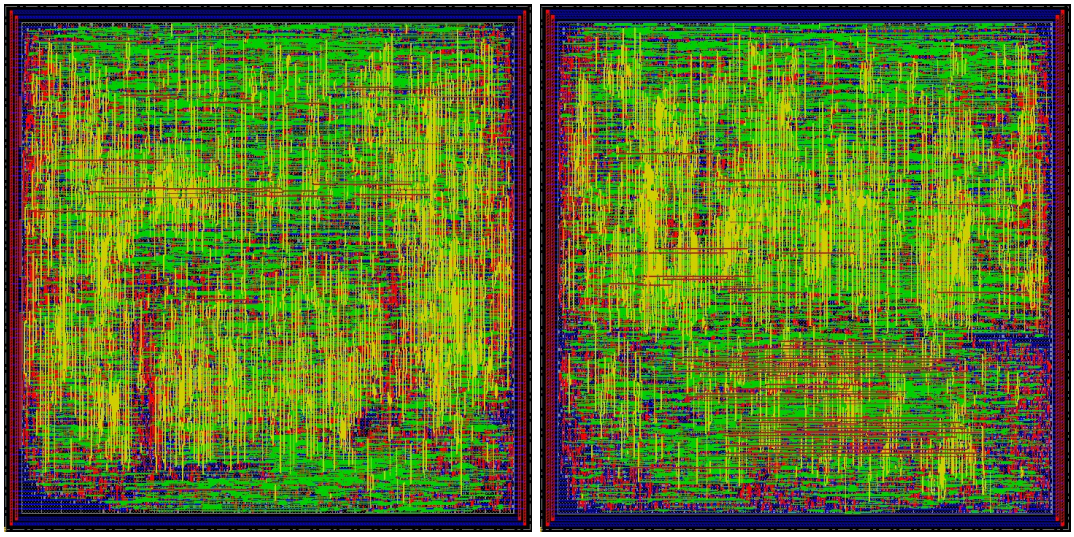
- Importing the design;
- Floorplanning;
- Power planning and routing;
- Cell placing;
- Signal routing;
- Timing and design analysis.

The procedure returned no violations in connections and geometry. The resulting netlist was saved together with the final gate count.

	RISCV	**Modified RISCV**
Area	13533.0 μm^2	14133.6 μm^2

Table 6.2: **Innovus Reports**

Innovus was able to optimize the netlists and save a noticeable amount of area on both designs, with respect to the value obtained with Synopsys. Also in this case, the produced netlists were simulated to verify the compliance with the original design.



(a) RISCV (b) Modified RISCV

Figure 6.1: **Place and route of the two designs**