**Perceptron**

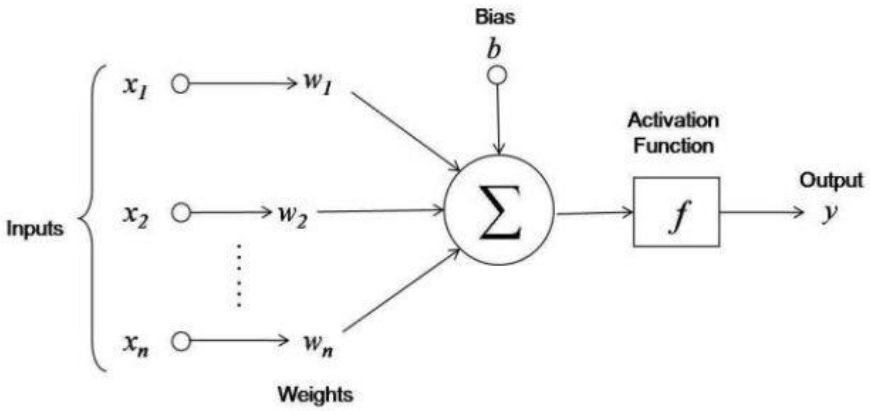
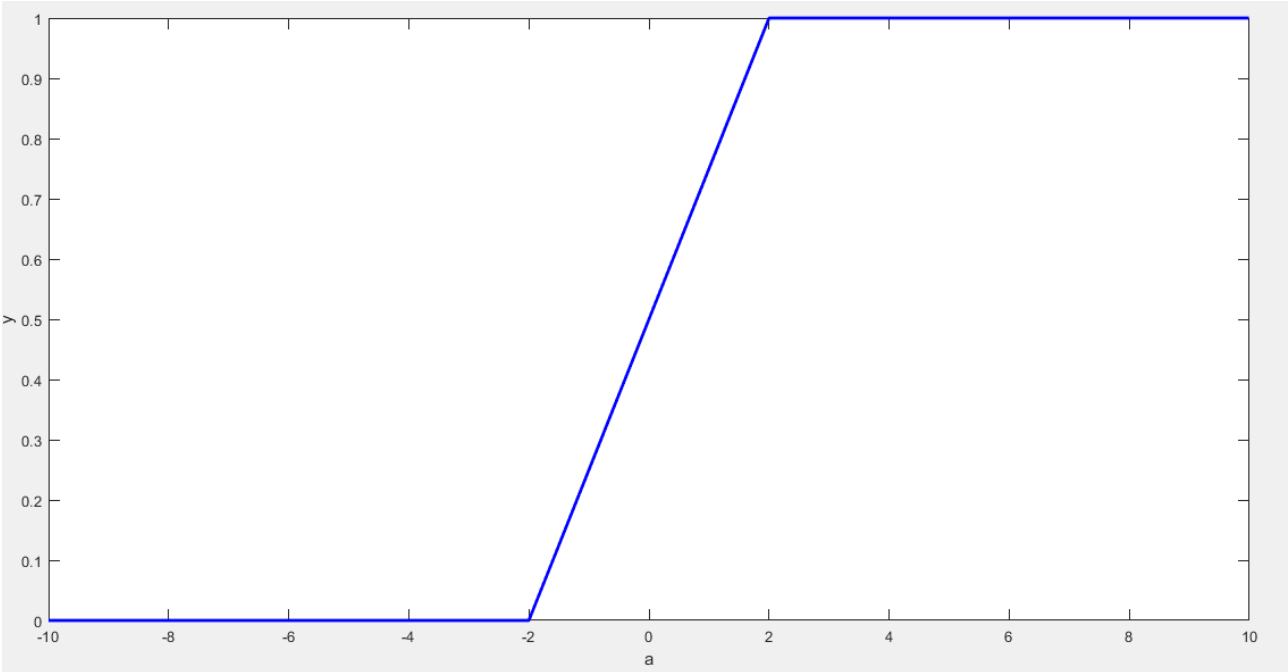



Image source: https://naadispeaks.wordpress.com/2017/11/08/artificial-neural-networks-with-net-in-azure-ml-studio/

Realize a network implementing a perceptron which takes $N_{IN} = 10$ inputs $x_n$represented by using $b_x = 8$ bit. The network carries out the products between $x_n$ and generic coefficients $w_n$ and adds the result with a bias b. $w_n$ and $b$ are represented by using $b_w = 9$ bits.
$x_n, w_n$and $b$ shall be considered in the range [-1,1].

The activation function of the perceptron shall be the one represented in the next figure:




The output of the system shall be represented by using $b_{out} = 16$ bits, truncating the least significant bits.

Final report must presents:

- Introduction (algorithm description, possible applications, possible architectures, …)
- Architecture description (block diagram, I/O interface, etc.)
- VHDL code (with detailed comments)
- Test-plan and relevant Testbenches for the functional verification of the system
- Report the power consumption, the maximum clock frequency and the resource utilization on a Zync Xilinx FPGA. Explain possible logic synthesis warning messages
- Conclusion

**Hint:** The activation function can be realized without using a look up table through a custom network which tests the amplitude of x and assigns the correct output $y$. In example, calling $a = b + \sum_{i=0}^{N_{IN}-1} w_n \cdot x_n$, when $-2 \leq a \leq 2$, the output shall be calculated through the linear function represented in figure, when $a > 2, y = 1$ and so on. By using $b_a$ bits to represent $a$, the comparison shall be realized by using the correspondent integer values of -2 and 2 in the range necessary to contain $a$. (e.g. if $a$ could be contained in the range [-4,4] for each combination of the inputs $x_n$, by using b = 10 bits, the integer representation of 2 would be: **floor(2 / lsb) = 256**, where lsb = 4 / (2^(b – 1)) = 0.0078, ).