VDD_ <u>DDR_1</u> V1											
	C28 10uF	C37 =1uF	C33 =100nF	C45 =10nF	C44 =10nF	C47 =10nF	C57 =10nF	C295	C302 10nF	C299 —10nF	C296
	6.3V,X5R C0402	10V,X5R C0402	10V,X5R C0201	16V,X7R C0201	16V,X71 C0201						
										=	<u>L</u>
VDD_DDR_1V1											
	C294	C40	C49	C67	C66	C54	C38	C29	C31	C34	C32
=	10uF 6.3V,X5R C0402	1uF 10V,X5R C0402	100nF 10V,X5R C0201	10nF 16V,X7R C0201	10nF 16V,X7 C0201						
										=	<u> </u>
VDD_IO_1V8											
L0603 2A BLM18PG121SN1D	C283	C30 =1uF	C50 100nF	C64 10nF	C65 10nF	C36 =10nF	C35 10nF	C52 10nF	C56 10nF	C60 10nF	C58 10nF
-	6.3V,X5R C0402	10V,X5R C0402	10V,X5R C0201	16V,X7R C0201	16V,X7I C0201						
										-	<u>_</u>