```
`timescale 1ns / 1ps
// Company:
// Engineer:
//
// Create Date: 2016/03/28 22:19:17
// Design Name:
// Module Name: vga
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
(* use dsp48 = "yes" *) module vga(
  input clk,
  input clk1,
  input rst,
  output reg hs,
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output reg vs,
   output [3:0] r,
   output [3:0] g,
   output [3:0] b
   );
//maximum value for the horizontal pixel counter
parameter HMAX=10'b1100100000; // 800
//maximum value for the vertical pixel counter
parameter VMAX=10'b1000001101; // 525
//total number of visible columns
parameter HLINES=10'b1010000000; // 640
// value for the horizontal counter where front porch ends
parameter HFP=10'b1010010000; // 648
//value for the horizontal counter where the synch pulse ends
parameter HSP=10'b1011110000; // 744
//total number of visible lines
parameter VLINES=10'b0111100000; // 480
// value for the vertical counter where the front porch ends
parameter VFP=10'b0111101010;
//value for the vertical counter where the synch pulse ends
parameter VSP=10'b0111101100;
//polarity of the horizontal and vertical synch pulse
// only one polarity used, because for this resolution they
coincide.
parameter SPP=1'b0;
// horizontal and vertical counters
reg [9:0] hcounter=10'b0000000000;
reg [9:0] vcounter=10'b0000000000;
```

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// active when inside visible screen area.
wire video enable ;
reg vidon;
reg [11:0] color;
reg [9:0] x zone;
reg [9:0] y zone;
reg [9:0] x center=10'b0011001000; //200
reg [9:0] y center=10'b0011001000; //200
assign r=color[11:8];
assign g=color[7:4];
assign b=color[3:0];
// increment horizontal counter at pixel_clk rate
// until HMAX is reached, then reset and keep counting
always @(posedge clk1)
begin
   if (x center <= 400)
      x center <= x center + 10;</pre>
   else
      x_center <= 200;
end
always @(posedge clk1)
begin
   if(y center <= 400)
      y center<=y center+10;</pre>
   else
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y center <= 200;
end
always @(posedge clk or posedge rst)
begin
if (rst)
    hcounter <= 10' b0000000000;
else
   if (hcounter == HMAX)
       hcounter <= 10' b0000000000;
    else
       hcounter <= hcounter+1;</pre>
end
//increment vertical counter when one line is finished
//(horizontal counter reached HMAX)
//until VMAX is reached, then reset and keep counting
always @(posedge clk or posedge rst)
begin
if (rst)
    vcounter <= 10' b0000000000;
else
      if (hcounter == HMAX)
        if(vcounter == VMAX)
           vcounter <= 10' b0000000000;
        else
           vcounter <= vcounter + 1;
end
```

```
//The HS is active (with polarity SPP) for a total of 96 pixels.
always@(posedge clk)
begin
  if((hcounter >= HFP) && (hcounter < HSP))</pre>
        hs<=SPP;
 else
        hs \le \text{SPP};
end
// The VS is active (with polarity SPP) for a total of 2 video
lines
// = 2*HMAX = 1600 pixels.
always@(posedge clk)
begin
 if((vcounter >= VFP) && (vcounter < VSP))</pre>
            vs <=SPP;
 else
            vs <= ^{\sim}SPP:
end
//enable video output when pixel is in visible area
assign video_enable=((hcounter < HLINES) && (vcounter < VLINES))?
1'b1: 1'b0;
always@(posedge clk)
begin
 vidon <= ~video_enable;</pre>
end
always @(hcounter)
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```
begin
if (hcounter<=x_center)</pre>
     x_zone=x_center-hcounter;
else
     x_zone=hcounter-x_center;
end
always@(vcounter)
begin
if(vcounter<=y_center)</pre>
     y zone=y center-vcounter;
else
     y zone=vcounter-y center;
end
always @(*)
begin
if (vidon==1'b0)
  if((x zone*x zone+y zone*y zone)<=10000)
    color=12' b110000000000;
 else
    color=12' b000111000000;
else
    color=12' b000000000000;
end
```

endmodule