

```
1  /*-----
2  REG51.H
3
4  Header file for generic 80C51 and 80C31 microcontroller.
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7  -----*/
8
9  #ifndef __REG51_H__
10 #define __REG51_H__
11
12 /* BYTE Register */
13 sfr P0    = 0x80;
14 sfr P1    = 0x90;
15 sfr P2    = 0xA0;
16 sfr P3    = 0xB0;
17 sfr PSW   = 0xD0;
18 sfr ACC   = 0xE0;
19 sfr B     = 0xF0;
20 sfr SP    = 0x81;
21 sfr DPL   = 0x82;
22 sfr DPH   = 0x83;
23 sfr PCON  = 0x87;
24 sfr TCON  = 0x88;
25 sfr TMOD  = 0x89;
26 sfr TL0   = 0x8A;
27 sfr TL1   = 0x8B;
28 sfr TH0   = 0x8C;
29 sfr TH1   = 0x8D;
30 sfr IE    = 0xA8;
31 sfr IP    = 0xB8;
32 sfr SCON  = 0x98;
33 sfr SBUF  = 0x99;
34
35
36 /* BIT Register */
37 /* PSW */
38 sbit CY    = 0xD7;
39 sbit AC    = 0xD6;
40 sbit F0    = 0xD5;
41 sbit RS1   = 0xD4;
42 sbit RS0   = 0xD3;
43 sbit OV    = 0xD2;
44 sbit P     = 0xD0;
45
46 /* TCON */
47 sbit TF1   = 0x8F;
48 sbit TR1   = 0x8E;
49 sbit TF0   = 0x8D;
50 sbit TR0   = 0x8C;
51 sbit IE1   = 0x8B;
52 sbit IT1   = 0x8A;
53 sbit IE0   = 0x89;
54 sbit IT0   = 0x88;
55
56 /* IE */
57 sbit EA    = 0xAF;
58 sbit ES    = 0xAC;
59 sbit ET1   = 0xAB;
60 sbit EX1   = 0xAA;
61 sbit ET0   = 0xA9;
62 sbit EX0   = 0xA8;
63
64 /* IP */
65 sbit PS    = 0xBC;
66 sbit PT1   = 0xBB;
67 sbit PX1   = 0xBA;
68 sbit PT0   = 0xB9;
69 sbit PX0   = 0xB8;
70
71 /* P3 */
72 sbit RD    = 0xB7;
```

```
73  sbit  WR    = 0xB6;
74  sbit  T1    = 0xB5;
75  sbit  T0    = 0xB4;
76  sbit  INT1  = 0xB3;
77  sbit  INT0  = 0xB2;
78  sbit  TXD   = 0xB1;
79  sbit  RXD   = 0xB0;
80
81  /*  SCON  */
82  sbit  SM0    = 0x9F;
83  sbit  SM1    = 0x9E;
84  sbit  SM2    = 0x9D;
85  sbit  REN    = 0x9C;
86  sbit  TB8    = 0x9B;
87  sbit  RB8    = 0x9A;
88  sbit  TI     = 0x99;
89  sbit  RI     = 0x98;
90
91  #endif
92
```