IC Design

Homework # 2

Due on 11/6/2012, 9:10AM in class

✧ Plagiarism is not allowed. 10% penalty for each day of delay.

✧ Any further questions, you can leave messages on the board of the class website or send e-mail to the TA

In this homework, you will learn the following:

- Cadence tool;
- Nanosim;
- SPICE language;
- nWave.

Three of the following cells are assigned to each of you. Everyone must do cells （10）, and （11）. Those whose student ID end with '*k*' must also do cell *k*.

(0) EO3
(1) ND2
(2) EO
(3) AN2
(4) NR2
(5) AN3
(6) DRIVER
(7) IV
(8) EN
(9) OR2
(10) FD2
(11) FA1

For each cell,

a. Base on the layout view, draw transistor-level and gate-level circuit diagrams (using Visio or 小畫家)

b. Identify all inputs and outputs

c. List truth table

d. Revise the given netlist file to assemble your cells. All PMOS transistors have width 0.9um and length 0.18um. All NMOS transistors have width

0.45um and length 0.18um. Parameters of 0.18um model file (nn018.l) must be included during the simulation. The substrate of PMOS is connected to V_{DD}, on the contrary, the substrate of NMOS is connected to V_{SS}.

e. Run *Nanosim* simulation on all possible input combinations. Assume V_{DD}=1.8V and V_{SS}=0V. Use *nWave* to verify the truth table. Copy the I/O waveform to your report. State what you have observed.

f. Please discuss problems you have encountered.

Files that you will need (available on the class website)

HW2_2012.rar includes the following files

- HW2.pdf (this document)
- sample_netlist

References (available on the class website)

[1] HW2 tutorial

[2] "SPICE," CIC handout, 2001

[3] "鳥哥的 Linux 私房菜," http://linux.vbird.org/

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HW2 Office hours: 11/2 19:00-21:00

11/5 19:00-21:00

If you have no time at office hours, you can email TA to discuss another time for appointment.