IC Design

Homework # 3

Due on 12/04/2012, 9:10AM in class,
10% penalty for each day of delay

- ❖ Plagiarism is not allowed.
- ➢ Any further questions, you can search the solutions on the PTT "ICDESIGN" board or send e-mail to the TA:
  b96901055@ntu.edu.tw or r00943118@ntu.edu.tw .
  HW3 Office hours: 11/30 19:00-21:00
  12/03 19:00-21:00
  If you have no time at office hours, you can email TA to discuss another time for appointment.

Specifications

In this homework, you are asked to design a gate-level combinational circuit that finds the minimum among five given numbers. The inputs of this circuit are **five distinct 6-bit unsigned** digital values, denoted as *i0*, *i1*, *i2*, *i3*, *i4*. The output of the circuit, denoted as *min*, is a **3-bit number** that indicates which one is the minimum. The relationship between input and output is listed as follows:

- ➢ If *i0* is the minimum, *min* will be 3'b000.
- ➢ If *i1* is the minimum, *min* will be 3'b001.
- ➢ If *i2* is the minimum, *min* will be 3'b010.
- ➢ If *i3* is the minimum, *min* will be 3'b011.
- ➢ If *i4* is the minimum, *min* will be 3'b100.

Following are some examples of the I/O:

Input					Output
i0	*i1*	*i2*	*i3*	*i4*	*min*
101101	010010	000011	111100	101111	010
000111	000010	011100	111011	000000	100
000011	111111	010101	101010	111000	000

There are some important things that you should notice:

- ➢ Your design should base on the **standard cells in the lib.v**. All logic operations in your design **MUST consist of the standard cells** instead of using the operands such as "+", "-", "&", "|", ">", and "<".
- ➢ Design your homework in the given "Comparator_51.v" file. **You are NOT**

ALLOWED to change the filename and the header of the top module (i.e. the module name and the I/O ports).

- If your design contains more than one module, don't create new file for them, just put those modules in "Comparator_51.v."
- You don't need to consider the situation of two or more identical minimums. The five given numbers are always different.
- The output waveform will be dumped to file "**Comparator_51.fsdb."** You can use nWave to examine it.

Grading

1. Gate-level design using Verilog (70%)

Your score will depend on both the correctness and performance of your design. We provide a test bench which automatically grades your design. Following is the grading policy:

Correctness & Performance	Score
Fail to pass the test bench.	40 * (1-err #/1000)
Functionally correct	40
Critical path < 10ns	45
Critical path < 7ns	50
Critical path < 6ns	55
Critical path < 5ns	60
Critical path < 4ns	65
Critical path < 3ns	70
Using operands, not standard cell logic	0
Plagiarism	0

2. Report (30%) You should also introduce and discuss about your design. Following are some requirements of your report.

- Circuit diagram (15%)
  Plot the circuit diagram of your design. You are encouraged to plot it hierarchically so that the reader can understand your design easily.
- Discussion (15%)
  Discuss about your design. For example, introduce you design, how do you do the comparison, which technique is adopted in your design, how do you improve your critical path.
- You have to put the simulation result in your report. Ex:

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Congratulations! Your score is 70!
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- You also have to put your Verilog code (Comparator_51.v) in your report.

Notification

- Following are the files you will need (available on the class website)
  HW3.rar includes
  - **hw3.pdf** : this document.
  - **Comparator_51.v**:
    Dummy design file. Program the design in this file.
    The header of the top module and the declaration of the I/O ports are predefined in this file and you are not allowed to change them.
  - **lib.v**: standard cells.
  - **tb_Comparator_51.v**:
    Test bench for your design.
  - **in0.dat, in1.dat, in2.dat, in3.dat, in4.dat**:
    Input patterns for test bench. Please put these files in the folder that contains tb_Comparator_51.v when doing simulation.
  - **answer.dat**:
    Output patterns of correct answers for test bench. Please put the file in the folder that contains tb_Comparator_51.v when doing simulation.
- You also should compress the following files into a single RAR file, and then E-mail your RAR file to **tonychopperchu@gmail.com** (this e-mail account is only for homework submission) before the deadline.
  (1) Report (PDF format)
  (2) Comparator_51.v

  - Filename rule: *hw3_(student id)_v#.rar*
    Ex. hw3_b99901001_v1.rar
    hw3_b99901001_v2.rar
  - Subject (title of the email):
    [IC design] hw3_(student id)_v#,
    Ex. [IC design] hw3_b99901001_v1.
    Other subjects will not be accepted.