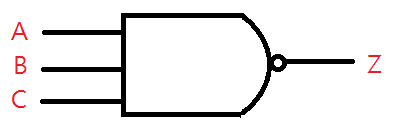
Cell name:ND3

(a)

Transistor-level circuit diagram



Gate-level circuit diagram



(b)

Input: A B C

Output: Z

(C)

Truth table

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | C | Z |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

(d)

.subckt ND3 Z A B C

MN0 Z C n01 gnd n w=0.45u l=0.18u

MN2 n12 A gnd gnd n w=0.45u l=0.18u

MN1 n01 B n12 gnd n w=0.45u l=0.18u

MP0 Z A vdd vdd p w=0.9u l=0.18u

MP1 Z B vdd vdd p w=0.9u l=0.18u

MP2 Z C vdd vdd p w=0.9u l=0.18u

.ends ND3

(e)

Waveform

從上到下分別為A B C Z

