R04943133
電子一
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MSOC HW2 Report

1-1

The interchange unit uses direct_read() and direct_write() functions to pass the pointer to its local memory.

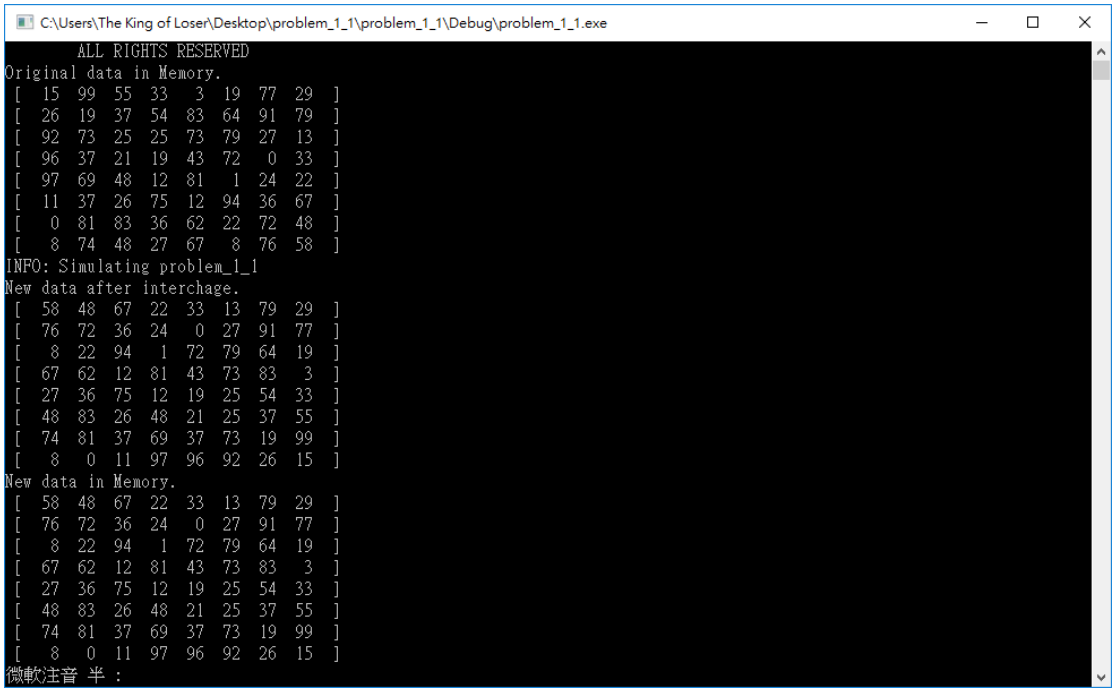
```
class mem_if: virtual public sc_interface {
public:
    //Functional model
    virtual void direct_read (int** block) = 0;
    virtual void direct_write(int** block) = 0;
```

```
SC_MODULE(interchange){
    sc_port<mem_if> m_mem;

    SC_HAS_PROCESS(interchange);
    interchange(sc_module_name _name);

    void interchange_thread();

private:
    int **mem_inter;
};
```

```
void interchange::interchange_thread(){
    m_mem->direct_read(mem_inter);
```

```
    //write back
    m_mem->direct_write(mem_inter);
    m_mem->notify();


}
```

將記憶體位置的 pointer 傳入 interchange 做運算



1-2

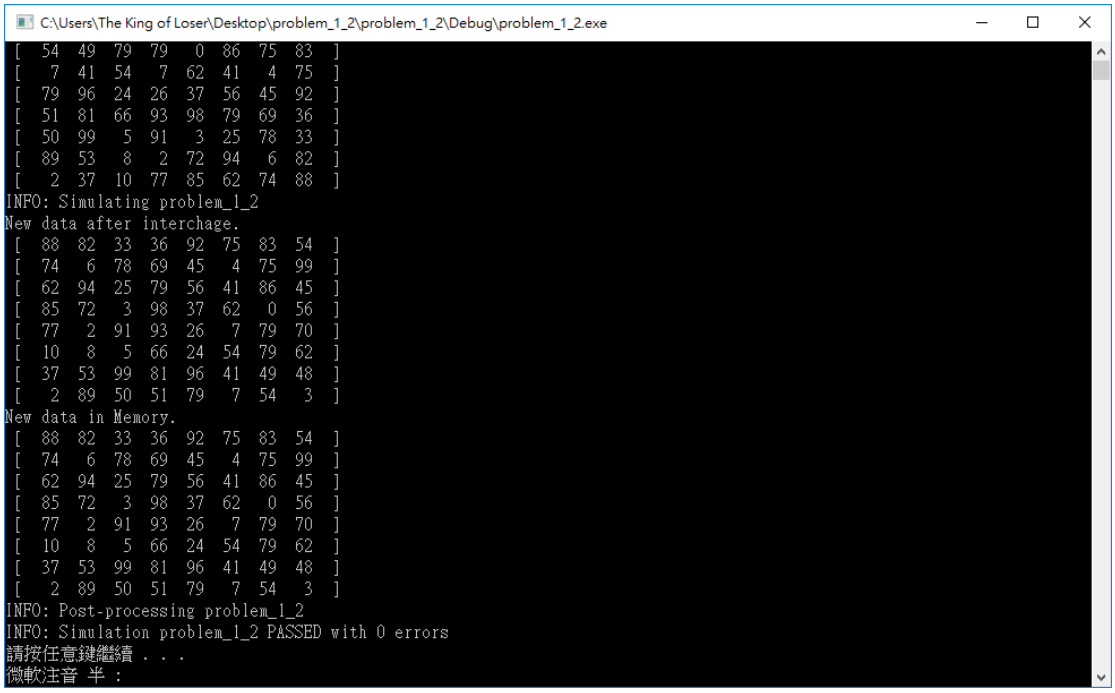
The interchange unit uses word_read() and word_write() functions to copy data from and to memory. You may use delay notification to model the timing in interchange unit or channel.

```
class mem_if: virtual public sc_interface {
public:
    //Functional model
    //virtual void direct_read (int** block) = 0;
    //virtual void direct_write(int** block) = 0;

    virtual void word_read(unsigned x, unsigned y, int& d) = 0;
    virtual void word_write(unsigned x, unsigned y, int d) = 0;

    //delay notification
    virtual void notify() = 0;
    virtual const sc_event& default_event() const = 0;
};
```

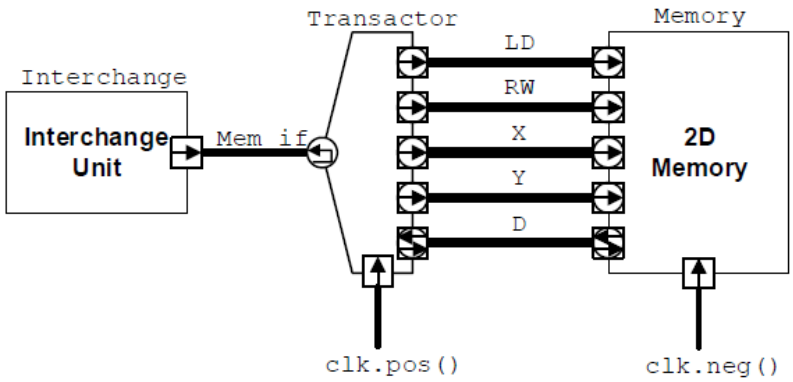
```
void interchange::interchange_thread(){
    //m_mem->direct_read(mem_inter);
    for(int i = 0; i < 8; i++){
        for(int j = 0; j < 8; j++){
            m_mem->word_read(i, j, mem_inter[i][j]);
        }
    }
```

```
    //write back
    //m_mem->direct_write(mem_inter);
    for(int i = 0; i < 8; i++){
        for(int j = 0; j < 8; j++){
            m_mem->word_write(i, j, mem_inter[i][j]);
        }
    }
    m_mem->notify();

}
```

一次只從 memory 中讀取一個值或存取一個值，透過 notify()通知 memory 資料已寫入完畢。



2-1



```
SC_MODULE(transactor), mem_if{
    sc_in_clk          clk;
    sc_out<bool>       LD;
    sc_out<bool>       RW;
    sc_out<unsigned>   X;
    sc_out<unsigned>   Y;
    sc_inout_rv<32>    D;
```

```
void transactor::word_read(unsigned x, unsigned y, int& d)
{
    wait(clk->posedge_event());
    LD->write(true);
    RW->write(true);
    X->write(x);
    Y->write(y);
    wait(clk->posedge_event());
    LD->write(false);
    d = D->read().to_long();
}

void transactor::word_write(unsigned x, unsigned y, int d)
{
    wait(clk->posedge_event());
    LD->write(true);
    RW->write(false);
    X->write(x);
    Y->write(y);
    D->write(d);
    wait(clk->posedge_event());
    LD->write(false);
}
```

```
SC_MODULE(memory) {
    sc_in_clk        clk;
    sc_in<bool>      LD;
    sc_in<bool>      RW;
    sc_in<unsigned>  X;
    sc_in<unsigned>  Y;
    sc_inout_rv<32>  D;

    SC_HAS_PROCESS(memory);
```

```
C:\Users\The King of Loser\Desktop\problem_2_1\problem_2_1\Debug\problem_2_1.exe
[   7  84  37  88  21  89  90  88  ]
[  67  93  79  50  57  20  23  47  ]
[  21  95  42  33  13   7  20  59  ]
[  81  61  69  37  67  75  21  61  ]
[  82  86   5  50  37  14  47  88  ]
[  76   5  99  52  11   0  75  98  ]
[  62  78  97  96  41  90  81  72  ]
INFO: Simulating problem_2_1
New data after interchage.
[  72  98  88  61  59  47  88  99  ]
[  81  75  47  21  20  23  90   5  ]
[  90   0  14  75   7  20  89  20  ]
[  41  11  37  67  13  57  21  76  ]
[  96  52  50  37  33  50  88  83  ]
[  97  99   5  69  42  79  37   2  ]
[  78   5  86  61  95  93  84  26  ]
[  62  76  82  81  21  67   7  85  ]
New data in Memory.
[  72  98  88  61  59  47  88  99  ]
[  81  75  47  21  20  23  90   5  ]
[  90   0  14  75   7  20  89  20  ]
[  41  11  37  67  13  57  21  76  ]
[  96  52  50  37  33  50  88  83  ]
[  97  99   5  69  42  79  37   2  ]
[  78   5  86  61  95  93  84  26  ]
[  62  76  82  81  21  67   7  85  ]
INFO: Post-processing problem_2_1
INFO: Simulation problem_2_1 PASSED with 0 errors
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```
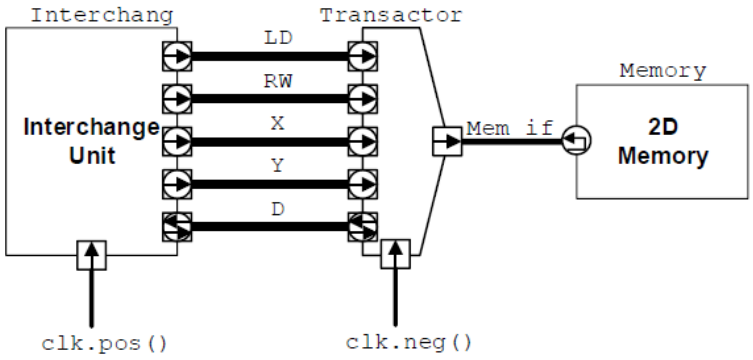

2-2




```
SC_MODULE(interchange){
    //sc_port<mem_if>   m_mem;
    sc_in_clk         clk;
    sc_out<bool>      LD;
    sc_out<bool>      RW;
    sc_out<unsigned>  X;
    sc_out<unsigned>  Y;
    sc_inout_rv<32>   D;
```

```
SC_MODULE(transactor){
    sc_in_clk         clk;
    sc_in<bool>       LD;
    sc_in<bool>       RW;
    sc_in<unsigned>   X;
    sc_in<unsigned>   Y;
    sc_inout_rv<32>   D;
    sc_port<mem_if>   m_mem;
```

```
C:\Users\The King of Loser\Desktop\problem_2_2\problem_2_2\Debug\problem_2_2.exe
[  93  88  40  55  76  56   6  65  ]
[  64  92  33  99  84   0  10  38  ]
[  40  10  89  22  32  80  27  15  ]
[  61  70  90  86  78  31  89   0  ]
[  87  68   9  84  18  47  60  99  ]
[  56  56  88  37  23  14   8  29  ]
[  19  88   1  90  17  85   7  44  ]
INFO: Simulating problem_2_2
New data after interchage.
[  44  29  99   0  15  38  65  23  ]
[   7   8  60  89  27  10   6  39  ]
[  85  14  47  31  80   0  56  55  ]
[  17  23  18  78  32  84  76  70  ]
[  90  37  84  86  22  99  55  22  ]
[   1  88   9  90  89  33  40   1  ]
[  88  56  68  70  10  92  88  18  ]
[  19  56  87  61  40  64  93  37  ]
New data in Memory.
[  44  29  99   0  15  38  65  23  ]
[   7   8  60  89  27  10   6  39  ]
[  85  14  47  31  80   0  56  55  ]
[  17  23  18  78  32  84  76  70  ]
[  90  37  84  86  22  99  55  22  ]
[   1  88   9  90  89  33  40   1  ]
[  88  56  68  70  10  92  88  18  ]
[  19  56  87  61  40  64  93  37  ]
INFO: Post-processing problem_2_2
INFO: Simulation problem_2_2 PASSED with 0 errors
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```
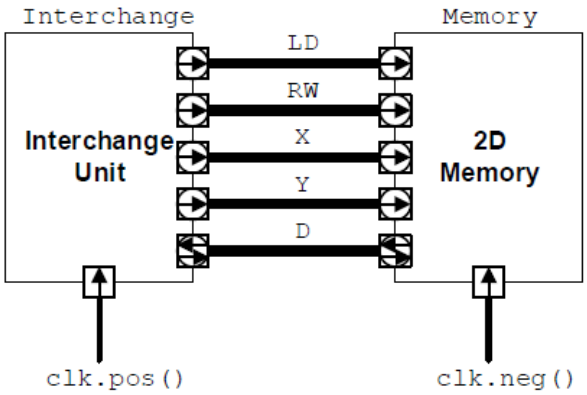
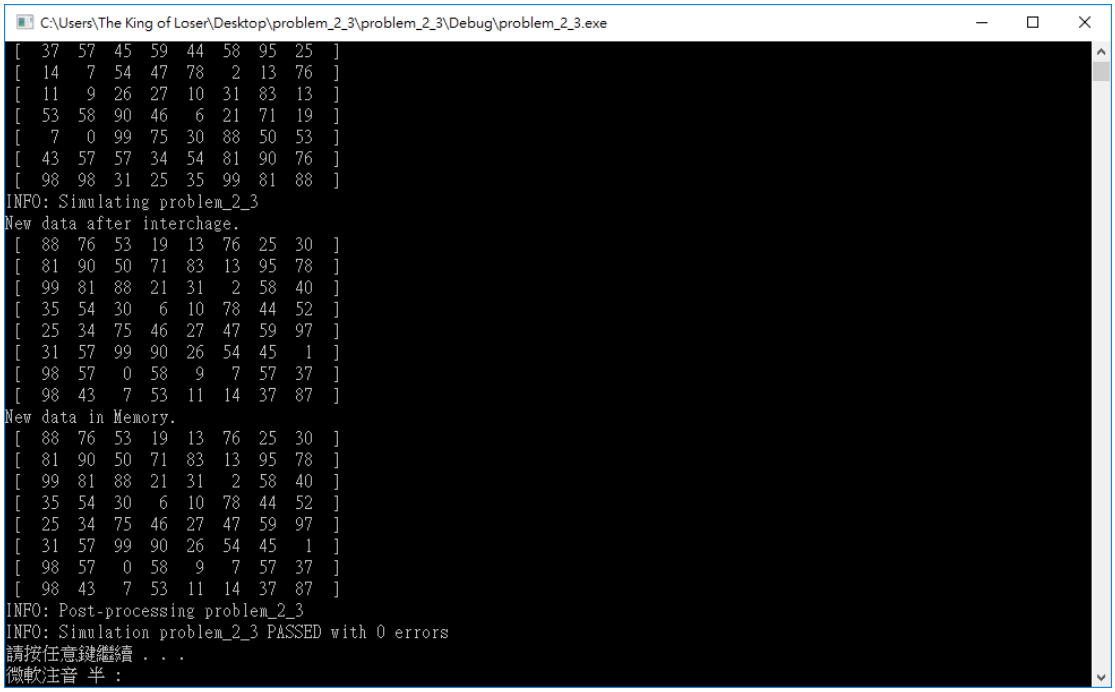

2-3




```
SC_MODULE(interchange){
    //sc_port<mem_if>   tran_mem;
    sc_in_clk          clk;
    sc_out<bool>       LD;
    sc_out<bool>       RW;
    sc_out<unsigned>   X;
    sc_out<unsigned>   Y;
    sc_inout_rv<32>    D;
```

```
SC_MODULE(memory){
    sc_in_clk          clk;
    sc_in<bool>        LD;
    sc_in<bool>        RW;
    sc_in<unsigned>    X;
    sc_in<unsigned>    Y;
    sc_inout_rv<32>    D;
```


C:\Users\The King of Loser\Desktop\problem_2_3\problem_2_3\Debug\problem_2_3.exe
[37 57 45 59 44 58 95 25]
[14 7 54 47 78 2 13 76]
[11 9 26 27 10 31 83 13]
[53 58 90 46 6 21 71 19]
[7 0 99 75 30 88 50 53]
[43 57 57 34 54 81 90 76]
[98 98 31 25 35 99 81 88]
INFO: Simulating problem_2_3
New data after interchage.
[88 76 53 19 13 76 25 30]
[81 90 50 71 83 13 95 78]
[99 81 88 21 31 2 58 40]
[35 54 30 6 10 78 44 52]
[25 34 75 46 27 47 59 97]
[31 57 99 90 26 54 45 1]
[98 57 0 58 9 7 57 37]
[98 43 7 53 11 14 37 87]
New data in Memory.
[88 76 53 19 13 76 25 30]
[81 90 50 71 83 13 95 78]
[99 81 88 21 31 2 58 40]
[35 54 30 6 10 78 44 52]
[25 34 75 46 27 47 59 97]
[31 57 99 90 26 54 45 1]
[98 57 0 58 9 7 57 37]
[98 43 7 53 11 14 37 87]
INFO: Post-processing problem_2_3
INFO: Simulation problem_2_3 PASSED with 0 errors
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