homework1

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1 Q1.Cost and Price

a)

$$\text{Dies per wafer} = \frac{\pi \times (300/2)^2}{389} - \frac{\pi \times 300}{\sqrt{2 \times 389}} = 148$$

b)

$$\text{Die yield} = 1 \times \left(1 + \frac{0.3 \times 3.89}{4}\right)^{-4} = 0.36$$

c)

$$\text{Cost of die} = \frac{\$1000}{148 \times 0.36} = \$18.77$$

$$\text{Cost per old chip} = \$18.77 + \$20 = \$38.77$$

d)

$$\text{Dies per wafer} = \frac{\pi \times (300/2)^2}{186} - \frac{\pi \times 300}{\sqrt{2 \times 186}} = 331$$

e)

$$\text{Die yield} = 1 \times \left(1 + \frac{0.7 \times 1.86}{4}\right)^{-4} = 0.32$$

f)

$$\text{Cost of die} = \frac{\$1000}{331 \times 0.32} = \$9.44$$

$$\text{Cost per new chip} = \$9.44 + \$20 = \$29.44$$

g)

$$\text{Price per old chip} = \$38.77 \times (1 + 40\%) = \$54.28$$

h)

$$\text{Price per new chip} = \$54.28 \times 2 = \$108.56$$

$$\text{Difference} = \$108.56 - \$29.44 = \$79.125$$

i)

$$\frac{\$1.5 \times 10^9}{(79.125 \times 0.5) \times (5 \times 10^5 \times 3)} = 25 \text{ (months)}$$

2 Q2.Performance Metrics

a)

$$\text{CPI}_{\text{overall}} = 5 \times 55\% + 4 \times 30\% + 4 \times 15\% = 4.55$$

b)

$$\text{CPI}_{\text{overall}} = \frac{5 \times 55\% \times 75\% + 4 \times 30\% \times 95\% + 6 \times 15\%}{55\% \times 75\% + 30\% \times 95\% + 15\%} = 4.84$$

c) Old processor, instructions per second:

$$\frac{1\text{GHz}}{4.55} = 2.20 \times 10^8 \ (s^{-1})$$

New processor, instructions per second:

$$\frac{600\text{MHz}}{4.84} = 1.24 \times 10^8 \ (s^{-1})$$

$$\frac{2.20 \times 10^8}{1.24 \times 10^8 \div (55\% \times 75\% + 30\% \times 95\% + 6 \times 15\%)} \times 100\% - 1 = 50\%$$

So the new one runs slower.It needs 50% more time than the old one.

3 Q3.Amdahl' s Law

a)

$$200 \times 30\% + \frac{200 \times 60\%}{x} + 200 \times 10\% = \frac{200}{2}$$

$$x = 6$$

It should be enhanced by 6 times.

b)

$$\frac{200 \times 30\%}{x} + 200 \times 60\% + 200 \times 10\% = \frac{200}{2}$$

$$x = -1.5$$

It's impossible.

c)

$$200 \times 30\% \times 1.2 + \frac{200 \times 60\%}{5} + 200 \times 10\% = 116\ (s)$$

$$\text{speedup} = 200/116 = 1.72$$

4 Q4. Pipelining

a) (Please zoom in.)

	t0	t1	t2	t3	t4	t5	t6	t7	t8	t9	t10	t11	t12	t13	t14	t15	t16	t17	t18	t19	t20	t21
lw R10, X(R20)	IF	ID	EX	MA	WB																	
lw R11, Y(R20)		IF	ID	EX	MA	WB																
subu R10, R10, R11			IF	ID	ID	EX	MA	WB														
sw Z(R20), R10				IF	IF	ID	EX	MA	WB													
addiu R20, R20, 4						IF	ID	EX	MA	WB												
subu R5, R23, R20							IF	ID	EX	MA	WB											
bnez R5, LOOP								IF	ID	EX	MA	WB										
nop									IF	ID												
lw R10, X(R20)											IF	ID	EX	MA	WB							
lw R11, Y(R20)												IF	ID	EX	MA	WB						
subu R10, R10, R11													IF	ID	ID	EX	MA	WB				
sw Z(R20), R10														IF	IF	ID	EX	MA	WB			
addiu R20, R20, 4																IF	ID	EX	MA	WB12		
subu R5, R23, R20																	IF	ID	EX	MA13	WB13	
bnez R5, LOOP																		IF	ID	EX	MA	WB
nop																			IF	ID		

Cycles = 22

	t0	t1	t2	t3	t4	t5	t6	t7	t8	t9	t10	t11	t12	t13	t14	t15	t16	t17	t18	t19	t20	t21	t22	t23	t24	t25	t26	t27	t28	t29	t30	t31	t32	t33	t34	t35	t36	t37	t38
lw R10, X(R20)	IF1	IF2	ID	RF	EX1	EX2	M1	M2	WB																														
lw R11, Y(R20)		IF1	IF2	ID	RF	EX1	EX2	M1	M2	WB																													
subu R10, R10, R11			IF1	IF2	ID	RF	RF	RF	RF	EX1	EX2	M1	M2	WB																									
sw Z(R20), R10				IF1	IF2	ID	ID	ID	ID	RF	RF	EX1	EX2	M1	M2	WB																							
addiu R20, R20, 4					IF1	IF2	IF2	IF2	IF2	ID	ID	RF	EX1	EX2	M1	M2	WB																						
subu R5, R23, R20						IF1	IF1	IF1	IF1	IF2	IF2	ID	RF	RF	EX1	EX2	M1	M2	WB																				
bnez R5, LOOP										IF1	IF1	IF2	ID	ID	RF	RF	EX1	EX2	M1	M2	WB																		
nop												IF1	IF2	IF2	ID	ID	RF	EX1																					
nop													IF1	IF1	IF2	IF2	ID	RF																					
nop															IF1	IF1	IF2	ID																					
nop																	IF1	IF2																					
nop																		IF1																					
lw R10, X(R20)																			IF1	IF2	ID	RF	EX1	EX2	M1	M2	WB											
lw R11, Y(R20)																				IF1	IF2	ID	RF	EX1	EX2	M1	M2	WB										
subu R10, R10, R11																					IF1	IF2	ID	RF	RF	RF	RF	EX1	EX2	M1	M2	WB						
sw Z(R20), R10																						IF1	IF2	ID	ID	ID	ID	RF	RF	EX1	EX2	M1	M2	WB				
addiu R20, R20, 4																							IF1	IF2	IF2	IF2	IF2	ID	ID	RF	EX1	EX2	M1	M2	WB			
subu R5, R23, R20																								IF1	IF1	IF1	IF1	IF2	IF2	ID	RF	RF	EX1	EX2	M1	M2	WB	
bnez R5, LOOP																												IF1	IF1	IF2	ID	RF	RF	RF	EX1	EX2	M1	M2	WB
nop																														IF1	IF2	IF2	ID	ID	RF	EX1			
nop																															IF1	IF1	IF2	IF2	ID	RF			
nop																																	IF1	IF1	IF2	ID			
nop																																			IF1	IF2			
nop																																				IF1			

b) Pipeline branch delay=5
Pipeline load delay=3
cycles=39

5 Q5. Pipeline Hazards

	Dependence type	Independent instruction	Dependent instruction	Storage loaction
1	RAW	1(LD)	2(DADD)	R1
2	RAW	1(LD)	2(DSUB)	R1
3	RAW	1(LD)	3(OR)	R1
4	WAW	1(LD)	3(OR)	R1
5	RAW	2(DADD)	5(BENZ)	R7
6	WAR	1(LD)	7(XOR)	R2
7	WAR	2(DADD)	4(OR)	R1
8	WAR	3(DSUB)	4(OR)	R1

6 Q6. Scoreboarding

Instruction	j	k	Issue	Read Operand	Exection Complete	Wirte Result
LD F6	12+	R2	1	2	3	4
LD F2	16+	R3	5	6	7	8
ADDD F0	F2	F4	6	9	13	14
DIVD F10	F0	F6	7	15	39	40
SUBD F8	F6	F2	8	10	14	15
ADDI R2	R2	8	9	10	11	12
ADDI R3	R3	16	10	11	12	13
ADDD F6	F8	F2	11	16	20	21

7 Q7. SimpleScalar Assignment

Alpha-ISA

1. Anagram
   instruction statistics

	number
total instructions	25597558
load	6491600
store	2541971
uncond branch	1142226
cond branch	2636148
int computation	11423189
fp computation	1360117
trap	2306

top ten popular instructions

ldq a,o(b)	3846907
bis a,b,c	3069934
lda a,o(b)	2239880
stq a,o(b)	1898540
ldq_u a,o(b)	1499766
bne a,j	1347550
ldl a,o(b)	1140459
beq a,j	1011528
and a,i,c	459418
extbl a,b,c	435402

address modes

(const)	0
(gp + const)	257197
(sp + const)	3655988
(fp + const)	351885
(reg + const)	4768501
(reg + reg)	0

2. cc1
instruction statistics

	number
total instructions	337341100
load	83205322
store	38693114
uncond branch	13903378
cond branch	44969505
int computation	156184435
fp computation	374706
trap	10639

top ten popular instructions

ldq a,o(b)	56431106
stq a,o(b)	30225830
bis a,b,c	26866535
lda a,o(b)	21998244
beq a,j	20023124
bne a,j	18657564
ldl a,o(b)	18335854
xor a,i,c	14492445
zapnot a,i,c	9350554
ldah a,o(b)	8688777

address modes

(const)	0
(gp + const)	5432011
(sp + const)	55349931
(fp + const)	5405499
(reg + const)	55710995
(reg + reg)	0

3. compress95
instruction statistics

	number
total instructions	88124
load	1395
store	69828
uncond branch	171
cond branch	5034
int computation	11681
fp computation	0
trap	14

top ten popular instructions

stq a,o(b)	69645
subq a,i,c	8683
bge a,j	4365
ldq a,o(b)	991
bis a,b,c	607
addq a,b,c	384
subl a,i,c	323
lda a,o(b)	307
addq a,i,c	294
bgt a,j	256

address modes

(const)	0
(gp + const)	457
(sp + const)	521
(fp + const)	0
(reg + const)	70245
(reg + reg)	0

4. go
instruction statistics

	number
total instructions	545811932
load	167116107
store	44574321
uncond branch	14108462
cond branch	59795840
int computation	260042139
fp computation	174876
trap	186

top ten popular instructions

ldl a,o(b)	114615427
s4addq a,b,c	77675978
lda a,o(b)	57613261
ldq a,o(b)	38312514
stl a,o(b)	33307727
bis a,b,c	29821626
bne a,j	29736672
beq a,j	25769595
ldah a,o(b)	15332408
ldq_u a,o(b)	14187820

address modes

(const)	0
(gp + const)	33308946
(sp + const)	81429406
(fp + const)	3248690
(reg + const)	93703386
(reg + reg)	0