# NATIONAL TSING HUA UNIVERSITY
## DEPARTMENT OF COMPUTER SCIENCE
## CS 4100: Computer Architecture
## Spring 2021, Final Examination

1. (20%) Consider the I-type instruction: `addi`.
   (a) (5%) What additional logic blocks, if any, are needed for the five-stage pipelined processor to correctly execute an `addi` instruction?
   (b) (7%) What are the values of the signals generated by the Control unit when executing an `addi` instruction on the five-stage pipelined processor given in (a)?
   (c) (8%) How many bits should the EX/MEM pipeline register contain? Give your reasons.

2. (10%) Draw a diagram to show where the branch predictor and branch target predictor should be placed in the five-stage pipelined processor. Explain how your design works to fetch the instruction from the predicted branch target address in the next cycle.

3. (20%) Consider the execution of the following sequence of four instructions on the five-stage pipelined processor:

```
sub x10, x11, x12
add x11, x6, x12
beq x11, x12, LABEL
sd x11, 0(x12)
```

   Suppose the third instruction (`beq`) is detected to have a TLB miss in the IF stage (i.e., in clock cycle 3), causing an exception.
   (a) (4%) What instructions will appear in the IF, ID, EX, and MEM stages, respectively, in clock cycle 4? Note that each instruction in your answer should be one chosen from the given four instructions, the NOP instruction (or bubble), and the first instruction of the exception handler.
   (b) (4%) What value will be stored in the SEPC (Supervisor Exception Program Counter) at the end of clock cycle 3?
   (c) (4%) Suppose in clock cycle 4, an ALU malfunction exception occurs. What instructions will appear in the IF, ID, EX, and MEM stages, respectively, in clock cycle 5?
   (d) (4%) What value will be stored in the SEPC (Supervisor Exception Program Counter) at the end of clock cycle 4?
   (e) (4%) If (d) should occur, what happen to the TLB miss exception in (a)? When will that exception be handled, assuming the ALU malfunction can be fixed in the exception handler and the program can be restarted?

4. (5%) Show all your work to determine whether 100101000101 is a correct 12-bit Hamming single error correcting code word or not. If it is an incorrect code word, you also need to correct it.

5. (11%) Consider a processor with one level of cache. Assume that the cache has the hit time of 2 clock cycles, each main memory access (including all the miss handling) takes 100 clock cycles, and the average memory access time (AMAT) per instruction is 22 clock cycles. **Show all your work when answering the following questions.**
   (a) (3%) What is the cache miss rate per instruction?
   (b) (4%) Suppose you want to reduce the AMAT per instruction to 10 clock cycles by adding a second-level cache. If the hit time of the second-level cache takes 15 clock cycles, what is the local miss rate per instruction of the second-level cache?

(c) (4%) Given the two-level cache system in (b), suppose you want to further reduce the AMAT per instruction to 8 clock cycles or lower by adding a third-level cache. For the third-level cache, if it has a local miss rate of 30%, what is the largest hit time it can have?

6. (6%) Suppose you are designing a direct-mapped cache of a fixed capacity and considering one of the following two possible configurations: (i) more data elements per block but fewer blocks; (ii) fewer data elements per block but more blocks.

   (a) (4%) Give one advantage and one disadvantage of each configuration.
   (b) (2%) Which configuration is a better choice if there is a very high frequency of accessing data in consecutive memory addresses? Why?

7. (12%) Given that each memory address consists of 32 bits and stores a byte, consider a 64 KiB (1 KiB = 1024 bytes) cache. **Show all your work when answering the following questions.**

   (a) (3%) Assume that the cache is a fully associative cache with 64-byte blocks and a write back policy is used. Compute the total number of bits required to store the valid, dirty, and tag bits in the cache.
   (b) (3 points) Assume that the cache is a 4-way set associative cache with 32-byte blocks. For each memory address, how many bits are respectively used for the tag, index, and (block and byte) offset?
   (c) (2%) Assume that the cache is an N-way set associative cache and each memory address is divided into 4 bits of (block and byte) offset, 11 bits of index, and 17 bits of tag. What is N?
   (d) (4%) Given the cache in (c), if the two different memory addresses $0553FF0F_{16}$ and $0099\boldsymbol{y}F02_{16}$ are assigned to the same cache set, what hexadecimal digit can $\boldsymbol{y}$ be? You must give all possible values for $\boldsymbol{y}$.

8. (16%) Consider a byte-addressable virtual memory system. Each virtual address has 16 bits, each page has 4KiB, and the main memory has 32KiB. Each process has a single-level page table, and for each page table entry, 5 bits are reserved for the operating system functions (valid, reference, dirty, etc.) and the other bits are used to store a physical page number. Note that the disk addresses of all virtual pages of a process are stored in another data structure which is separate from the page table. **Show all your work when answering the following questions.**

   (a) (2%) What is the maximum size (in bytes) of virtual memory that a process can have?
   (b) (2%) What is the maximum number of virtual pages that a process can have?
   (c) (2%) How many bits are required for each page table entry?
   (d) (2%) What is the maximum size (in bytes) that a page table can have?
   (e) (3%) Assume that each process has a page table of maximum size and 25% of the main memory is allocated for storing page tables. What is the maximum number of page tables that can reside in the main memory?
   (f) (5%) Suppose this virtual memory system has a TLB with the following characteristics:
      - The TLB is a fully associative cache with 4 entries.
      - Each entry of the TLB has a valid bit, a dirty bit, a tag, and a physical page number.

      Determine the total number of bits in the TLB.