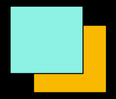
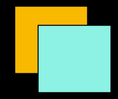
Vivado FPGA Guide

9/23/2021



NTHU Logic Design Laboratory (Fall. 2021)



By Prof. Chun-Yi Lee

Agenda

Overview

Preparation

Generate Bit Stream

Design Verification on FPGA

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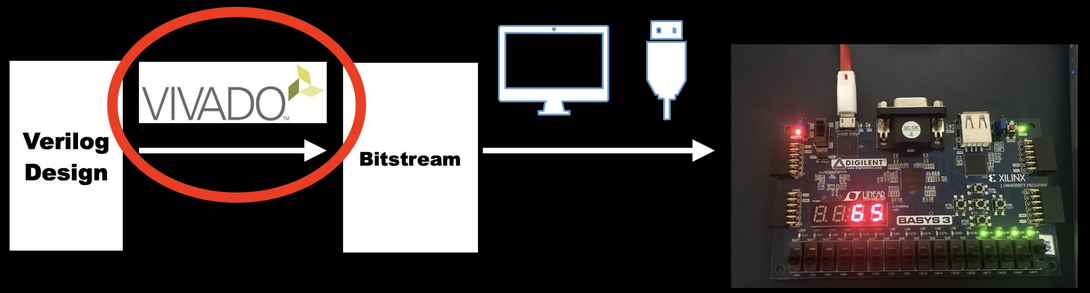
Overview (1/1)

- To program our verilog design into the FPGA, it first needs to be turn into Bitstream
- Done with the help from ***Vivado***



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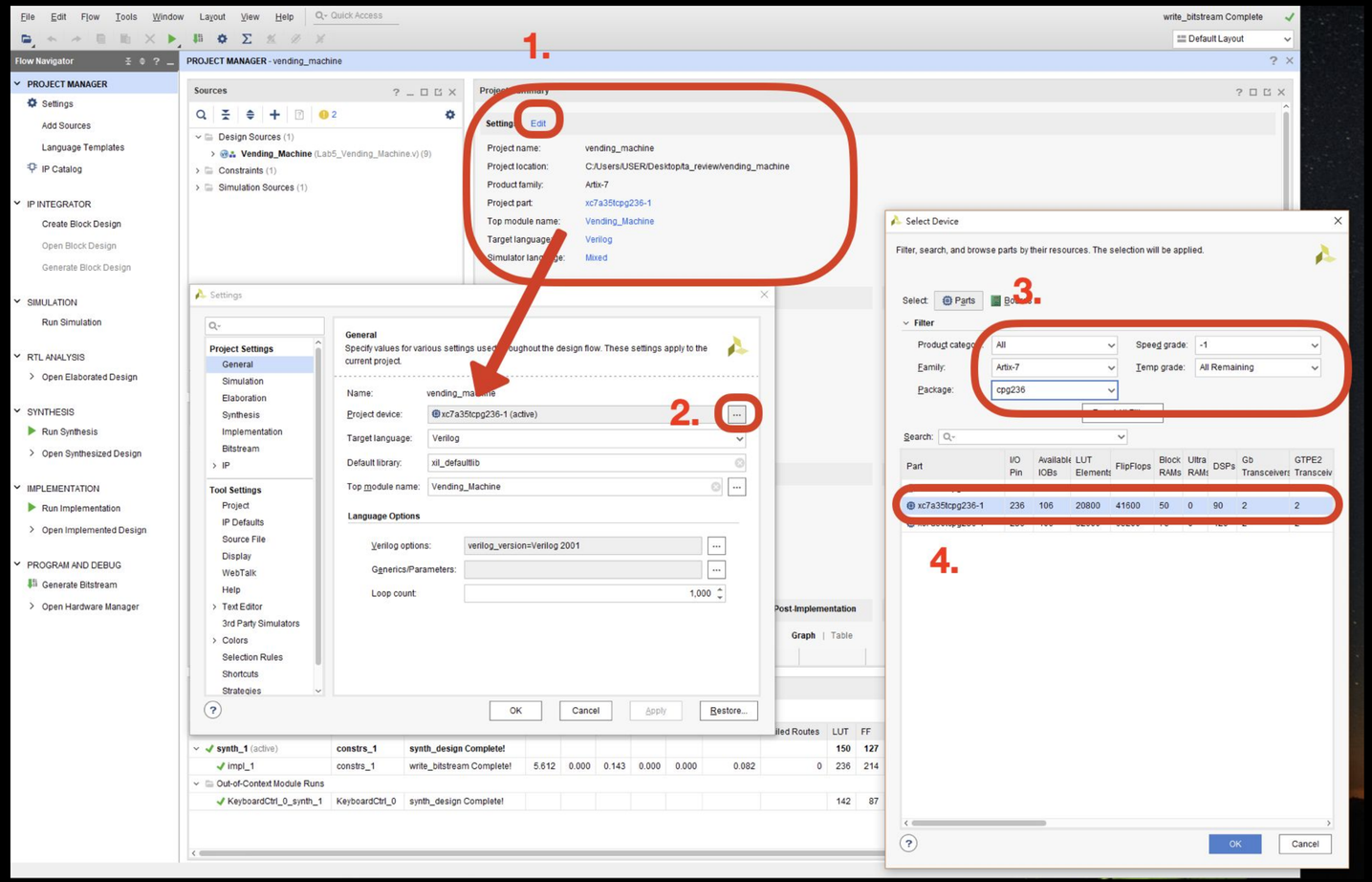
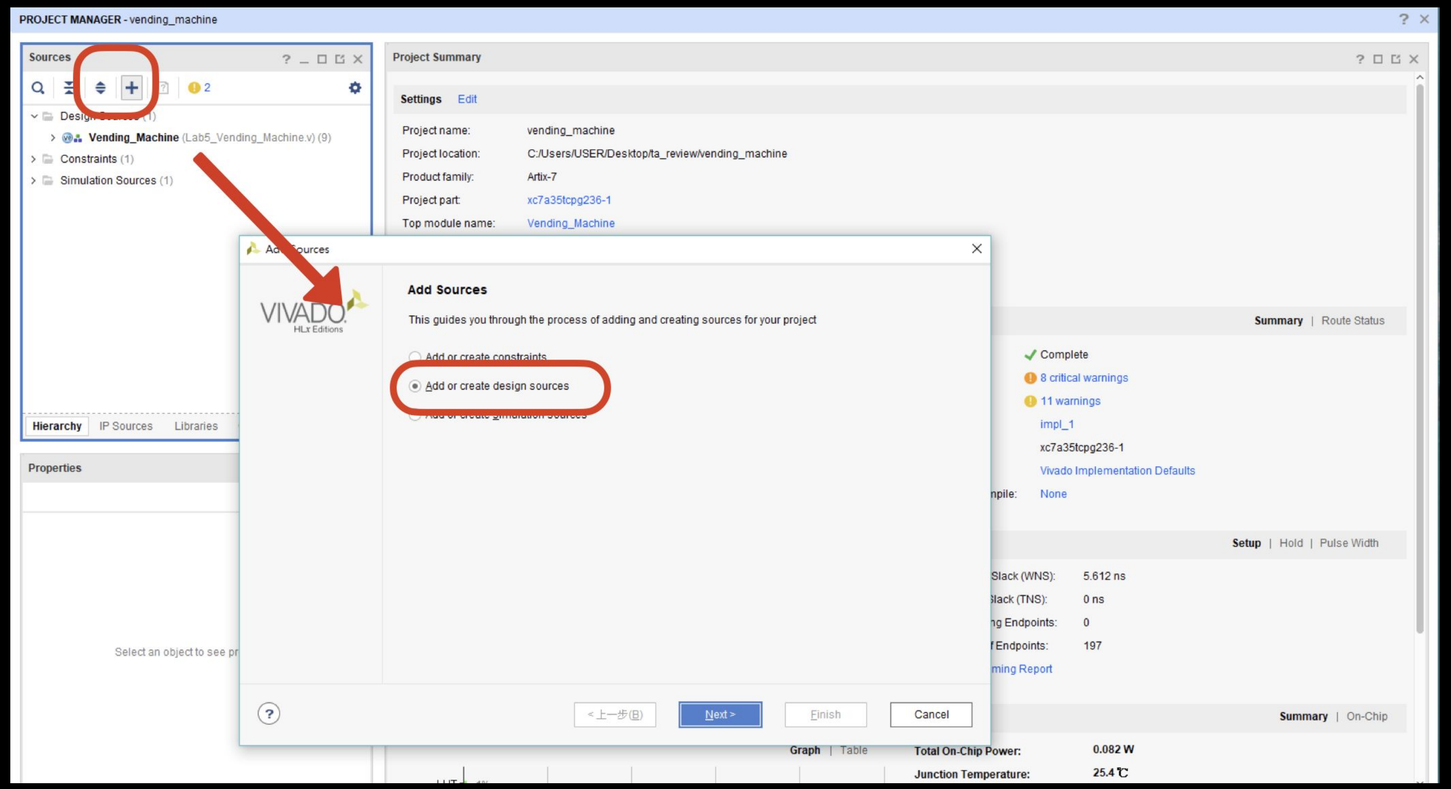
Preparation (1/5)

- First, we need to make sure that the correct board is selected



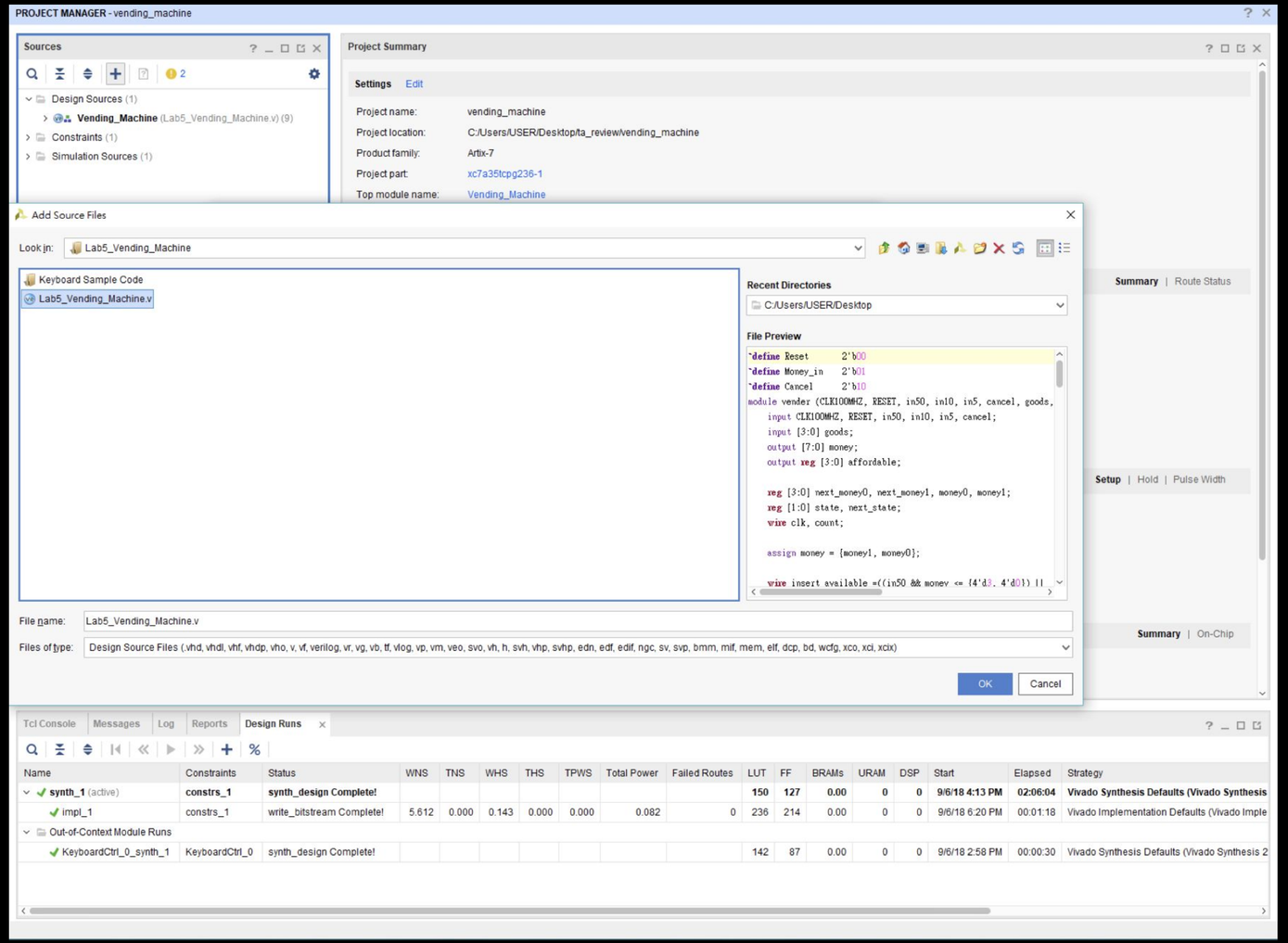
Preparation (2/5)

- Next, we need to add the design source file into the project (ignore this step if it is already added)



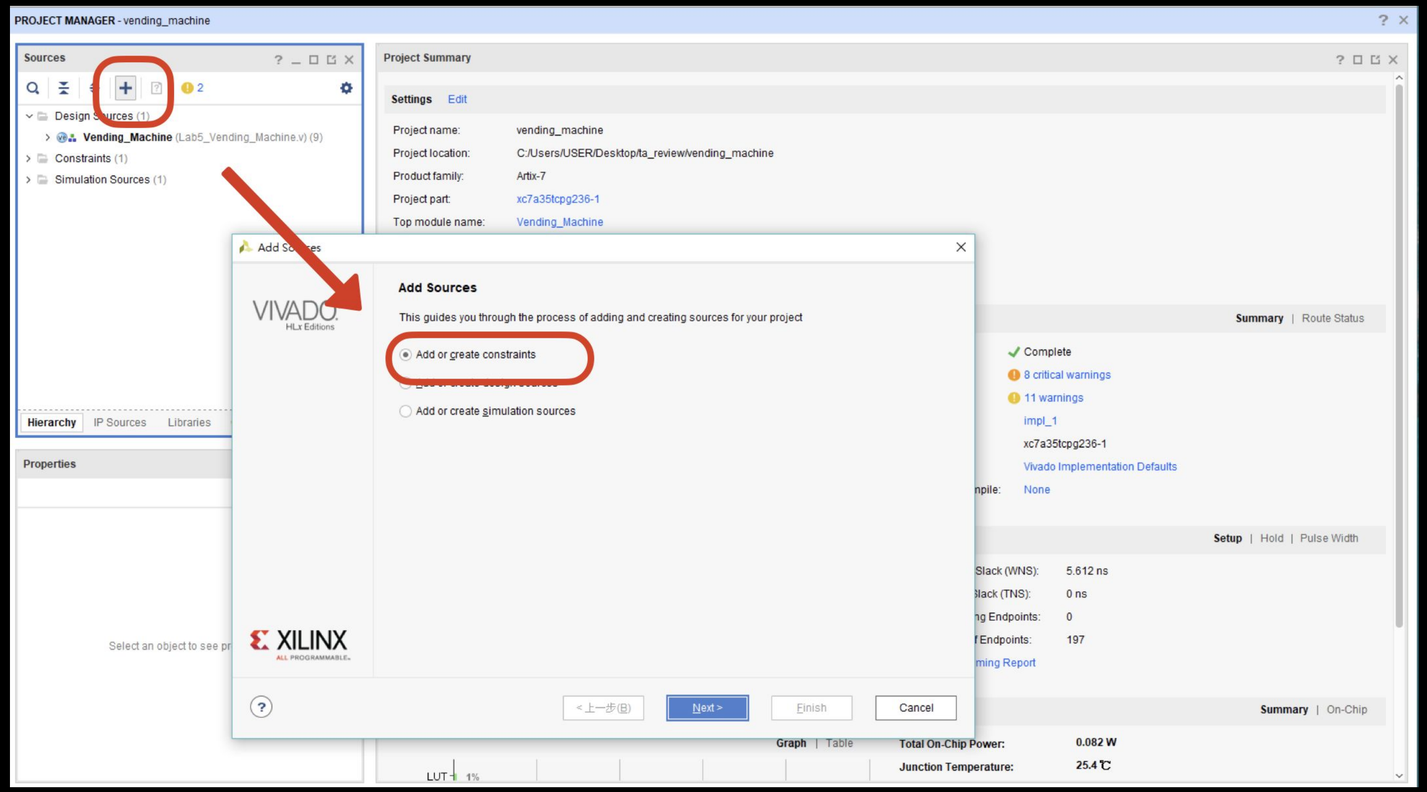
Preparation (3/5)

- Select the design source files you want to add to this project (ignore this step if they are already included in the project.)
-



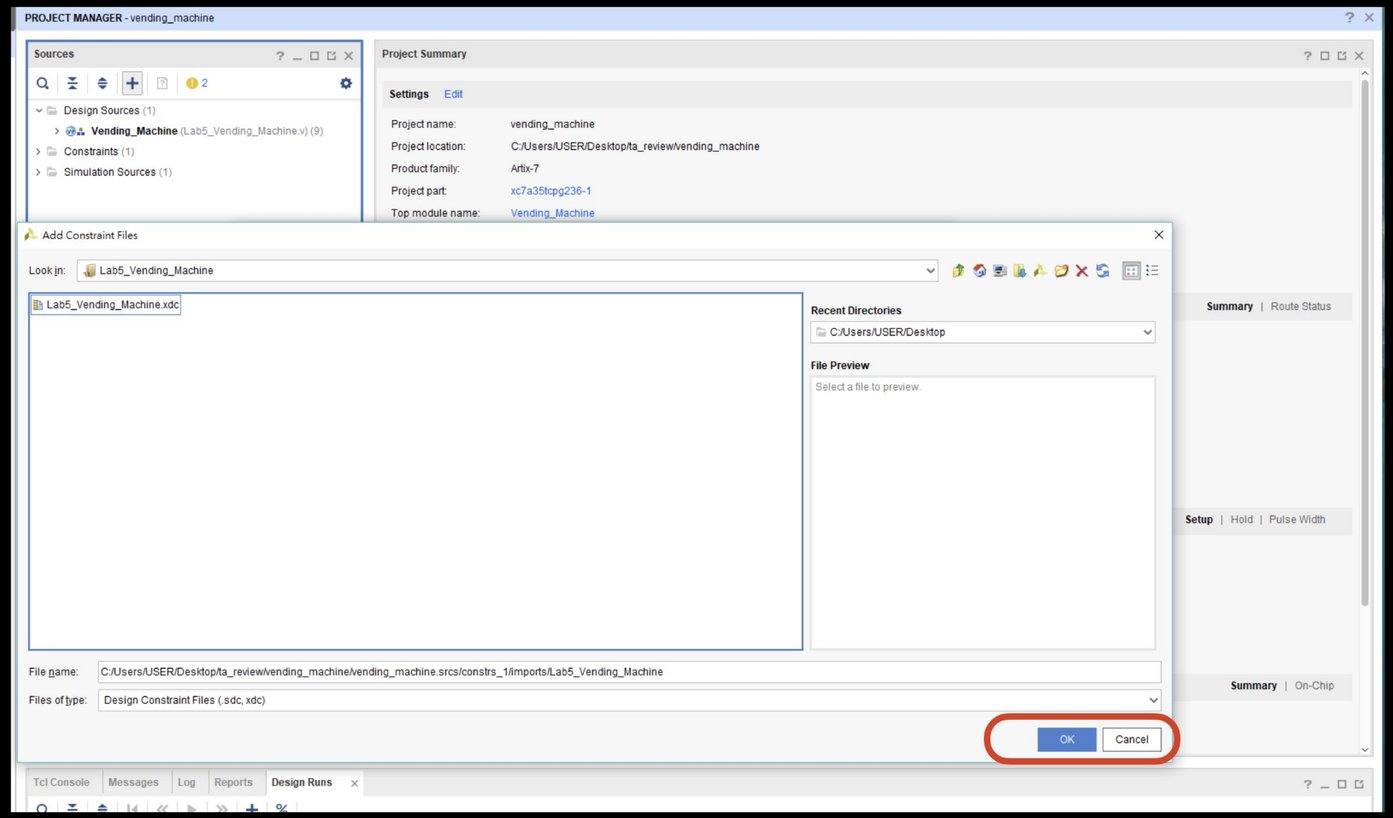
Preparation (4/5)

- Finally, we need to add the design constraint (.xdc file) to the project (ignore these steps if it is already included)



Preparation (5/5)

- Select the design constraint you want to add (ignore this step if it is already included)



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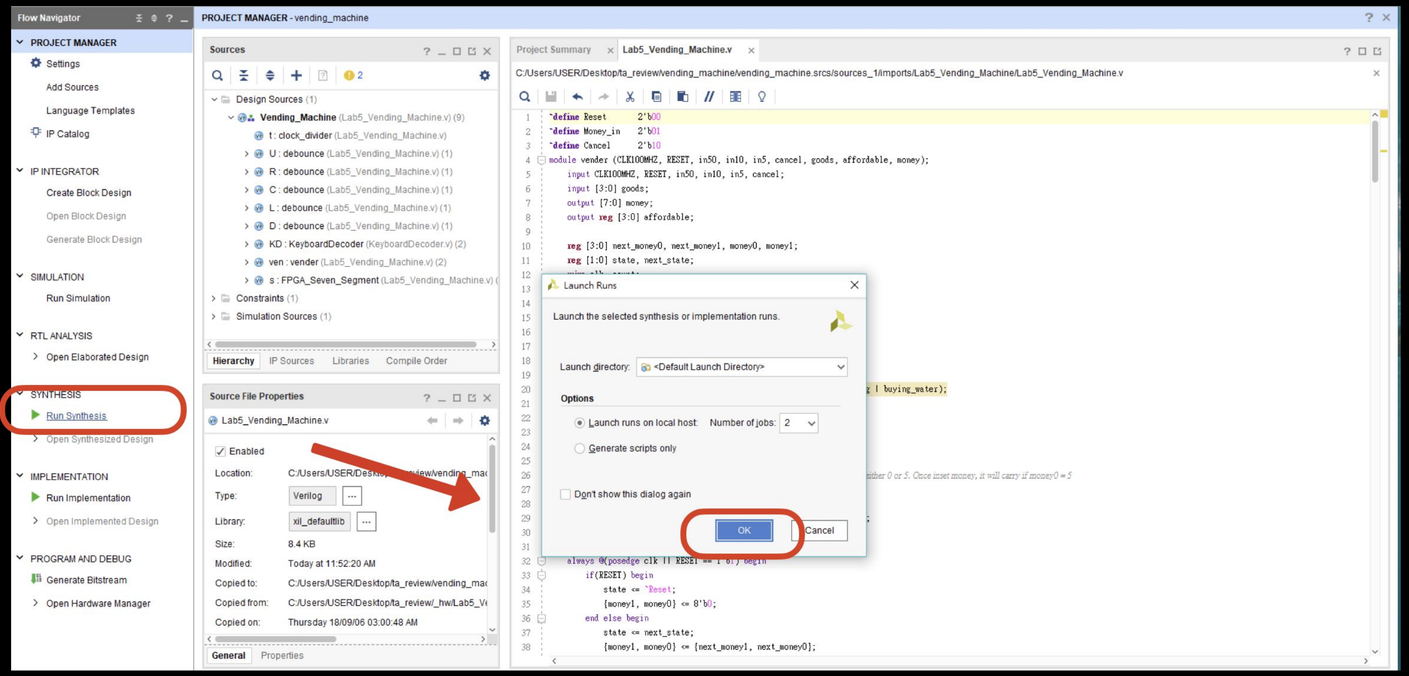
Generate Bit Stream (1/7)

- Synthesize our RTL design

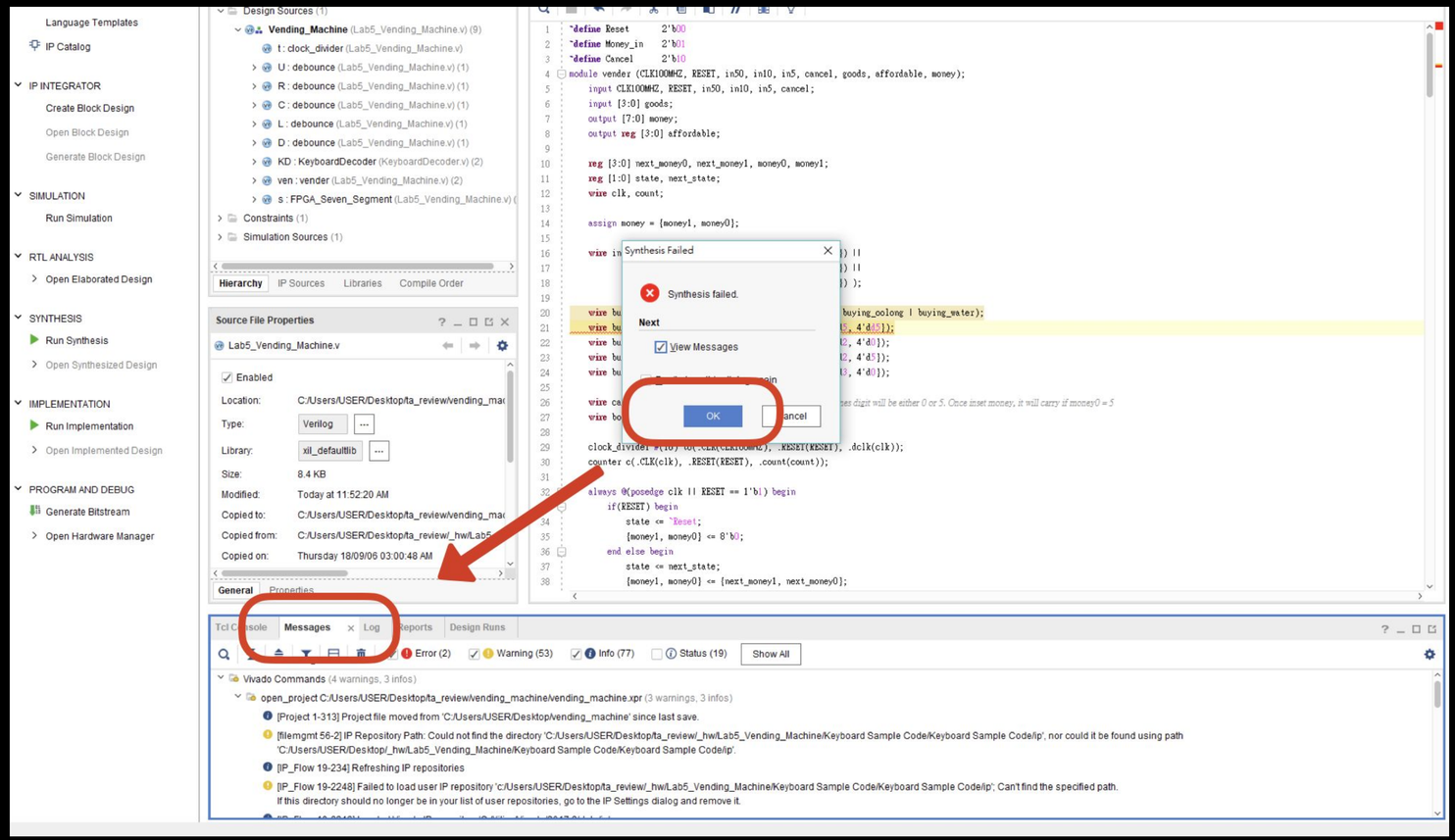
  by clicking ***Run Synthesis***

  and then hit ***OK***.



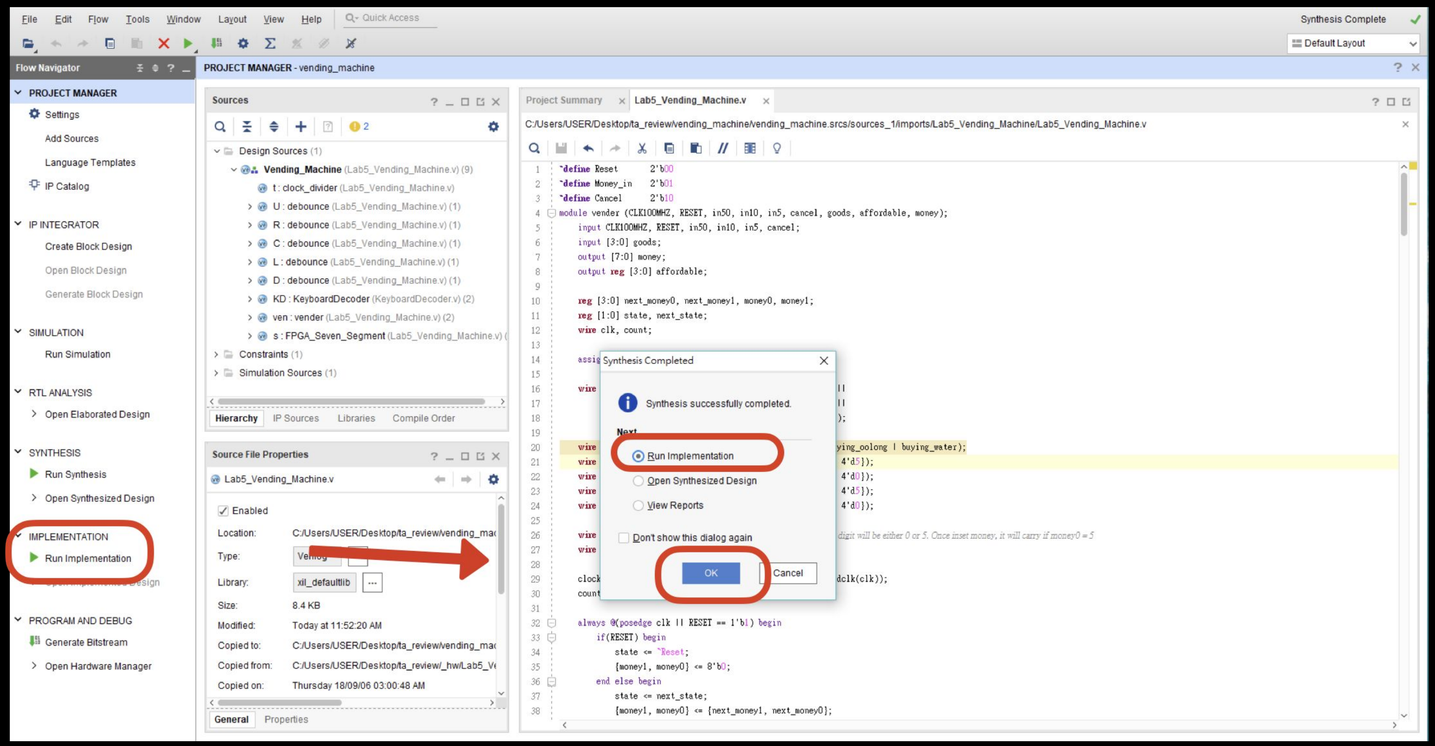
Generate Bit Stream (2/7)

- If there are any error during the synthesis process, go to the Messages window below to check the error(s) and correct them.



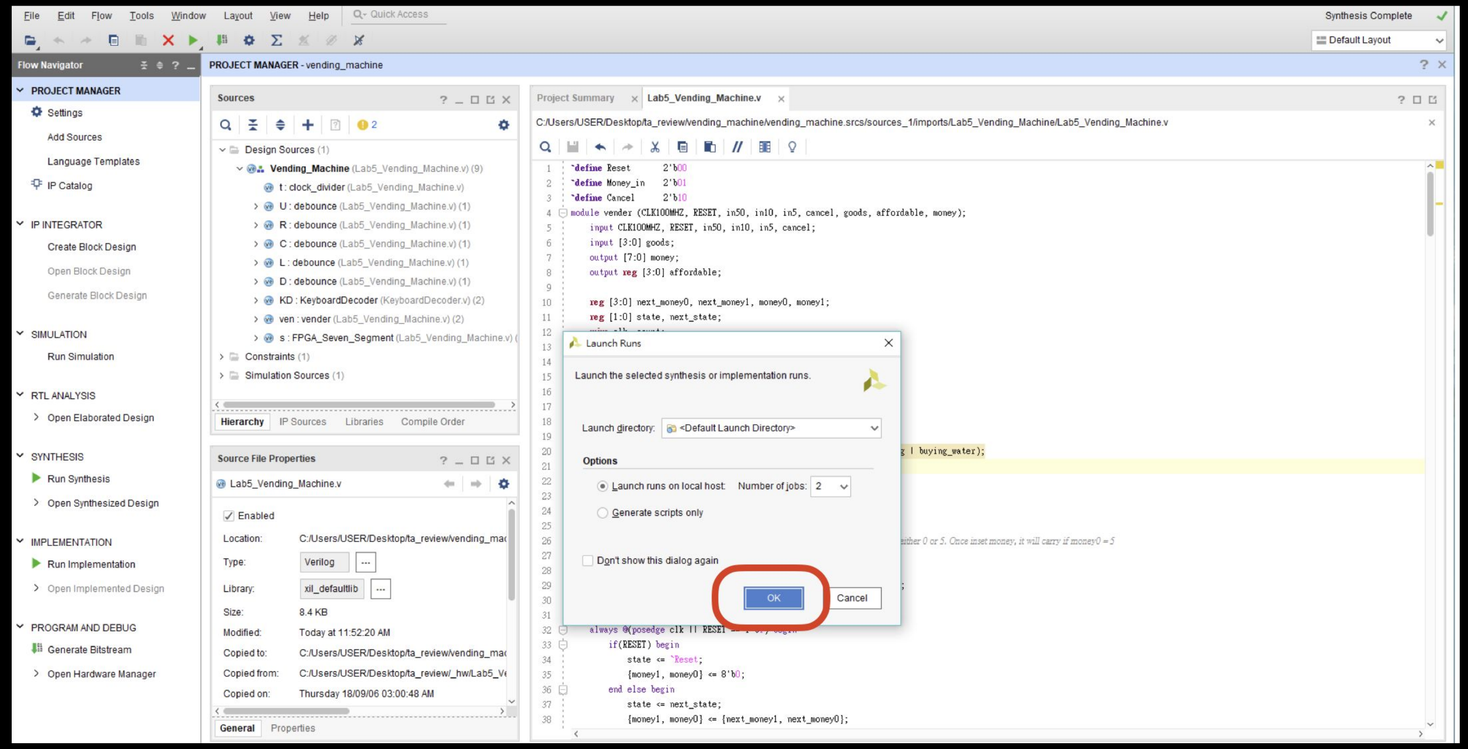
Generate Bit Stream (3/7)

- Next, we need to run implementation to turn the netlist into a complete implementation.
- Hit ***Run Implementation*** and hit ***OK***.



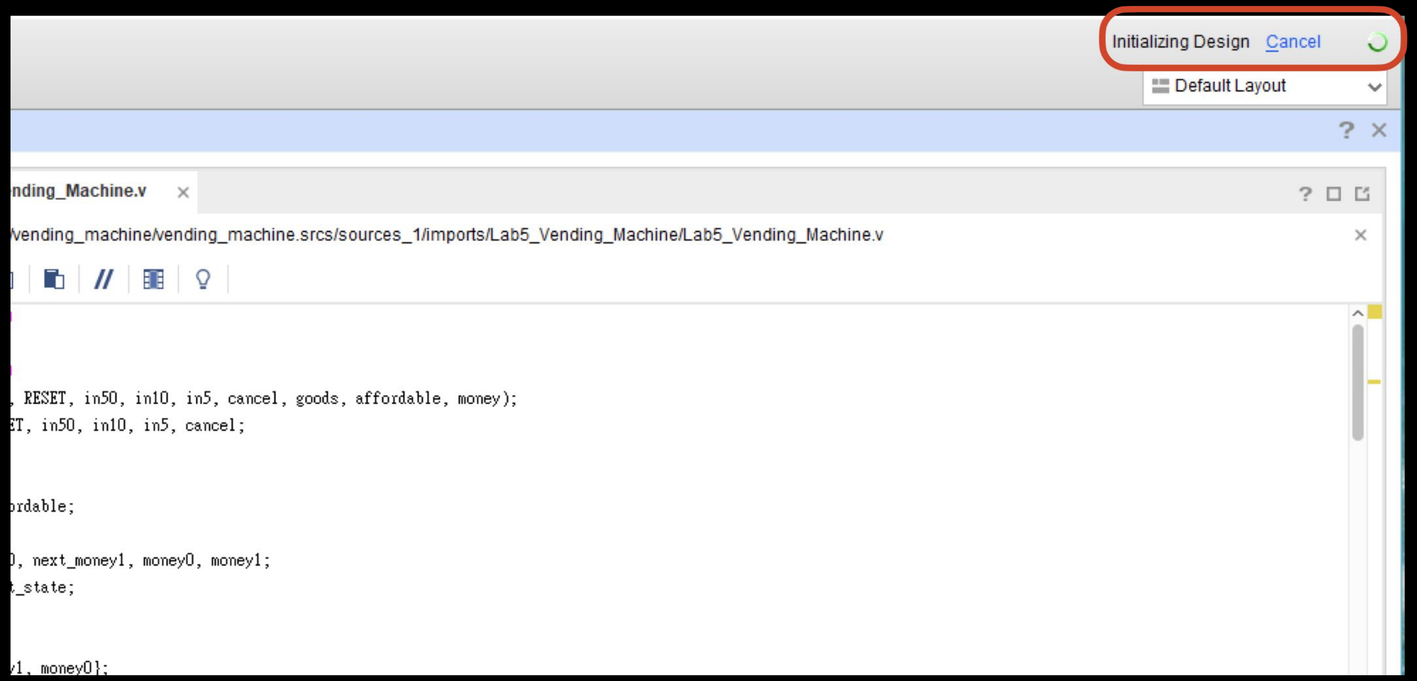
Generate Bit Stream (4/7)

- Click ***OK*** once more



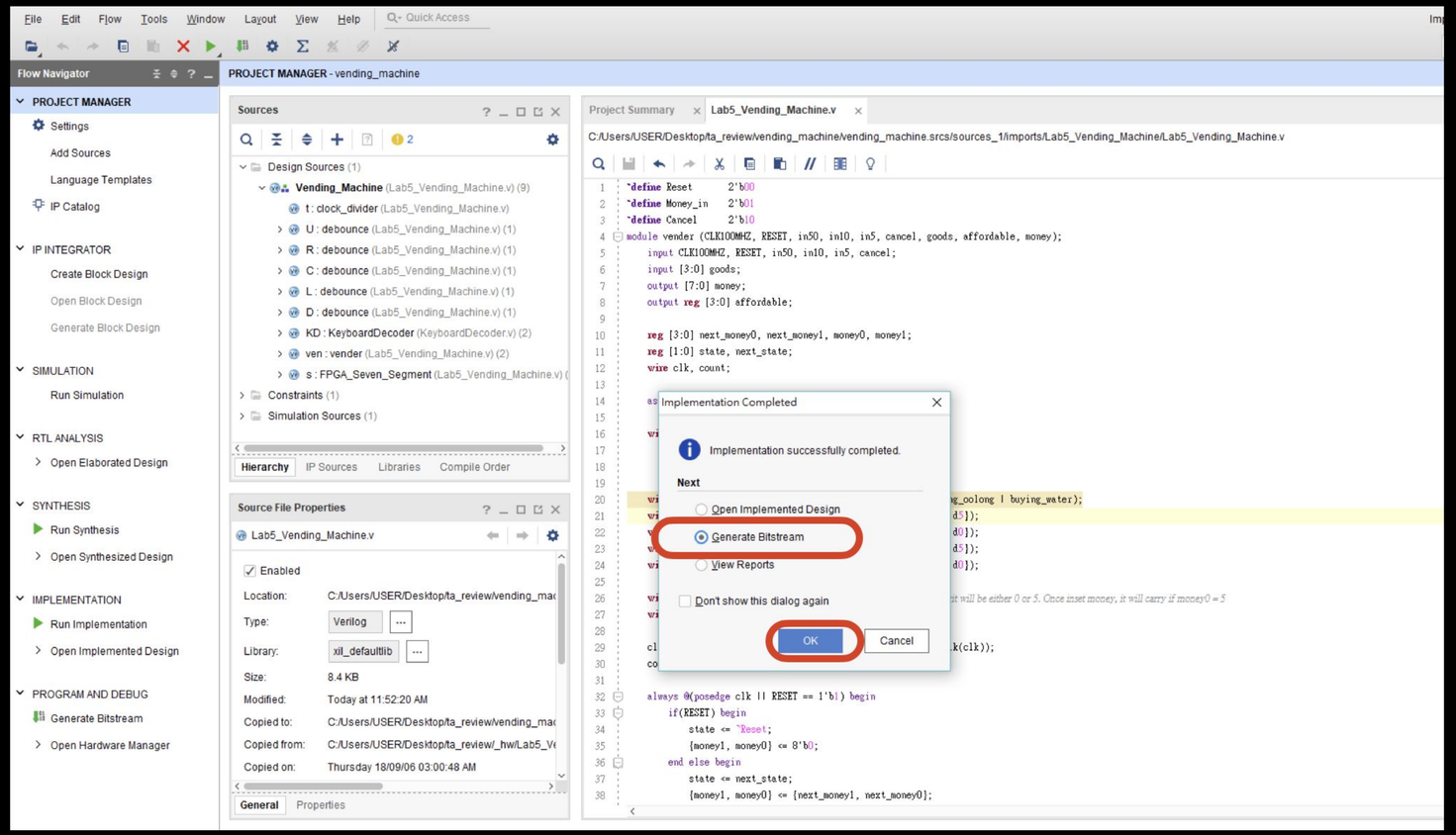
Generate Bit Stream (5/7)

- The Run Implementation process will run in background, this may take some time.



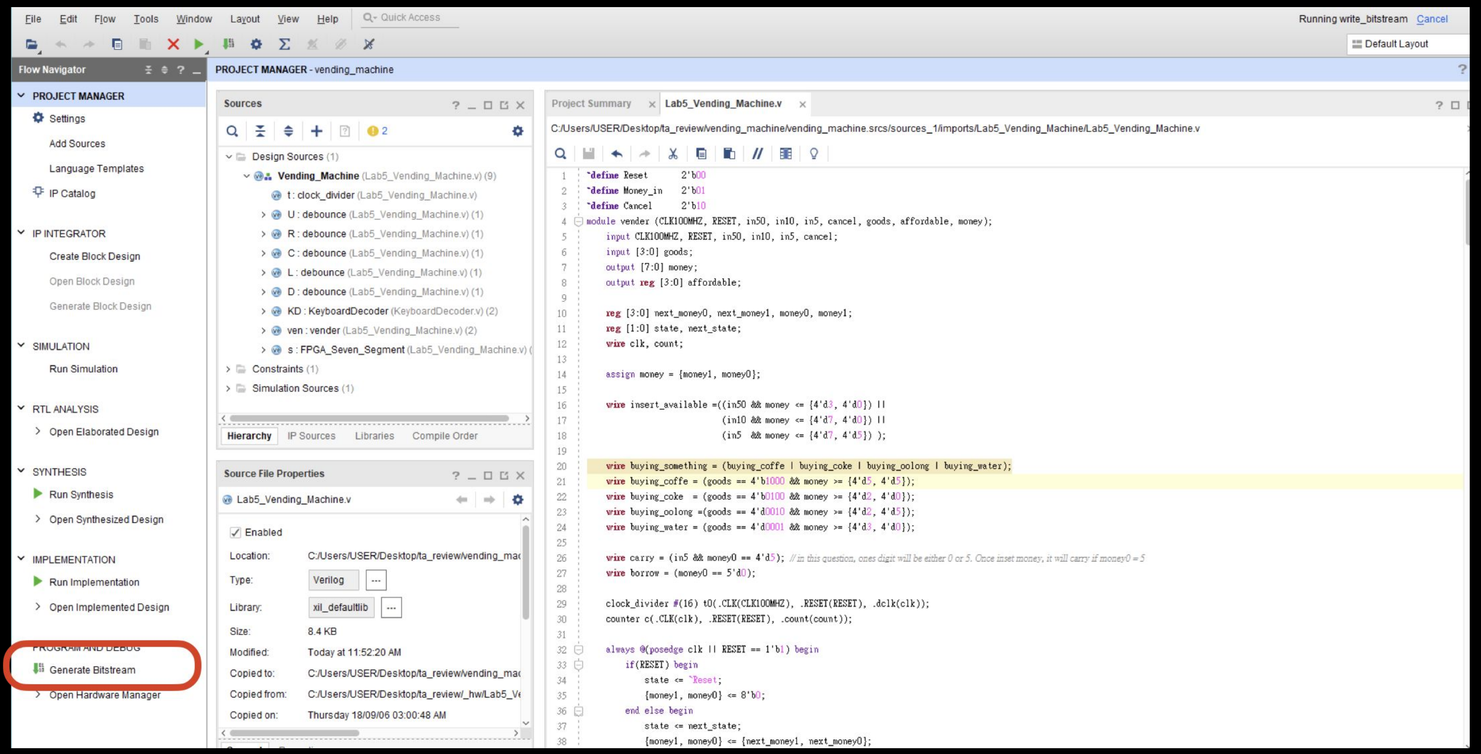
Generate Bit Stream (6/7)

- When Run Implementation is completed, select ***Generate Bitstream*** and hit ***OK***.



Generate Bit Stream (7/7)

- Or you can just click ***Generate Bitstream*** in the very beginning, Vivado will automatically run Synthesis and Implementation for you.



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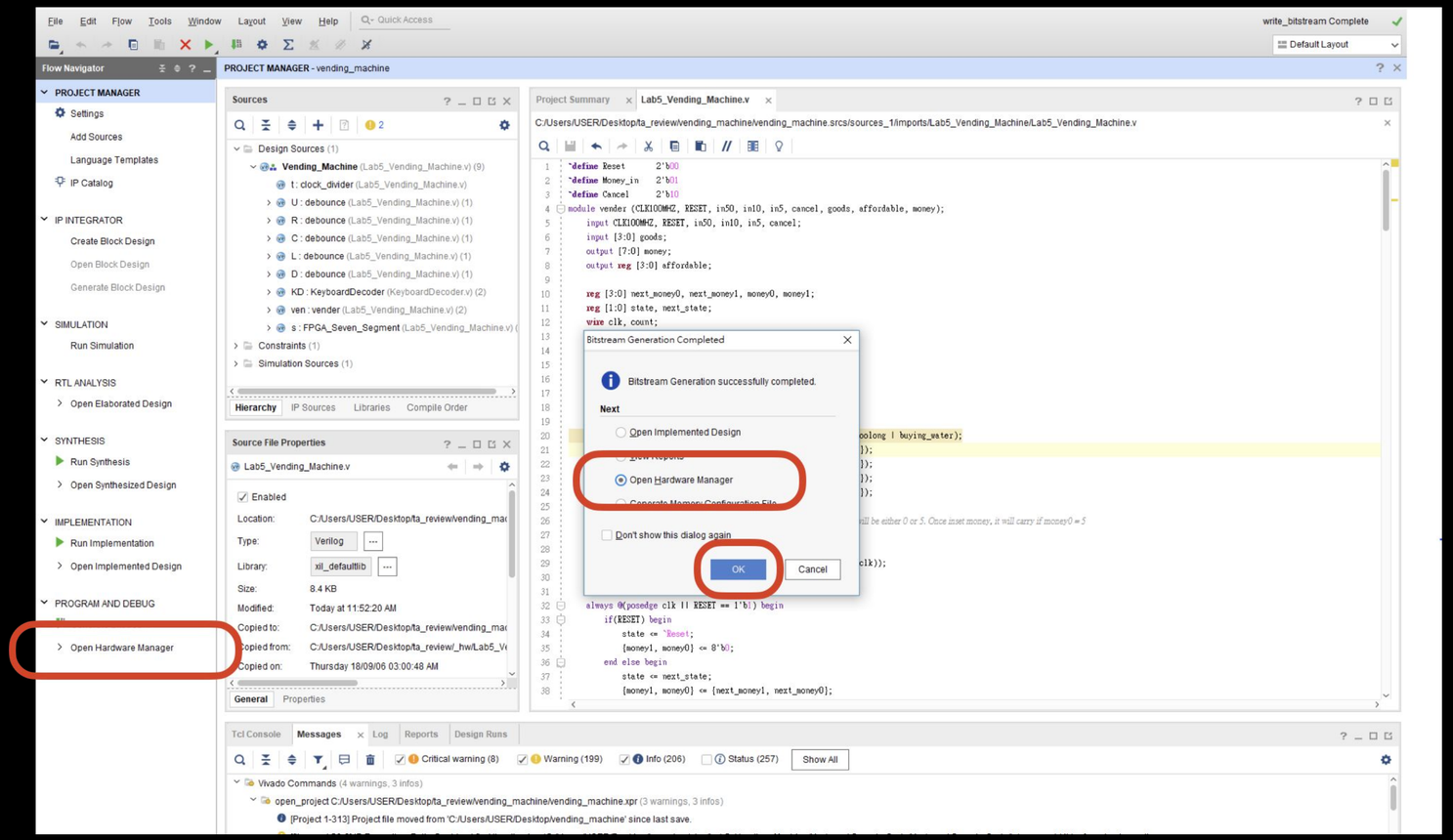
Design Verification on FPGA (1/11)

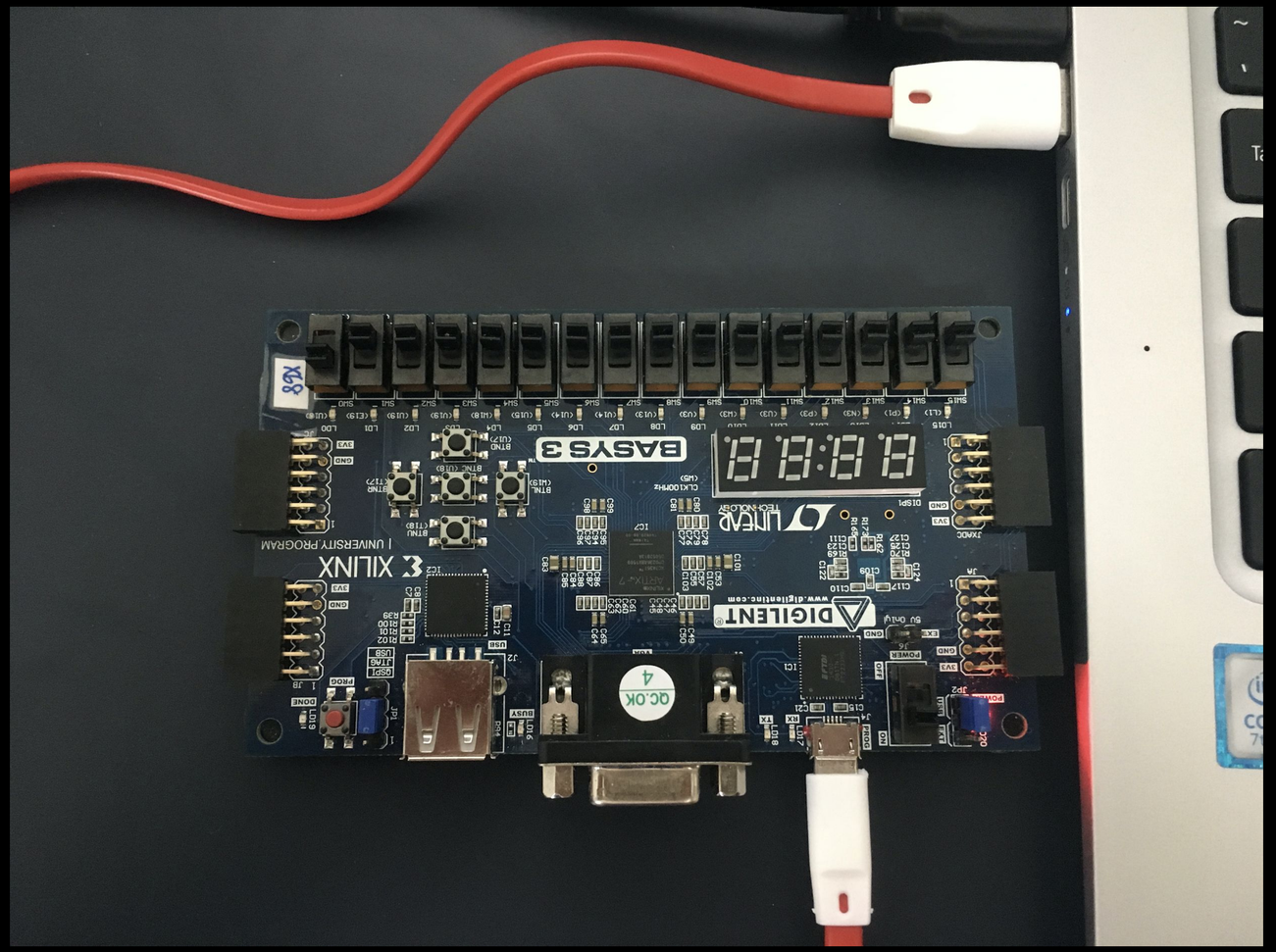
- After the bitstream generation, select ***Open Hardware Manager*** and hit ***OK***.



Design Verification on FPGA (2/11)

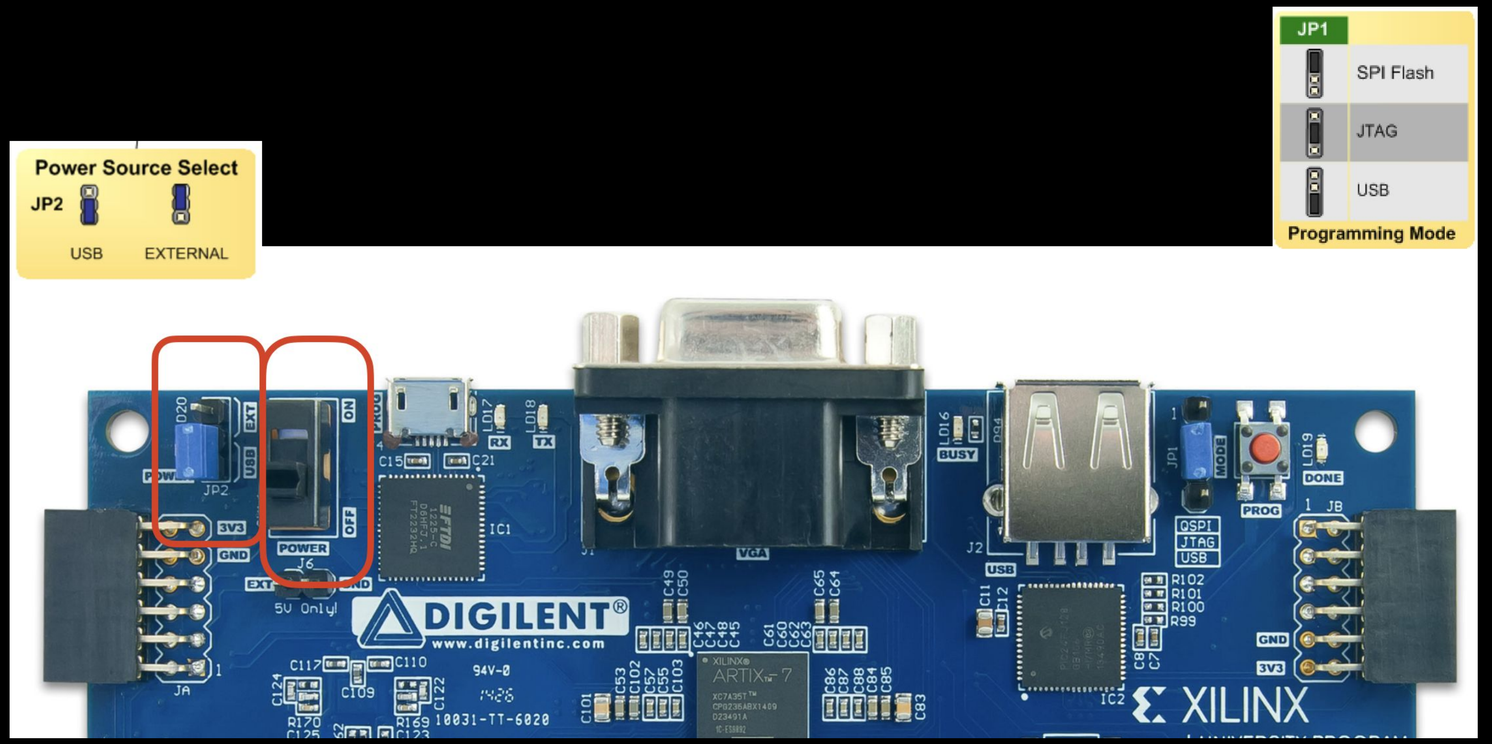
- Connect the FPGA board

  to your computer



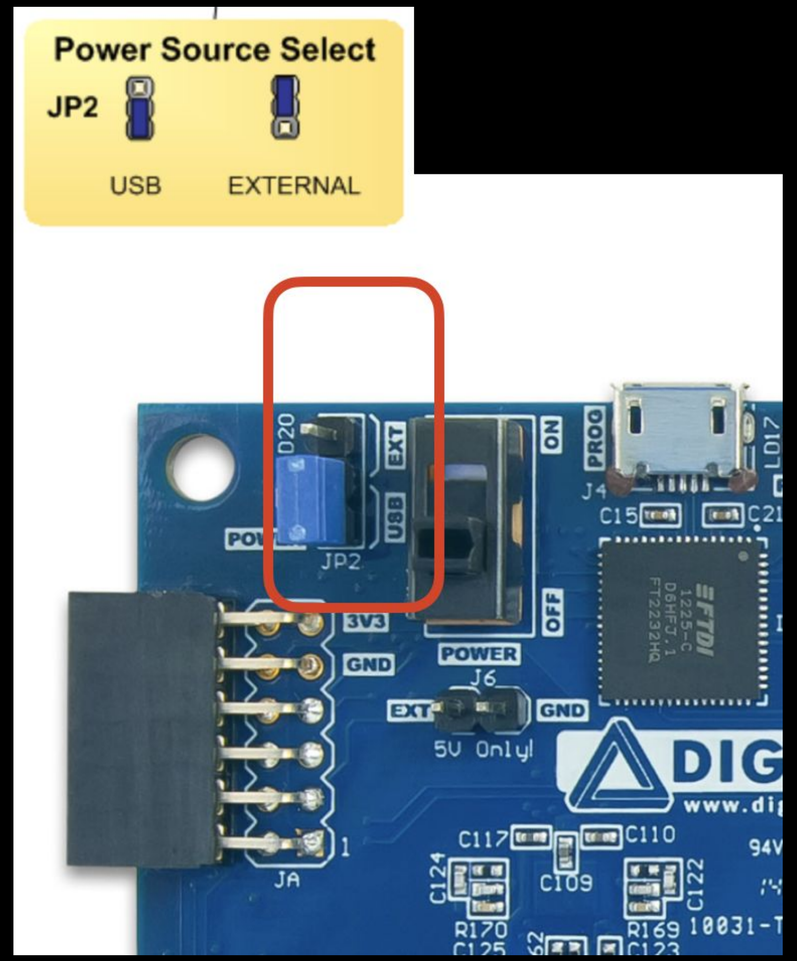
Design Verification on FPGA (3/11)

- Make sure JP1 has JTAG mode selected and JP2 has USB mode selected.
- Switch the power switch to ***ON***.

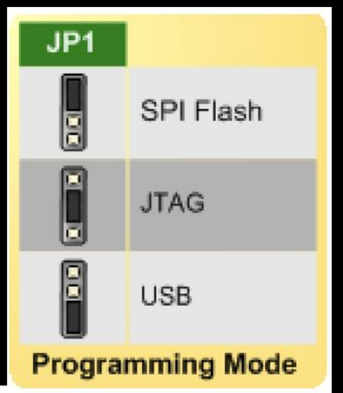


Design Verification on FPGA (4/11)

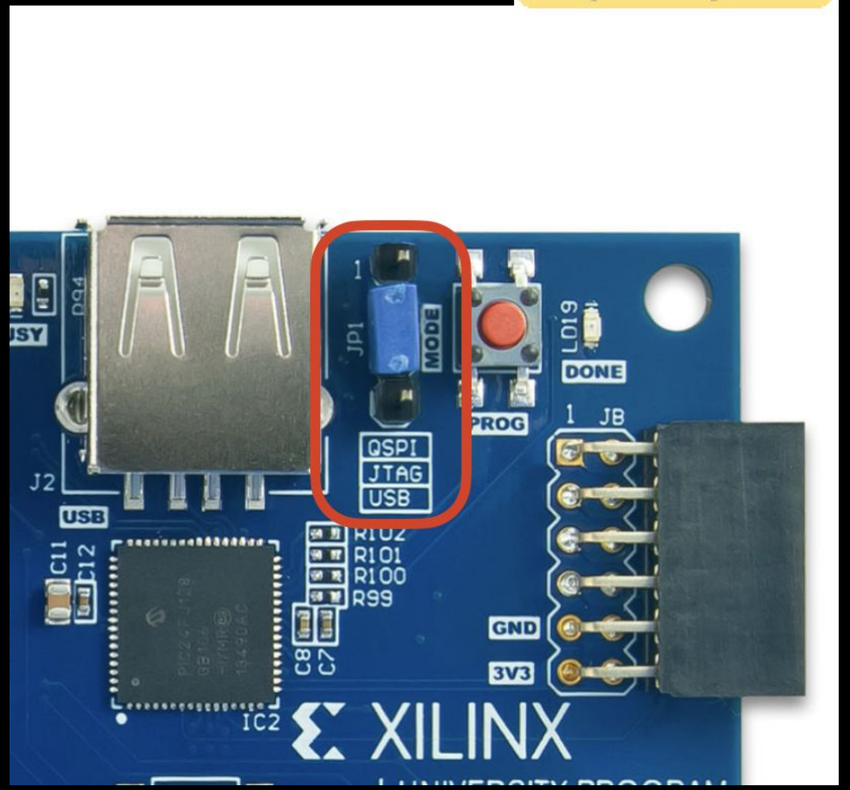
- JP2: power source selection
  - USB: the FPGA board is powered by the microUSB port (recommended)
  - EXTERNAL: the FPGA board is powered by 5V power supply (e.g. power bank)



Design Verification on FPGA (5/11)

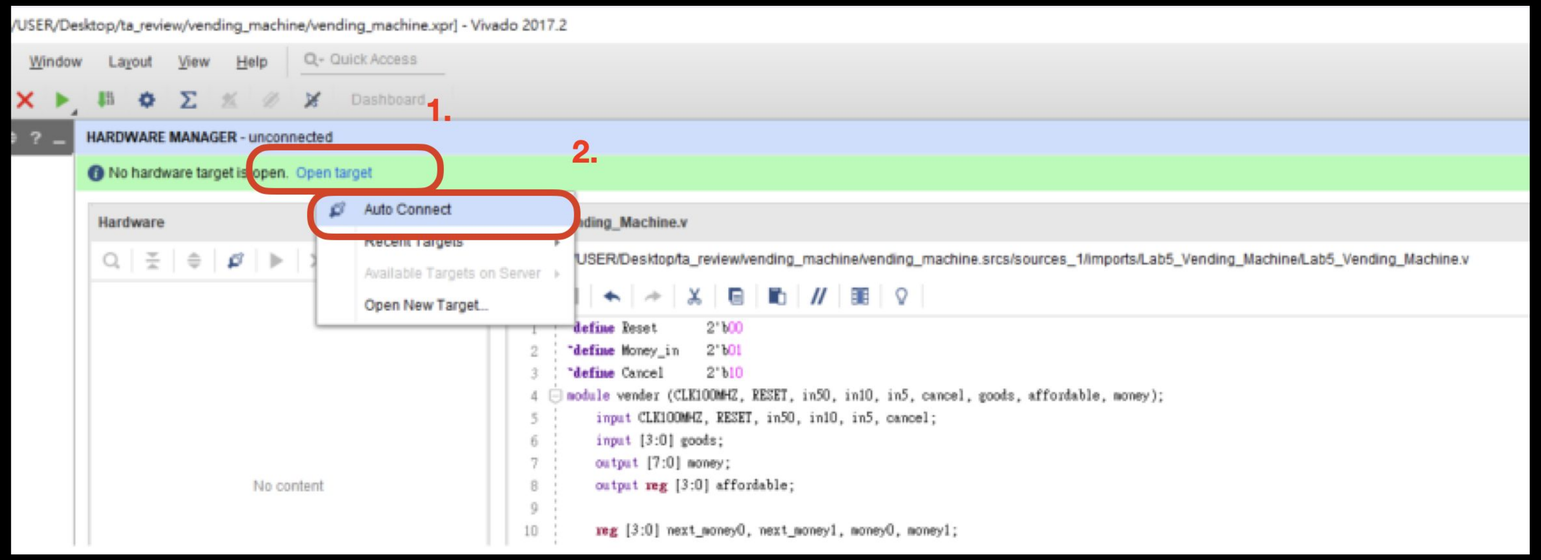


- JP1: Programming mode selection
- Receive Bitstream from:
  - Flash (on board, non-volatile)
  - JTAG (on board, volatile, recommend)
  - USB Drive



Design Verification on FPGA (6/11)

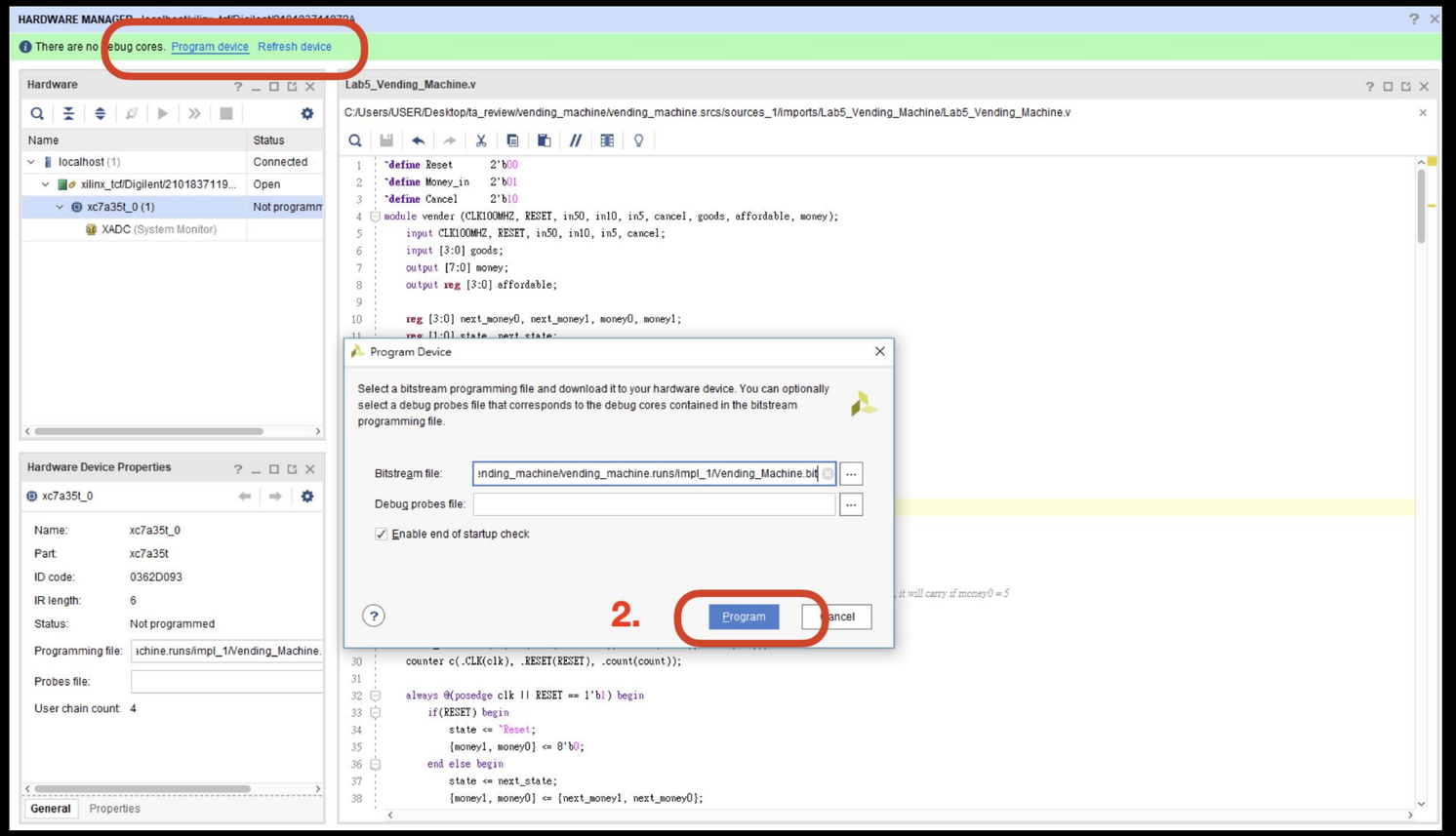
- Connect to our FPGA board in Vivado by hitting ***Open target*** and then ***Auto Connect***.



Design Verification on FPGA (7/11)

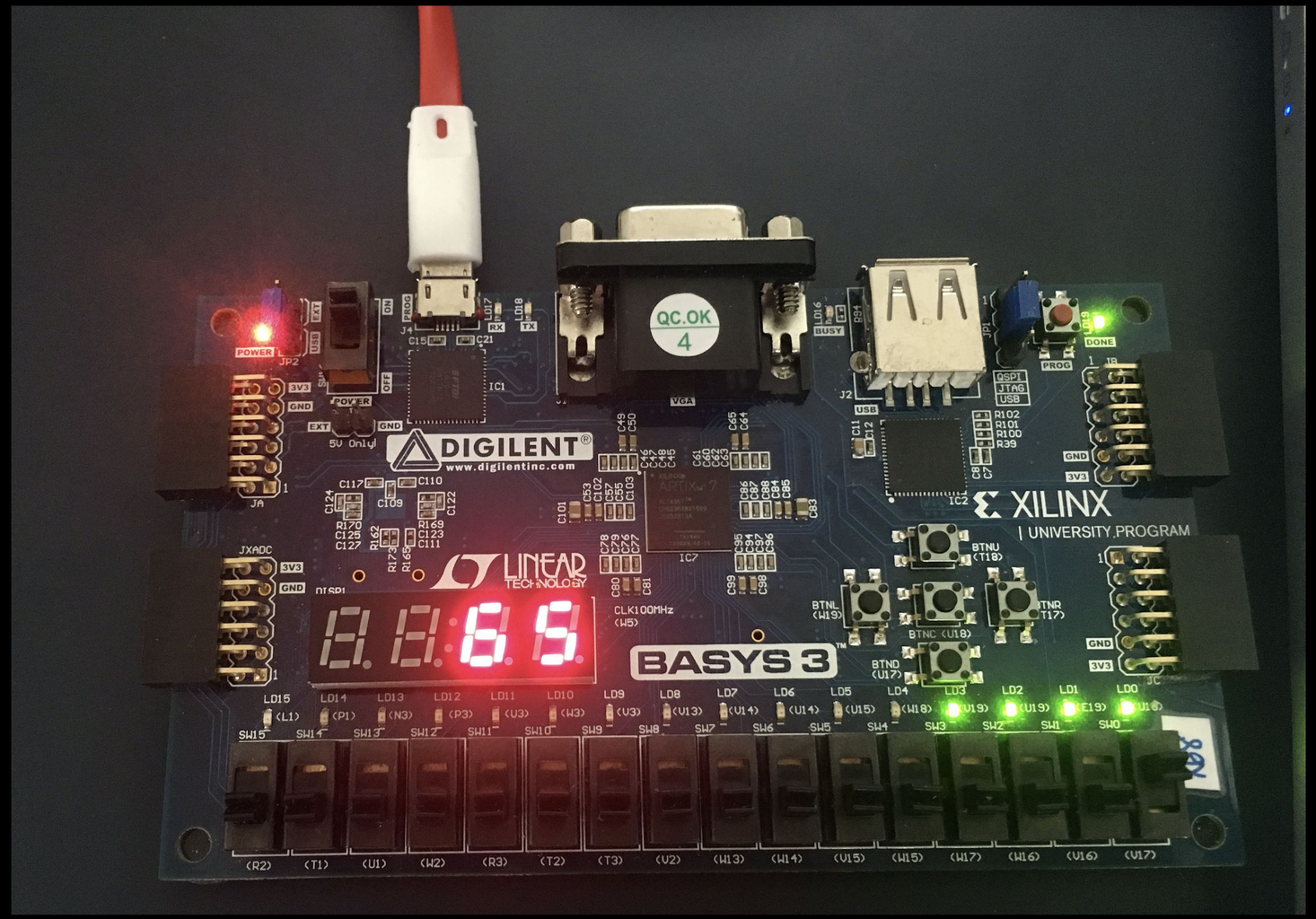
- Finally, hit ***Program device***

  and hit ***Program***.



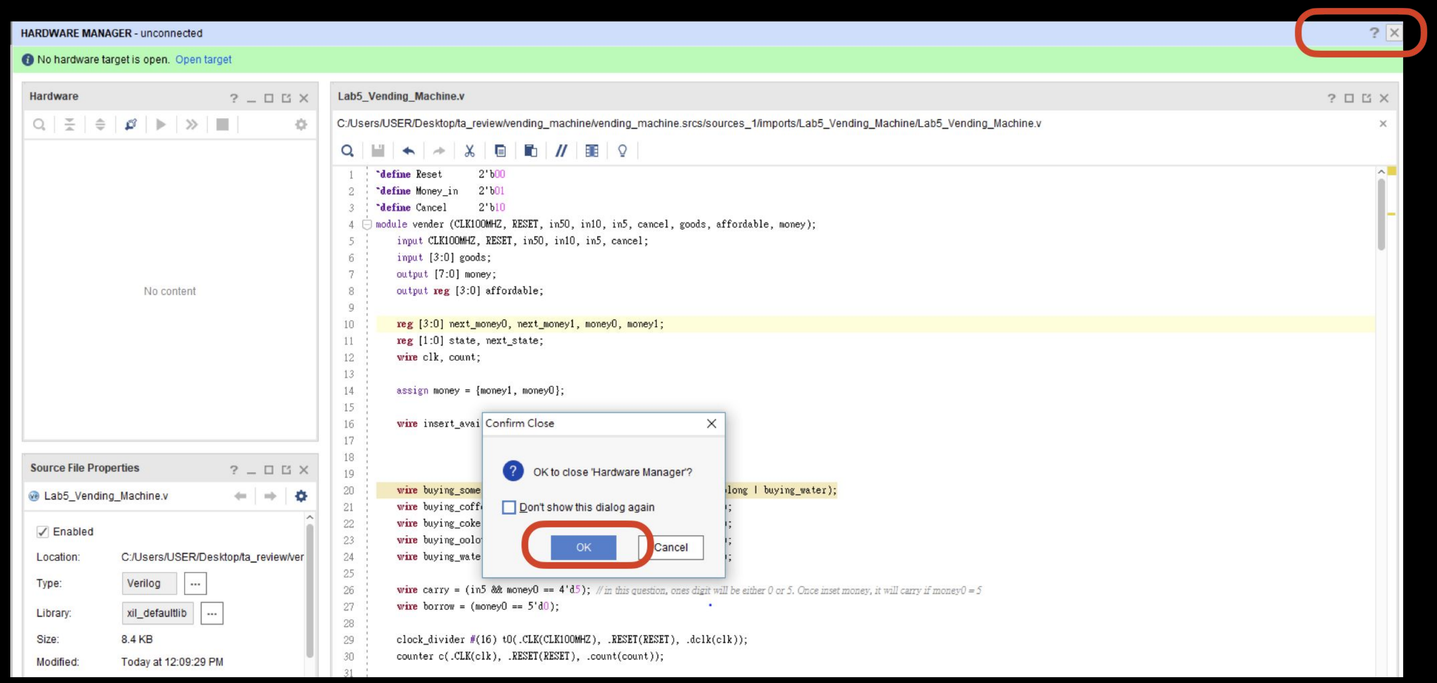
Design Verification on FPGA (8/11)

- Done, your verilog design is now programmed into your FPGA board.
- Verify that your design is correct.



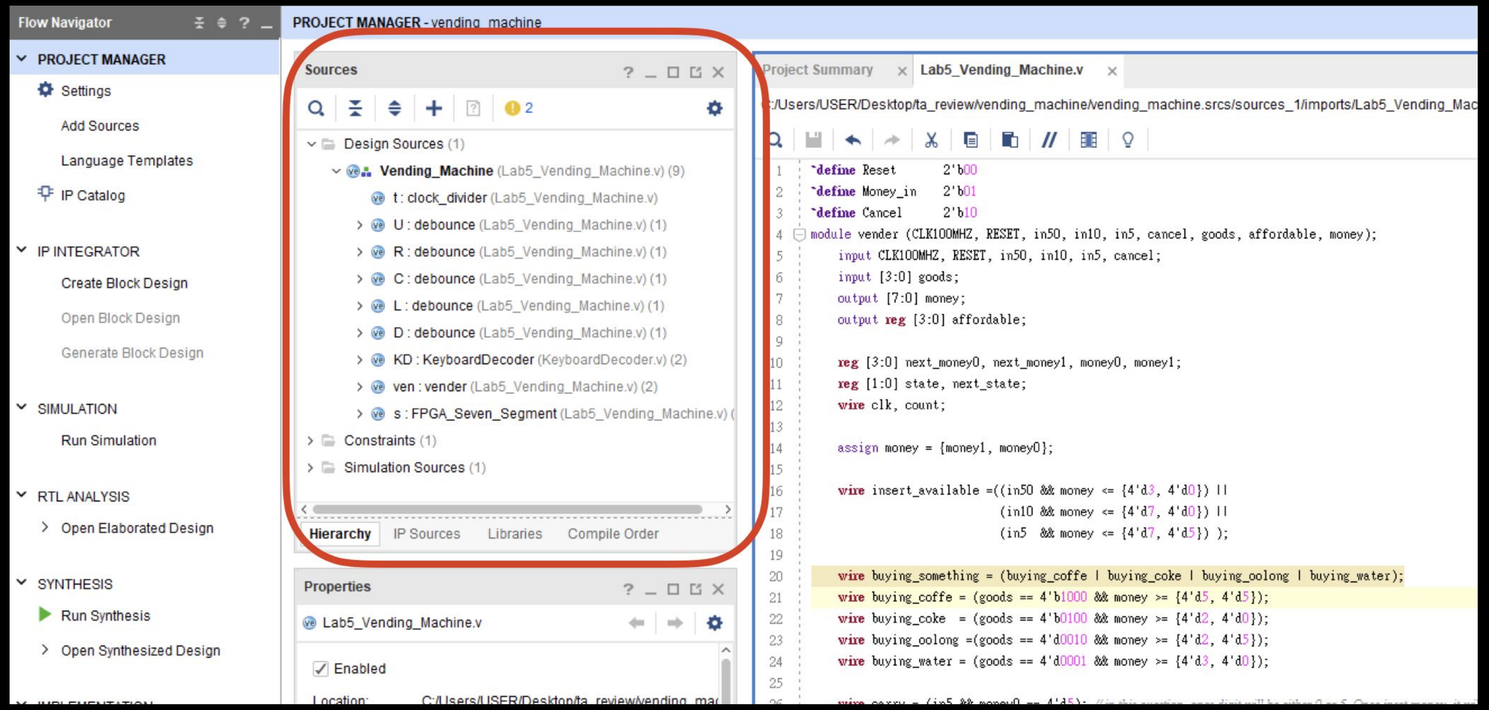
Design Verification on FPGA (9/11)

- To go back to the source panel, close the Hardware Manager.



Design Verification on FPGA (10/11)

- Done



Design Verification on FPGA (11/11)

- For additional information (e.g., configuration in to FPGA's flash ROM), please refer to:
  - https://reference.digilentinc.com/basys3/refmanual
  - https://www.youtube.com/watch?v=6_GxkslqbcU

Q&A