



[Project 2]

[SPI Slave with single port RAM]

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1.Verilog Code:

- RTL Code:
 - Wrapper Module:

```
module SPI_Wrapper (MOSI,SS_n,clk,rst_n,MISO);
// DEFINE PARAMETERS
parameter MEM_DEPTH = 256 ;
parameter ADDR_SIZE = 8 ;
// DEFINE INPUTS
input MOSI,SS_n,clk,rst_n;
// DEFINE OUTPUT
output MISO;
// DEFINE INTERNAL WIRES
wire [9:0] rx_data;
wire rx_valid,tx_valid;
wire [7:0] tx_data;
// INSTANTIATION RAM MODULE
Single_port_SYNC_RAM ram(rx_data,rx_valid,tx_data,tx_valid,clk,rst_n);
// INSTANTIATION SPI_slave_interface MODULE
SPI_slave_interface SPI(MOSI,MISO,SS_n,clk,rst_n,tx_valid,tx_data,rx_valid,rx_data);
endmodule
```

- RAM module:

```
module Single_port_SYNC_RAM (din,rx_valid,dout,tx_valid,clk,rst_n);
// DEFINE PARAMETERS
parameter MEM_DEPTH = 256 ;
parameter ADDR_SIZE = 8 ;
// DEFINE INPUTS
input [9:0] din;
input clk,rst_n,rx_valid;
// DEFINE OUTPUTS
output reg [7:0] dout;
output reg tx_valid;
// GENERATE MEMORY
reg [7:0] RAM [MEM_DEPTH-1:0];
// DEFINE 2 ADDRESSES ONE FOR WRITE AND ONE FOR READ
reg [ADDR_SIZE-1 :0] wr_address , rd_address ;
// DESIGN IMPLEMENTATION
always @(posedge clk) begin
    if(~rst_n)begin
        dout <= 0;
        tx_valid <= 0;
        wr_address <= 0;
        rd_address <= 0;
    end
    else begin
        if(rx_valid)begin
```

```

        case (din[9:8])
            2'b00: wr_address <= din[7:0];
            2'b01: RAM[wr_address] <= din[7:0];
            2'b10: rd_address <= din[7:0];
            2'b11:begin
                dout <= RAM[rd_address];
                tx_valid <= 1;
            end
        endcase
    end
end
end
endmodule

```

- SPI module:

```

module SPI_slave_interface (MOSI,MISO,SS_n,clk,rst_n,tx_valid,tx_data,rx_valid,rx_data);
// DEFINE STATES ENCODING
parameter IDLE =3'b000;
parameter CHK_CMD =3'b001;
parameter WRITE =3'b010;
parameter READ_ADD =3'b011;
parameter READ_DATA =3'b100;
// DEFINE INPUTS
input MOSI,SS_n,tx_valid,clk,rst_n;
input [7:0] tx_data;
// DEFINE OUTPUTS
output reg rx_valid,MISO;
output reg [9:0] rx_data;
// DEFING INTERNAL COOUNTER & signal
reg [3:0] counter;
reg rd_control;
// DEFINE CURRENT AND NEXT STATES
(* fsm_encoding = "one_hot" *) // FOR ENCODING IN VIVADO
reg [2:0] cs,ns;
reg [7:0] tx_data_temp;
// STATE MEMORY BLOCK
always @(posedge clk) begin
    if(~rst_n)begin
        cs <= IDLE;
    end
    else begin
        cs <= ns;
    end
end
// NEXT STATE LOGIC BLOCK
always @(*) begin
    case (cs)
        IDLE:begin

```

```

        if(SS_n == 1)
            ns = IDLE ;
        else
            ns = CHK_CMD;
        end
    CHK_CMD:begin
        if((SS_n == 0) && (MOSI == 0))
            ns = WRITE;
        else if((SS_n == 0) && (MOSI == 1) && (rd_control == 0))
            ns = READ_ADD;
        else if((SS_n == 0) && (MOSI == 1) && (rd_control == 1))
            ns = READ_DATA;
        else
            ns = IDLE;
        end
    WRITE:begin
        if(SS_n == 1)
            ns = IDLE;
        else
            ns = WRITE;
        end
    READ_ADD:begin
        if(SS_n == 1)
            ns = IDLE;
        else
            ns = READ_ADD;
        end
    READ_DATA:begin
        if(SS_n == 1)
            ns = IDLE;
        else
            ns = READ_DATA;
        end
        default: ns = IDLE;
    endcase
end
// OUTPUT LOGIC BLOCK
always @(posedge clk) begin
    if(~rst_n)begin
        rx_valid <= 0;
        rx_data <= 0;
        MISO <= 0;
        counter <= 0;
        rd_control <= 0;

    end
    else begin
        case (cs)
            IDLE:begin
                rx_valid <=0;

```

```

        counter <= 0;
        MISO <=0;
    end
    CHK_CMD:begin
        rx_valid <=0;
        counter <= 0;
    end
    WRITE:begin
        if(counter <= 9)begin
            rx_data[9-counter] <= MOSI ;
            rx_valid <= 0;
            counter <= counter + 1;

        end
        else begin
            rx_valid <= 1;
        end
    end
end
    READ_ADD:begin
        if(counter <= 9)begin
            rx_data[9-counter] <= MOSI ;
            rx_valid <= 0;
            counter <= counter + 1;
            rd_control <= 1;

        end
        else begin
            rx_valid <= 1;
        end
    end
end
    READ_DATA:begin
        if(counter <= 9) begin
            rx_data[9-counter] <= MOSI;
            rx_valid <= 0;
            counter <= counter + 1;

        end
        else if(tx_valid && counter >= 3) begin
            MISO <= tx_data[counter - 3];
            counter <= counter - 1;

        end
        if(counter > 9) begin
            rx_valid <= 1;
            rd_control <= 0;

        end
    end
end
endcase
end
endmodule

```

- Test bench:

```
module SPI_Wrapper_tb ();

parameter MEM_DEPTH_tb = 256 ;
parameter ADDR_SIZE_tb = 8 ;

reg MOSI_tb,SS_n_tb,clk_tb,rst_n_tb;
wire MISO_dut;

SPI_Wrapper DUT(MOSI_tb,SS_n_tb,clk_tb,rst_n_tb,MISO_dut);

integer i,j;
reg [9:0] data;

integer flag;

initial begin
    clk_tb = 0;
    forever begin
        #1 clk_tb = ~ clk_tb ;
    end
end

initial begin
    $readmemh("mem.dat",DUT.ram.RAM);
    rst_n_tb = 0;
    MOSI_tb =0;
    SS_n_tb=1;
    flag = 0;
    data =0;
    @(negedge clk_tb);
    rst_n_tb = 1;
    // TEST WRITE OPERATION
    for(i=0;i<49;i=i+1)begin
        // START COMMUNICATION
        SS_n_tb = 0;
        MOSI_tb = 0;
        repeat(2) @(negedge clk_tb);
        if(flag == 0)begin
            data[9:8] = 0;
            flag = 1;
        end
        else begin
            data [9:8] = 1;
            flag = 0;
        end

        for(j=0;j<=1;j=j+1)begin
            MOSI_tb = data[9-j];
            @(negedge clk_tb);
```

```

end
data[7:0] = $random;

    for(j=0;j<=7;j=j+1)begin
        MOSI_tb = data[7-j];
        @(negedge clk_tb);
    end
    if(DUT.SPI.rx_data != data[9:0])begin
        $display("Error");
        $stop;
    end
    SS_n_tb = 1;          // END COMMUNICATION
    @(negedge clk_tb);
end
// TEST READ OPERATION
flag =2;
for(i=0;i<49;i=i+1)begin
    // START COMMUNICATION
    SS_n_tb = 0;
    MOSI_tb = 1;
    repeat(2) @(negedge clk_tb);
    if(flag == 2)begin
        data[9:8] = 2;
        flag = 3;
    end
    else begin
        data [9:8] = 3;
        flag = 2;
    end
    for(j=0;j<=1;j=j+1)begin
        MOSI_tb = data[9-j];
        @(negedge clk_tb);
    end
    data[7:0] = $random;
    for(j=0;j<=7;j=j+1)begin
        MOSI_tb = data[7-j];
        @(negedge clk_tb);
    end
    if(DUT.SPI.tx_data != DUT.ram.RAM[data[9:0]])begin
        $display("Error");
        $stop;
    end
    SS_n_tb = 1;          // END COMMUNICATION
    @(negedge clk_tb);
end
$stop;
end
initial begin

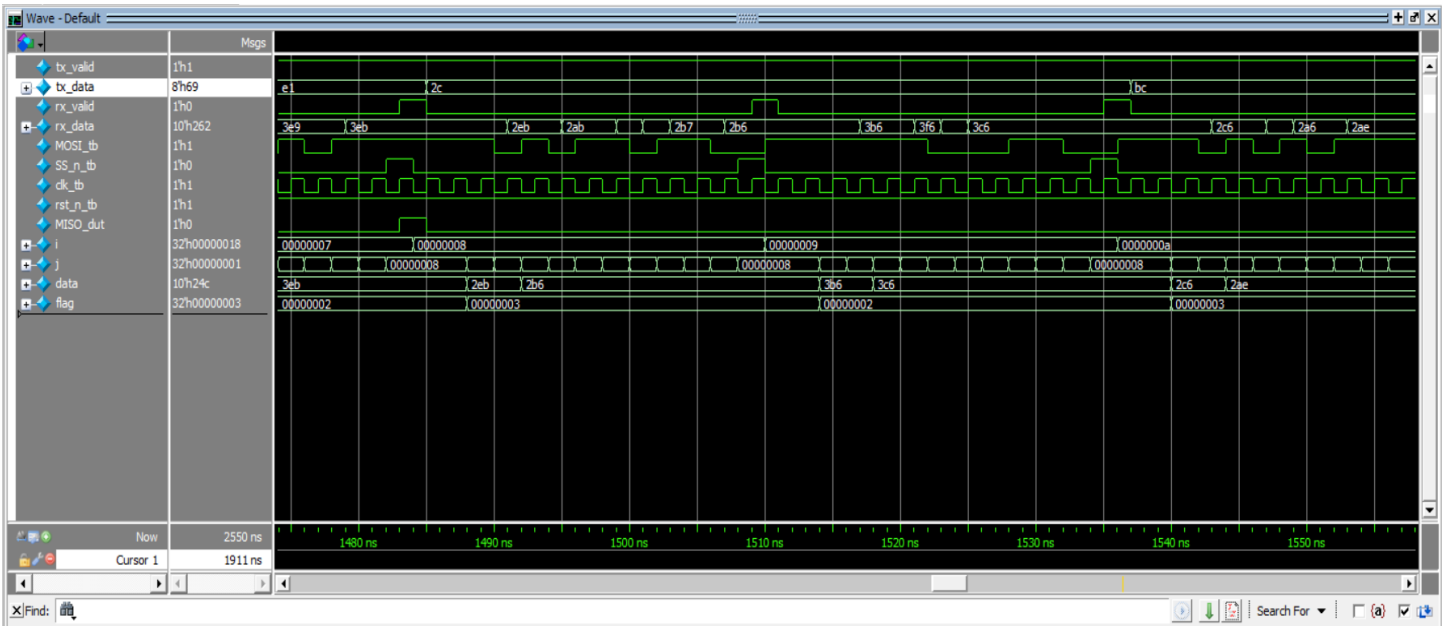
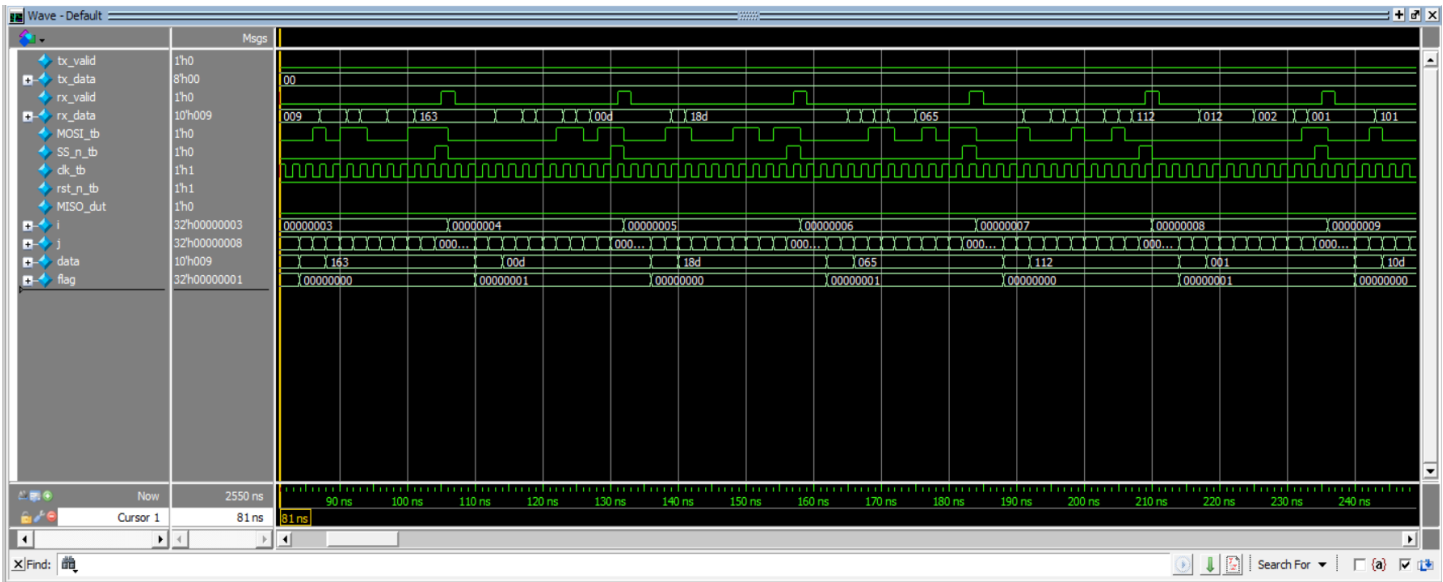
```

```
$monitor("MOSI_tb=%d,SS_n_tb=%d,rst_n_tb=%d,MISO_dut=%d,rx_data=%d,rx_valid=%d,tx_data=%d,tx_valid=%d")
,MOSI_tb,SS_n_tb,rst_n_tb,MISO_dut,DUT.rx_valid,DUT.rx_valid, DUT.tx_data,DUT.tx_valid);
end
endmodule
```

2.Simulation Tool:

- Do File:
vlib work
vlog SPI_Wrapper.v SPI_Slave.v Ram.v project_2_tb.v
vsim -voptargs=+acc work.SPI_Wrapper_tb
add wave -position insertpoint \
sim:/SPI_Wrapper_tb/DUT/tx_valid
add wave -position insertpoint \
sim:/SPI_Wrapper_tb/DUT/tx_data
add wave -position insertpoint \
sim:/SPI_Wrapper_tb/DUT/rx_valid
add wave -position insertpoint \
sim:/SPI_Wrapper_tb/DUT/rx_data
add wave *
run -all
//quit -sim

- Wave Form:



3.Synthesis Tool:

- Constraint File:

```
## This file is a general .xdc for the Basys3 rev B board
## To use it in a project:
## - uncomment the lines corresponding to used pins
## - rename the used ports (in each line, after get_ports) according to the top level signal
names in the project

## Clock signal
set_property -dict { PACKAGE_PIN W5    IOSTANDARD LVCMOS33 } [get_ports clk]
create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk]

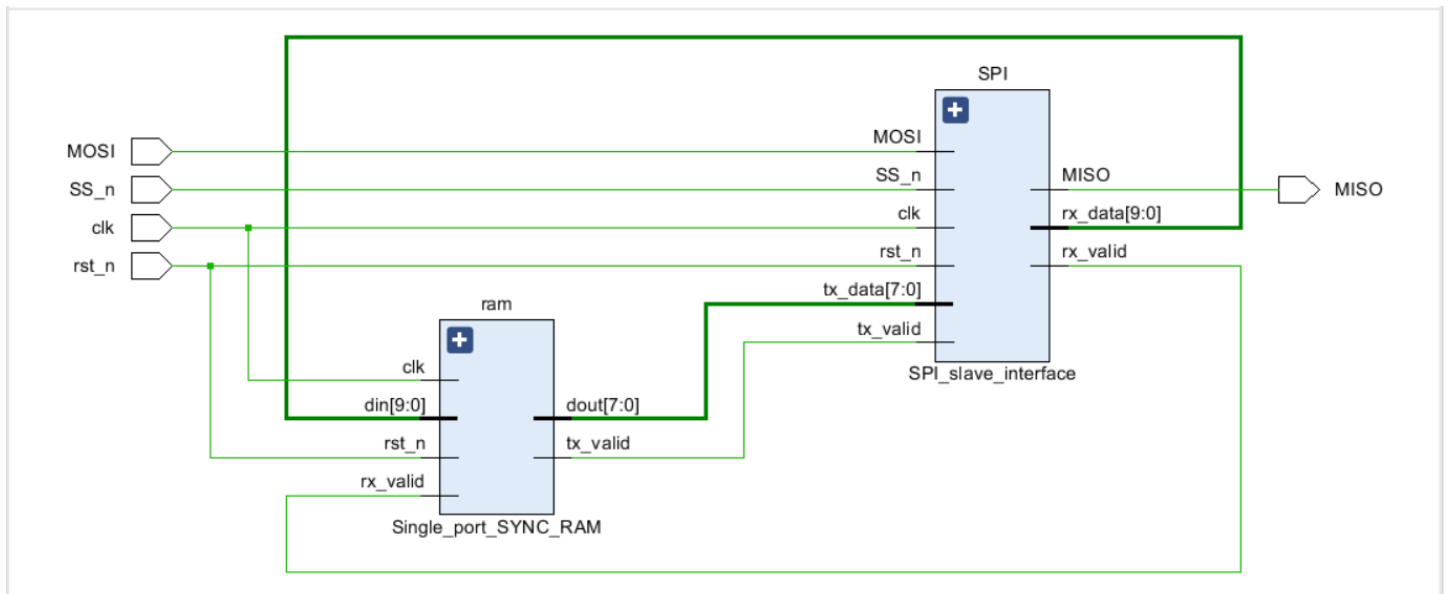
## Switches
set_property -dict { PACKAGE_PIN V17    IOSTANDARD LVCMOS33 } [get_ports {rst_n}]
set_property -dict { PACKAGE_PIN V16    IOSTANDARD LVCMOS33 } [get_ports {SS_n}]
set_property -dict { PACKAGE_PIN W16    IOSTANDARD LVCMOS33 } [get_ports {MOSI}]

## LEDs
set_property -dict { PACKAGE_PIN U16    IOSTANDARD LVCMOS33 } [get_ports {MISO}]

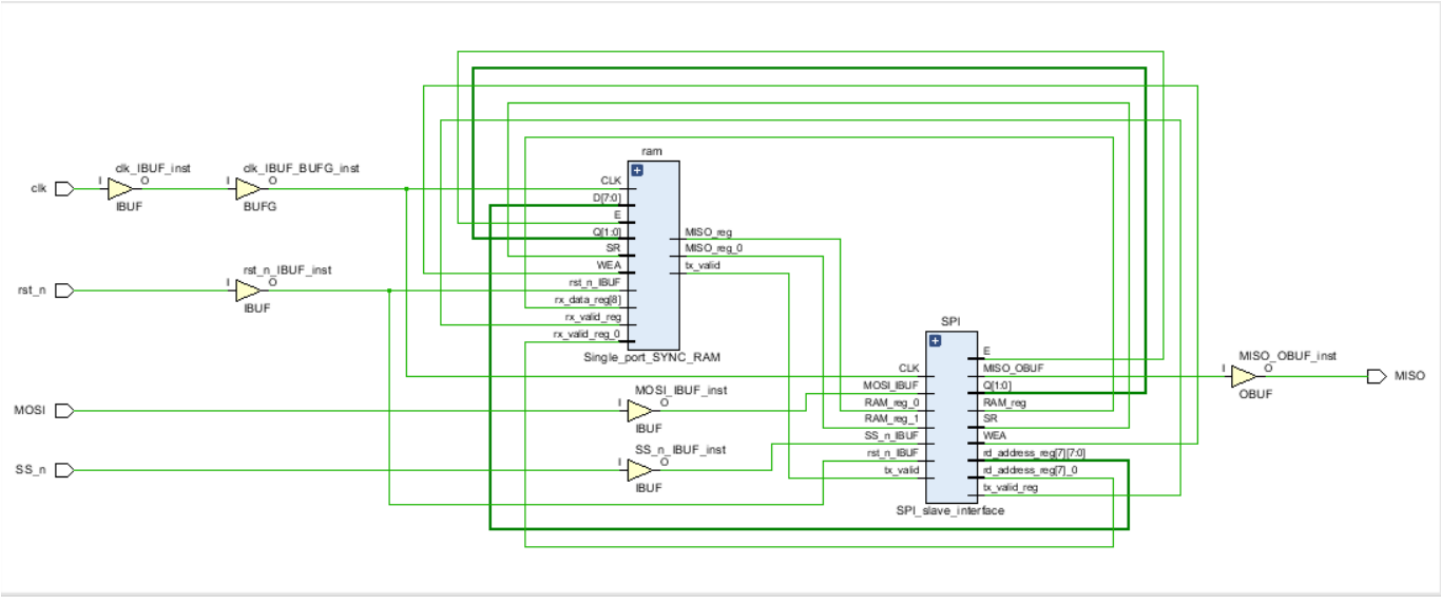
## Configuration options, can be used for all designs
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCC0 [current_design]

## SPI configuration mode options for QSPI boot, can be used for all designs
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.CONFIGRATE 33 [current_design]
set_property CONFIG_MODE SPIx4 [current_design]
```

- Sequential Encoding:
- Elaboration:



• Synthesis:



Name	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
✓ N SPI_Wrapper	32	37	0.5	5	1
ram (Single_port_SYN...	2	17	0.5	0	0
SPI (SPI_slave_interfa...	30	20	0	0	0

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.898 ns	Worst Hold Slack (WHS): 0.139 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 85	Total Number of Endpoints: 85	Total Number of Endpoints: 40
All user specified timing constraints are met.		

- Implementation:
 - Without Set Up Debug:

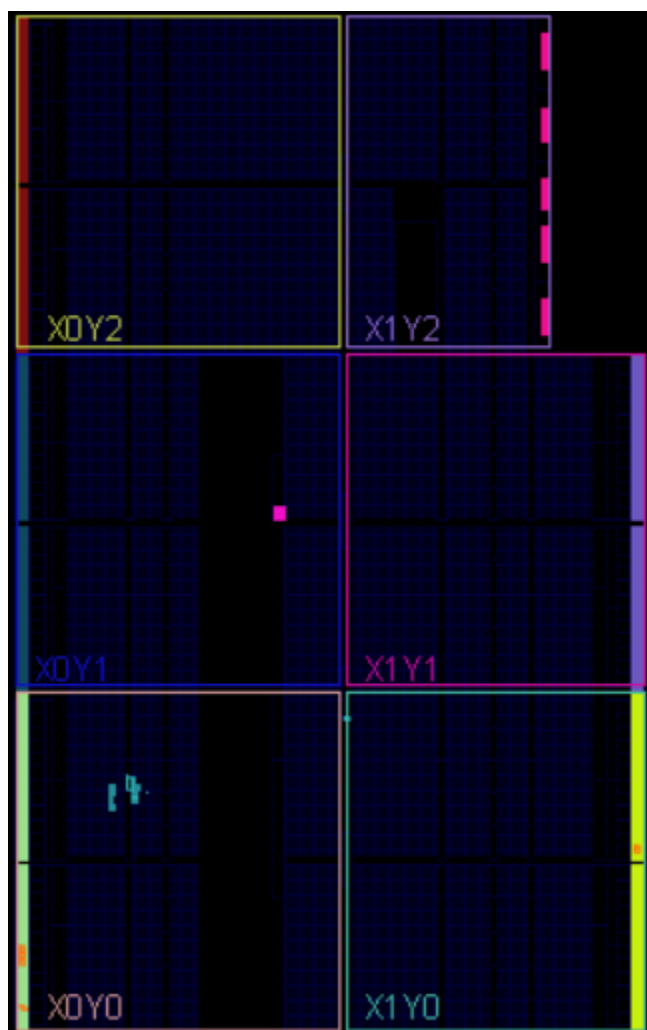
Tcl Console Messages x Log Reports Design Runs Power Methodology Timing ? _ □ □

Warning (1) Info (245) Status (491) Show All

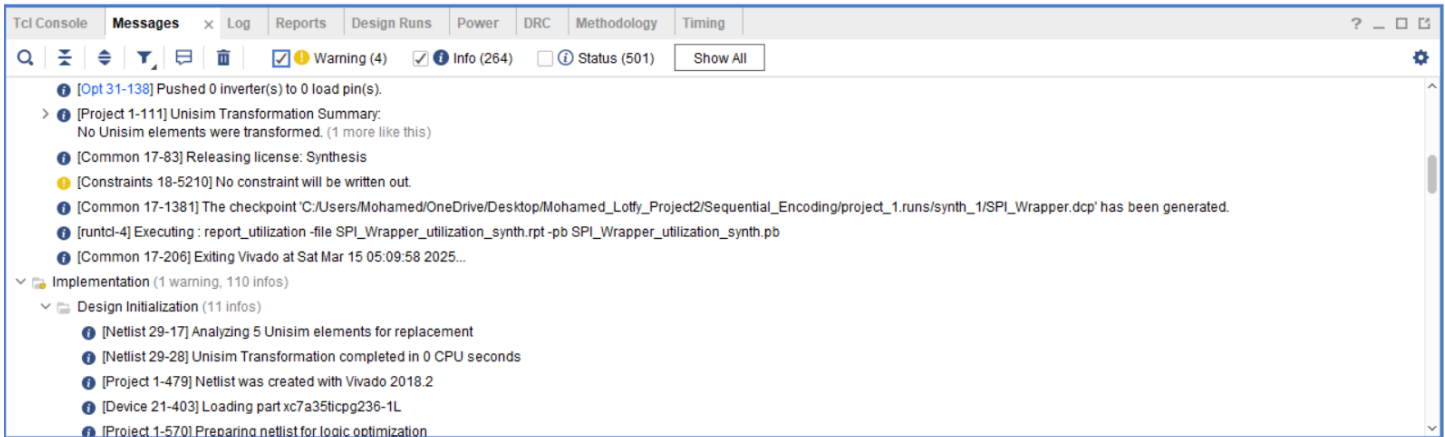
- [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'sequential' in module 'SPI_slave_interface'
- [Synth 8-4480] The timing for the instance i_0/ram/RAM_reg (implemented as a block RAM) might be sub-optimal as no optional output register could be merged into the block ram. Providing additional output register may help in improving timing. (1 more like this)
- [Project 1-571] Translating synthesized netlist
- [Netlist 29-17] Analyzing 5 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- [Project 1-570] Preparing netlist for logic optimization (1 more like this)
- [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed. (1 more like this)
- [Common 17-83] Releasing license: Synthesis
- [Constraints 18-5210] No constraint will be written out.
- [Common 17-1381] The checkpoint 'C:/Users/Mohamed/OneDrive/Desktop/Final_Project/project_1/project_1.runs/synth_1/SPI_Wrapper.dcp' has been generated.
- [runtcl-4] Executing : report_utilization -file SPI_Wrapper_utilization_synth.rpt -pb SPI_Wrapper_utilization_synth.pb

Name	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
▼ N SPI_Wrapper	32	37	0.5	5	1
ram (Single_port_SYN...	2	17	0.5	0	0
SPI (SPI_slave_interfa...	30	20	0	0	0

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.545 ns	Worst Hold Slack (WHS): 0.101 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 86	Total Number of Endpoints: 86	Total Number of Endpoints: 40
All user specified timing constraints are met.		



○ Using Set Up Debug :



Setup

Worst Negative Slack (WNS): 4.186 ns
 Total Negative Slack (TNS): 0.000 ns
 Number of Failing Endpoints: 0
 Total Number of Endpoints: 3775

Hold

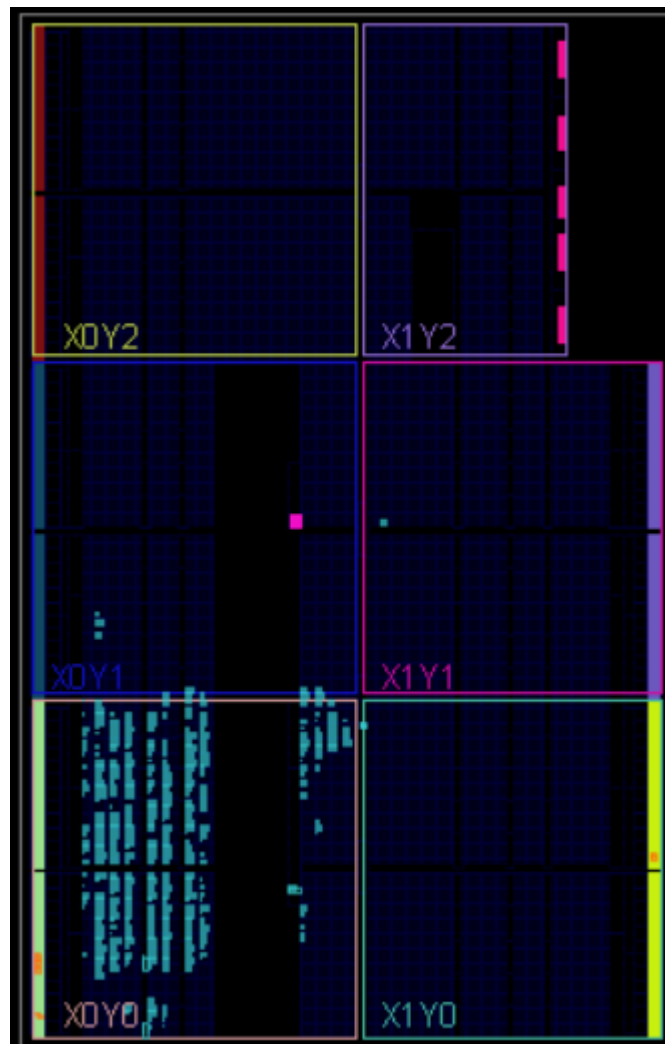
Worst Hold Slack (WHS): 0.047 ns
 Total Hold Slack (THS): 0.000 ns
 Number of Failing Endpoints: 0
 Total Number of Endpoints: 3759

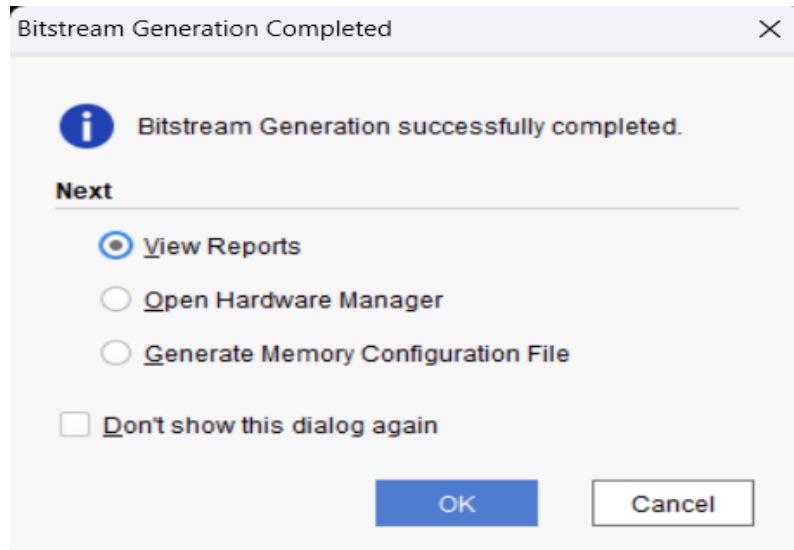
Pulse Width

Worst Pulse Width Slack (WPWS): 3.750 ns
 Total Pulse Width Negative Slack (TPWS): 0.000 ns
 Number of Failing Endpoints: 0
 Total Number of Endpoints: 2076

All user specified timing constraints are met.

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (815 0)	LUT as Logic (20800)	LUT as Memory (9600)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)	BSCANE2 (4)
▼ N SPI_Wrapper	1221	1899	8	608	1118	103	719	1	5	2	1
> 🛠️ dbg_hub (dbg_hub)	475	727	0	239	451	24	311	0	0	1	1
🛠️ ram (Single_port_SYN...	2	17	0	5	2	0	0	0.5	0	0	0
🛠️ SPI (SPI_slave_interfa...	30	20	0	17	30	0	10	0	0	0	0
> 🛠️ u_ila_0 (u_ila_0)	714	1135	8	358	635	79	396	0.5	0	0	0





SPI_Wrapper_45780.backup.vdi																
00000000	00	01	02	03	04	05	06	07	08	09	0a	0b	0c	0d	0e	0f
00000000	23	2d	2d	2d	2d	2d	2d	2d	2d	2d	2d	2d	2d	2d	2d	2d
00000010	2d	2d	2d	2d	2d	2d	2d	2d	2d	2d	2d	2d	2d	2d	2d	2d
00000020	2d	2d	2d	2d	2d	2d	2d	2d	2d	2d	2d	2d	2d	2d	2d	2d
00000030	2d	2d	2d	2d	2d	2d	2d	2d	2d	2d	2d	2d	0a	23	20	56
00000040	69	76	61	64	6f	20	76	32	30	31	38	2e	32	20	28	36
00000050	34	2d	62	69	74	29	0a	23	20	53	57	20	42	75	69	6c
00000060	64	20	32	32	35	38	36	34	36	20	6f	6e	20	54	68	75
00000070	20	4a	75	6e	20	31	34	20	32	30	3a	30	33	3a	31	32
00000080	20	4d	44	54	20	32	30	31	38	0a	23	20	49	50	20	42
00000090	75	69	6c	64	20	32	32	35	36	36	31	38	20	6f	6e	20
000000a0	54	68	75	20	4a	75	6e	20	31	34	20	32	32	3a	31	30
000000b0	3a	34	39	20	4d	44	54	20	32	30	31	38	0a	23	20	53
000000c0	74	61	72	74	20	6f	66	20	73	65	73	73	69	6f	6e	20
000000d0	61	74	3a	20	53	61	74	20	4d	61	72	20	31	35	20	30
000000e0	30	3a	33	38	3a	35	38	20	32	30	32	35	0a	23	20	50
000000f0	72	6f	63	65	73	73	20	49	44	3a	20	34	35	37	38	30
00000100	0a	23	20	43	75	72	72	65	6e	74	20	64	69	72	65	63
00000110	74	6f	72	79	3a	20	43	3a	2f	55	73	65	72	73	2f	4d
00000120	6f	68	61	6d	65	64	2f	4f	6e	65	44	72	69	76	65	2f
00000130	44	65	73	6b	74	6f	70	2f	46	69	6e	61	6c	5f	50	72
00000140	6f	6a	65	63	74	2f	70	72	6f	6a	65	63	74	5f	31	2f
00000150	70	72	6f	6a	65	63	74	5f	31	2e	72	75	6e	73	2f	69
00000160	6d	70	6c	5f	31	0a	23	20	43	6f	6d	6d	61	6e	64	20
00000170	6c	69	6e	65	3a	20	76	69	76	61	64	6f	2e	65	78	65
00000180	20	2d	6c	6f	67	20	53	50	49	5f	57	72	61	70	70	65
00000190	72	2e	76	64	69	20	2d	61	70	70	6c	6f	67	20	2d	70
000001a0	72	6f	64	75	63	74	20	56	69	76	61	64	6f	20	2d	6d
000001b0	65	72	72	61	67	65	44	62	70	76	60	76	61	64	6f	20

- Gray Encoding:
 - Elaboration:

Tcl Console Messages x Log Reports Design Runs

Info (15) Status (11) Show All

Vivado Commands (3 infos)

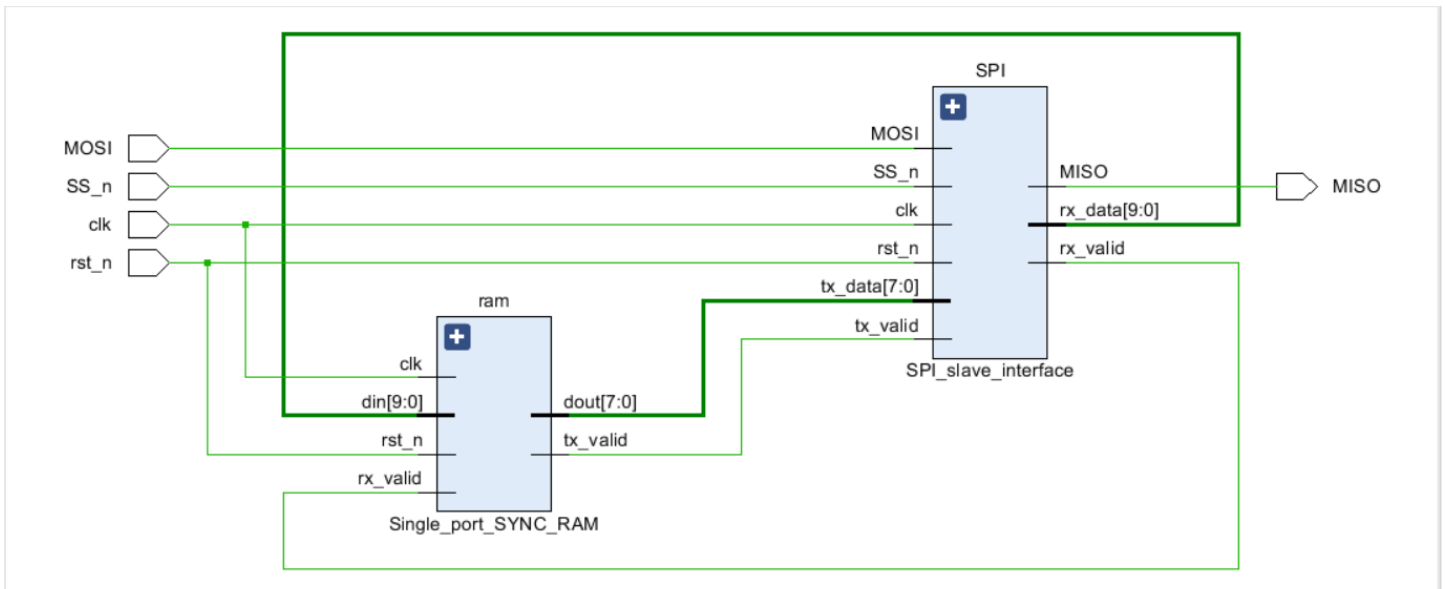
General Messages (3 infos)

- [IP_Flow 19-234] Refreshing IP repositories
- [IP_Flow 19-1704] No user IP repositories specified
- [IP_Flow 19-2313] Loaded Vivado IP repository 'D:/Vivado/2018.2/data/ip'.

Elaborated Design (12 infos)

General Messages (12 infos)

- [Synth 8-6157] synthesizing module 'SPI_Wrapper' [SPI_Wrapper.v:1] (2 more like this)
- [Synth 8-5534] Detected attribute (* fsm_encoding = "gray" *) [SPI_Slave.v:19]
- [Synth 8-155] case statement is not full and has no default [SPI_Slave.v:81]
- [Synth 8-6155] done synthesizing module 'Single_port_SYNC_RAM' (1#1) [Ram.v:1] (2 more like this)
- [Device 21-403] Loading part xc7a35ticipg236-1L
- [Project 1-570] Preparing netlist for logic optimization
- [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).



○ Synthesis:

Tcl Console Messages x Log Reports Design Runs Debug ? _ □

Warning (1) Info (52) Status (39) Show All

- [Project 1-571] Translating synthesized netlist
- [Netlist 29-17] Analyzing 5 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- > [Project 1-570] Preparing netlist for logic optimization (1 more like this)
- [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- > [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed. (1 more like this)
- [Common 17-83] Releasing license: Synthesis
- [Constraints 18-5210] No constraint will be written out.
- [Common 17-1381] The checkpoint 'C:/Users/Mohamed/OneDrive/Desktop/Final_Project/project_1/project_1.runs/synth_1/SPI_Wrapper.dcp' has been generated.
- [runctl-4] Executing : report_utilization -file SPI_Wrapper_utilization_synth.rpt -pb SPI_Wrapper_utilization_synth.pb
- [Common 17-206] Exiting Vivado at Sat Mar 15 00:54:17 2025...

✓ Synthesized Design (6 infos)

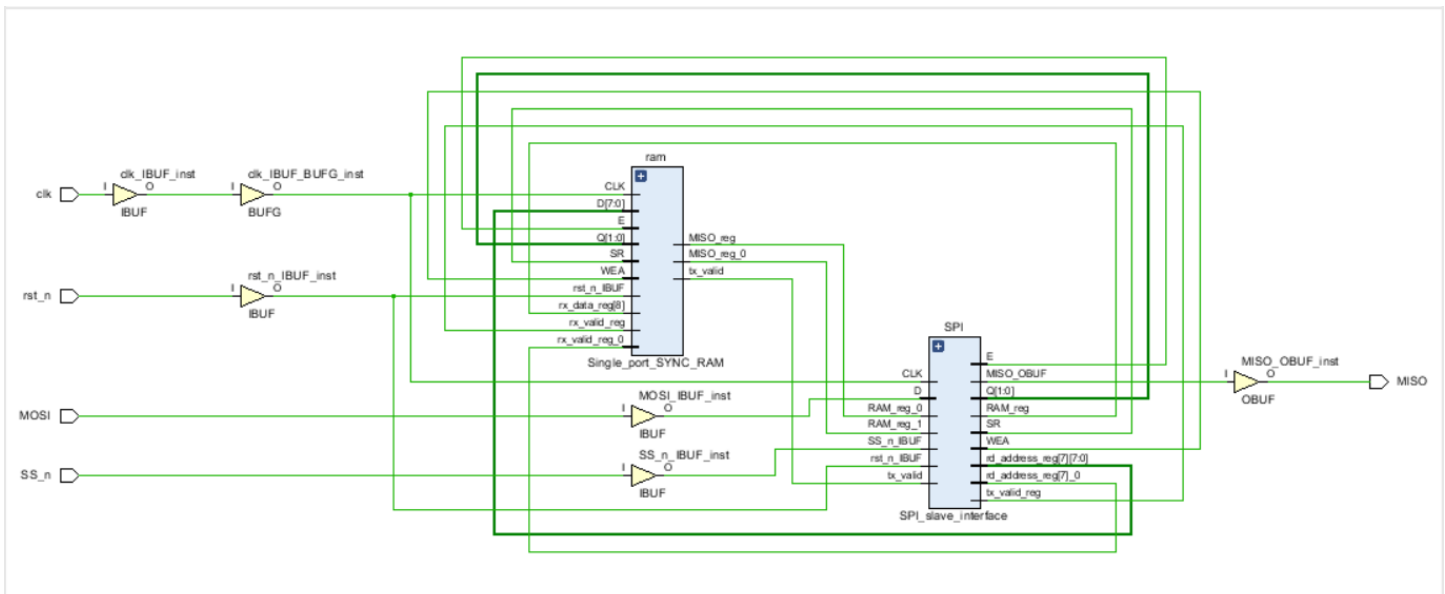
✓ General Messages (6 infos)

- [Netlist 29-17] Analyzing 5 Unisim elements for replacement

Name	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
✓ N SPI_Wrapper	32	37	0.5	5	1
ram (Single_port_SYN...	2	17	0.5	0	0
SPI (SPI_slave_interfa...	30	20	0	0	0

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.445 ns	Worst Hold Slack (WHS): 0.139 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 85	Total Number of Endpoints: 85	Total Number of Endpoints: 40

All user specified timing constraints are met.



- Implementation:
- Without Using Set Up Debug:

Tcl Console Messages x Log Reports Design Runs Power Methodology Timing

Warning (1) Info (239) Status (479) Show All

- [Netlist 29-17] Analyzing 5 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- [Project 1-570] Preparing netlist for logic optimization (1 more like this)
- [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed. (1 more like this)
- [Common 17-83] Releasing license: Synthesis
- [Constraints 18-5210] No constraint will be written out.
- [Common 17-1381] The checkpoint 'C:/Users/Mohamed/OneDrive/Desktop/Final_Project/project_2/project_2.runs/synth_1/SPI_Wrapper.dcp' has been generated.
- [runtcl-4] Executing : report_utilization -file SPI_Wrapper_utilization_synth.rpt -pb SPI_Wrapper_utilization_synth.pb
- [Common 17-206] Exiting Vivado at Sat Mar 15 02:53:08 2025...

Implementation (98 infos)

Design Initialization (11 infos)

- [Netlist 29-17] Analyzing 5 Unisim elements for replacement

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
SPI_Wrapper	33	37	19	33	9	0.5	5	1
ram (Single_port_SYN...	3	17	5	3	0	0.5	0	0
SPI (SPI_slave_interfa...	30	20	17	30	9	0	0	0

Setup

Worst Negative Slack (WNS): 5.390 ns
Total Negative Slack (TNS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 86

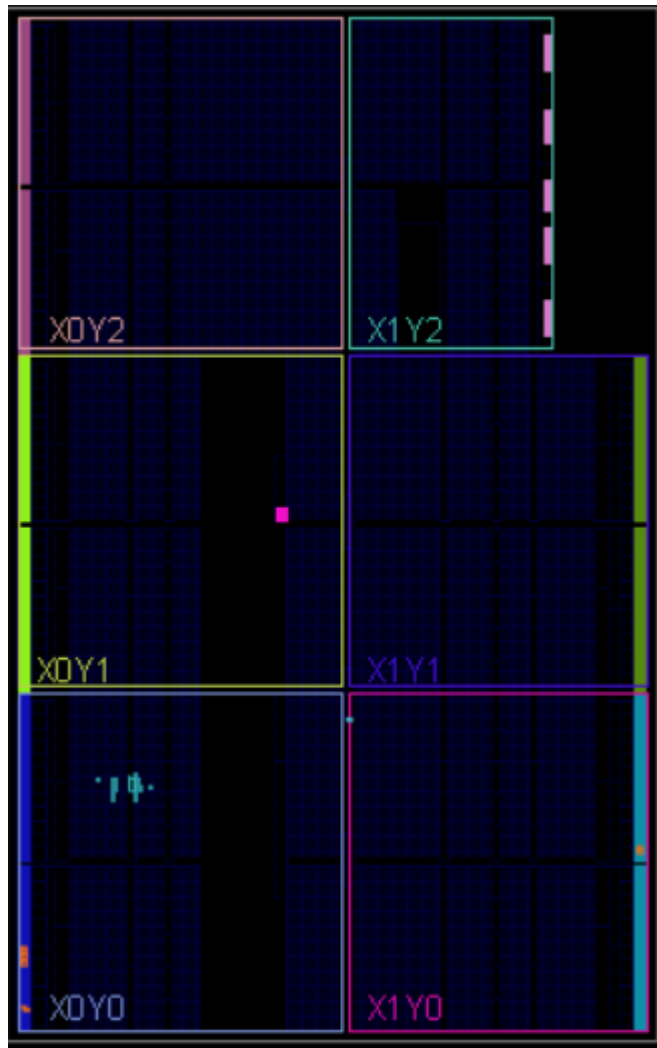
Hold

Worst Hold Slack (WHS): 0.096 ns
Total Hold Slack (THS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 86

Pulse Width

Worst Pulse Width Slack (WPWS): 4.500 ns
Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 40

All user specified timing constraints are met.



○ Using Set Up Debug:

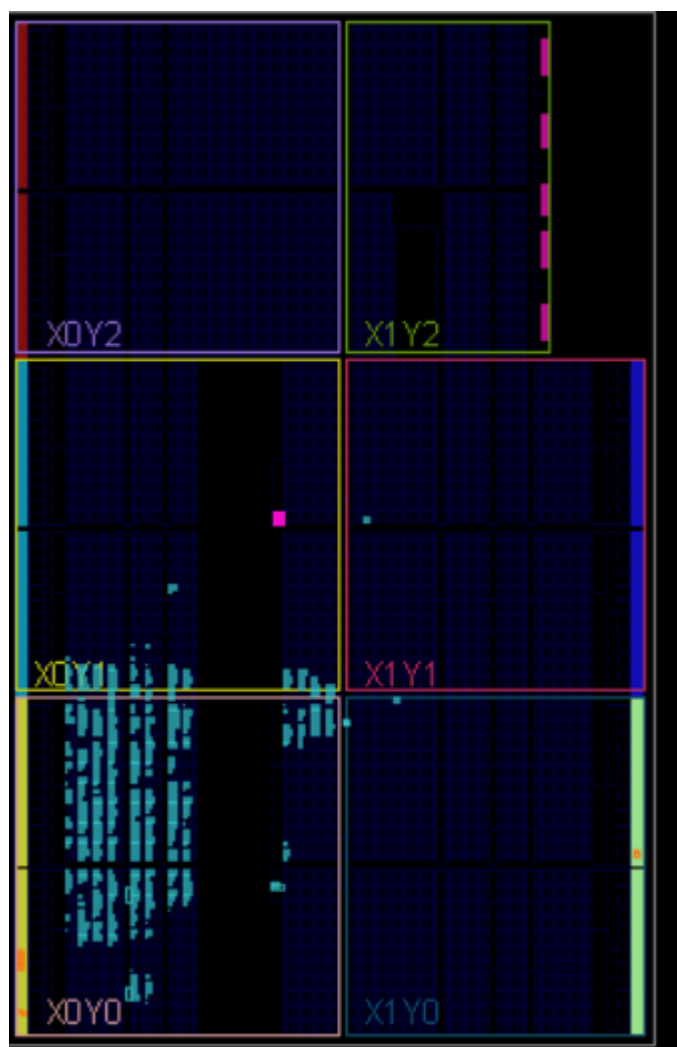
Tcl Console Messages x Log Reports Design Runs Power DRC Methodology Timing ?

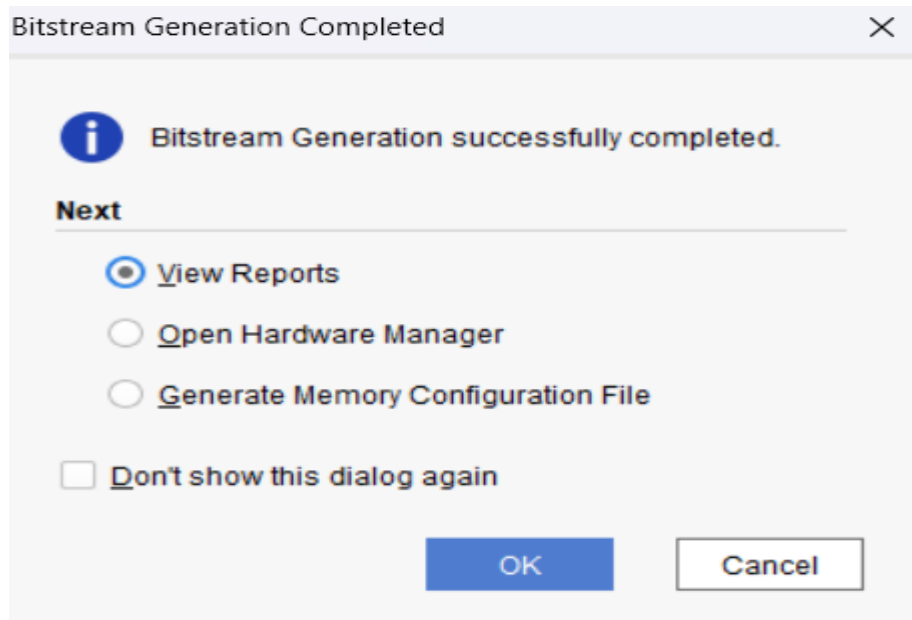
Warning (4) Info (263) Status (495) Show All

- [Common 17-1381] The checkpoint 'C:/Users/Mohamed/OneDrive/Desktop/Mohamed_Lotfy_Project2/Gray_Encoding/project_2.runs/impl_1/SPI_Wrapper_routed.dcp' has been generated.
- [IP_Flow 19-1839] IP Catalog is up to date.
- > [DRC 23-27] Running DRC with 2 threads (1 more like this)
 - [Coretd 2-168] The results of DRC are in file [SPI_Wrapper_drc_routed.rpt](#).
- > [runtcl-4] Executing : report_drc -file SPI_Wrapper_drc_routed.rpt -pb SPI_Wrapper_drc_routed.pb -rpx SPI_Wrapper_drc_routed.rpx (7 more like this)
- > [Timing 38-35] Done setting XDC timing constraints. (2 more like this)
 - [DRC 23-133] Running Methodology with 2 threads
 - [Coretd 2-1520] The results of Report Methodology are in file [SPI_Wrapper_methodology_drc_routed.rpt](#).
 - [Timing 38-436] There are set_bus_skew constraint(s) in this design. Please run report_bus_skew to ensure that bus skew requirements are met.
 - [Vivado_Tcl 4-545] No incremental reuse to report, no incremental placement and routing data was found.
- > [Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max, Timing Stage: Requireds. (1 more like this)
- > [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs (1 more like this)
- Implemented Design (1 warning, 10 Infos)
 - General Messages (1 warning, 10 Infos)

Name	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
▼ N SPI_Wrapper	32	37	0.5	5	1
dbg_hub (dbg_hub_CV)	0	0	0	0	0
ram (Single_port_SYN...	2	17	0.5	0	0
SPI (SPI_slave_interfa...	30	20	0	0	0
u_ila_0 (u_ila_0_CV)	0	0	0	0	0

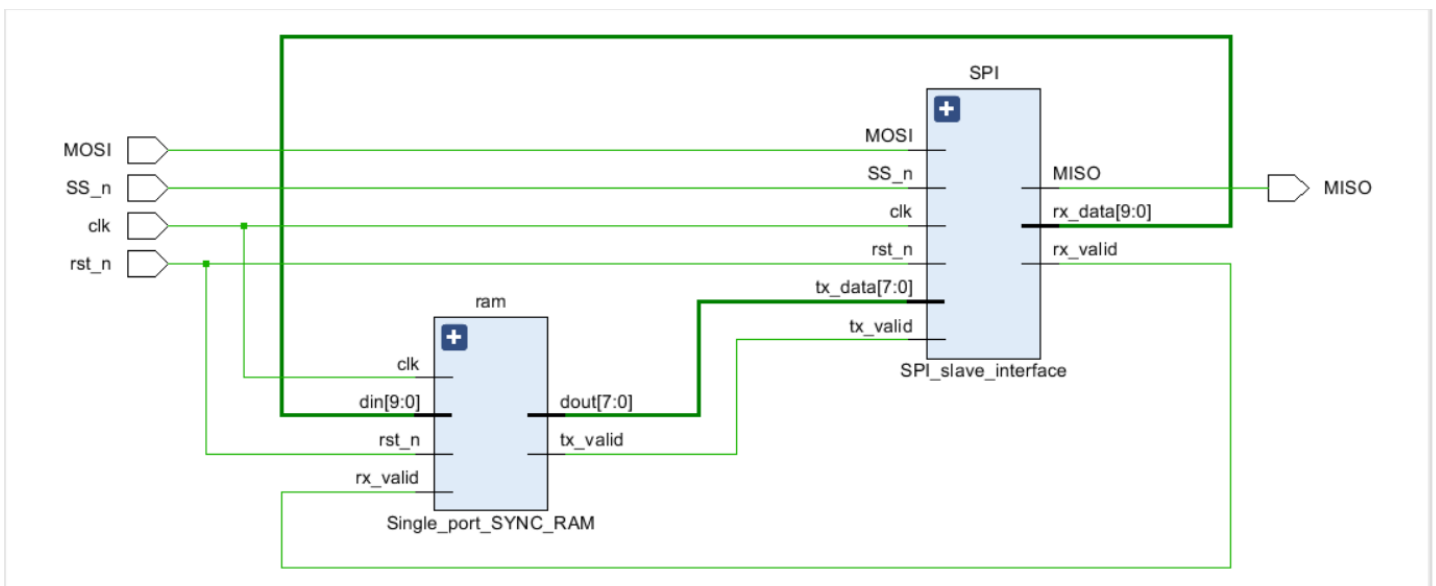
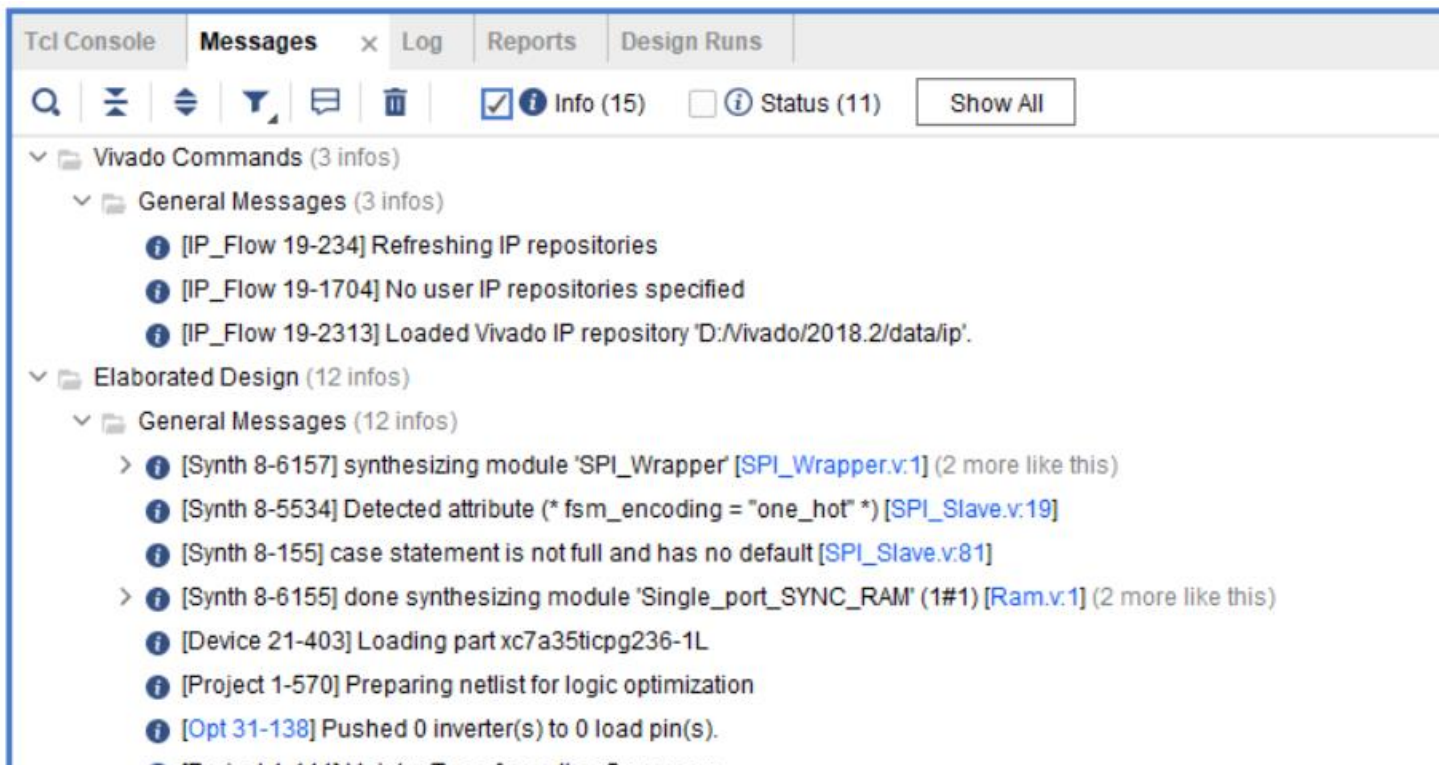
Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 4.041 ns	Worst Hold Slack (WHS): 0.069 ns	Worst Pulse Width Slack (WPWS): 3.750 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 3775	Total Number of Endpoints: 3759	Total Number of Endpoints: 2076
All user specified timing constraints are met.		





00000000						05	06	07	08	09	0a	0b	0c	0d	0e	0f
00000000	0a	b8	04	0a	ff	02	54	68	65	20	68	6f	73	74	20	4f
00000010	53	20	6f	6e	6c	79	20	61	6c	6c	6f	77	73	20	32	36
00000020	30	20	63	68	61	72	61	63	74	65	72	73	20	69	6e	20
00000030	61	20	6e	6f	72	6d	61	6c	20	70	61	74	68	2e	20	54
00000040	68	65	20	70	72	6f	6a	65	63	74	20	69	73	20	73	74
00000050	6f	72	65	64	20	69	6e	20	61	20	70	61	74	68	20	77
00000060	69	74	68	20	6d	6f	72	65	20	74	68	61	6e	20	38	30
00000070	20	63	68	61	72	61	63	74	65	72	73	2e	20	49	66	20
00000080	79	6f	75	20	65	78	70	65	72	69	65	6e	63	65	20	69
00000090	73	73	75	65	73	20	77	69	74	68	20	49	50	2c	20	42
000000a0	6c	6f	63	6b	20	44	65	73	69	67	6e	73	2c	20	6f	72
000000b0	20	66	69	6c	65	73	20	6e	6f	74	20	62	65	69	6e	67
000000c0	20	66	6f	75	6e	64	2c	20	70	6c	65	61	73	65	20	63
000000d0	6f	6e	73	69	64	65	72	20	6d	6f	76	69	6e	67	20	74
000000e0	68	65	20	70	72	6f	6a	65	63	74	20	74	6f	20	61	20
000000f0	6c	6f	63	61	74	69	6f	6e	20	77	69	74	68	20	61	20
00000100	73	68	6f	72	74	65	72	20	70	61	74	68	2e	20	41	6c
00000110	74	65	72	6e	61	74	65	6c	79	20	63	6f	6e	73	69	64
00000120	65	72	20	75	73	69	6e	67	20	74	68	65	20	4f	53	20
00000130	73	75	62	73	74	20	63	6f	6d	6d	61	6e	64	20	74	6f
00000140	20	6d	61	70	20	70	61	72	74	20	6f	66	20	74	68	65
00000150	20	70	61	74	68	20	74	6f	20	61	20	64	72	69	76	65
00000160	20	6c	65	74	74	65	72	2e	0a	43	75	72	72	65	6e	74
00000170	20	70	72	6f	6a	65	63	74	20	70	61	74	68	20	69	73
00000180	20	27	25	73	27	10	05	1a	01	35	2a	0b	70	72	6f	6a
00000190	65	63	74	62	61	73	65	32	91	01	0a	7d	63	3a	2f	55
000001a0	73	65	72	73	2f	4d	6f	68	61	6d	65	64	2f	4f	6e	65
000001b0	44	72	60	76	65	2f	44	65	72	6b	74	6f	70	2f	46	60

- One_hot Encoding:
 - Elaboration:



○ Synthesis:

Tcl Console Messages x Log Reports Design Runs Debug

Warning (1) Info (40) Status (19) Show All

- [Netlist 29-17] Analyzing 5 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- > [Project 1-570] Preparing netlist for logic optimization (1 more like this)
- [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- > [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed. (1 more like this)
- [Common 17-83] Releasing license: Synthesis
- [Constraints 18-5210] No constraint will be written out.
- [Common 17-1381] The checkpoint 'C:/Users/Mohamed/OneDrive/Desktop/Final_Project/project_3/project_3.runs/synth_1/SPI_Wrapper.dcp' has been generated.
- [runtcl-4] Executing : report_utilization -file SPI_Wrapper_utilization_synth.rpt -pb SPI_Wrapper_utilization_synth.pb
- [Common 17-206] Exiting Vivado at Sat Mar 15 02:21:11 2025...

▼ Synthesized Design (6 infos)

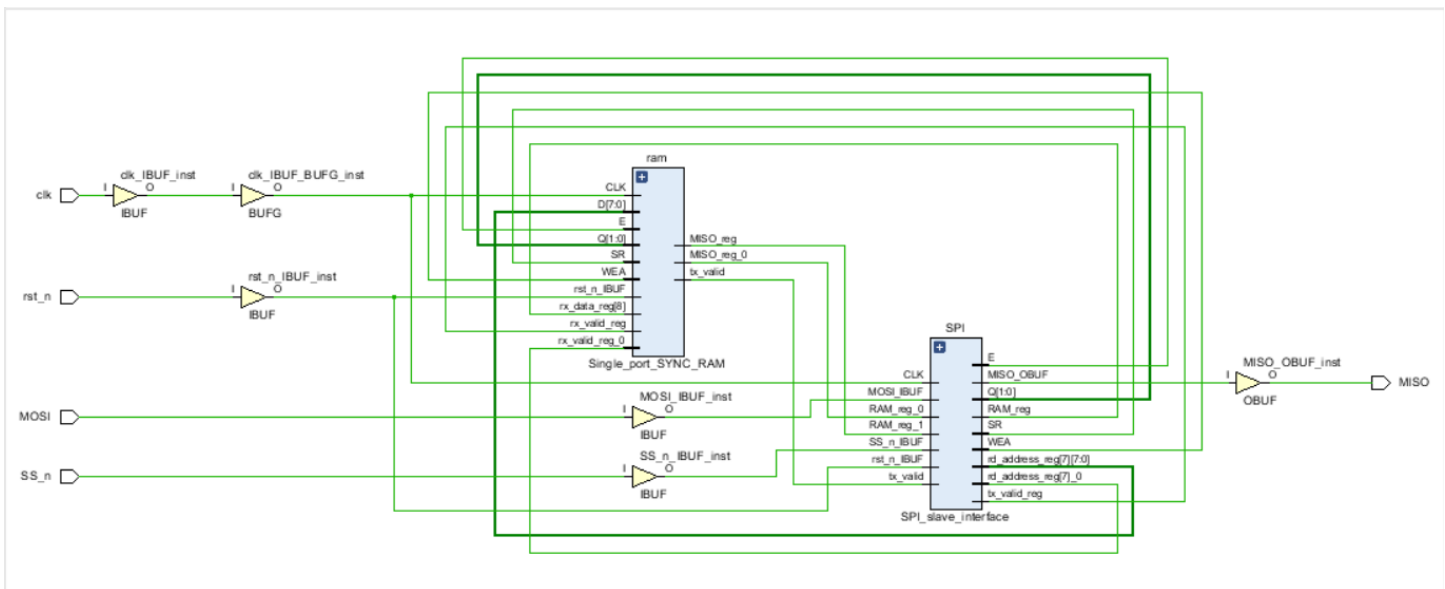
▼ General Messages (6 infos)

- [Netlist 29-17] Analyzing 5 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

Name	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
▼ N SPI_Wrapper	35	39	0.5	5	1
ram (Single_port_SYN...	2	17	0.5	0	0
SPI (SPI_slave_interfa...	33	22	0	0	0

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.898 ns	Worst Hold Slack (WHS): 0.142 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 87	Total Number of Endpoints: 87	Total Number of Endpoints: 42

All user specified timing constraints are met.



○ Implementation:

Tcl Console Messages x Log Reports Design Runs Power Methodology Timing

Warning (1) Info (241) Status (477) Show All

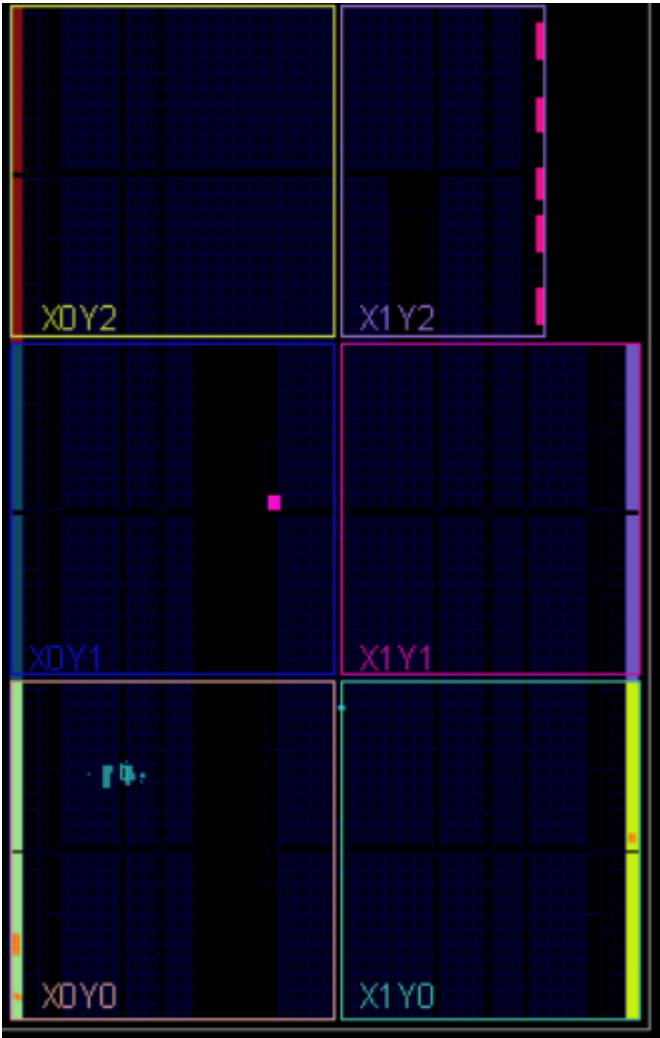
- [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed. (1 more like this)
- [Common 17-83] Releasing license: Synthesis
- [Constraints 18-5210] No constraint will be written out.
- [Common 17-1381] The checkpoint 'C:/Users/Mohamed/OneDrive/Desktop/Final_Project/project_3/project_3.runs/synth_1/SPI_Wrapper.dcp' has been generated.
- [runtcl-4] Executing : report_utilization -file SPI_Wrapper_utilization_synth.rpt -pb SPI_Wrapper_utilization_synth.pb
- [Common 17-206] Exiting Vivado at Sat Mar 15 03:01:27 2025...

Implementation (99 Infos)

- Design Initialization (11 infos)
 - [Netlist 29-17] Analyzing 5 Unisim elements for replacement
 - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
 - [Project 1-479] Netlist was created with Vivado 2018.2
 - [Device 21-403] Loading part xc7a35ticpg236-1L
 - [Project 1-570] Preparing netlist for logic optimization

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
▼ N SPI_Wrapper	36	39	17	36	12	0.5	5	1
ram (Single_port_SYN...	3	17	5	3	0	0.5	0	0
SPI (SPI_slave_interfa...	33	22	15	33	12	0	0	0

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.648 ns	Worst Hold Slack (WHS): 0.042 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 88	Total Number of Endpoints: 88	Total Number of Endpoints: 42
All user specified timing constraints are met.		



○ Using Set Up Debug:

Tcl Console Messages x Log Reports Design Runs DRC Power Methodology Timing ? _ □ ✕

🔍 ⚙️ ⚠️ Warning (4) ⓘ Info (264) ⚙️ Status (503) Show All ⚙️

- ❗ [Project 1-236] Implementation specific constraints were found while reading constraint file [C:/Users/Mohamed/OneDrive/Desktop/Final_Project/Constraints_basys3.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [Xil/SPI_Wrapper_proplmpt.xdc]. Resolution: To avoid this warning, move constraints listed in [Undefined] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
- ❗ [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'SPI_slave_interface'
- > ❗ [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5) (3 more like this)
- ❗ [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'SPI_slave_interface'
- > ❗ [Synth 8-4480] The timing for the instance i_0/ram/RAM_reg (implemented as a block RAM) might be sub-optimal as no optional output register could be merged into the block ram. Providing additional output register may help in improving timing. (1 more like this)
- ❗ [Project 1-571] Translating synthesized netlist
- ❗ [Netlist 29-17] Analyzing 5 Unisim elements for replacement
- ❗ [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- > ❗ [Project 1-570] Preparing netlist for logic optimization (1 more like this)
- ❗ [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- > ❗ [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed. (1 more like this)

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (815 0)	LUT as Logic (20800)	LUT as Memory (9600)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)	BSCANE2 (4)
▼ N SPI_Wrapper	1224	1901	8	605	1121	103	708	1	5	2	1
> 🛠️ dbg_hub (dbg_hub)	475	727	0	234	451	24	306	0	0	1	1
🛠️ ram (Single_port_SYN...	2	17	0	5	2	0	0	0.5	0	0	0
🛠️ SPI (SPI_slave_interfa...	33	22	0	17	33	0	12	0	0	0	0
> 🛠️ u_ila_0 (u_ila_0)	714	1135	8	354	635	79	389	0.5	0	0	0

Setup

Worst Negative Slack (WNS): **4.400 ns**

Total Negative Slack (TNS): **0.000 ns**

Number of Failing Endpoints: **0**

Total Number of Endpoints: **3777**

Hold

Worst Hold Slack (WHS): **0.025 ns**

Total Hold Slack (THS): **0.000 ns**

Number of Failing Endpoints: **0**

Total Number of Endpoints: **3761**

Pulse Width

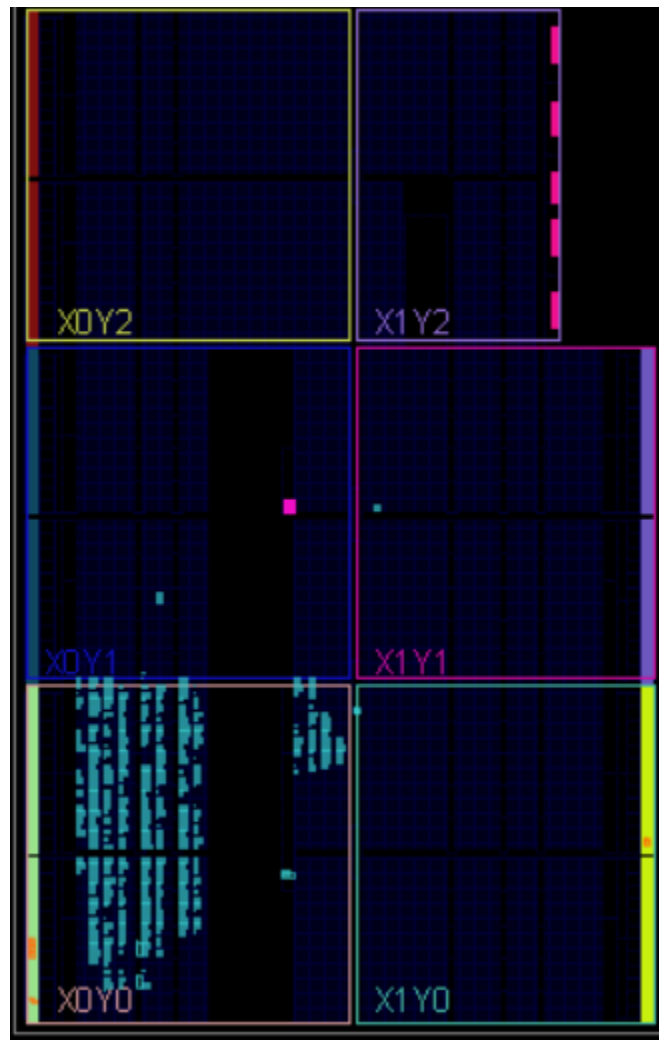
Worst Pulse Width Slack (WPWS): **3.750 ns**

Total Pulse Width Negative Slack (TPWS): **0.000 ns**

Number of Failing Endpoints: **0**

Total Number of Endpoints: **2078**

All user specified timing constraints are met.



Bitstream Generation Completed

i Bitstream Generation successfully completed.

Next

☒ View Reports

☐ Open Hardware Manager

☐ Generate Memory Configuration File

☐ Don't show this dialog again

OK Cancel

00000000	00	01	02	03	04	05	06	07	08	09	0a	0b	0c	0d	0e	0f
00000000	0a	b8	04	0a	ff	02	54	68	65	20	68	6f	73	74	20	4f
00000010	53	20	6f	6e	6c	79	20	61	6c	6c	6f	77	73	20	32	36
00000020	30	20	63	68	61	72	61	63	74	65	72	73	20	69	6e	20
00000030	61	20	6e	6f	72	6d	61	6c	20	70	61	74	68	2e	20	54
00000040	68	65	20	70	72	6f	6a	65	63	74	20	69	73	20	73	74
00000050	6f	72	65	64	20	69	6e	20	61	20	70	61	74	68	20	77
00000060	69	74	68	20	6d	6f	72	65	20	74	68	61	6e	20	38	30
00000070	20	63	68	61	72	61	63	74	65	72	73	2e	20	49	66	20
00000080	79	6f	75	20	65	78	70	65	72	69	65	6e	63	65	20	69
00000090	73	73	75	65	73	20	77	69	74	68	20	49	50	2c	20	42
000000a0	6c	6f	63	6b	20	44	65	73	69	67	6e	73	2c	20	6f	72
000000b0	20	66	69	6c	65	73	20	6e	6f	74	20	62	65	69	6e	67
000000c0	20	66	6f	75	6e	64	2c	20	70	6c	65	61	73	65	20	63
000000d0	6f	6e	73	69	64	65	72	20	6d	6f	76	69	6e	67	20	74
000000e0	68	65	20	70	72	6f	6a	65	63	74	20	74	6f	20	61	20
000000f0	6c	6f	63	61	74	69	6f	6e	20	77	69	74	68	20	61	20
00000100	73	68	6f	72	74	65	72	20	70	61	74	68	2e	20	41	6c
00000110	74	65	72	6e	61	74	65	6c	79	20	63	6f	6e	73	69	64
00000120	65	72	20	75	73	69	6e	67	20	74	68	65	20	4f	53	20
00000130	73	75	62	73	74	20	63	6f	6d	6d	61	6e	64	20	74	6f
00000140	20	6d	61	70	20	70	61	72	74	20	6f	66	20	74	68	65
00000150	20	70	61	74	68	20	74	6f	20	61	20	64	72	69	76	65
00000160	20	6c	65	74	74	65	72	2e	0a	43	75	72	72	65	6e	74
00000170	20	70	72	6f	6a	65	63	74	20	70	61	74	68	20	69	73
00000180	20	27	25	73	27	10	05	1a	01	35	2a	0b	70	72	6f	6a
00000190	65	63	74	62	61	73	65	32	91	01	0a	7d	63	3a	2f	55
000001a0	73	65	72	73	2f	4d	6f	68	61	6d	65	64	2f	4f	6e	65
000001b0	44	72	60	76	65	2f	44	65	72	6b	74	6f	70	2f	46	60