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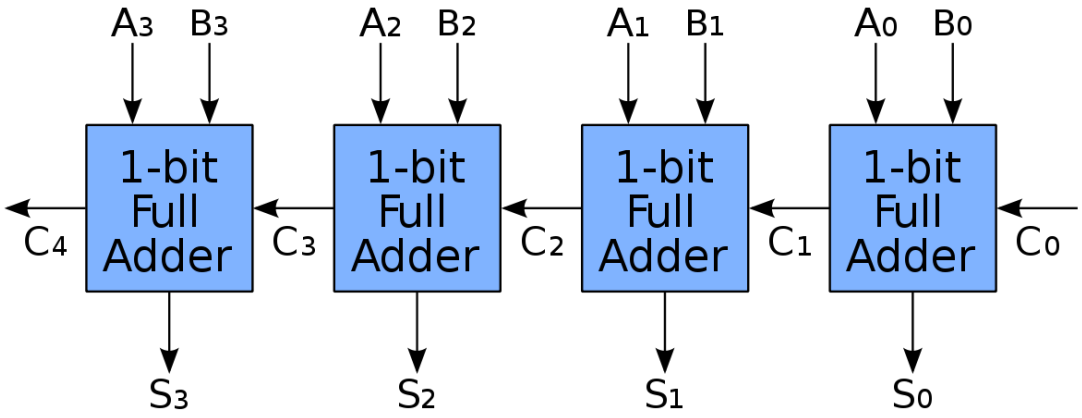
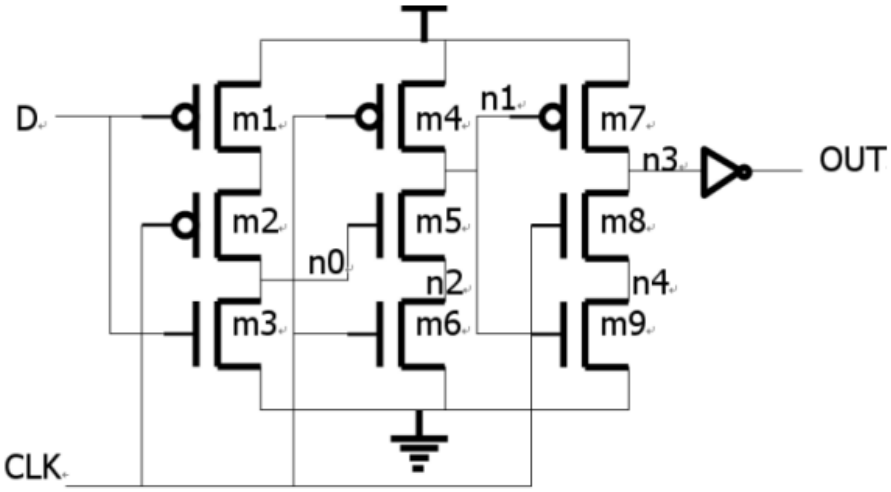
1. A 4-bit ripple adder as ahown at Fig.1 is designed with Fully Complementary Static Logic Gate for FA. Input signals are A[3:0], B[3:0] and Cin which are provided by a unit size inverter. Outputs are Sum[3:0] with loading of 5 unit size inverters connected in parallelism (FO5). You shall provide SPICE simulation results of timing and power waveforms.

(1) Try your best to design the fastest adder. First, show your block diagrams in terms of the 1-bit Full-Adder(FA). Second, show the circuit schematic of each block. Use logic effort concepts (you do not have to write down the procedure) to design transistor widths. Describe your design concept. (40%)

下圖是 4-bit ripple adder 的 block diagram，其中 A、B、C 皆有通過 INV 以及 DFF 才接到 FULL ADDER 的輸入，輸出也有接上 DFF。

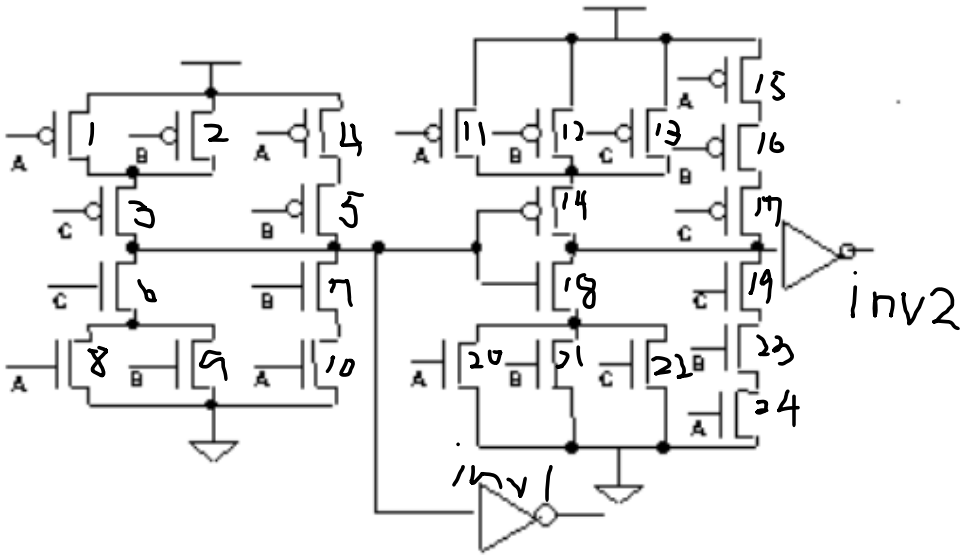




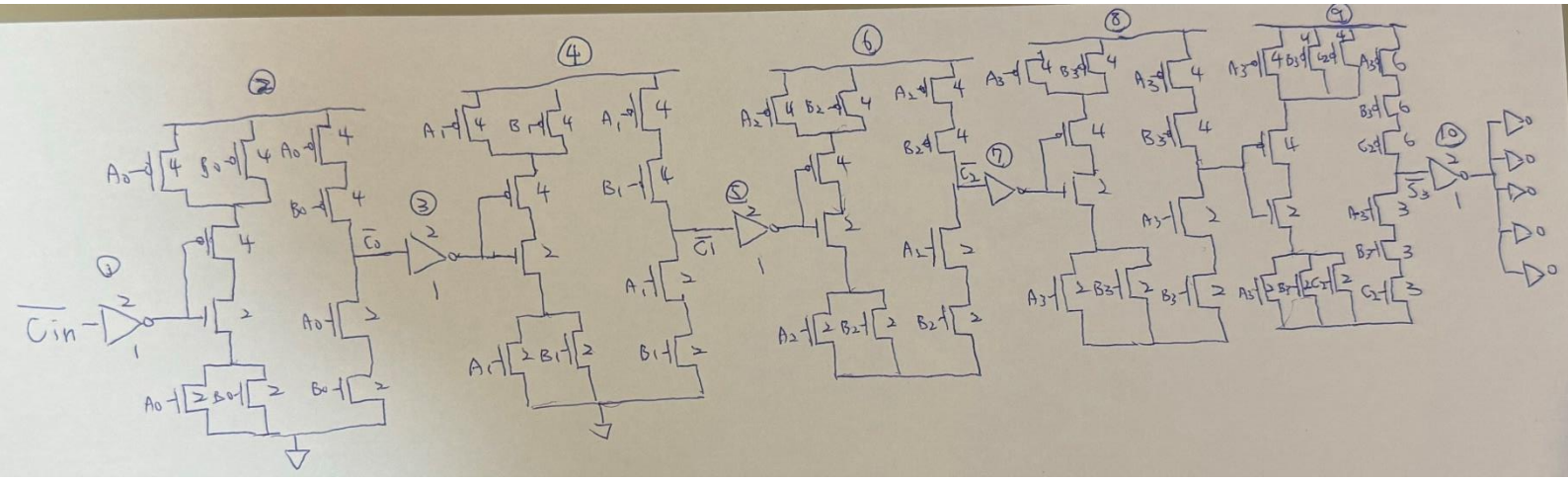
我根據講義對於此電路的分析來 sizing 此 DFF 的 transistor，而最後的 size 如下表。

	M1	M2	M3	M4	M5	M6	M7	M8	M9	INVp	INVn
nfin	4	4	2	4	2	2	4	2	2	2	1

而下圖是 1-bit Full Adder 的 Schematic，電晶體的編號會在 SIZING 的時候使用到



題目要求我們使用 logic effort concept 來 sizing 電晶體，因此我打算分析最長的那條 critical path，也就是 Cin 到 S3 的路徑，而下圖是這條路徑的架構圖。



而我們可以將電路分級來計算 logic effort，因題目說無須列出過程，則以下省略。

Level	1	2	3	4	5	6	7	8	9	10
g	3/3	4/3	3/3	6/3	3/3	6/3	3/3	6/3	9/3	3/3
P	3/3	12/3	3/3	12/3	3/3	12/3	3/3	12/3	15/3	3/3

透過計算 logic effort，並考慮 SUM 的每個 bit 都有接一組 FO5 的情況下，我會將四組 FULL ADDER 分開 SIZING，並且會越來越大。

第一級 full adder

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
nfin	1	1	1	1	1	7	7	7	7	7	5	5	5	5
	15	16	17	18	19	20	21	22	23	24	Inv1p	Inv1n	Inv2p	Inv2n
nfin	5	5	5	3	3	3	3	3	3	3	2	1	2	1

第二級 full adder

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
nfin	1	1	1	1	1	8	8	8	8	8	6	6	6	6
	15	16	17	18	19	20	21	22	23	24	Inv1p	Inv1n	Inv2p	Inv2n
nfin	6	6	6	4	4	4	4	4	4	4	2	1	2	1

第三級 full adder

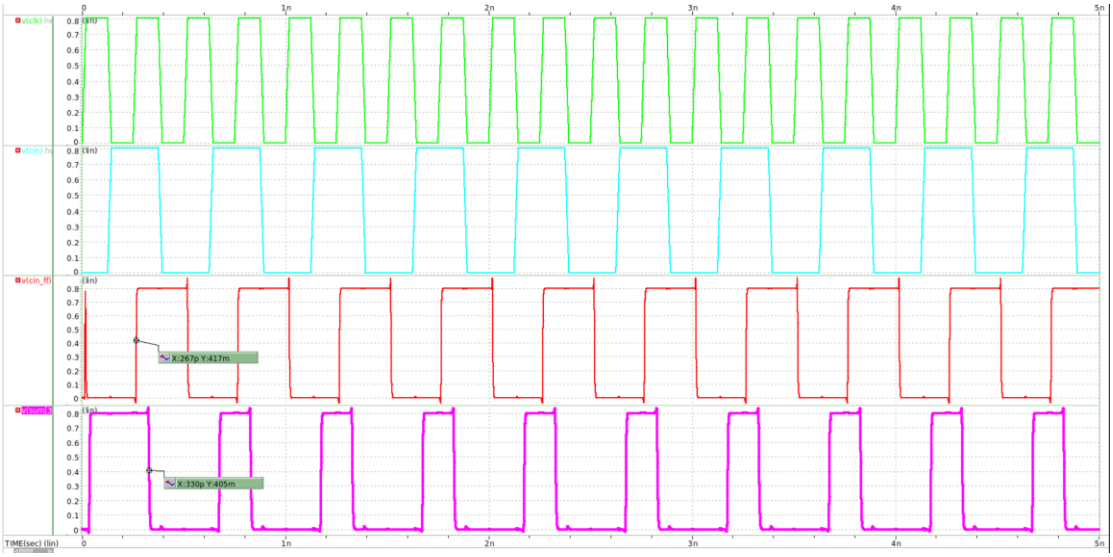
	1	2	3	4	5	6	7	8	9	10	11	12	13	14
nfin	1	1	1	1	1	9	9	9	9	9	7	7	7	7
	15	16	17	18	19	20	21	22	23	24	Inv1p	Inv1n	Inv2p	Inv2n
nfin	7	7	7	5	5	5	5	5	5	5	2	1	2	1

第四級 full adder

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
nfin	1	1	1	1	1	10	10	10	10	10	8	8	8	8
	15	16	17	18	19	20	21	22	23	24	Inv1p	Inv1n	Inv2p	Inv2n
nfin	8	8	8	6	6	6	6	6	6	6	2	1	2	1

(2) Based on the design of (1), run SPICE to find the the propagation delay time (with pattern from 000011110 to 000011111 (A[3:0]@B[3:0]@Cin). Determine the maximum propagation of a clock with the delay time estimated by SPICE. (20%)

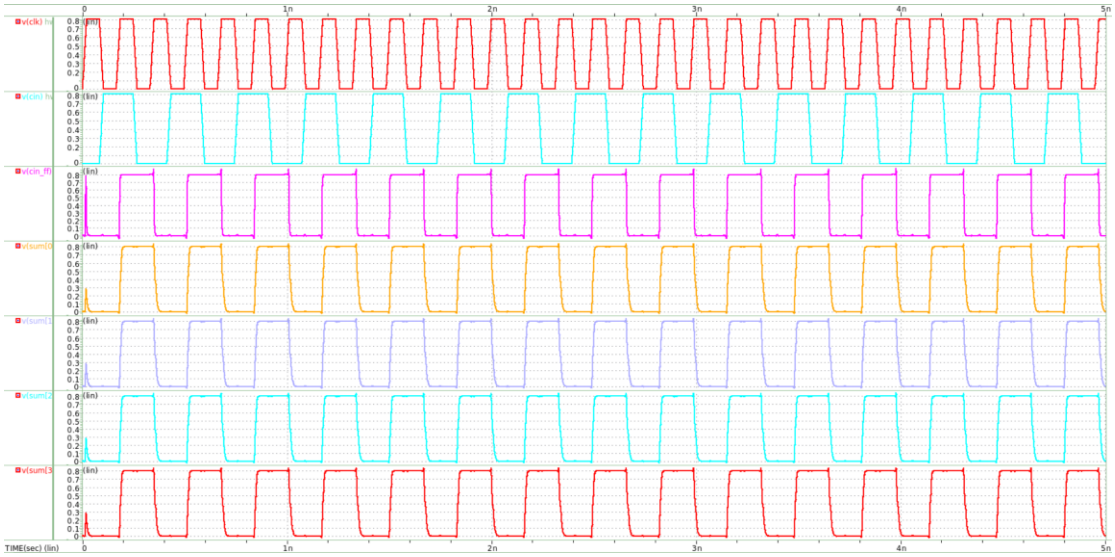
tpd 為經過 DFF 後的 Cin=0.5VDD 到 critical path 輸出=0.5VDD 的所花的時間，因此我在模擬時將 Cin 從 0 變成 VDD，並觀察波型，由下圖可看出 tpd=63ps。



而透過 meas 指令，可得出精確的 tpd=63.4306ps。

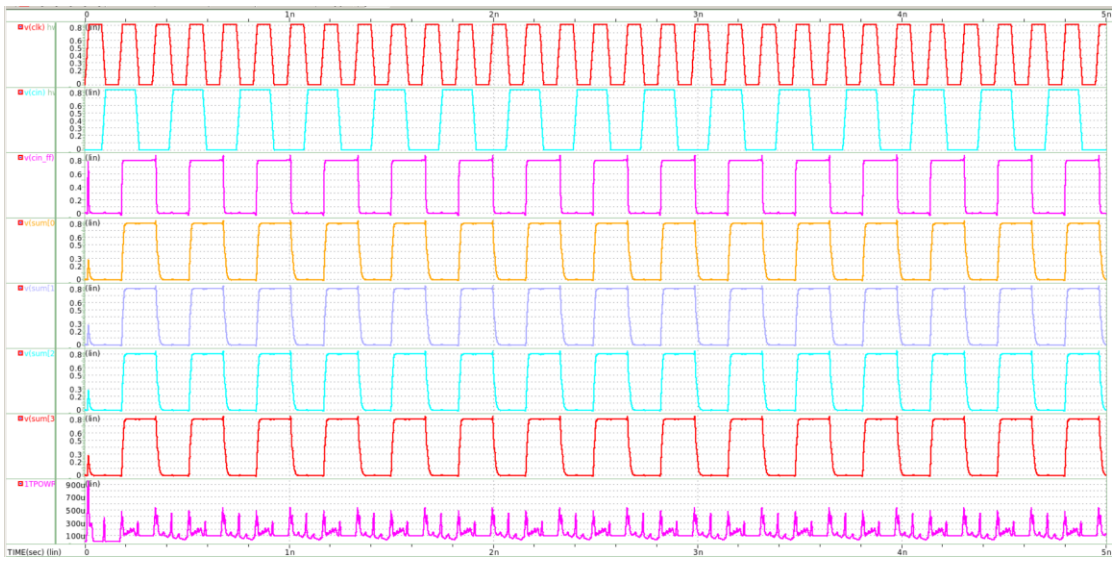
```
****** transient analysis tnom=  25.000 temp=  25.000 ******
tpd=  63.4306p  targ= 330.4724p   trig= 267.0418p
```

propagation delay time 為86.8991ps(worst case)，因 tr 和 tf 皆為 20ps，因此將 clock period 設為 104ps ，但經過模擬後發現這樣電路無法正常運作，而之後我透過 spice 模擬發現當 clock period=165ps 時，電路能正常運作，因此 max clock frequency=6.06GHz。



(3) Run SPICE to get the average, peak and leakage power dissipation and energy/bit, respectively of this adder with loading (FO4) when working at the maximum working frequency. (20%)

下圖是有包含 power 的波型。



我們可以使用 meas 指令來計算 average power 及 peak power。

```
avgpower= 135.6107u  from=   0.              to=   5.0000n
peakpower= 940.0539u    at=  15.6062p
           from=   0.            to=   5.0000n
```

之後再將 input 電壓皆設為 0 來計算 leakage power。

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
leakagepower=  10.5518u  from=   0.             to=   5.0000n

         ***** job concluded
```

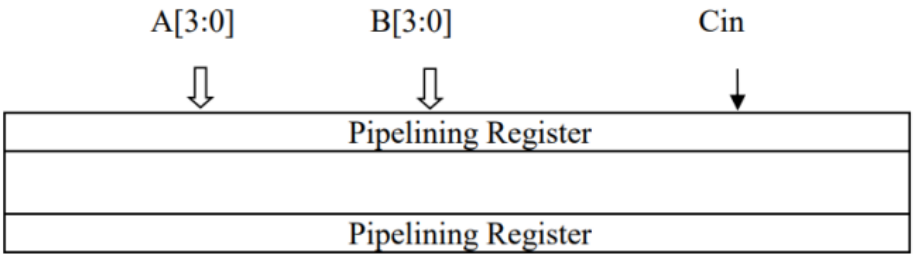
接下來要計算 Energy/bit，maximum working frequency=6.06GHz。

*Average power/frequency=2.238*10^{-14}*

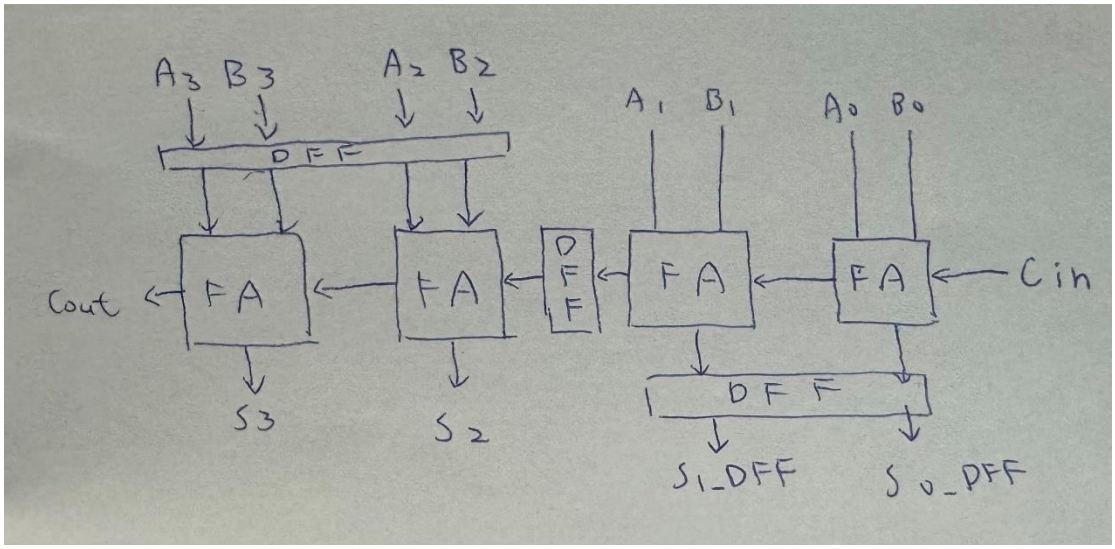
*Energy/bit=2.238*10^{-14}/4=0.56*10^{-14}J/bit=5.6fJ/bit*。

Average power	Peak power	Leakage power	Energy/bit
135.6107μW	*940.0539μW*	*10.5518μW*	*5.6fJ/bit*

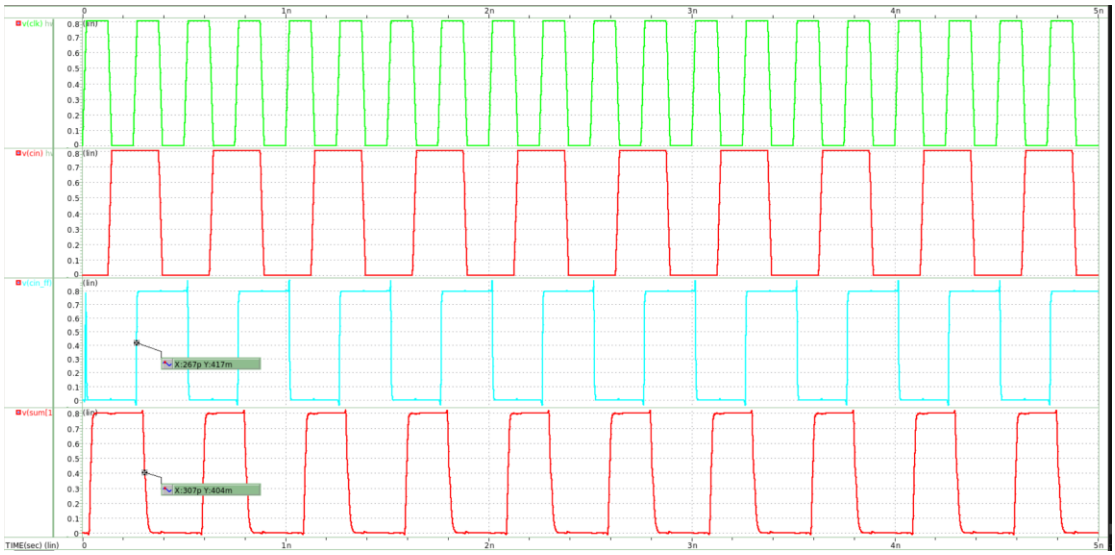
(4) Add one pipelining stage using the designed D register into the 4-bit ripple adder as shown at Fig.1(b). Run SPICE to find the the propagation delay time (with pattern from 000011110 to 000011111 (A[3:0]@B[3:0]@Cin) between pipelining stages to determine the maximum working frequency of the clock with the delay time estimated by SPICE. (20%)



下圖是我將電路加上 pipeline register 後的 block diagram，其中 A、B、C 皆有通過 DFF 以及 INV，且 S0_DFF、S1_DFF、S2、S3 也都有接 DFF。



因為加了 pipeline register，因此新的 critical path 變成 Cin 經過 DFF 後到 S1，而從下方波型可看出 tpd=40ps。



而我透過 meas 指令計算出精確的 tpd=39.77ps。

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
tpd=  39.7700p  targ= 306.8090p   trig= 267.0390p

          ***** job concluded
```

我先將 clock period 用 80ps 代入，發現電路無法正常工作，而經過我的模擬發現， clock working frequency=10GHz(period=100ps)時，電路才能正常運作，波型如下圖。