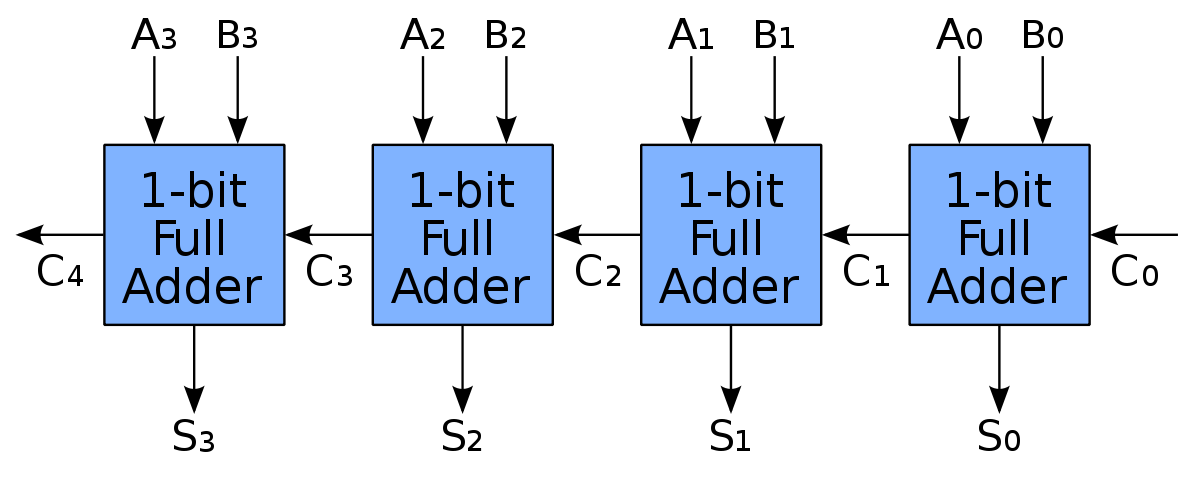
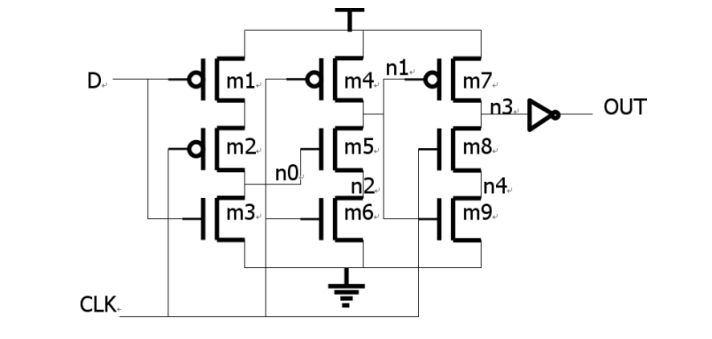
312510239 王則惟

1. A 4-bit ripple adder as ahown at Fig.1 is designed with Fully Complementary Static Logic Gate for FA. Input signals are A[3:0], B[3:0] and Cin which are provided by a unit size inverter. Outputs are Sum[3:0] with loading of 5 unit size inverters connected in parallelism (FO5). You shall provide SPICE simulation results of timing and power waveforms.
2. Try your best to design the fastest adder. First, show your block diagrams in terms of the 1-bit Full-Adder(FA). Second, show the circuit schematic of each block. Use logic effort concepts (you do not have to write down the procedure) to design transistor widths. Describe your design concept. (40%)

下圖是4-bit ripple adder的block diagram，其中A、B、C皆有通過INV以及DFF才接到FULL ADDER的輸入，輸出也有接上DFF。

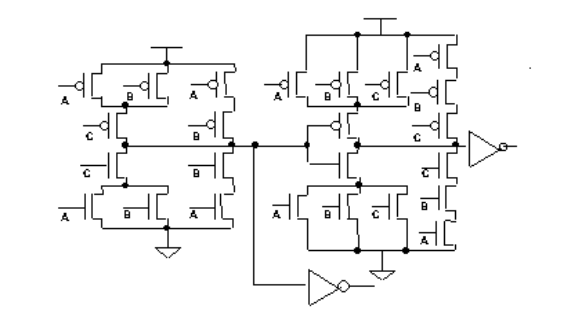




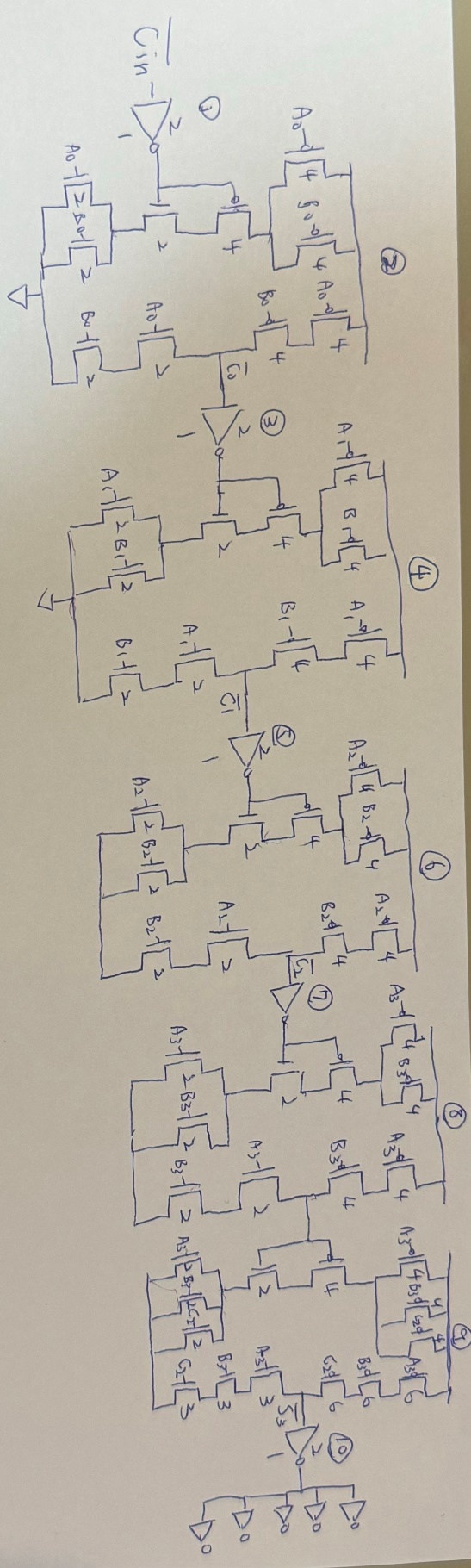
我根據講義對於此電路的分析來sizing此DFF的transistor，而最後的size如下表。

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | M1 | M2 | M3 | M4 | M5 | M6 | M7 | M8 | M9 | INVp | INVn |
| nfin | 4 | 4 | 2 | 4 | 2 | 2 | 4 | 2 | 2 | 2 | 1 |

而下圖是1-bit Full Adder的Schematic，電晶體的編號會在SIZING的時候使用到





題目要求我們使用logic effort concept來sizing電晶體，因此我打算分析最長的那條critical path，也就是Cin到S3的路徑，而下圖是這條路徑的架構圖。

而我們可以將電路分級來計算logic effort，因題目說無須列出過程，則以下省略。

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Level | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
| g | 3/3 | 4/3 | 3/3 | 6/3 | 3/3 | 6/3 | 3/3 | 6/3 | 9/3 | 3/3 |
| P | 3/3 | 12/3 | 3/3 | 12/3 | 3/3 | 12/3 | 3/3 | 12/3 | 15/3 | 3/3 |

透過計算logic effort，並考慮SUM的每個bit都有接一組FO5的情況下，我會將四組FULL ADDER分開SIZING，並且會越來越大。

第一級full adder

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |
| nfin | 1 | 1 | 1 | 1 | 1 | 7 | 7 | 7 | 7 | 7 | 5 | 5 | 5 | 5 |
|  | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | Inv1p | Inv1n | Inv2p | Inv2n |
| nfin | 5 | 5 | 5 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 2 | 1 | 2 | 1 |

第二級full adder

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |
| nfin | 1 | 1 | 1 | 1 | 1 | 8 | 8 | 8 | 8 | 8 | 6 | 6 | 6 | 6 |
|  | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | Inv1p | Inv1n | Inv2p | Inv2n |
| nfin | 6 | 6 | 6 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 2 | 1 | 2 | 1 |

第三級full adder

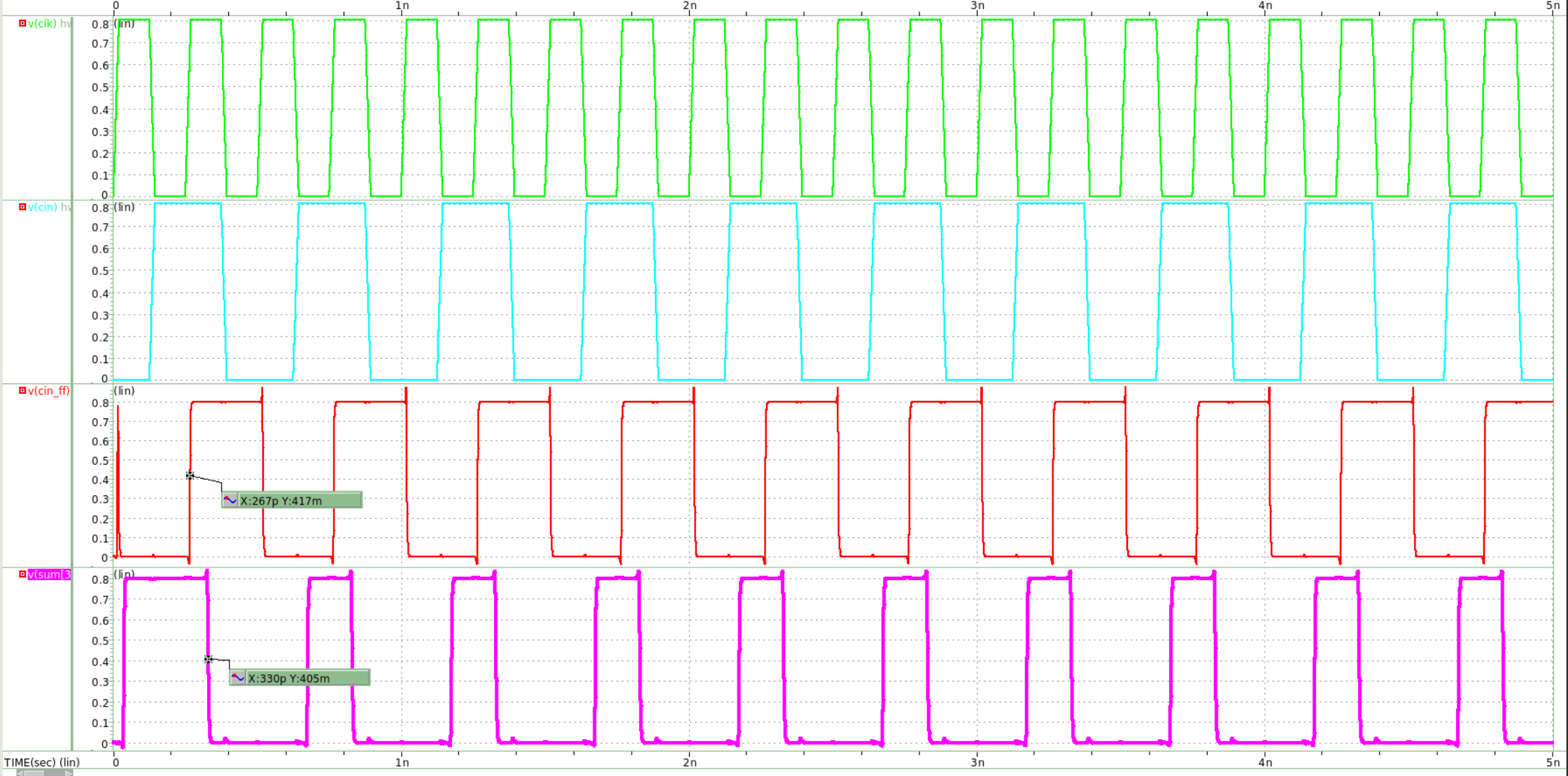
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |
| nfin | 1 | 1 | 1 | 1 | 1 | 9 | 9 | 9 | 9 | 9 | 7 | 7 | 7 | 7 |
|  | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | Inv1p | Inv1n | Inv2p | Inv2n |
| nfin | 7 | 7 | 7 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 2 | 1 | 2 | 1 |

第四級full adder

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |
| nfin | 1 | 1 | 1 | 1 | 1 | 10 | 10 | 10 | 10 | 10 | 8 | 8 | 8 | 8 |
|  | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | Inv1p | Inv1n | Inv2p | Inv2n |
| nfin | 8 | 8 | 8 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 2 | 1 | 2 | 1 |

1. Based on the design of (1), run SPICE to find the the propagation delay time (with pattern from 000011110 to 000011111 (A[3:0]@B[3:0]@Cin). Determine the maximum propagation of a clock with the delay time estimated by SPICE. (20%)

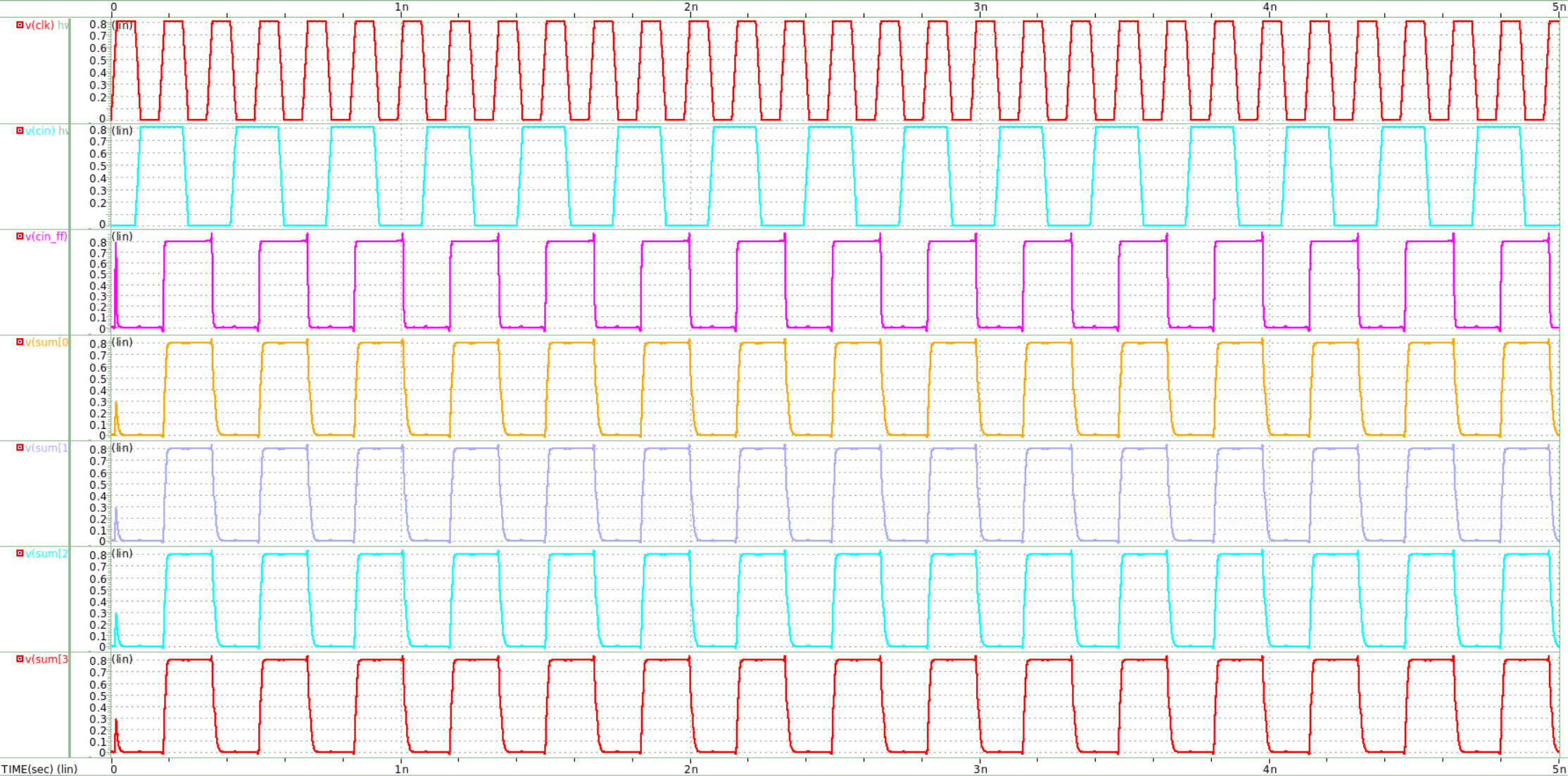
tpd為經過DFF後的Cin=0.5VDD到critical path輸出=0.5VDD的所花的時間，因此我在模擬時將Cin從0變成VDD，並觀察波型，由下圖可看出tpd=63ps。



而透過meas指令，可得出精確的tpd=63.4306ps。

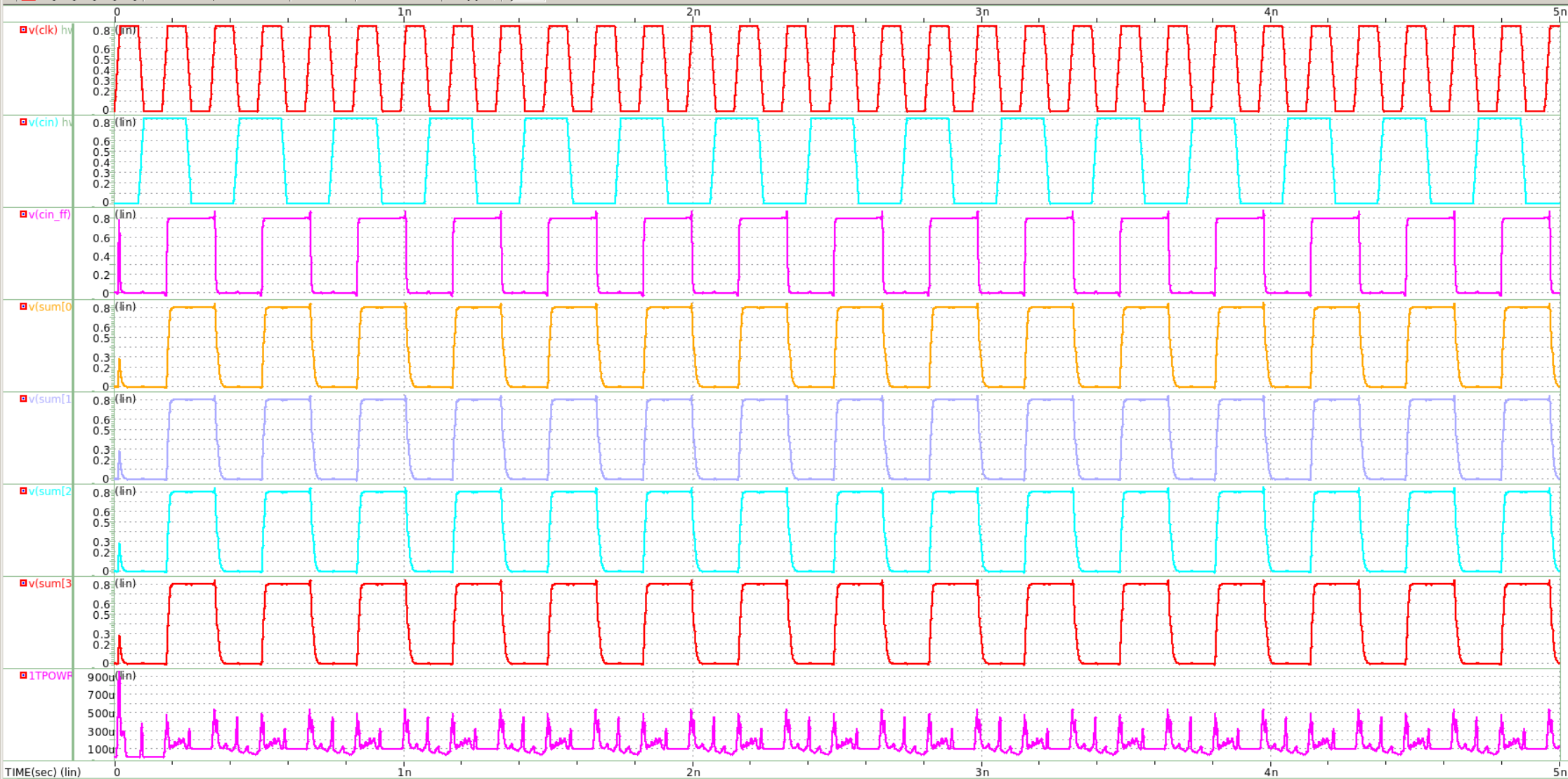


propagation delay time為ps(worst case)，因tr和tf皆為20ps，因此將clock period設為104ps ，但經過模擬後發現這樣電路無法正常運作，而之後我透過spice模擬發現當clock period=165ps時，電路能正常運作，因此max clock frequency=6.06GHz。



1. Run SPICE to get the average, peak and leakage power dissipation and energy/bit, respectively of this adder with loading (FO4) when working at the maximum working frequency. (20%)

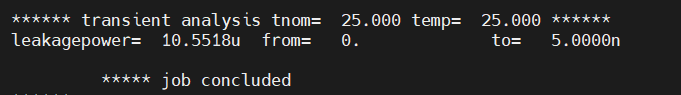
下圖是有包含power的波型。



我們可以使用meas指令來計算average power及peak power。



之後再將input電壓皆設為0來計算leakage power。



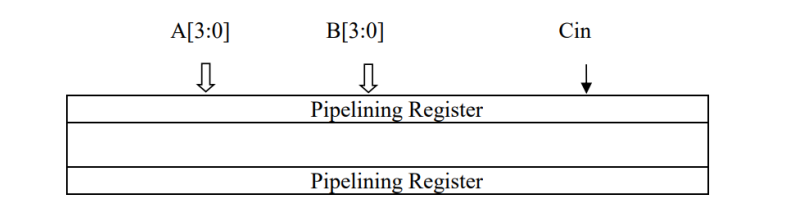
接下來要計算Energy/bit，maximum working frequency=6.06GHz。

*Average power/frequency=2.238\*10-14*

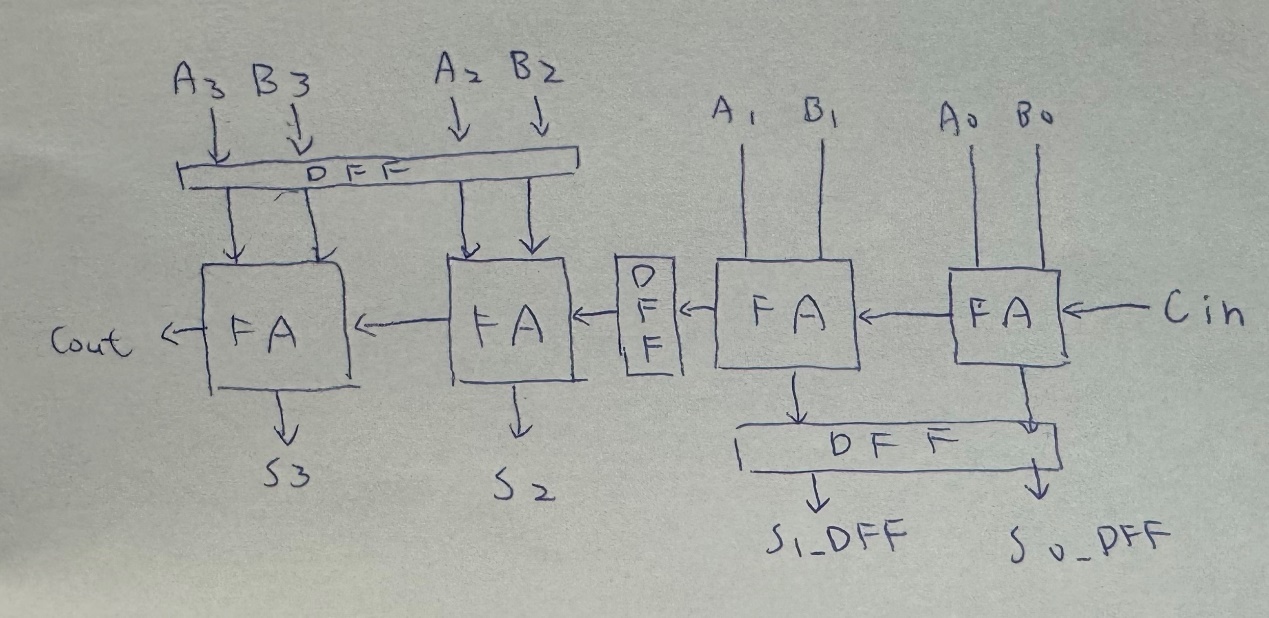
*Energy/bit=2.238\*10-14/4=0.56\*10-14J/bit=5.6fJ/bit。*

|  |  |  |  |
| --- | --- | --- | --- |
| Average power | Peak power | Leakage power | Energy/bit |
| *135.6107𝜇W* | *940.0539𝜇W* | *10.5518𝜇W* | *5.6fJ/bit* |

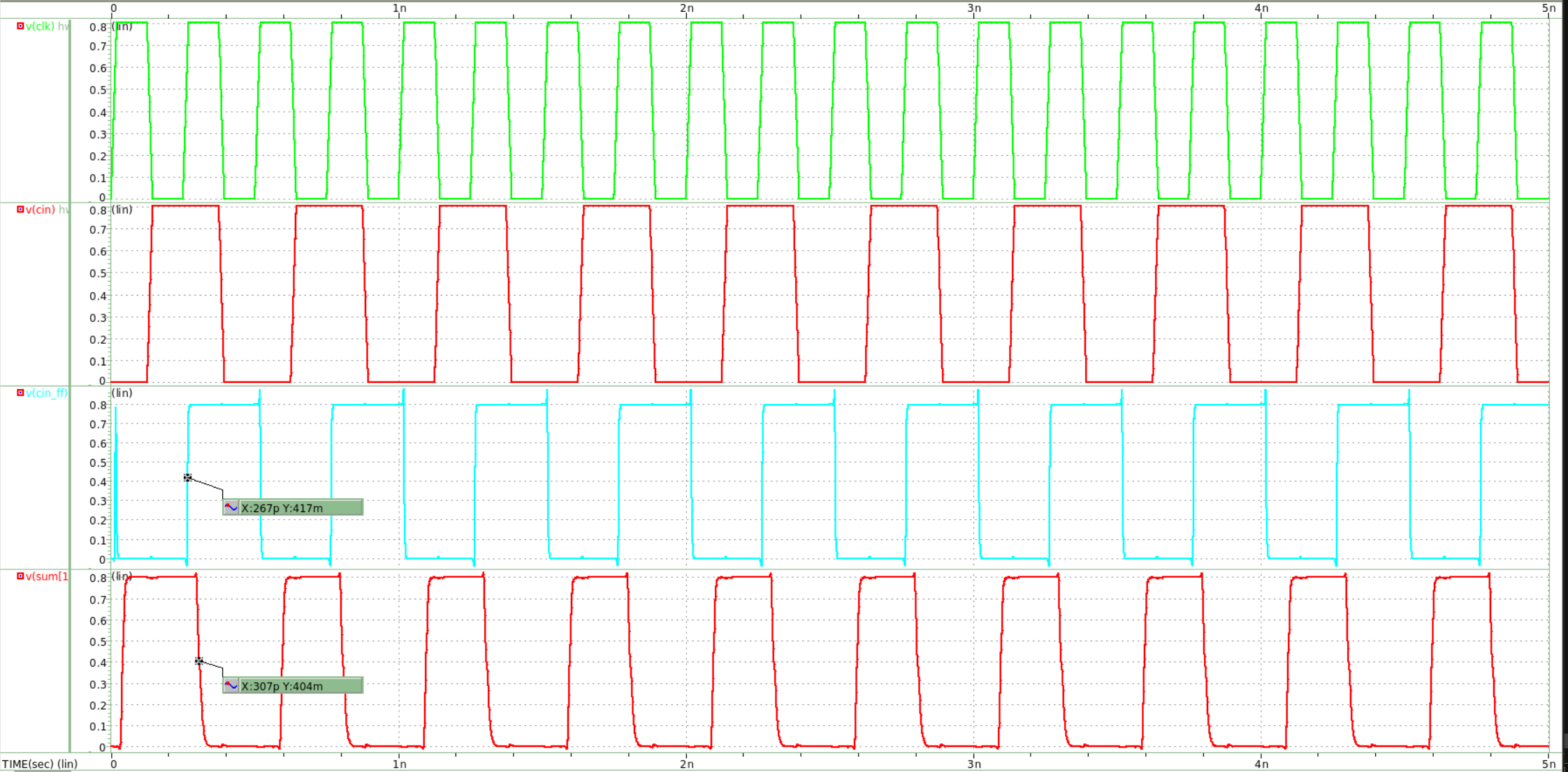
1. Add one pipelining stage using the designed D register into the 4-bit ripple adder as shown at Fig.1(b). Run SPICE to find the the propagation delay time (with pattern from 000011110 to 000011111 (A[3:0]@B[3:0]@Cin) between pipelining stages to determine the maximum working frequency of the clock with the delay time estimated by SPICE. (20%)



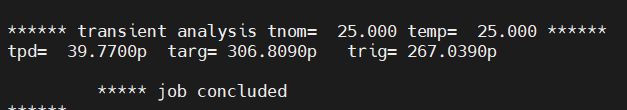
下圖是我將電路加上pipeline register後的block diagram，其中A、B、C皆有通過DFF以及INV，且S0\_DFF、S1\_DFF、S2、S3也都有接DFF。



因為加了pipeline register，因此新的critical path變成Cin經過DFF後到S1，而從下方波型可看出tpd=40ps。



而我透過meas指令計算出精確的tpd=39.77ps。



我先將clock period用80ps代入，發現電路無法正常工作，而經過我的模擬發現， clock working frequency=10GHz(period=100ps)時，電路才能正常運作，波型如下圖。

