Notes Archi

Louis Thevenet

1. LEDs

```
1 PILE = 0x200 // fond de pile à l'adresse 0x200
2 set PILE, %sp //initialisation du pointeur de pile : ABSOLUMENT NECESSAIRE
4 LEDS = 0 \times B00000000
5 N = 10
6 set N, %r1
7 call Afficher_LEDs
8 Fin: ba Fin
10
11
12 Afficher LEDs:
13
     // affiche le contenu de %rl sur les LEDs
       push %r1
14
       push %r20
16
       set LEDS, %r20
       st %r1, [%r20]
17
18
       pop %r20
       pop %r1
19
       ret
```

2. Nombre d'occurences

```
1 PILE=0x200
3 Prog_Principal:
4 set PILE, %sp
5 set 2, %r2
6 set Tab, %r3
7 set 12, %r4
8 call Nb_Occ
9 FinProg: ba FinProg
11 Nb Occ:
12 // entrées : %r2 : le nombre à chercher
       %r3 : début du tableau
13 //
              %r4 : taille du tableau
14 //
15 // sortie : %5 : le nb d'occurrences de %r2 dans Tab
16 push %r6
17 push %r7
19 set 0,%r5
20 set 0,%r6
21 Boucle:
22 cmp %r6,%r4
23 bge FinBoucle
24 ld [%r3+%r6],%r7
```

```
cmp %r7,%r2
    bne FinSi
    inc %r5
28
    FinSi:
29
    inc %r6
30
    ba Boucle
31
    FinBoucle:
32
    pop %r7
33
    pop %r6
34
    ret // IMPORTANT
35
36
   Tab:.word 2,5,4,2,5,4,1,3,2,5,8,2
```

3. Interruptions

```
PILE = 0x200
2
   LEDS = 0 \times B00000000
3
4
5
   ba Prog_Principal
6
   Handler_IT:
7
   // affiche le contenu de %r2 sur les LEDs
   push %r20
9
   set LEDS, %r20
10
11
   st %r2, [%r20]
   pop %r20
12
   reti // IMPORTANT
13
14
15
   Prog_Principal:
16
   set PILE,%sp
17
   set 0, %r2
18 set N, %r3
19 Boucle: cmp %r2, %r3
   bl Suite
21
   set 0, %r2
   Suite:
23
   inc %r2
24 ba Boucle
```

4. MiniCraps

Sure, here's a brief summary of your CPU:

The CPU is a 4-stage pipeline that executes instructions in a loop starting from Fetch and ending with PCPlus1, then repeating the cycle. It has a total of 16 possible instructions, some of which can perform arithmetic operations on memory operands. The CPU fetches an instruction from memory in the « Fetch » stage, decodes it in the « Decode2PCPlus1 » stage, increments the PC value by adding it to the contents of the Memory module at the address determined by the PCPlus1 signal in the « PCPlus1 » stage, and finally sets the flags N.