MicroATX Electrical Design Suggestions

Design Guide

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Revision History

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600571	1.1	• No change in the Content. Applied the latest Intel Template and formatted the document.	July 2018

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1 Overview

microATX is a new motherboard form factor designed to meet new market trends and PC technologies. Lower system cost is the main driving force for the new form factor. The size of the form factor allows for smaller chassis, motherboard, and power supply, thus reducing the cost of entire system. The microATX form factor is also backward-compatible with the ATX form factor with some modifications. This document is intended to provide electrical design suggestions as a reference for OEMs to help them realize the benefits of the microATX form factor. The document does not provide design details.

1.1 Related Documents

- PC98 System Design Guide
- microATX Motherboard Interface Specification (refer Web site http://www.formfactor.org)
- microATX Chassis Design Suggestions
- microATX EMC Design Suggestions
- microATX System Design Suggestions
- microATX Thermal Design Suggestions
- SFX12V Power Supply Design Guide
- TFX12V (Thin Form Factor with 12-V Connector) Power Supply Design Guide
- PCI Specifications (refer Web site http://www.pcisig.com/specifications/conventional/)
- PCI-Express* Specification (refer Web site http://www.pcisig.com/specifications)
- Design Guide for ATX I/O Implementations, V.1.0

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2 Motherboard Electrical Design Suggestions

The electrical constraints of microATX are similar to those of ATX. However, because of the smaller size of the microATX form factor, landscape use is a critical issue. The following sections address some possible problems and issues with a smaller form factor.

2.1 PCI Bus

Because the PCI bus is a high speed bus, special care is needed to route this bus on microATX systems. The following are suggestions for routing the PCI bus on the motherboard.

2.1.1 PCI Simulation

This section summarizes how the PCI bus was simulated in a microATX system. Below Figure shows the motherboard layout that was used in the simulation exercise. Refer the next section for simulation results and recommendations.

2.1.2 Simulation Results and Recommendations

This section describes the results and recommendations based on the PCI simulation. The results presented are for a specific motherboard chipset combination. To ensure proper PCI bus operation, motherboard OEMs should perform their own independent simulations to help guide their choice and layout of components.

The results from the simulation show that with typical implementations, termination should not be needed. The sum of L1 and L2 in below figure should be less than 12 inches (304.8mm). Simulations also show that an additional 0.8 inch (20.32mm) to the second slot has negligible impact on the PCI bus timing. In most cases, using a load card in either PCI slot does not have a significant effect on the PCI bus.

2.1.3 PCI REQ#/GNT# Implementation

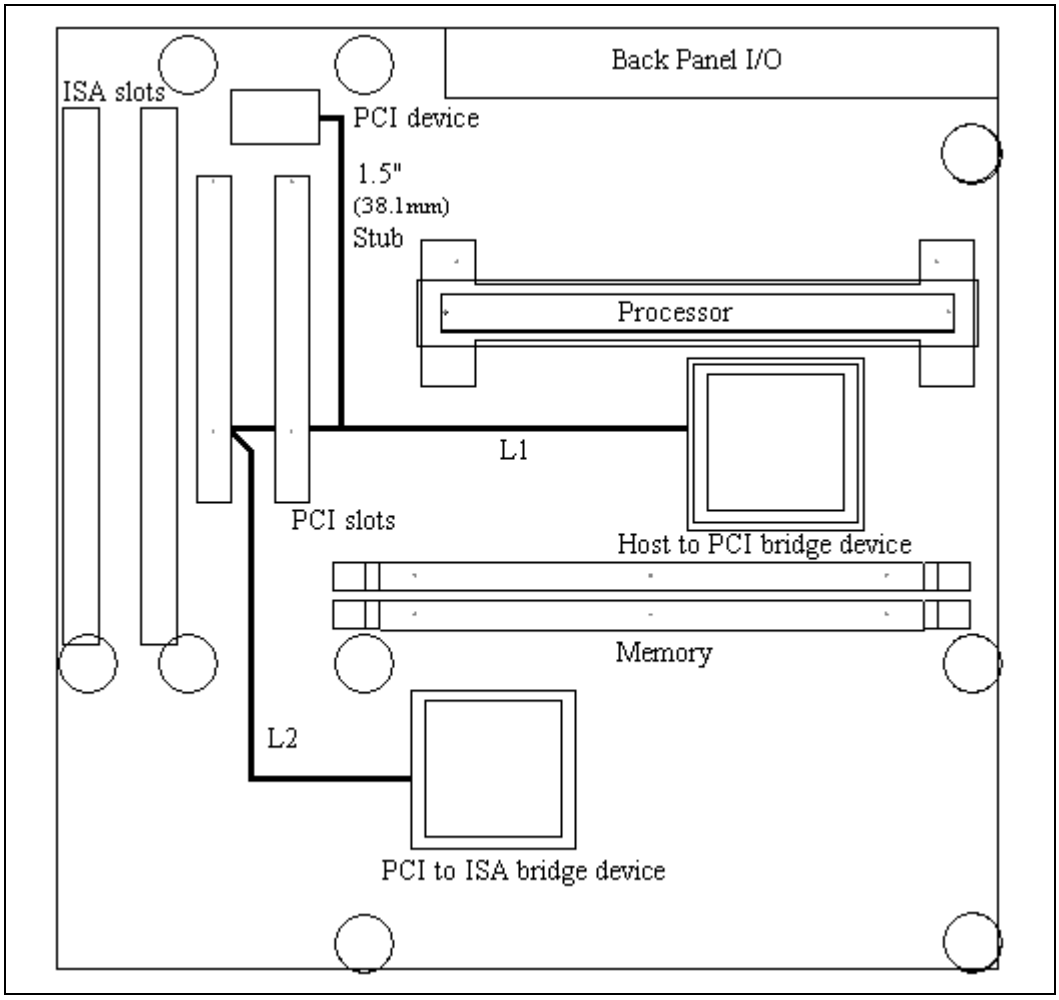
PCI REQ#/GNT# pair should be connected carefully. A possible problem exists when there are bus-mastering motherboard devices. If the REQ#/GNT# pair of the motherboard device is routed to the PCI slot, a contention problem will exist when a bus-mastering device is installed in the slot that has the same REQ#/GNT# pair.

- To alleviate this contention, when you have a motherboard device that uses a REQ#/GNT# pair, do not route the same pair to the connector.
- Also, route one REQ#/GNT# pair to each of the connectors, and do not route each pair to more than one connector.

2.1.4 64-bit PCI

OEMs designing motherboards should take into account that add-in cards supporting the 64-bit extension to the PCI bus may be used in the 32-bit connectors. Therefore, the board designer should give special attention to ensure that no components are placed in areas that may conflict with the 64-bit extension of these cards.

Figure 2-1. Motherboard Layout for Simulation Exercise



2.1.5 IDSEL Assignment

The motherboard should begin assigning IDSEL signals from the lower address lines. This has implications for the system BIOS in terms of which PCI devices are initialized first within a system. For example, if the system BIOS scans downward in the initialization routine (i.e., AD31 to AD11), the devices on the add-in boards will be initialized before the motherboard devices. The opposite is true if the BIOS scans upward: the BIOS will find the motherboard devices before the devices on the add-in boards. For a BIOS that scans upward, the following is true:

- IDSEL for device 0 is connected to AD16
- IDSEL for device 1 is connected to AD17
- IDSEL for device 2 is connected to AD18

Therefore, device 0 will be initialized first. Address lines [15:11] are used for decoding target address port bits.

2.1.6 3VSB

3VSB should be routed to the PCI slot for cards that require standby voltage. For details, refer to the PCI Local Bus Specification.

2.1.7 PCI_PME#

The exception to PCI termination is the PCI power management signal.Because power management is driven by motherboard circuitry, which in turn may be at various power wells, the motherboard should pull the PCI_PME signal up to the motherboard-defined power level.

2.2 IDE Signals

For ATA-33 support, the motherboard IDE signal length should be minimized. Keep in mind that the IDE cables can be as long as 18 inches (457.2mm). The exact motherboard trace length depends on the design. The below Table shows the IDE signals as they relate to the IDE connector.

Table 2-1. IDE Signals

Primary IDE Header	Signal Name	Primary IDE Header	Signal Name
1	IDE_RESET#	2	GND
3	IDE_DD7	4	IDE_DD8
5	IDE_DD6	6	IDE_DD9
7	IDE_DD5	8	IDE_DD10
9	IDE_DD4	10	IDE_DD11
11	IDE_DD3	12	IDE_DD12
13	IDE_DD2	14	IDE_DD13
15	IDE_DD1	16	IDE_DD14
17	IDE_DD0	18	IDE_DD15
19	GND	20	KEY
21	IDE_DMARQ	22	GND
23	IDE_DIOW#	24	GND
25	IDE_DIOR#	26	GND

Primary IDE Header	Signal Name	Primary IDE Header	Signal Name
27	IDE_IORDY	28	IDE_CSEL
29	IDE_DMACK#	30	GND
31	IDE_INTRQ	32	IDE_RESRV
33	IDE_DA1	34	RESERVED
35	IDE_DA0	36	IDE_DA2
37	IDE_CS0#	38	IDE_CS1#
39	IDE_DASP#	40	GND

2.3 Floppy Signals

All signals requiring termination should be terminated near the connector. The below Table shows the floppy signals as they relate to the floppy connector. The pullup resistors required for the active low floppy signals should be greater than 1K ohm. No special care is needed other than standard routing practices. If a system does not support more than one floppy drive, signals FDS1# and FDME1# should not be connected.

Table 2-2. Floppy Signals

FDC Header	Signal Name	FDC Header	Signal Name
1	DRV2#	2	DENSEL
3	GND	4	FLPY_RSVD
5	KEY	6	DRATE0
7	GND	8	INDX#
9	GND	10	FDME0#
11	GND	12	FDS1#
13	GND	14	FDS0#
15	GND	16	FDME1#
17	MSEN1	18	DIR#
19	GND	20	STEP#
21	GND	22	WRDATA#
23	GND	24	WE#
25	GND	26	TRK0#
27	MSEN0	28	WP#
29	GND	30	RDDATA#
31	GND	32	HDSEL#
33	GND	34	DSKCHG#

2.4 Power Signals

The following sections briefly summarize the power signal requirements on a microATX system. For a detailed explanation of these requirements, refer the SFX12V (Small Form Factor with 12V Connector) Power Supply Design Guide or TFX12V (Thin Form Factor with 12V Connector) Power Supply Design Guide. For systems supporting PCI-Express requirements it is recommended that a 24 pin main power header be used. This header may be a MOLEX* 44206-0007 or equivalent 2x24 ATX power supply connector should be used on the microATX motherboard.

When routing power planes, the motherboard designer should take into account the maximum current that the motherboa rd can draw. The below Table shows the power signals as they relate to the power connector.

Table 2-3. Power Signals

Pin	Signal Name	Pin	Signal Name
1	+3.3V	13	+3.3V
2	+3.3V	14	-12V
3	COM	15	COM
4	+5V	16	PS_ON#
5	COM	17	COM
6	+5V	18	COM
7	GND	19	COM
8	PWR_OK	20	N/C
9	+5VSB	21	+5V
10	+12V	22	+5V
11	+12V	23	+5V
12	+3.3V	24	COM

2.4.1 -5V

It is no longer recommended to have -5V signal as an option. Pin 20 is now designated a no connect or NC.

2.4.2 PWR_OK

This signal is asserted high by the power supply to indicate that +5 VDC and +3.3VDC outputs are above the voltage thresholds specified by the power supply. The logic designer can assume that when this signal is asserted, the power supply will deliver the continuous energy specified by the power supply. Refer the *SFX12V (Small Form Factor with 12V Connector) Power Supply Design Guide* or *TFX12V (Thin Form Factor with 12V Connector) Power Supply Design Guide* for electrical and timing characteristics of the PWR_OK signal. Many power supplies have limited drive capability, so the designer is encouraged to consult the power supply documentation and provide bulk capacitors where needed.

2.4.3 PS_ON#

This signal is driven by circuitry on the motherboard to toggle the power state of the power supply. This is an active low signal. When asserted, the power supply will turn on, leaving the standby voltage off. When deasserted, the power supply will shut down, leaving only the standby voltage on. For the exact timing required by the power supply, refer to the *SFX12V (Small Form Factor with 12V Connector) Power Supply Design Guide* or *TFX12V (Thin Form Factor with 12V Connector) Power Supply Design Guide*.

2.4.4 5VSB

This is a standby voltage provided by the power supply while the system is off. The exact amount of current available on this signal is different from each power supply. For details, refer to the *SFX12V (Small Form Factor with 12V Connector) Power Supply Design Guide* or *TFX12V (Thin Form Factor with 12V Connector) Power Supply Design Guide*.

2.4.5 Power Design

Care is needed to reduce EMI emission.

- VCC and VCC3—The appropriate numbers of bulk and decoupling capacitors are required to adequately support system requirements.
  - The bulk capacitors should be low in ESR and range from 10 to 22uF, and the number needed is system-specific.
  - The decoupling capacitors should be in the range of 0.1 uF and should be placed around the power connectors and power pins of devices.
  - There should be an adequate number of stitching capacitors linking the VCC and VCC3 power planes.
- +12V, -12V, -5V, 5VSB—These other power sources are typically routed as thick traces. Bulk and decoupling capacitors should be added to the trace to support the power requirements of the system.
- PS_ON#—This signal should be routed to the power connector to allow the motherboard the ability to cycle power in the system. Care is needed to reduce EMI emission.
- PWR_OK—Route to the power supply connector. Care is needed to reduce EMI emission.

2.5 Front Panel Signals

The following sections define the signals routed to the front panel header. To save motherboard space, a 2x9-pin header can be used. The below Table shows an example of a 2x9 front panel header pinout. The exact header pinout and design are chassis-dependent.

Table 2-4. 2x9 Front Panel Header Pinout, Example

Pin	Signal Name	Pin	Signal Name
1	HD_PWR	2	LED_GRN
3	HDA#	4	LED_YEL
5	GND	6	FPBUT_IN
7	FP_RST#	8	GND
9	+5V	10	FPSLP#
11	IRRX	12	GND
13	GND	14	KEY
15	IRTX	16	IR_PWR
17	Reserved	18	Reserved

2.5.1 HD_PWR, HDA#, LED_GRN, and LED_YEL Signals

These signals are used to drive LEDs to indicate different operating states. The LEDs should indicate System active, System sleep, and Hard drive active. Optional message-waiting state can also be implemented. The exact implementation of these states is up to the designer. The trace should have a current-limiting resistor. The designer should also be aware of system indicator guidelines such as those mentioned in the *PC 98 System Design Guide*; for more detail, refer to that document.

2.5.2 FPBUT_IN

This signal is the front panel On/Off signal. It should be implemented using a momentary contact switch on the front panel. When the switch is triggered, the system turns on if the system was initially off or turns off if the system was initially on. This function may vary depending on system implementation. Proper debounce circuit should be implemented.

2.5.3 FPSLP#

This signal is routed to provide a request for the system to enter a power-saving mode. One implementation is to use this signal in conjunction with power management software and hardware to place the system in a sleep state. This functionality is typically implemented using a momentary contact switch on the front panel. The motherboard should provide any required debounce circuit.

2.5.4 FP_RST#

This signal corresponds to a front panel reset signal to the motherboard. This should be implemented using a momentary contact switch on the front panel. When the switch makes contact, the signal is grounded, causing a system-wide reset. The motherboard should have any required debounce pullup resistor.

2.5.5 IRRX, IRTX, and IR_PWR Infrared Signals

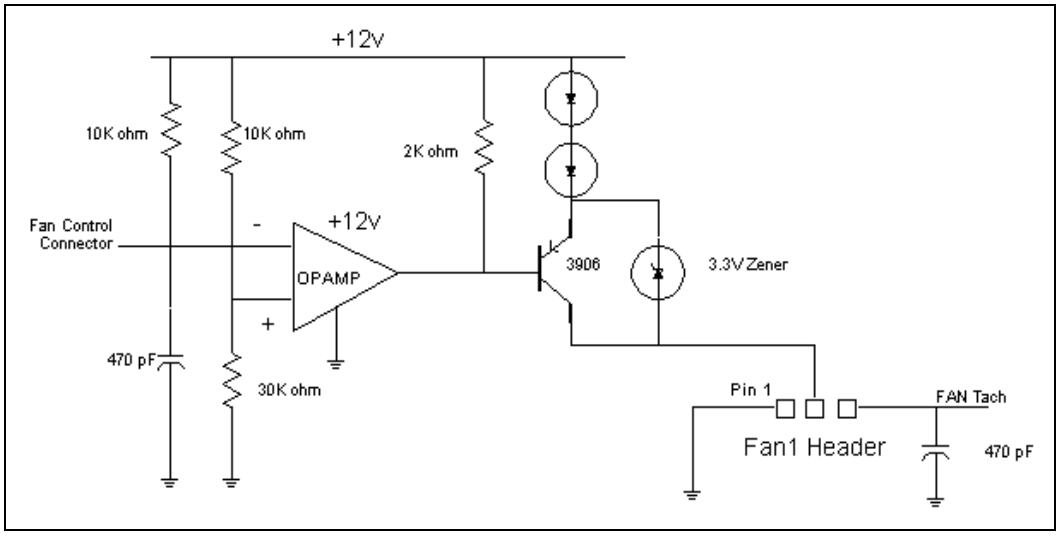
- IRRX—This pin corresponds to the IRDA serial input signal.
- IRTX—This pin corresponds to the IRDA serial output signal.
- IR_PWR—This pin provides IR power.

2.6 Fan Control

The number of fan connectors required on a motherboard depends on many different factors, such as type of processor used, type of onboard component used, and type of chassis used. For proper cooling, the system designer should allow for a sufficient number of fan connectors. The designer should also be aware of system-level requirements described in the *PC 98 System Design Guide*. The minimal fan control design should allow the system to turn the fan on or off depending on operating state. Variable speed fan control can also be used; the exact speed of the fans will depend on the implementation. Because of this dependency on the specific implementation, the designer should ensure that all system acoustics and cooling requirements are met when the variable speed fan control is set for maximum fan speeds. For more detail, refer to the *PC 98 System Design Guide.*

Circuitry similar to that shown in below figure can be used to drive the fan on the motherboard. The voltage across the fan will be either 10.6V or 7.3V, depending on the output of the comparator, which in turn depends on whether the input is above or below 9V. Decoupling capacitors should be used on this signal to minimize noise on the line.

Figure 2-2. Fan Control Circuitry



2.7 Tamper Detection

Current implementations of this signal have a switch on the motherboard, powered from either VBAT or 5VSB which is activated when the chassis cover is removed.

Once activated, the motherboard can do one of several actions, such as turning the power off if the system power is on. This would prevent someone from trying to remove the motherboard while the system is in a power-managed state.

Here is a brief comparison of powering the tamper-detect switch from either VBAT or 5VSB:

- From VBAT—The advantage is that you can detect intrusion even if the system has the power cord removed. The disadvantage is that you adversely affect the life of the battery in system.
- From 5VSB—The advantage is that you do not adversely affect system battery life, and the system will detect intrusion in all powered states. The disadvantage is that the intrusion detect can be disabled if someone pulls the power cord from the system.

2.7.1 Tamper Detect Design

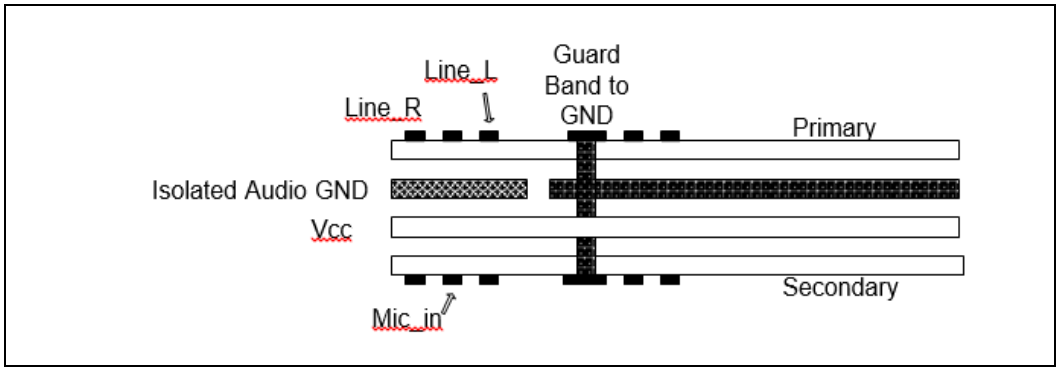
To help prevent the removal of the motherboard with the power on, chassis intrusion circuitry can be used to warn when the chassis cover is removed. Also, an intrusion switch can be mounted on the chassis to warn if the chassis cover is removed. This detection feature can be bypassed by depopulating the tamper-detect enable jumper.

A possible implementation could be if the cover is removed, the onboard speaker immediately starts beeping. The speaker will continue to beep until the lid is replaced, the tamper-enable jumper is removed, or the system is unplugged (removing power from 5VSB). If the system is in a sleep mode when the cover is removed, the onboard speaker will immediately start beeping again.

2.8 Implementing Audio on microATX Platforms

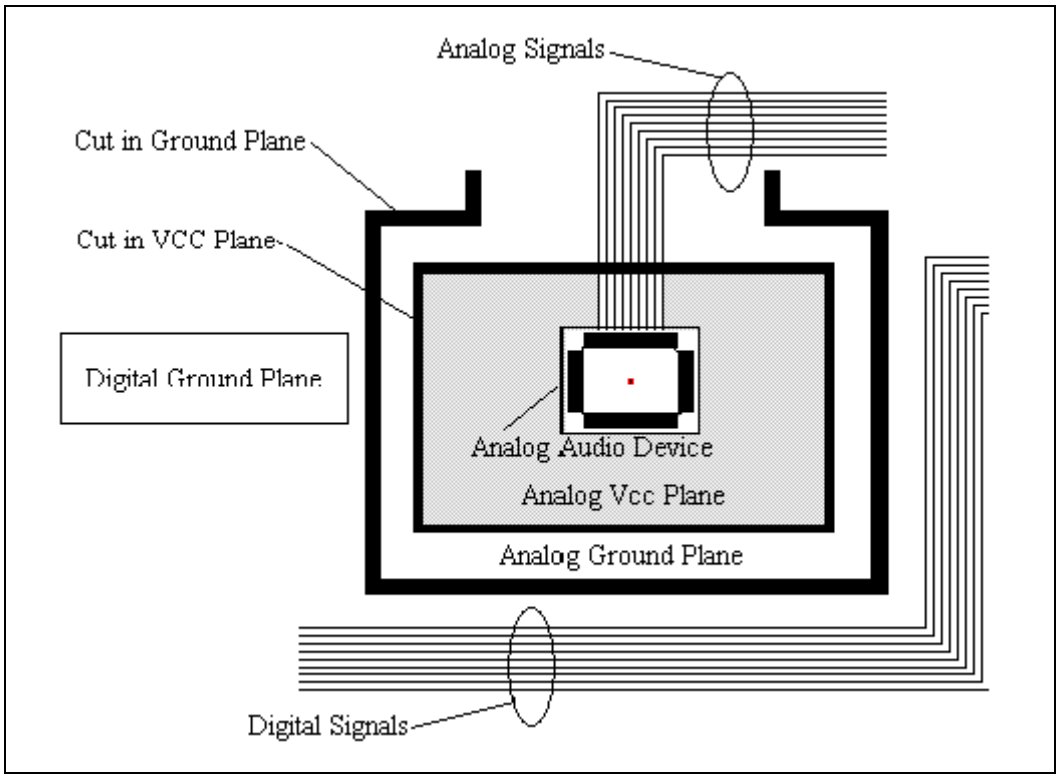
Implementing audio in the computer has always been challenging because of the analog signals that must be routed. Audio traces need to be routed carefully to reduce noise from nearby digital signals. To avoid digital signals, the designer should route analog traces away from any digital signals. To further reduce the effects of nearby digital signals, a guard band tied to ground can be routed between the audio signals and the digital signals (Below Figure).

Figure 2-3. Routing Audio, Example



Because the impedance will be high for the return path that is directly under the audio traces, the returning signals would normally use the ground plane as a return path. For this reason the portion of the ground plane under the audio signals and circuitry should be isolated. This isolated ground should be tied back to the digital ground. The power supply plane for the audio section must also be separated from the rest of the motherboard supply planes (Below Figure). As is always the case, stitching ferrites between the analog and digital planes may be needed if EMI becomes a problem. The designer should also be aware of special audio specifications like the *Audio Codec '97 Component Specification* that the system may need to comply with.

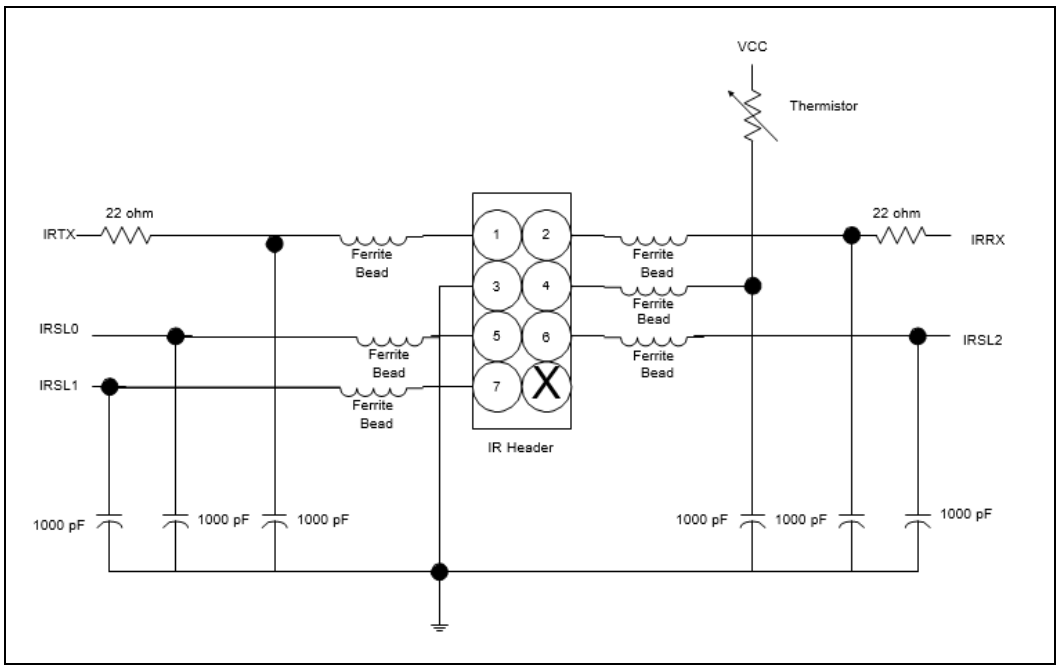
Figure 2-4. Plane Splits, Example



2.9 Infrared Design

To support front panel infrared, the designer can route the bus to a header or, in chassis-specific implementations, to an IR connector on the PCB. Below Figure shows a possible implementation of supporting an IR header. As is always the case, ferrites may be needed if EMI becomes a problem.

Figure 2-5. IR Implementation, Example



2.10 Modem Wake

If it is necessary to include the ability to have an add-in modem card wake up the system from a sleep state, then a header will be needed on the motherboard. This header will need to have standby power so that power to the modem is supplied while the system is asleep.

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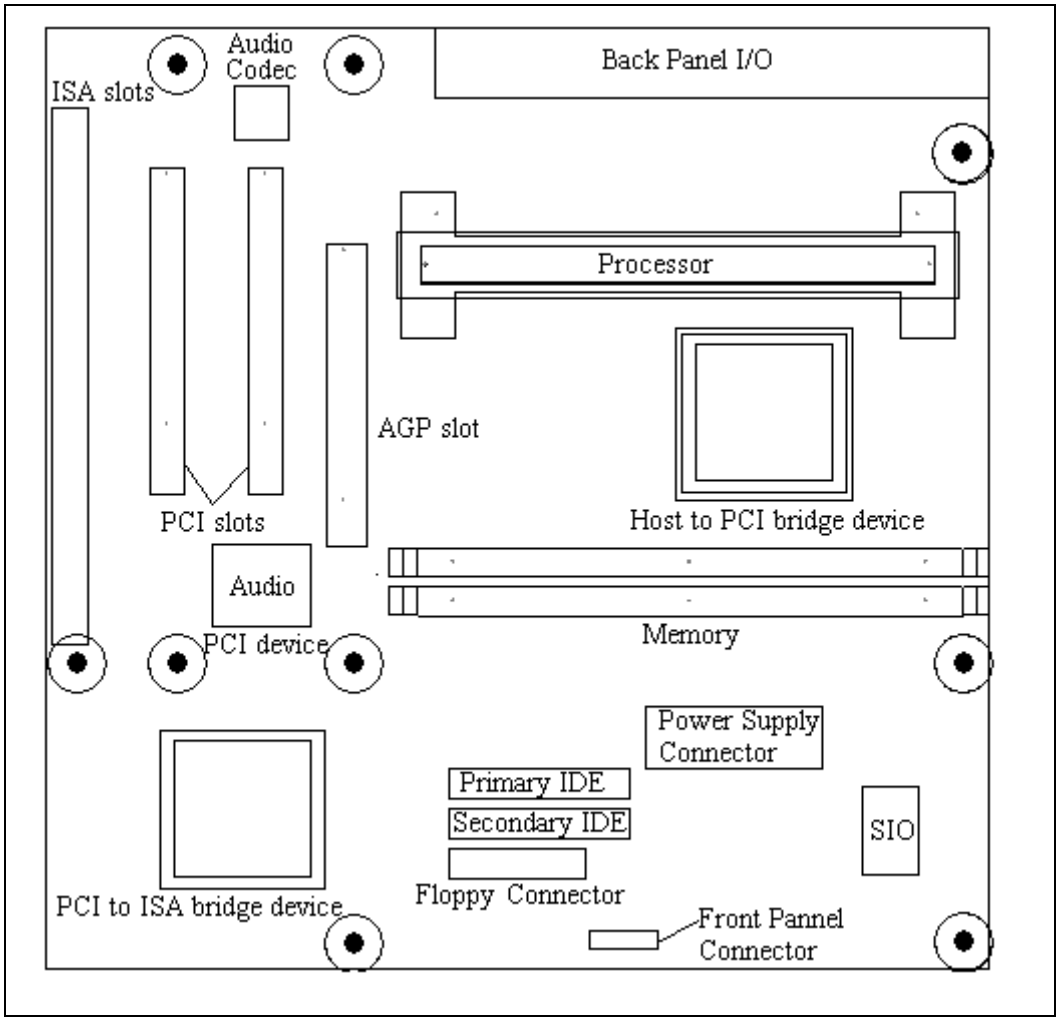
3 Motherboard Device Placement

The following section provides some device placement suggestions for a microATX motherboard. To ensure that proper timing is meet, the designer should do post-routing simulations.

3.1 AGP-up Design

Below figure shows an example of a motherboard with AGP implemented on an add-in card (AGP-up). The designer should be aware that keepouts for microATX chassis differ from those for ATX. For more information, refer to the *microATX Motherboard Interface Specification*.

Figure 3-1. AGP-up Motherboard Layout, Example

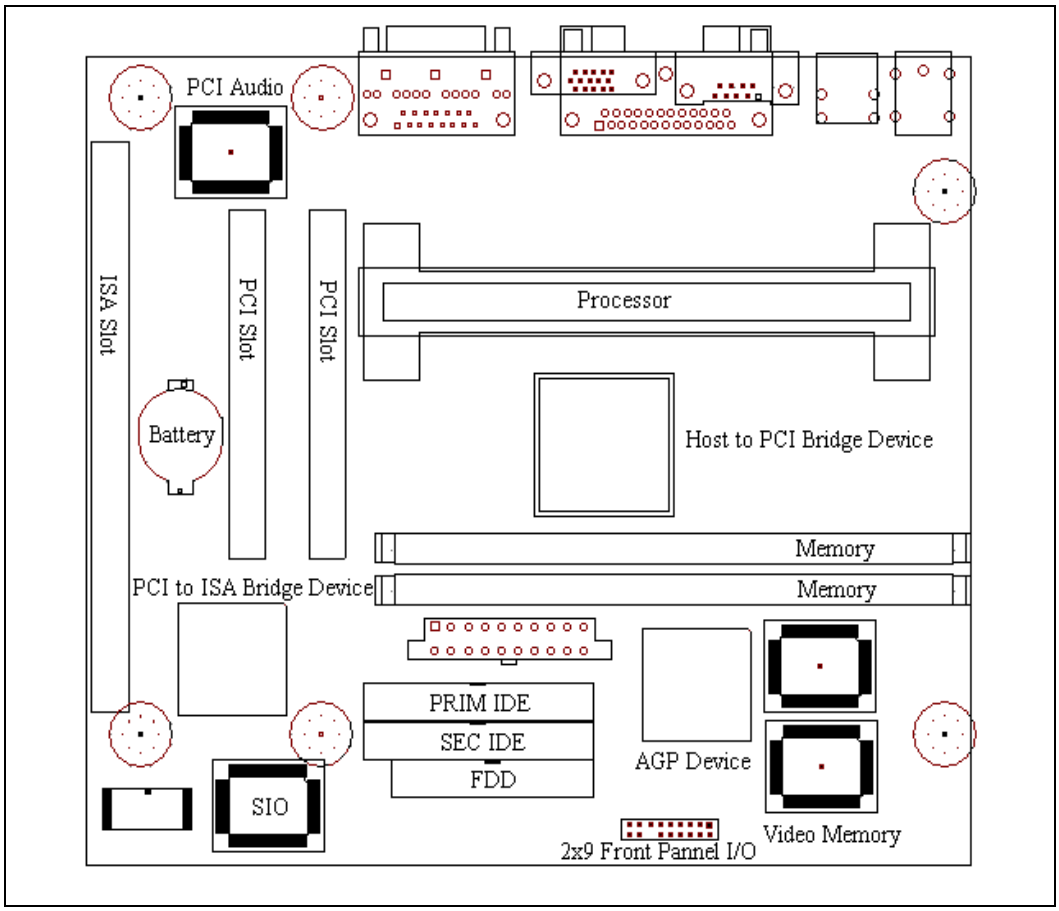


The motherboard in above figure is a full size microATX implementation 9.6 inches (244mm) x9.6 inches (244mm). Because a main focus of the microATX form factor is to reduce cost, it is possible to reduce the motherboard size according to feature set. The designer must ensure that with a smaller board size and possibly fewer mounting holes, the board is still mechanically sound

3.2 AGP-down Design

Below figure shows an example of a motherboard with AGP implemented onboard (AGP-down). It is strongly recommended that the designer do post-routing simulation on the AGP bus to ensure that timing margins are met. The designer should be aware that keepouts for microATX chassis differ from those for ATX. For more information, refer to the microATX Motherboard Interface Specification.

Figure 3-2. AGP-down Motherboard Layout, Example



The flexibility of the microATX form factor allows the designer to use a smaller board size. The designer should do routing studies to ensure that the component layout allows sufficient routing channels for all signals.

3.2.1 Motherboard Design Checklist

This section provides an informal checklist of suggestions about the motherboard electrical design. The checklist is meant for reference only and is not intended to be comprehensive.

Note: It is strongly recommended that the designer review the *microATX Motherboard Interface Specification* in sufficient detail to be confident that the design complies with the specification.

Motherboard Mechanical/Placement Requirements

- Ensure that board size is no larger than 9.6 inches (244mm) x 9.6 inches (244mm).
- Ensure that mounting holes are placed in accordance with the microATX Motherboard Interface Specification.
- If an AGP connector is supported, it must be placed as shown in microATX Motherboard Interface Specification.
- Ensure that the motherboard primary side keepout zones are not in violation of the microATX Motherboard Interface Specification.
- Ensure that height restrictions on the rear I/O panel are not violated.
- Ensure that component height restrictions are not in violation of the microATX Motherboard Interface Specification.
- Observe keepout zones suggested in the microATX Motherboard Interface Specification.
- Ensure that add-in cards can be removed without hitting chassis features.
- Ensure that cables are easily accessible.
- If a tamper-detect switch is implemented, ensure the integrity of the switch with the chassis cover on and off

EMI Concerns

- VCC and VCC3
  - The bulk capacitors should be low in ESR and range from 10 to 22uF; the number needed is system-specific.
  - The decoupling capacitors should be in the range of 0.1 uF and should be placed around the power connectors and power pins of devices.
  - There should be an adequate number of stitching capacitors linking the VCC and VCC3 power planes.
- +12V, -12V, -5V, 5VSB—These other power sources are typically routed as thick traces. Bulk and decoupling capacitors should be added to support the power requirements of the system.
- PS_ON#—This signal should be routed to the power connector to allow the motherboard the ability to cycle power in the system. Care is needed to reduce EMI emission.
- PWR_OK—Route to the power supply connector. Care is needed to reduce EMI emission.

- Keep analog and digital signals apart.
- Keep externally routed signals (e.g., keyboard, mouse, front panel) away from high-speed logic signals.
- Do not route traces under devices that supply clock signals.
- Route high-speed signals on the bottom or inner signal layer when possible.
- Ensure that rear I/O connectors are located in the correct position so they make good contact with the I/O shield.

PCI Signals

Generally ensure that all AD and control signals are as short as possible. PCI_PM# needs to be pulled up near the host controller. Refer to previous sections "PCI Simulation," page 7, and "Simulation Results and Recommendations," page 7, for details on PCI simulation results.

- PCI Interrupts—Ensure that these signals have a termination/pullup resistor.
- PCI Clocks—For single I/O device support, use PCICLK0; for two devices, use PCICLK0 and PCICLK1; and so on. Take great care to minimize clock length and skew.
- REQ#/GNT#—For single master support, use REQ0#/GNT0#; for two devices, use REQ0#/GNT0# and REQ1#/GNT1#; and so on. Ensure that the appropriate pullup resistors are in place. Unused REQ#/GNT# pairs should be pulled up.
- DEVSEL#—Ensure that DEVSEL# is pulled high with a weak pullup resistor.
- SER_IRQ—Route to the appropriate device.
- IDSEL Assignment—Begin assigning IDSEL signals from the upper address options (start by using IDSEL0).
- PCI_PM#—Should be routed to all PCI I/O slots. No pullup resistor should be in place.
- FRAME#, TRDY#, IRDY#, STOP#, SERR#, PERR# and LOCK#—Should be pulled high.
- REQ64#—Should be pulled high.
- ACK64#—Should be pulled high.
- SBO# and SDONE—Should be pulled up separately with a ~5KΩ resistor

Power Signals

- 5VDC/3.3VDC/+12V/-12V/5VSB—Routed as planes or thick traces with the appropriate number of bulk and decoupling capacitors.
- PS_ON#—Route to on/off control on the power supply. The power supply provides the pullup.
- PWR_OK—Route to microATX connector and power supply connector.

ISA Signals

- All signals—Route all signals directly to ISA connectors or ISA-based circuitry.

IDE Signals

- Take great care to minimize trace lengths between the controller and the connector.

Floppy Signals

- All signals—Ensure that all signals requiring termination are properly terminated.

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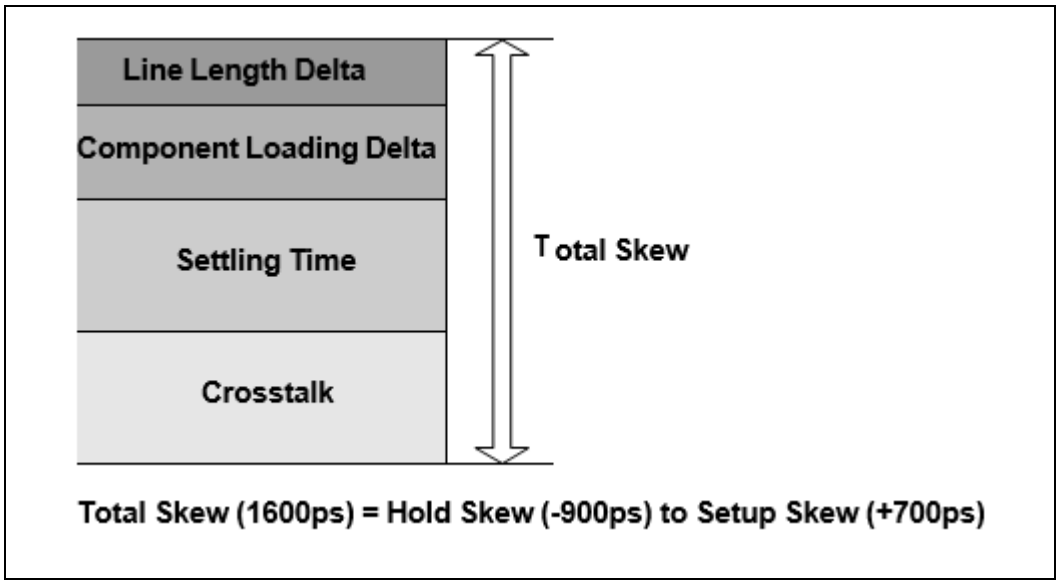
4 Electrical Implementation of AGP

A main issue that must be addressed in implementing AGP on microATX systems is the skew between traces during synchronous (2X Mode) operations. The skew is affected by such parameters as line length mismatch, capacitive loading variations, settling time, and crosstalk. Below figure shows the components of skew. As shown, settling time and crosstalk have the largest effects on skew; these interact with each other and the other parameters to compound the problems.

Figure 4-1. Skew Components



4.1 Simulation Results

The simulation results presented are for a specific motherboard and chipset combination. Therefore, motherboard OEMs are encouraged to perform their own independent simulations that will help guide the choice and layout of the components. Table 5 summarizes the recommendations resulting from our simulation studies.

The first column of the below Table signifies that the maximum line length depends on the routing rules on the motherboard. The width: space designation refers to the width of the trace in relation to the distances between traces. Because crosstalk is a key contributor to skew and crosstalk is decreased with increasing distance between traces, it is no surprise that you can achieve longer line lengths with larger ratios.

Table 4-1. Motherboard Recommendations for AGP

Width: Space	Zo	Trace	Line Length	Line Length Matching
1:1	50Ω to 85Ω	Data / Strobe	1.0in < line length < 4.5in	-0.5in, strobe longest trace
1:2	50Ω to 85Ω	Data / Strobe	1.0in < line length < 9.5in	-0.5in, strobe longest trace

The below Table shows the constraints imposed on the clock and control signals of the AGP bus. Because some of the control signals require pullup resistors, the stub to these resistors should be tightly controlled. The clock lines on the motherboard strictly depend on the clock driver that is being used and on the motherboard trace topology, so specific simulation needs to be done on these signals.

Table 4-2. Control and Clock Signal Recommendations

Width: Space	Board	Trace	Line Length	Pullup Stub Length
1:1	Motherboard	Control Signals	1.0in < line length < 8.5in	< 0.1in
1:2	Motherboard	Control Signals	1.0in < line length < 10.0in	< 0.1in
1:4 to strobe	Motherboard	Clock		

In multilayer motherboards, the designer must ensure that all signals are routed as a group. This implies that the group is collectively routed as either microstrip or stripline but not combined.

Grouping is necessary because traces routed on the external layer (microstrip) have different propagation delays than traces routed on internal layers (stripline).

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5 Definitions

This list defines how terms are used in this document; the terms are not intended to be industry definitions.

AGP

Accelerated Graphics Port. Refers to the devices supporting 1.0 of the AGP specification.

Bus Mastering

The ability for a PCI agent to function as an initiator in PCI transactions. For this to be possible, the agent must have access to a REQ#/GNT# pair of the PCI arbiter.

I/O Slot

Either a PCI or ISA connector that supports an add-in card.

PCI Agent

Either a PCI device or add-in card.

Pulldown Resistor

A resistive element used to place an undriven signal in a logic low state.

Pullup Resistor

A resistive element used to place an undriven signal in a logic high state.

REQ#/GNT#

Refers to the PCI request and grant signals on the PCI bus. Each request signal has an associated grant signal.

Parallel Termination

The process of adding a resistive element between a signal and either power or ground sources.

Series Termination

The process of adding a resistive element in series with a signal to provide a means of reducing ringing and ensuring signal integrity.

Termination

The process of adding either series or parallel termination to a signal.

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