Lab 4: Design of a 16-bit Adder

Report Due Date: April 24, 2020 at 11:59pm

- The goal of this lab is to design a 16-bit adder
- You will optimize the adder design for speed and area
- An important part of this lab is to verify the adder's functionality and characterize its performance

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1 Design of a 16-bit adder

Your goal is to design a **16-bit adder** according to the specifications shown in the grading section and under the following constraints:

1. Your adder must include a carry-in for the least-significant bit (LSB) and a carry-out for the most-significant bit (MSB).
2. All output bits, including the final carry-out, must drive a load of 10 fF.
3. Input signals have a 10 ps rise and fall time. Create a Verilog-A block to generate the input signals for the worst-case and best-case transitions (instead of analogLib components). Also use Verilog-A to generate other test input signals to verify the functionality of your adder design.
4. VDD = 1.2V and the standard operation temperature (25°) **cannot** be changed.
5. You must follow the standard-cell dimensions that have been used in the previous labs.

Hints:

- You may use the `lab2_signal_gen` file from Lab 2 as a template to generate the inputs for this Lab.
- You may use the `lab2_testing.m` file from Lab 2 as a template to verify (in terms of correctness and timing) the outputs of your circuit.
- There are multiple adder topologies; some simplify design and layout and also make it smaller, faster, or more energy efficient. You may have to try out different designs to maximize your score.
- You are allowed to size the transistor widths however you want.
- Spend effort in finding the worst-case delay of your adder.
- Test and verify corner cases of your adder to ensure proper functionality. It may be helpful to write a script that generates the test signals in the Verilog-A block.
- This lab will be completed in groups of four, specifically you will use your final project groups. A good adder design will likely help with completing your final project, so feel free to use the design from this lab for your group's final project.

2 Grading

Delay and area (30pts): The grade for delay and area will be determined using the following table:

Score	Delay **(15pts)**	Area **(15pts)**
5	$\max\{t_{\text{pHL}}, t_{\text{pLH}}\} \leq 1\text{ns}$	$\leq 1800\,\mu\text{m}^2$
4	$\max\{t_{\text{pHL}}, t_{\text{pLH}}\} \leq 1.1\text{ns}$	$\leq 2000\,\mu\text{m}^2$
3	$\max\{t_{\text{pHL}}, t_{\text{pLH}}\} \leq 1.2\text{ns}$	$\leq 3000\,\mu\text{m}^2$
2	$\max\{t_{\text{pHL}}, t_{\text{pLH}}\} \leq 1.3\text{ns}$	$\leq 4000\,\mu\text{m}^2$
1	$\max\{t_{\text{pHL}}, t_{\text{pLH}}\} \leq 1.4\text{ns}$	$\leq 8000\,\mu\text{m}^2$
0	otherwise	otherwise

The area is measured from the bounding box around your adder design that goes from half the top-most power rail to half the bottom-most power rail. The delay must be obtained using a simulation with parasitic extraction (i.e., using the `av_extracted` view) of the top-level module.

Layout (15pts): We will verify the quality of your layout (e.g., that standard-cell design rules and dimensions were properly used, that adjacent metal layers are routed in orthogonal directions, that nearby wires do not run in parallel for long distances, that a proper amount of metal layers is used, etc.)

Verification and testing (15pts): Fully test and verify the functionality of your design through MATLAB as you have learned in Lab 2. You should add a few slides explaining the following items:

- How did you compute/extract/identify the worst-case propagation delay?
- How did you verify the functionality of your adder? Does your adder really add any pair of numbers correctly? Does the carry-in and carry-out work properly?

Report (35pts): Complete the PowerPoint report template posted on Canvas. Make sure your schematics and plots are clear and legible. You can label Cadence screenshots or draw the schematics in a program of your choice. Make sure that you clearly label your screenshots, plots, and schematics. **Do not forget to include one slide explaining your design choice(s).**

Follow the rules (5 pts): If you follow all of our instructions, then you will get 5 points! If you fail in one of these, you get zero points. Turn in a *single* zip file containing all Cadence files and the report. Name the zip file Lab4-Group(groupnumber).zip without the parentheses. Convert your report to pdf, but include the original PowerPoint file in your submission too. Be sure to include all specified files in your zip file. Make sure none of your files are corrupted. We will not grade what we cannot open.

Important: We are going to try out all the submitted designs and compare our results to the reported numbers. In case you fudge on benchmark numbers, and the schematics and symbols are not submitted, the entire group gets penalized by 20%. In addition, we are going to use the performance numbers of the submitted design.