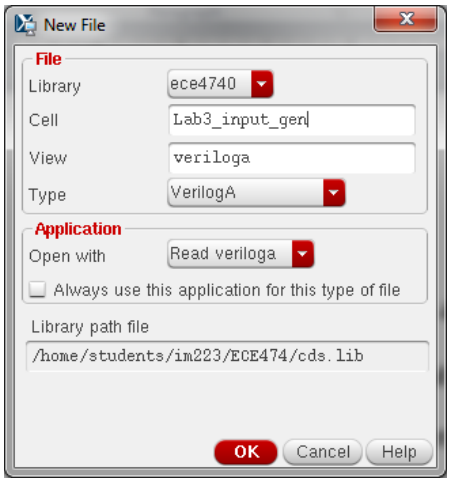
ECE 4740: Digital VLSI Design
Spring 2018

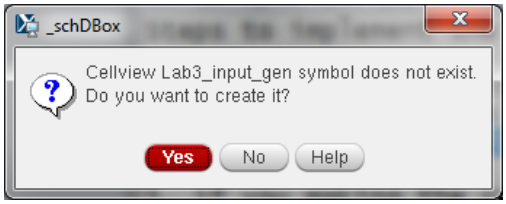
Quick start to implement Verilog-A block in Cadence virtuoso

1. Create a cellview of type verilog A



2. The new block comes with some preexisting code as the following:

3. Edit the code according to you specifications.
4. Save & quit.
5. If you making the cellview for the first time, cadence will automatically ask for making a symbol. Click yes.



Note: If you are just editing your existing code, Cadence won't ask anything. Just save & quit.

6. Follow through the instructions that pop-up and edit the symbol if you want. Click check & save.
7. Add the generated symbol in your test bench.
8. Check and save the test bench.
9. Launch ADE L. Click on “Netlist & Run”. Netlist is created for your Verilog-A block too along with rest of your circuit.