Lab 3: Timing of D flip-flops

Report Due Date: April 10 at 11:59 PM

- The goal is to design a D-flip-flop with layout
- You will simulate the key timing properties using Cadence Virtuoso
- You will also simulate a simple shift register

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1 Overview

In this lab, you will (i) layout a single-positive-edge-triggered master-slave D-flip-flop, and (ii) measure its setup, propagation, and hold times. You will then cascade two flip-flops and analyze the impact of clock skew on this simple shift register. The schematic of the D-flip-flop you have to layout and analyze is given in Fig. 1. It is a conventional master-slave single-positive-edge-triggered flip-flop where two MUX latches are put in series with two complementary clocks driving each latch. The transistors are all minimum sized with ratio 2:1 (width of PMOS by width of NMOS) as the D-flip-flop is assumed to drive only a small load of 2 fF. The bulk connections of the transmission gates should be connected to VDD and GND for the PMOS and NMOS, respectively.

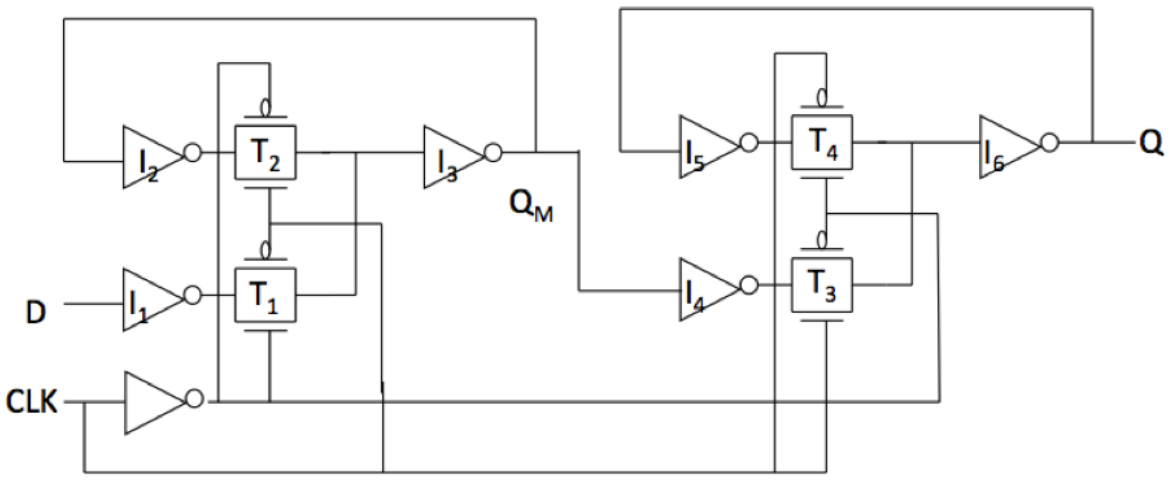


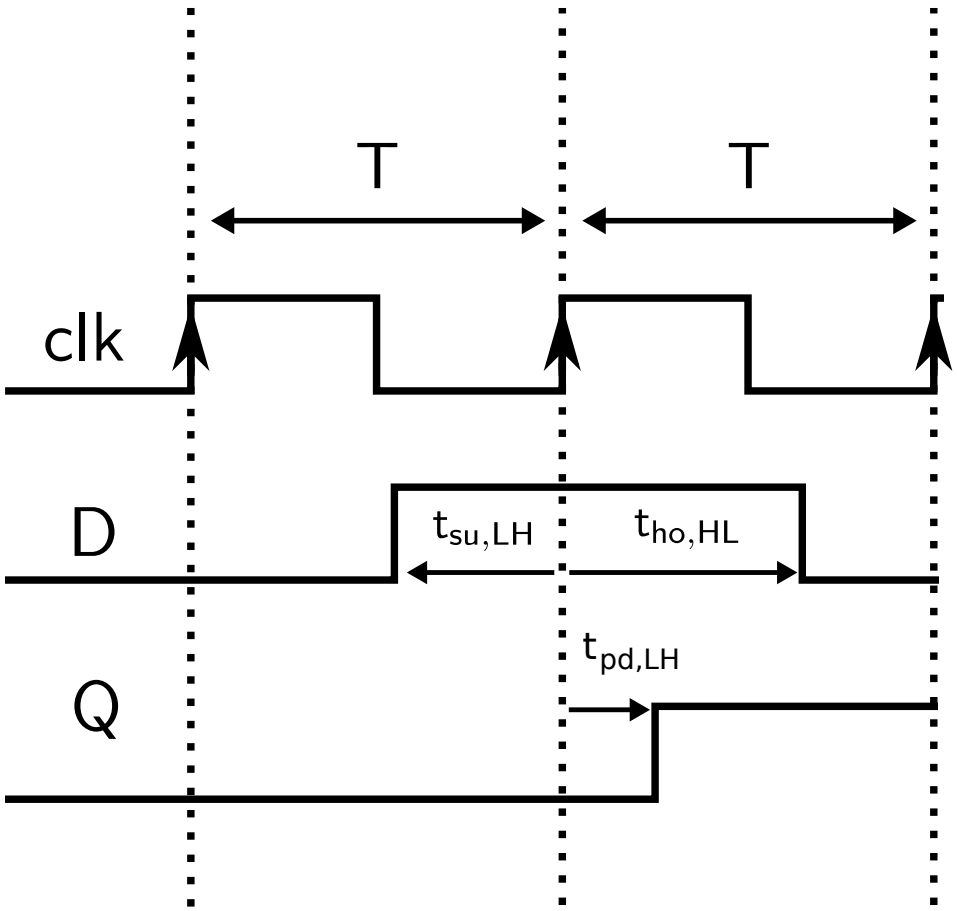
Figure 1: Schematic of the D flip-flop to implement

2 Build the layout (30pts)

Following the standard-cell dimensions that have been used for the previous labs, layout a single D-flip-flop with an *area that is not greater than* 50 μm^2. Your layout must pass DRC and LVS. You must perform parasitic extraction of your layout.

3 Design a test bench

Design a test bench that enables you to measure the setup time, propagation delay, and hold time as shown in the figure below (and as learned in class). Here, clk and D are inputs, and Q is the output. The output must drive a 2 fF load capacitance and the supply voltage must be VDD = 1.2 V. For both the input signal and the clock signal, use a rise and fall times of 10 ps. The parameter T denotes the clock period (usually measured in nanoseconds), and $t_{su,LH}$, $t_{pd,LH}$, and $t_{ho,HL}$ denote the low-to-high setup time, low-to-high propagation delay, and high-to-low hold times, respectively.



In the report, show the input and output waveforms from Cadence Virtuoso to demonstrate that your flip-flop circuit is indeed working. To do this, pick a setup and hold time that enables your flip-flop to sample the input value. Show that you can sample both high and low levels. Do not forget to include the output load capacitance in your schematic. Use a reasonable zoom so that one can see the transitions.

4 Measure the setup and hold times (30pts)

Use Cadence Virtuoso to measure the setup and hold times of your flip-flop. Recall that the setup and hold time are the minimum time *before* and *after* the rising clock edge the input signal must remain constant to

store the signal and to generate a stable output, respectively.

In the lecture, we considered (for simplicity) a single setup time t_{su} and hold time t_{ho}. In practice, however, these quantities typically depend on the signal transition (i.e., whether the input is going from low-to-high or from high-to-low) or the propagation delay that is allowed. To see these dependencies and to simulate all timing values, follow the directions below.

4.1 Simulate $t_{su,LH}$ and $t_{ho,HL}$ for a given propagation delay $t_{pd,LH}$

For an input signal going low-to-high and then high-to-low, as in the figure of the previous page, choose an appropriately large clock period T, hold time $t_{ho,HL}$, and setup time $t_{su,LH}$ where the output signals are stable. Now, try to decrease the setup time $t_{su,LH}$ until the output signal is affected. As you will see, instead of the output signal suddenly becoming unstable, its propagation delay will gradually increase until at one point the flip-flop is not working anymore (the input signal is no longer stored in the flip-flop). So the value of $t_{su,LH}$ can be different depending on the $t_{pd,LH}$ that is allowed. By sweeping $t_{su,LH}$ in a reasonable range, plot the propagation delay $t_{pd,LH}$ for a sufficiently fine resolution. From this plot, extract the value of $t_{su,LH}$ for which $t_{pd,LH} = 90\,\text{ps}$.

Now set $t_{su,LH}$ to the value you measured and try to decrease $t_{ho,HL}$ until the output signal becomes unstable. You will see a similar trend where the $t_{ho,HL}$ depends on the $t_{pd,LH}$ that is allowed. By sweeping $t_{ho,HL}$ in a reasonable range, plot the propagation delay $t_{pd,LH}$ and report the value of $t_{ho,HL}$ for which $t_{pd,LH} = 91\,\text{ps}$.

Remark: You have now identified a suitable setup and hold time pair for your flip-flop, assuming a propagation delay constraint of 91 ps. Note that these timing values only apply for the given load; other loads would result in different timing values.

4.2 Simulate $t_{su,HL}$ and $t_{ho,LH}$ for a given propagation delay $t_{pd,HL}$

For an input signal going high-to-low and then low-to-high, follow similar steps to Part 4.1 and plot the propagation delay $t_{pd,HL}$ vs. $t_{su,HL}$ and $t_{ho,LH}$ and compute the values of $t_{su,HL}$ and $t_{ho,LH}$ for which $t_{pd,HL} = 90\,\text{ps}$ and 91 ps, respectively.

Remark: In practice, one would only specify the worst-case of the rising and falling setup and hold times. But modern tools actually consider all the different setup and hold times for accurate timing analysis.

5 Cascade two D-flip-flops (30pts)

Assuming an input pulse of low-to-high and high-to-low, cascade two flip-flops together connected to the same clock signal. Here, the final load capacitance at the output of the 2nd flip-flop is still 2 fF. Does your simple shift register circuit still work? Specifically, does the output of the second flip-flop sample the input pulse after two clock cycles? Explain why your setup does/does not work.

Now, assume that there is a positive clock skew on the clock signal of the second flip-flop (the clock for the second flip-flop is delayed). By simulating your circuit, find out what is the maximum clock skew for which the shift register stops working? Repeat all the above steps for a high-to-low and low-to-high input pulse.

Important: For this section, you do **not** *need to make a layout where you interconnect both flip-flops. You can just instantiate two single flip-flops and connect them together. However, you must use the* `av_extracted` *view for the simulation.*

6 Follow the directions (10pts)

If you follow our instructions, then you will get 10 points!

- Complete the PowerPoint report template posted on Canvas. Make sure your schematics and plots are clear and legible. You can label Cadence screenshots or draw the schematics in a program of your choice. Be sure that you clearly label your screenshots, plots, and schematics. The objective is to create a concise report that could be evaluated quickly. Finally, convert the report into a pdf file.
- Turn in a *single* zip file containing your Cadence files (schematics, layouts, and symbols) and the report. Name the zip file Lab3-(NetID).zip without the parentheses. Also have your report converted to pdf and be sure to include all specified files in your zip file. Also make sure none of your files are corrupted. What we cannot open, we will not grade.
- The report is due on April 10 at 11:59 PM.
- *Note: There is no real-time evaluation for this lab!*

Important: We will try out all the submitted designs and compare it to the reported numbers. In case you fudge on benchmark numbers, and the Cadence files (schematics, layouts, and symbols) are not submitted, you will get penalized by 20%. In addition, we are going to use the performance numbers of the submitted design.