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ece4740_yyyy_fir-release.zip
  readme.pdf          # this file
  report.pdf          # project report
  presentation.pdf    # presentation slides
  ece4740_yyyy_fir-release
    adder_group        # adder group (used in FIR_GL)
    addg_sigen         # signal generator of adder group
    addg_tb            # adder group testbench
    and_tb             # AND gate testbench
    AND2               # 2-input AND
    AND4X1             # NOT IN USE
    carry_group        # carry group (used in CSA16)
    CSA16              # 16-bit carry skip adder
    DFF                # D-flip-flop
    DFF_reset          # D-flip-flop with synchronous reset (active low)
    FIR_GL             # FIR filter
    FIR_GL_sigen       # signal generator of FIR filter
    FIR_GL_tb          # FIR filter testbench
    HA                 # half adder
    INVX1              # inverter
    MFA                # mirror full adder
    MFA_sigen          # signal generator of MFA
    MFA_test            # MFA testbench
    MUL_GL              # multiplier
    mul_sigen          # signal generator of multiplier
    mul_tb              # multiplier testbench
    MUX2X1              # 2-input mux
    NAND4X1             # 4-input NAND
    rFA                 # reduced full adder
    reg_sigen           # signal generator of RSTReg16
    reg_tb              # RSTReg16 testbench
    RSTReg16            # 16-bit register with synchronous reset (active low)
    XOR2X1              # 2-input XOR

matlab
  ADDG_testing.m      # used for testing the adder group
  FIR_testing.m       # used for testing the FIR filter
  MUL_testing.m       # used for testing the multiplier

tbgen
  addtbggen.py        # used to generate the VerilogA addg_sigen. "python addtbggen.py -h" for help.
  firtbgen.py          # used to generate the VerilogA FIR_GL_sigen. "python firtbgen.py -h" for help.
  multbgen.py          # used to generate the VerilogA mul_sigen. "python multbgen.py -h" for help.
  regtbgen.py          # used to generate the VerilogA reg_sigen. "python regtbgen.py -h" for help.
  addg_sigen.txt       # text to be copied into VerilogA addg_sigen
  FIR_GL_sigen.txt    # text to be copied into VerilogA FIR_GL_sigen
  mul_sigen.txt        # text to be copied into VerilogA mul_sigen
  reg_sigen.txt        # text to be copied into VerilogA reg_sigen

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ASIC_evaluation      # please refer to tutorials of ECE4750 and ECE5745 for details
asic
designs
    flow.py      # used to configure the ASIC tool flow
    .mflowgen.yml
sim
    FIRRTL.py    # pymtl3 wrapper of the FIR filter
    FIRRTL.v     # source code of the FIR filter
    FIRRTL_test.py # pymtl3 testbench of the FIR filter
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ECE4750 : <https://www.csl.cornell.edu/courses/ece4750/handouts.html>

ECE5745 : <https://www.csl.cornell.edu/courses/ece5745/handouts.html>

pymtl3 : <https://github.com/pymtl/pymtl3>