Design of Digital FIR Filter

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Introduction

This proposed project is to design a digital finite impulse response (FIR) filter in the standard cell-based full-custom design methodology. The whole project will be divided into 3 parts: standard cell, baseline design, and alternative design. The reason why we focus on FIR filters is that the other type of digital filter, infinite impulse response (IIR) filter, could be composed with 2 FIR filters, and, more importantly, FIR filters are more widely used in the industry than IIR filters due to their stability and powerful CAD support.

In this project, we will use MATLAB or Python to simulate the function level model of the design, exploring the trade-off between data precision and area. We will also use the RTL synthesizer and simulator to verify the correctness of our schematic. We will also combine MATLAB or Python with Cadence Virtuoso to perform post-layout verification.

Project Contents

1. Standard Cell

Project group members will collect their designs in the previous labs to form a standard cell library.

2. Baseline Design

The baseline design we proposed is to implement an FIR filter for a given frequency response shown in Fig.1 and its structure is shown in Fig.2. This is a 16-bit, fixed-point, full-precision, 3-order FIR filter. The implementation of the baseline design is divided into 3 steps: Functional simulation, layout design, and post-layout verification.

3. Alternative Design

We have 3 choices of alternative design. One is to further optimize the baseline design, including cutting off some trivial bits of the multipliers and adders, decreasing the data precision to achieve lower area and better performance. Another choice is to make the filter coefficients configurable - now we could modify its frequency response by inputting different sets of coefficients into it. The last choice is not to implement an alternative design if it takes us too much time on the baseline design, which is to be an “emergency exit button” since none of us have the experience of digital full-custom design so our estimation on the workload and our capability might be wrong.

4. Possible trade-offs

Area-performance: Generally, given the same function, the more area you take, the better performance you are likely to have, which will determine the max clock frequency, thus the max sample rate.

Area-precision: In general, better precision (both for intermediate results and inputs) will lead to a larger area.

Performance-power: This is an everlasting trade-off in digital circuits. If the design is to be clocked at a higher speed, it will consume more power. The power overhead not only comes from the increased switching speed but also from the extra hardware used to optimize the critical path (e.g. pipeline registers).

Background

The Digital finite impulse response (FIR) filter has lots of arithmetic and logical operations. The optimized design of adders and multipliers can impact the performance of the FIR system. Therefore, choosing and designing the arithmetic operation architecture is at the top of the agenda. Some of the modern FIR system design [1] suggests Regular Carry Select Adder (RCSA) which consumes a large area and has a long delay because it uses several Ripple Carry Adders and multiplexers. One possible way to reduce the delay is by using n-bit Binary to Excess-1 Converter (CSLA using BEC), calculating two possible results in parallel. Some architectures for the full adder we might use in our project are Static CMOS Full Adder which uses 28 transistors and The Mirror Adder which only uses 24 transistors.

The other important part of the FIR Filter System is the implementation of the multiplier. Wallace Tree Multiplier [1] is the most common multiplier we can see in the VLSI implementation. It is a fast way to multiply two binary integers but sacrifices the area to improve the speed of operation. Another possible optimization of the multiplier for the FIR Filter is Computation Sharing Multiplier (CSM) [2]. This system has a pre-computation module that pre-cooks some common possible results and just does some small adjustment by the full adder to produce correct results. This novel idea can be used when we are doing the alternative design: configurable FIR Filter.

There are many other researches that propose faster filters by improving the architecture of the multiplier and the adder to harvest the potential parallelism of the system [3][4]. These novel architectures could calculate intermediate results concurrently, while some optimized for power and others for area efficiency.

Foreseeable challenges and questions

1. Multiplier design:

There are plenty of architectures of multipliers and we need to choose one that performs well in terms of timing or area and at the same time easy to implement for full-custom design.

2. The trade-off on the decimal precision:

As is mentioned in the introduction part, we plan to use software simulation to observe the trade-offs and then decide the decimal precision.

3. Synchronization:

The data input uses the sampling clock while the multipliers should use a different clock (which is expected to be faster than the sampling clock) so there comes the problem of how to synchronize between the two clock domains.

Project management

1. Members:

Yixiao Du (yd383), Yibang Xiao (yx455), Yuxiang Long (yl3377), Yifan Yang (yy887)

2. Division of labor:

Yixiao Du: Architect, verification and all software work.
Yibang Xiao: Multiplier design, final layout.
Yuxiang Long: Multiplier design, final layout.
Yifan Yang: Adder design, final layout.

3. Timeline and milestones:

	Hardware	Software
Apr 8 - Apr 14	Adder and Multiplier Design	Functional simulation
Apr 15- Apr 21	System Design (1st milestone)	Test adder and multiplier
Apr 22 - Apr 28	Floorplanning and wiring	Develop system verification
Apr 29 - May 5	Alternative Design (2nd milestone)	Test alternative design
May 6 - May 12	Final verification and report	
May 13	Presentation and Q & A	

Reference:

[1] *P.C.Franklin, M. Ramya, R. Nagarajan, T.M. Mini Priya, M. Balamurugan, "Design of Resource Efficient FIR Filter Structure Using Adders and Multiplier" International Journal of Advanced Research in Computer and Communication Engineering, vol. 3, Issue 2, February 204.*

[2] *V. Thamizharasan, V. Parthipan, "An Efficient VLSI Architecture for FIR Filter using Computation Sharing Multiplier" International Journal of Computer Applications (0975 - 8887), vol. 54-No.14, September 2012*

[3] *Haridas, G., & George, D. S. (2016). Area Efficient Low Power Modified Booth Multiplier for FIR Filter. Procedia Technology, 24, 1163-1169.*

[4] *Jayashree, M. Design of High Speed and Area Efficient FIR Filter Architecture using modified Adder and Multiplier.*

Appendix:

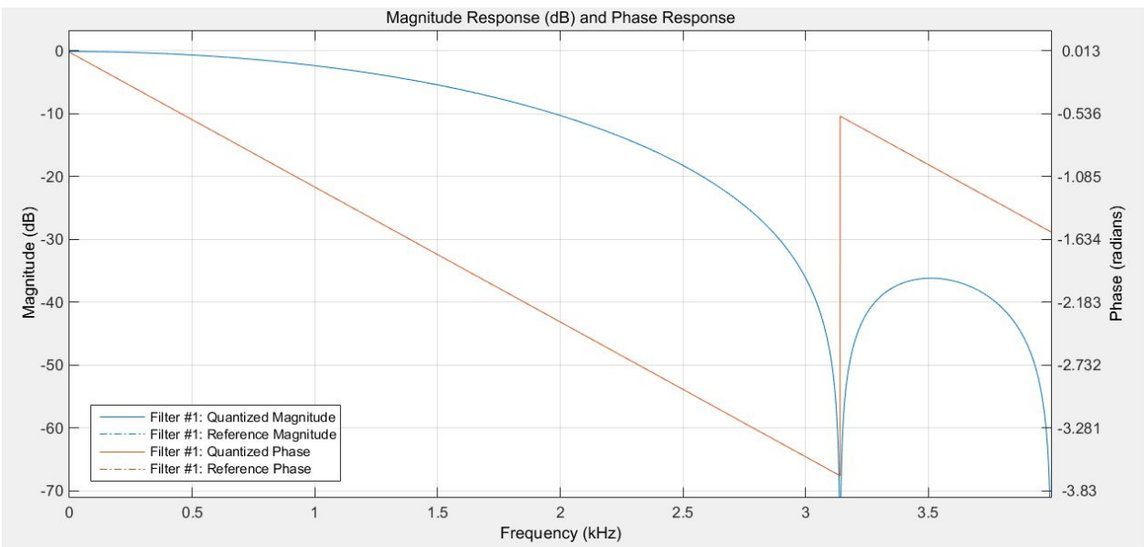

Fig. 1 Frequency Response of Baseline Design Filter

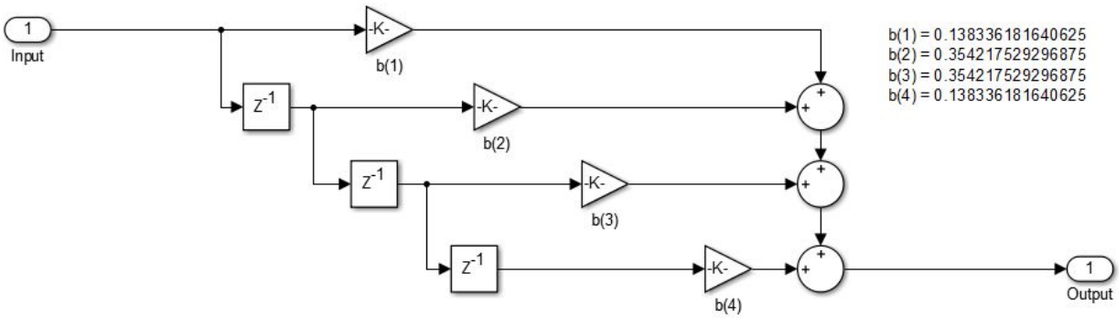

Fig. 2 Structure of Baseline Design Filter