

## ECE 4740 Final Project

### GROUP / DESIGNATOR:

#### DIFFICULTY (display of time and effort spent) :

Is FULL CUSTOM layout DRC clean?	0	1	2	3	4	5		
Is FULL CUSTOM layout LVS clean?	0	2	2	3	4	5		
Estimated Transistor count:	0	1	2	3	4	5	6	7
Estimated difficulty of project:	0	1	2	3	4	5	6	7

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#### COMPLEXITY (demonstration of fluency with course content) :

understanding of metrics / trade-offs:	0	1	2	3	4	5		
how many types of logic were used?				3		5		7
hierarchical design methodology/optimization	0	1	2	3	4	5	6	
back-of-envelope analysis	0	1	2	3	4	5	6	

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#### CREATIVITY (how well did they use course content and go beyond) :

Used sub-blocks beyond "basic" / lecture	0	1	2	3	4	5	6	
Demonstration of problem-solving /opt	0	1	2	3	4	5	6	
Creativity of overall endeavor	0	1	2	3	4	5	6	
Creativity of demonstration	0	1	2	3	4	5	6	

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#### PERFORMANCE :

Exhaustive simulation/proof of function	0	1	2	3	4	5	6	7
Rigor of presented comparison	0	1	2	3	4	5	6	7
Awareness of approximations/inaccuracies	0	1	2	3	4	5	6	
wow factor	0	1	2	3	4	5	6	

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PRESENTATION (10 pts)

**(4 pts)** Completeness (-1 for each missing element)

Literature review

FoM

Full system architecture block diagram

Critical sub-block function/performance

Full system function/performance

Overview of member contributions

**(6 pts)** Presentation Quality

Clarity of communication	0	1	2	3	4	5	6
Quality of slides	0	1	2	3	4	5	6
Effective/efficient use of allotted time	0	1	2	3	4	5	6

REPORT (15 pts)

**(10 pts)** Completeness (-2 for missing element; -1 for incomplete element)

Introduction to trade-offs and metrics

Hierarchy

Design methodology

Comparison

Functionality

Troubleshooting

**(5 pts)** Report Quality

Clarity, organization, and formatting	0	1	2	3	4	5
Quality of diagrams and data	0	1	2	3	4	5
Technical correctness	0	1	2	3	4	5