

ece4740\_yyyy\_fir-release.zip

readme.pdf # this file  
report.pdf # project report  
presentation.pdf # presentation slides

ece4740\_yyyy\_fir-release

add\_group # adder group (used in FIR\_GL)  
addg\_sigen # signal generator of adder group  
addg\_tb # adder group testbench  
and\_tb # AND gate testbench  
AND2 # 2-input AND  
AND4X1 # NOT IN USE  
carry\_group # carry group (used in CSA16)  
CSA16 # 16-bit carry skip adder  
DFF # D-flip-flop  
DFF\_reset # D-flip-flop with synchronous reset (active low)  
FIR\_GL # FIR filter  
FIR\_GL\_sigen # signal generator of FIR filter  
FIR\_GL\_tb # FIR filter testbench  
HA # half adder  
INVX1 # inverter  
MFA # mirror full adder  
MFA\_sigen # signal generator of MFA  
MFA\_test # MFA testbench  
MUL\_GL # multiplier  
mul\_sigen # signal generator of multiplier  
mul\_tb # multiplier testbench  
MUX2X1 # 2-input mux  
NAND4X1 # 4-input NAND  
rFA # reduced full adder  
reg\_sigen # signal generator of RSTReg16  
reg\_tb # RSTReg16 testbench  
RSTReg16 # 16-bit register with synchronous reset (active low)  
XOR2X1 # 2-input XOR

matlab

ADDG\_testing.m # used for testing the adder group  
FIR\_testing.m # used for testing the FIR filter  
MUL\_testing.m # used for testing the multiplier

tbgen

addtbgen.py # used to generate the VerilogA addg\_sigen. "python addtbgen.py -h" for help.  
firtbgen.py # used to generate the VerilogA FIR\_GL\_sigen. "python firtbgen.py -h" for help.  
multbgen.py # used to generate the VerilogA mul\_sigen. "python multbgen.py -h" for help.  
regtbgen.py # used to generate the VerilogA reg\_sigen. "python regtbgen.py -h" for help.  
addg\_sigen.txt # text to be copied into VerilogA addg\_sigen  
FIR\_GL\_sigen.txt # text to be copied into VerilogA FIR\_GL\_sigen  
mul\_sigen.txt # text to be copied into VerilogA mul\_sigen  
reg\_sigen.txt # text to be copied into VerilogA reg\_sigen

ASIC\_evaluation           # please refer to tutorials of ECE4750 and ECE5745 for details  
  asic  
    designs  
      flow.py           # used to configure the ASIC tool flow  
      .mflowgen.yml  
  sim  
    FIRRTL.py          # pymtl3 wrapper of the FIR filter  
    FIRRTL.v           # source code of the FIR filter  
    FIRRTL\_test.py     # pymtl3 testbench of the FIR filter

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ECE4750 : <https://www.csl.cornell.edu/courses/ece4750/handouts.html>

ECE5745 : <https://www.csl.cornell.edu/courses/ece5745/handouts.html>

pymtl3 : <https://github.com/pymtl/pymtl3>