

Instruction Set

24 Oct. 2020

32-bit instruction format

31:29	28:24	23:16	15:8	7:0
opcode	raddr2 (s3)	raddr1 (s2)	raddr0 (s1)	waddr (dst)

opcode: complex operation code

raddr2: read address 2 of the data memory (5-bit)

raddr1: read address 1 of the data memory (8-bit)

raddr0: read address 0 of the data memory (8-bit)

waddr: write address of the data memory (8-bit)

Opcode:

000	001	010	011	101	110	111
LOAD	ADD	SUB	MUL	MAX	MULSUB	MULADD

All of the above are complex operations. (e.g. ADD: $(a+jb) + (c+jd)$)

Examples in RISC-V fashion:

Assembly	Operation	Instructions in Hex
ADD \$128, \$16, \$48	$R128 = R16 + R48$	32'h20_30_10_80
MUL \$129, \$17, \$49	$R129 = R17 + R49$	32'h60_31_11_81
MULADD \$130, \$18, \$50, \$0	$R130 = R18 + R0 * R50$	32'hF0_32_12_82
MULSUB \$131, \$129, \$128, \$1	$R131 = R129 + R1 * R128$	32'hE1_81_80_83

Assuming the overlay is comprised of an array of 256 PEs and each PE has 4 DSP blocks. The instruction schedule can be found as follows (if running at 500MHz, 1 cycle = 2ns):

Cycle	Operation	Instruction
256*32	Load input data¹	Nil
1*32	<i>Complex multiplication</i>	$(a+jb)*(c+jd) \rightarrow a' + jb'$
1*80	<i>FFT</i>	$a' + jb' + W_N(c'+jd') \rightarrow a'' + jb''$
1*80		$a' + jb' - W_N(c'+jd') \rightarrow c'' + jd''$
1*16	<i>Output half values</i>	Nil
32	<i>Shift internal data²</i>	Nil
1*32	<i>Complex multiplication</i>	$(a+jb)*(c+jd) \rightarrow a' + jb'; c' + jd'$
1*80	<i>FFT</i>	$a' + jb' + W_N(c'+jd') \rightarrow a'' + jb''$
1*80		$a' + jb' - W_N(c'+jd') \rightarrow c'' + jd''$
1*16	<i>Output half values</i>	Nil
32	<i>Shift data</i>	Nil
...
256*32	Fetch output data	Nil

^{1,2}Load input data, Shift internal data and Fetch output data do not require instructions.

They are handled by the SIPO and PISO modules.

$$\text{Latency} = (256*32 + (32+2*80+16) + 255*(32+32+2*80+16) + 256*32) * 2\text{ns} = 0.156 \text{ ms}$$

Q. How to do a MAX operation among all the outputs of the 256 PEs (after square operation)? Add logic fabrics after the 256 PEs?

Instructions for SCD kernel:

8 element-wise complex multiplications

MUL \$80, \$0, \$32

MUL \$81, \$1, \$33

MUL \$82, \$2, \$34

MUL \$83, \$3, \$35

MUL \$84, \$4, \$36

MUL \$85, \$5, \$37

MUL \$86, \$6, \$38

MUL \$87, \$7, \$39

8-point FFT (bit-reverse order)

stage 1

MULADD \$88, \$80, \$84, \$0

MULSUB \$89, \$80, \$84, \$0

MULADD \$90, \$82, \$86, \$0

MULSUB \$91, \$82, \$86, \$0

MULADD \$92, \$81, \$85, \$0

MULSUB \$93, \$81, \$85, \$0

MULADD \$94, \$83, \$87, \$0

MULSUB \$95, \$83, \$87, \$0

stage 2

MULADD \$96, \$88, \$90, \$0

MULSUB \$98, \$88, \$90, \$0

MULADD \$97, \$89, \$91, \$2

MULSUB \$99, \$89, \$91, \$2

MULADD \$100, \$92, \$94, \$0

MULSUB \$102, \$92, \$94, \$0

MULADD \$101, \$93, \$95, \$2

MULSUB \$103, \$93, \$95, \$2

stage 3

MULADD \$104, \$96, \$100, \$0

MULSUB \$108, \$96, \$100, \$0

MULADD \$105, \$98, \$102, \$1

MULSUB \$109, \$98, \$102, \$1

MULADD \$106, \$97, \$101, \$2

MULSUB \$110, \$97, \$101, \$2

MULADD \$107, \$99, \$103, \$3

MULSUB \$111, \$99, \$103, \$3

32 element-wise complex multiplications

MUL \$80, \$0, \$32
MUL \$81, \$1, \$33
MUL \$82, \$2, \$34
MUL \$83, \$3, \$35
MUL \$84, \$4, \$36
MUL \$85, \$5, \$37
MUL \$86, \$6, \$38
MUL \$87, \$7, \$39
MUL \$88, \$8, \$40
MUL \$89, \$9, \$41
MUL \$90, \$10, \$42
MUL \$91, \$11, \$43
MUL \$92, \$12, \$44
MUL \$93, \$13, \$45
MUL \$94, \$14, \$46
MUL \$95, \$15, \$47
MUL \$96, \$16, \$32
MUL \$97, \$17, \$33
MUL \$98, \$18, \$34
MUL \$99, \$19, \$35
MUL \$100, \$20, \$36
MUL \$101, \$21, \$37
MUL \$102, \$22, \$38
MUL \$103, \$23, \$39
MUL \$104, \$24, \$40
MUL \$105, \$25, \$41
MUL \$106, \$26, \$42
MUL \$107, \$27, \$43
MUL \$108, \$28, \$44
MUL \$109, \$29, \$45
MUL \$110, \$30, \$46
MUL \$111, \$31, \$47

32-point FFT (bit-reverse order)

stage 1

MULADD \$112, \$80, \$96, \$0
MULSUB \$113, \$80, \$96, \$0
MULADD \$114, \$88, \$104, \$0
MULSUB \$115, \$88, \$104, \$0
MULADD \$116, \$84, \$100, \$0
MULSUB \$117, \$84, \$100, \$0
MULADD \$118, \$92, \$108, \$0
MULSUB \$119, \$92, \$108, \$0
MULADD \$120, \$82, \$98, \$0
MULSUB \$121, \$82, \$98, \$0
MULADD \$122, \$90, \$106, \$0

MULSUB \$123, \$90, \$106, \$0
MULADD \$124, \$86, \$102, \$0
MULSUB \$125, \$86, \$102, \$0
MULADD \$126, \$94, \$110, \$0
MULSUB \$127, \$94, \$110, \$0
MULADD \$128, \$81, \$97, \$0
MULSUB \$129, \$81, \$97, \$0
MULADD \$130, \$89, \$105, \$0
MULSUB \$131, \$89, \$105, \$0
MULADD \$132, \$85, \$101, \$0
MULSUB \$133, \$85, \$101, \$0
MULADD \$134, \$93, \$109, \$0
MULSUB \$135, \$93, \$109, \$0
MULADD \$136, \$83, \$99, \$0
MULSUB \$137, \$83, \$99, \$0
MULADD \$138, \$91, \$107, \$0
MULSUB \$139, \$91, \$107, \$0
MULADD \$140, \$87, \$103, \$0
MULSUB \$141, \$87, \$103, \$0
MULADD \$142, \$95, \$111, \$0
MULSUB \$143, \$95, \$111, \$0

stage 2

stage 3

stage 4

stage 5