Instruction Scheduling of the PE Array

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Below is an idea of ***Iterative Modulo Scheduling*** which is very efficient on hardware.

Cycle	PE_0	PE_1	PE_2	PE_K	PE_K+1	PE255
32	$\boldsymbol{X_0^T, Y_0^T}$					
32	**MULT**	$\boldsymbol{X_1^T, Y_0^T}$				
160	**FFT_32**	**MULT**	$\boldsymbol{X_2^T, Y_0^T}$			
16	**Output**	**FFT_32**	**MULT**	……		
32	$X_0^T\ Y_1^T$	**Output**	**FFT_32**		……	
32	MULT	$X_1^T\ Y_1^T$	**Output**			$\boldsymbol{X_{255}^T, Y_0^T}$
160	FFT_32	MULT	$X_2^T\ Y_1^T$			**MULT**
16	Output	FFT_32	MULT	……		**FFT_32**
	……	Output	FFT_32		……	**Output**
		……	Output			X_{255}^T, Y_1^T
			……			MULT
				……		FFT_32
					……	Output
						……
	$\boldsymbol{X'^T_0, Y'^T_0}$					
		$\boldsymbol{X'^T_1, Y'^T_0}$				

II

Latency = 32 * 255 + (32 + 32 + 160 + 16) * 256 cycles = 69600 cycles = **0.139 ms** (@500MHz)

Throughput = 1 / II = 1 / ((32 + 32 + 160 + 16) * 256 * 2ns) = **8138 samples/s**

Proposed PE array consumes 1,024 DPSs and 512 BRAMs (1 PE uses 4 DSPs and 2 BRAMs).

Available resource on Xilinx RFSoC (ZCU111) platform:

LUT	FF	BRAM	DSP	URAM
425,280	850,560	1,080 (36Kb)	4,272	80 (288Kb)