Final testbench for 4-to1 IF

- A testbench is uploaded named “testbench_IF.sp”.
- You are supposed to change only
  1. Clock period which is defined as “period” in the testbench.
  2. Include your .sp or .spf file name. Change the pin names accordingly. (Follow the naming convention in the testbench when you draw your schematic and layout)
  3. Lib file (put your AFS directory path).
- Download the model_IF.txt and IF.sh files
- Run the testbench without renaming it.

```
>hspice –i testbench_IF.sp
```

- Change permissions of IF.sh and run it.

```
>chmod 774 IF.sh
>sh IF.sh
```

- If it shows “Passed” then your circuit is functioning correctly, otherwise you need to debug.