EELE 367 – Logic Design (4cr)
Department of Electrical & Computer Engineering
Montana State University - Bozeman, MT
Spring 2019

Description: This 4-credit course introduces students to advanced digital logic design. This course is a continuation of *EELE 261 – Introduction to Logic Circuits* and covers large scale digital system design using a hardware description language (VHDL). This course covers the VHDL language in depth and explains how to use it to describe complex combinational circuits, synchronous sequential logic circuits, and computer systems. Functional verification of VHDL designs is accomplished using a logic simulator. This course includes a weekly lab where students will get hands-on experience implementing digital systems on Field Programmable Gate Arrays.

Outcomes: At the end of this course the student should be able to:

1) Understand how to describe a digital system using a Hardware Description Language.
2) Model complex combinational logic in VHDL.
3) Model complex sequential logic in VHDL including state machines and counters.
4) Incorporate pre-existing logic cores into your VHDL design.
5) Understand the HDL design flow including synthesis and place/route and its effect on timing.
6) Perform logic simulations on a VHDL design.
7) Prototype digital systems on an FPGA.

Instructor:
Dr. Brock J. LaMeres
316-C Norm Asbjornson Hall
phone: 406-994-5987
email: lameres@montana.edu
web: www.montana.edu/blameres/

Lab TA: See course website for most up to date contact information.

Time & Location:

Lecture (EELE 367-01),	MWF,	11:00am – 11:50am,	043 Gains Hall
Lecture (EELE 367-02),	W,	2:10pm – 4:00pm,	601 Cobleigh Hall
Lecture (EELE 367-03),	W,	4:10pm – 6:00pm,	601 Cobleigh Hall
Lecture (EELE 367-04),	W,	6:10pm – 8:00pm,	601 Cobleigh Hall

Textbook: (required)
"Introduction to Logic Circuits and Logic Design with VHDL", by Brock J. LaMeres
Springer International Publishing, 1st edition, 2016.
Available in MSU Bookstore. However, it is typically cheaper through Amazon (~$60).

Website: https://ecat.montana.edu/ This is the *Brightspace* course management system. This website will be used for all materials within the course. If you have technical difficulties with the system (i.e., can't login, the system is down, etc…), contact the ITC help desk at 994-1777.

Office Hours: Check instructor website for up-to-date office hours.

Requisites: Prerequisite: EELE 261

Grading:

Distribution		Letter Assignment	
Homework	- 15%	90% - 100%	= A
Laboratory	- 45%	80% - 89%	= B
Quizzes	- 20%	70% - 79%	= C
Final Project	- 20%	60% - 69%	= D
		0% - 59%	= F

Instructor reserves the right to apply a grading curve and to assign +/-'s to grades as appropriate.

All assignments for homework and labs will be due on Wednesday at 11:59pm of the following week that the assignment/lab was covered. The exact due dates for each assignment are at the end of this document and also in BrightSpace.

Late assignments will not be accepted unless a prior arrangement has been made with the instructors.

Most labs can be accomplished in the allotted 2-hour lab time. If you don't get through a lab, you have until the following Wednesday to turn it in. That gives you the following lab period to work on it. But be cautious as it is easy to fall behind on the labs.

General Outline:

1) VHDL (Part 2)
2) Behavioral Modeling of Sequential Logic
3) Memory
4) Programmable Logic
5) Arithmetic Circuits
6) Computer System Design

Hardware & Software

All of the lab exercises will be performed using the *TerasIC* DE0-CV board containing the Altera Cyclone V FPGA and the *Digilent* Analog Discovery 2 (AD2) portable oscilloscope. In the Cobleigh 601 digital lab there is one of these boards located at each computer station for you to use. If you would like to purchase your own hardware to work on the assignments outside of class (NOT REQUIRED), you can purchase the DE0-CV from http://www.terasic.com.tw/ and the AD2 from https://analogdiscovery.com/.

The software used to synthesis the designs is free for download from www.altera.com (now owned by Intel) The name of the synthesizer to get is *Quartus Prime Lite* Edition. After going to the website, navigate to: Support → Intel FPGA Support Home → Download Center for FPGA Design Software. You will want to select the most current version of Quartus (18.1 as of January 2019), and then click on the Lite download icon. You'll need to create a free account. Along with the download you will need to specify the devices that you will be targeting. Just select the Cyclone V family to minimize the size of the download (i.e., unselect Arria II, Cyclone IV, etc...). You will also want to get the *Model-Altera Edition* software as part of the download, which is selected for download by default. We will be using ModelSim to perform functional simulations of your VHDL for homework and labs.

Academic Policies:

This course will follow the policies outlined in the *Conduct Guidelines and Grievance Procedures for Students" (http://www2.montana.edu/policy/student_conduct/)* and the *MSU Policy and Procedures Manual* (http://www2.montana.edu/policy/). Please consult these documents on policies regarding academic honesty, student and instructor rights, and general standards of conduct.

Collaboration: You are allowed and encouraged to collaborate on homework and lab exercises. A *collaboration* means that each member of the team contributes to the effort. It is considered cheating if a student simply provides, or receives, the solution to other team members. For homework problems in the form of multiple-choice quizzes, each student must complete the quiz in D2L. For homework problems in the form of VHDL assignments, each student must upload the requested deliverables. **You are NOT to work together on the quizzes**.

Plagiarism. It is considered plagiarism to simply "copy" VHDL code from the internet without citing it. The internet is a great resource for getting code examples and you are encouraged to use it. However, it is critical that if you use code from the internet, you insert a citation from the source. Citations can be inserted as comments within your VHDL. You should insert citations even if you just using the same approach that you found online.

EELE 367 - Logic Design (Activity Flow, Deadlines & Grading)

Dates	Module	Section / Topic / Activity	HW Points	Lab Points	Quiz Points	Project Points	Due Date
Week 1: 1/9 - 1/11	Course Intro	Course Logistics					
	Review Classical Digital Design	EELE 261 Review (XC)					Wed (1/16), 11:59pm
Week 2: 1/14 - 1/18	8 - VHDL (part 2)	8.1 - The Process	3				Wed (1/23), 11:59pm
		8.2 - Conditional Programming Constructs	12				Wed (1/23), 11:59pm
Week 3: 1/21 - 1/25	8 - VHDL (part 2)	8.3 - Signal Attributes	3				Wed (1/30), 11:59pm
		8.4 - Test Benches	14				Wed (1/30), 11:59pm
		Lab 8.1 - 7 Segment Decoders using if/then		50			Wed (1/30), 11:59pm
Week 4: 1/28 - 2/1	8 - VHDL (part 2)	8.5 - Packages	14				Wed (2/6), 11:59pm
		Lab 8.2 - Binary Characters using case		50			Wed (2/6), 11:59pm
		Module 8 Quiz			40		Wed (2/6), 11:59pm
Week 5: 2/4 - 2/8	9 - Behavioral Modeling	9.1 - Modeling Seq. Storage Devices in VHDL	3				Wed (2/13), 11:59pm
		9.2 - Modeling FSMs in VHDL	3				Wed (2/13), 11:59pm
		Lab 9.1 - Ripple Counter & Character Displays		50			Wed (2/13), 11:59pm
Week 6: 2/11 - 2/15	9 - Behavioral Modeling	9.3 - FSM Design Examples in VHDL	14				Wed (2/20), 11:59pm
		Lab 9.2 - Walking 1 FSM		50			Wed (2/20), 11:59pm
Week 7: 2/18 - 2/22	9 - Behavioral Modeling	9.4 - Modeling Counters	12				Wed (2/27), 11:59pm
		9.5 - RTL Modeling	3				Wed (2/27), 11:59pm
		Lab 9.3 - Counters using 1 Process		50			Wed (2/27), 11:59pm
Week 8: 2/25 - 3/1	9 - Behavioral Modeling	Lab 9.4 - BCD Counter		50			Wed (3/6), 11:59pm
		Module 9 Quiz			50		Wed (3/6), 11:59pm
Week 9: 3/4 - 3/8	10 - Memory	10.1 - Memory Architecture & Terminology	3				Wed (3/13), 11:59pm
		10.2 - Non-Volatile Memory Technology	3				Wed (3/13), 11:59pm
		10.3 - Volatile Memory Technology	3				Wed (3/13), 11:59pm
		10.4 - Modeling Memory in VHDL	14				Wed (3/13), 11:59pm
		Lab 10 - Accessing Memory (2 week lab)		50			Wed (3/27), 11:59pm
		Module 10 Quiz			40		Wed (3/13), 11:59pm
Week 10: 3/11 - 3/15	11 - Programmable Logic	11.1 - Programmable Arrays	3				Wed (3/27), 11:59pm
		11.2 - Field Programmable Gate Arrays	3				Wed (3/27), 11:59pm
		Module 11 Quiz			20		Wed (3/27), 11:59pm
Spring Break: 3/18 - 3/22 - No Class or Lab							
Week 11: 3/25 - 3/29	12 - Arithmetic Circuitry	12.1 - Addition	14				Wed (4/3), 11:59pm
		12.2 - Subtraction	14				Wed (4/3), 11:59pm
		12.3 - Multiplication	3				Wed (4/3), 11:59pm
		Lab 12.1 - HEX Adder		50			Wed (4/3), 11:59pm
Week 12: 4/1 - 4/5	12 - Arithmetic Circuitry	12.4 - Division	3				Wed (4/10), 11:59pm
		Lab 12.2 - BCD Adder		50			Wed (4/10), 11:59pm
		Module 12 Quiz			50		Wed (4/10), 11:59pm
Week 13: 4/8- 4/12	Module 13 - Computer Systems	13.1 - Computer Hardware	3				Wed (4/17), 11:59pm
		13.2 - Computer Software	3				Wed (4/17), 11:59pm
		13.3 - 8-Bit Computer Implementation					Wed (4/17), 11:59pm
		Lab 13.1 - VHDL Shell				20	Wed (4/17), 11:59pm
Week 14: 4/15 - 4/19	Module 13 - Computer Systems	13.3 - 8-Bit Computer Implementation					
		Lab 13.2 - Simulating 4x Basic Instructions				80	Wed (4/24), 11:59pm
Week 15: 4/22 - 4/26	Module 13 - Computer Systems	13.3 - 8-Bit Computer Implementation					
		Lab 13.3 - Implementating 4x Basic Instructions				40	Mon (4/29), 11:59pm
Finals Week: 4/29 - 5/3	Module 13 - Computer Systems	13.3 - 8-Bit Computer Implementation					
		Lab 13.4 - Implementating More Instructions				60	Wed (5/1), 11:59pm
		Total Points:	150	450	200	200	