3. Configuration & Testing

CII51003-2.2

IEEE Std. 1149.1 (JTAG) Boundary Scan Support

All Cyclone® II devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1. JTAG boundary-scan testing can be performed either before or after, but not during configuration. Cyclone II devices can also use the JTAG port for configuration with the Quartus® II software or hardware using either Jam Files (**.jam**) or Jam Byte-Code Files (**.jbc**).

Cyclone II devices support IOE I/O standard reconfiguration through the JTAG BST chain. The JTAG chain can update the I/O standard for all input and output pins any time before or during user mode through the CONFIG_IO instruction. You can use this capability for JTAG testing before configuration when some of the Cyclone II pins drive or receive from other devices on the board using voltage-referenced standards. Since the Cyclone II device might not be configured before JTAG testing, the I/O pins may not be configured for appropriate electrical standards for chip-to-chip communication. Programming the I/O standards via JTAG allows you to fully test I/O connections to other devices.

For information on I/O reconfiguration, refer to the *MorphIO: An I/O Reconfiguration Solution for Altera Devices White Paper*.

A device operating in JTAG mode uses four required pins: TDI, TDO, TMS, and TCK. The TCK pin has an internal weak pull-down resister, while the TDI and TMS pins have weak internal pull-up resistors. The TDO output pin and all JTAG input pin voltage is determined by the V_{CCIO} of the bank where it resides. The bank V_{CCIO} selects whether the JTAG inputs are 1.5-, 1.8-, 2.5-, or 3.3-V compatible.

Stratix® II, Stratix, Cyclone II and Cyclone devices must be within the first 8 devices in a JTAG chain. All of these devices have the same JTAG controller. If any of the Stratix II, Stratix, Cyclone II or Cyclone devices are in the 9th of further position, they fail configuration. This does not affect Signal Tap II.

Cyclone II devices also use the JTAG port to monitor the logic operation of the device with the SignalTap® II embedded logic analyzer. Cyclone II devices support the JTAG instructions shown in Table 3–1.

Table 3–1. Cyclone II JTAG Instructions (Part 1 of 2)

JTAG Instruction	Instruction Code	Description
SAMPLE/PRELOAD	00 0000 0101	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap II embedded logic analyzer.
EXTEST *(1)*	00 0000 1111	Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	11 1111 1111	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	00 0000 0111	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	00 0000 0110	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
HIGHZ *(1)*	00 0000 1011	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.
CLAMP *(1)*	00 0000 1010	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register.
ICR instructions		Used when configuring a Cyclone II device via the JTAG port with a USB Blaster™, ByteBlaster™ II, MasterBlaster™ or ByteBlasterMV™ download cable, or when using a Jam File or JBC File via an embedded processor.
PULSE_NCONFIG	00 0000 0001	Emulates pulsing the nCONFIG pin low to trigger reconfiguration even though the physical pin is unaffected.

Table 3–1. Cyclone II JTAG Instructions (Part 2 of 2)

JTAG Instruction	Instruction Code	Description
CONFIG_IO	00 0000 1101	Allows configuration of I/O standards through the JTAG chain for JTAG testing. Can be executed before, after, or during configuration. Stops configuration if executed during configuration. Once issued, the CONFIG_IO instruction holds nSTATUS low to reset the configuration device. nSTATUS is held low until the device is reconfigured.
SignalTap II instructions		Monitors internal device operation with the SignalTap II embedded logic analyzer.

Note to Table 3–1:
(1) Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.

The Quartus II software has an Auto Usercode feature where you can choose to use the checksum value of a programming file as the JTAG user code. If selected, the checksum is automatically loaded to the USERCODE register. In the **Settings** dialog box in the Assignments menu, click **Device & Pin Options**, then **General,** and then turn on the **Auto Usercode option**.

The Cyclone II device instruction register length is 10 bits and the USERCODE register length is 32 bits. Tables 3–2 and 3–3 show the boundary-scan register length and device IDCODE information for Cyclone II devices.

Table 3–2. Cyclone II Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP2C5	498
EP2C8	597
EP2C15	969
EP2C20	969
EP2C35	1,449
EP2C50	1,374
EP2C70	1,890

Table 3–3. 32-Bit Cyclone II Device IDCODE

Device	IDCODE (32 Bits) *(1)*			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	LSB (1 Bit) *(2)*
EP2C5	0000	0010 0000 1011 0001	000 0110 1110	1
EP2C8	0000	0010 0000 1011 0010	000 0110 1110	1
EP2C15	0000	0010 0000 1011 0011	000 0110 1110	1
EP2C20	0000	0010 0000 1011 0011	000 0110 1110	1
EP2C35	0000	0010 0000 1011 0100	000 0110 1110	1
EP2C50	0000	0010 0000 1011 0101	000 0110 1110	1
EP2C70	0000	0010 0000 1011 0110	000 0110 1110	1

Notes to Table 3–3:
(1) The most significant bit (MSB) is on the left.
(2) The IDCODE's least significant bit (LSB) is always 1.

For more information on the Cyclone II JTAG specifications, refer to the *DC Characteristics & Timing Specifications* chapter in the *Cyclone II Device Handbook, Volume 1*.

SignalTap II Embedded Logic Analyzer

Cyclone II devices support the SignalTap II embedded logic analyzer, which monitors design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry. You can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages, such as FineLine BGA® packages, because it can be difficult to add a connection to a pin during the debugging process after a board is designed and manufactured.

For more information on the SignalTap II, see the *Signal Tap* chapter of the *Quartus II Handbook, Volume 3*.

Configuration

The logic, circuitry, and interconnects in the Cyclone II architecture are configured with CMOS SRAM elements. Altera FPGA devices are reconfigurable and every device is tested with a high coverage production test program so you do not have to perform fault testing and can instead focus on simulation and design verification.

Cyclone II devices are configured at system power-up with data stored in an Altera configuration device or provided by a system controller. The Cyclone II device's optimized interface allows the device to act as controller in an active serial configuration scheme with EPCS serial configuration devices. The serial configuration device can be programmed via SRunner, the ByteBlaster II or USB Blaster download cable, the Altera Programming Unit (APU), or third-party programmers.

In addition to EPCS serial configuration devices, Altera offers in-system programmability (ISP)-capable configuration devices that can configure Cyclone II devices via a serial data stream using the Passive serial (PS) configuration mode. The PS interface also enables microprocessors to treat Cyclone II devices as memory and configure them by writing to a virtual memory location, simplifying reconfiguration. After a Cyclone II device has been configured, it can be reconfigured in-circuit by resetting the device and loading new configuration data. Real-time changes can be made during system operation, enabling innovative reconfigurable applications.

Operating Modes

The Cyclone II architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. You can use the 10MHz internal oscillator or the optional `CLKUSR` pin during the initialization. The 10 MHz internal oscillator is disabled in user mode. Together, the configuration and initialization processes are called command mode. Normal device operation is called user mode.

SRAM configuration elements allow Cyclone II devices to be reconfigured in-circuit by loading new configuration data into the device. With real-time reconfiguration, the device is forced into command mode with the nCONFIG pin. The configuration process loads different configuration data, reinitializes the device, and resumes user-mode operation. You can perform in-field upgrades by distributing new configuration files within the system or remotely.

A built-in weak pull-up resistor pulls all user I/O pins to V_{CCIO} before and during device configuration.

The configuration pins support 1.5-V/1.8-V or 2.5-V/3.3-V I/O standards. The voltage level of the configuration output pins is determined by the V_{CCIO} of the bank where the pins reside. The bank V_{CCIO} selects whether the configuration inputs are 1.5-V, 1.8-V, 2.5-V, or 3.3-V compatible.

Configuration Schemes

You can load the configuration data for a Cyclone II device with one of three configuration schemes (see Table 3–4), chosen on the basis of the target application. You can use a configuration device, intelligent controller, or the JTAG port to configure a Cyclone II device. A low-cost configuration device can automatically configure a Cyclone II device at system power-up.

Multiple Cyclone II devices can be configured in any of the three configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

Table 3–4. Data Sources for Configuration

Configuration Scheme	Data Source
Active serial (AS)	Low-cost serial configuration device
Passive serial (PS)	Enhanced or EPC2 configuration device, MasterBlaster, ByteBlasterMV, ByteBlaster II or USB Blaster download cable, or serial data source
JTAG	MasterBlaster, ByteBlasterMV, ByteBlaster II or USB Blaster download cable or a microprocessor with a Jam or JBC file

For more information on configuration, see the *Configuring Cyclone II Devices* chapter of the *Cyclone II Handbook, Volume 2*.

Cyclone II Automated Single Event Upset Detection

Cyclone II devices offer on-chip circuitry for automated checking of single event upset (SEU) detection. Some applications that require the device to operate error free at high elevations or in close proximity to earth's North or South Pole require periodic checks to ensure continued data integrity. The error detection cyclic redundancy code (CRC) feature controlled by the **Device & Pin Options** dialog box in the Quartus II software uses a 32-bit CRC circuit to ensure data reliability and is one of the best options for mitigating SEU.

You can implement the error detection CRC feature with existing circuitry in Cyclone II devices, eliminating the need for external logic. For Cyclone II devices, the CRC is pre-computed by Quartus II software and then sent to the device as part of the POF file header. The `CRC_ERROR` pin reports a soft error when configuration SRAM data is corrupted, indicating to the user to preform a device reconfiguration.

Custom-Built Circuitry

Dedicated circuitry in the Cyclone II devices performs error detection automatically. This error detection circuitry in Cyclone II devices constantly checks for errors in the configuration SRAM cells while the device is in user mode. You can monitor one external pin for the error and use it to trigger a re-configuration cycle. You can select the desired time between checks by adjusting a built-in clock divider.

Software Interface

In the Quartus II software version 4.1 and later, you can turn on the automated error detection CRC feature in the Device & Pin Options dialog box. This dialog box allows you to enable the feature and set the internal frequency of the CRC checker between 400 kHz to 80 MHz. This controls the rate that the CRC circuitry verifies the internal configuration SRAM bits in the FPGA device.

For more information on CRC, refer to *AN: 357 Error Detection Using CRC in Altera FPGAs*.

Document Revision History

Table 3–5 shows the revision history for this document.

Table 3–5. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2007 v2.2	• Added document revision history. • Added new handpara nore in "IEEE Std. 1149.1 (JTAG) Boundary Scan Support" section. • Updated "Cyclone II Automated Single Event Upset Detection" section.	• Added information about limitation of cascading multi devices in the same JTAG chain. • Corrected information on CRC calculation.
July 2005 v2.0	Updated technical content.	
February 2005 v1.2	Updated information on JTAG chain limitations.	
November 2004 v1.1	Updated Table 3–4.	
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	